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ABSTRACT

Output voltage total harmonic distortion (THD) of a 20kHz, 6kVA Mapham resonant inverter is characterized as a function of its switching-to-resonant frequency ratio, f_s/f_r, using the EASY5 Engineering Analysis System. EASY5 circuit simulation results are compared with hardware test results to verify the accuracy of the simulations. The effects of load on the THD versus f_s/f_r ratio is investigated for resistive, leading, and lagging power factor load impedances. The effect of the series output capacitor on the Mapham inverter output voltage distortion and inherent load regulation is characterized under loads of various power factors and magnitudes. An optimum series capacitor value which improves the inherent load regulation to better than 3% is identified. The optimum series capacitor value is different than the value predicted from a modeled frequency domain analysis. An explanation is proposed which takes into account the conduction overlap in the inductor pairs during steady-state inverter operation, which decreases the effective inductance of a Mapham inverter. A fault protection and current limit method is discussed which allows the Mapham inverter to operate into a short circuit, even when the inverter resonant circuit becomes overdamped.

1. INTRODUCTION

20kHz AC power distribution is currently baselined for use on the Space Station Freedom, and is under consideration for launch vehicles and aircraft utilizing compact and lightweight electro-mechanical actuators. The advantages of high frequency AC power distribution have been discussed in the literature [1][2]. To convert spacecraft photovoltaic, battery, solar dynamic, or other energy sources into 20kHz power, lightweight and efficient inverters with regulated, low-distortion outputs are required. A leading candidate is the Mapham inverter. The Mapham inverter uses resonant conversion, which results in the highest possible full load efficiency because of the lack of frequency sensitive turn-off losses.

To minimize Electro-Magnetic Interference (EMI) in 20kHz distribution systems, the Mapham inverter must be designed to achieve minimum output voltage distortion. It has been shown that the Mapham inverter output voltage total harmonic distortion (THD) is related to its switching-to-resonant frequency ratio, or normalized switching frequency f_{sn} [3]. However, a quantified relationship had not been identified, nor had the effects of load and power factor on the relationship been identified. Section 3 of this paper presents the results of circuit simulations which characterize the THD versus f_{sn} function, and the effects of load magnitude and power factor on that function.

Although active phasor-regulation of a series-output connected inverter pair (see figure 2-1b) has been shown to provide near perfect line and load regulation [4][5], the inherent load regulation of a single Mapham inverter module is important for practical reasons. To realize maximum efficiency in a series-output connection, the regulation angle Ø in figure 2-1c should be near zero at full load [6]. However, at Ø~0° the inverter pair output must maintain regulation under worst-case voltage drop conditions for the vectors V_{01} and V_{02}. Since inductive loads result in worst-case voltage drop in an uncompensated Mapham inverter, the regulation angle of Ø~0 must be reserved for lagging power factor loads to maintain a constant output voltage V_{OT}. This will result in a large value of Ø at unity power factors and a decrease in inverter pair efficiency. Thus, if the Mapham inverter inherent load regulation could be improved, the regulation angle could remain near zero at all power factors, which would improve the inverter pair efficiency. It has been shown that the inherent load regulation can be improved by placing a capacitor in series with the load (C_s in figure 2-1a). The optimum series capacitor value for best load regulation has been analytically determined from frequency domain analysis [7][8]. However, hardware testing has revealed that series capacitor values larger than the predicted value result in better inherent load regulation [6]. Thus the optimum series capacitor value from a regulation point of view needed further investigation.

The series output capacitor has also been shown to effect output voltage distortion[6][8], efficiency[6], and short circuit operation[3][6]. However, these relationships had not been well characterized. Section 4 of this paper presents the results of computer circuit simulations which characterize the effect of the series capacitor on inherent load regulation and on output voltage THD. A discussion of the effects of the series capacitor on short-circuit operation is also presented, as well as a method of limiting the short circuit output current and protecting the inverter semiconductor switches during forced commutation. Although the series capacitor affects efficiency, the circuit models used were not able to determine this relationship, therefore dicussion of it is beyond the scope of this paper.

2. INVERTER OPERATION

The Mapham inverter, shown in figure 2-1a, consists of four switches each with a flyback diode, four resonant inductors, a resonant capacitor C_r, a series output capacitor C_s, and an output transformer. The resonant inductors form a series-resonant circuit with the capacitor C_r. They also force each switch to turn-on and turn-off at zero current which virtually eliminates switching losses [2][3]. The series capacitor improves load regulation [7][8], and can also make the inverter inherently short circuit proof if small enough [3]. The output transformer is used for load isolation and load voltage magnitude

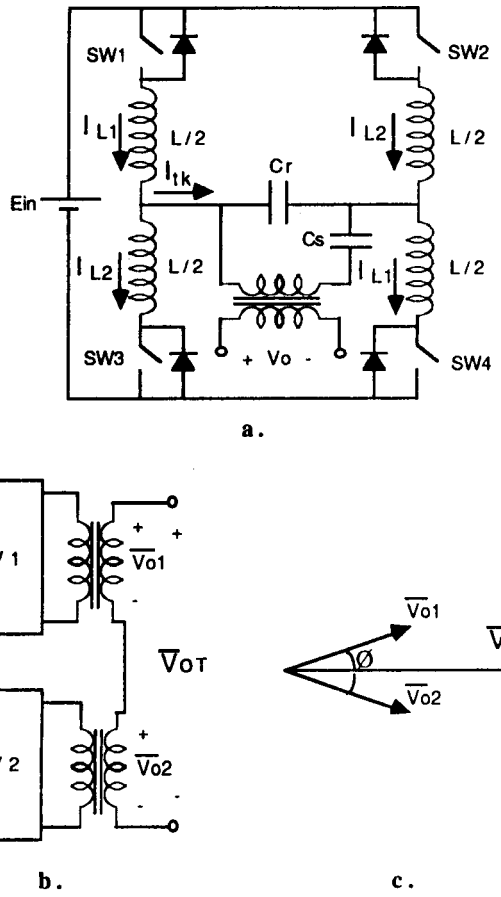


Figure 2-1. The Mapham inverter (a), the phasor regulated series-output connection (b), and a phasor diagram showing the vector addition of the series-output connection (c).

selection. It also allows for the series-output connection of two Mapham inverters as in the proposed Space Station Freedom Main Inverter Unit (MIU), shown in figure 2-1b. The series-output connection doubles power output and is required for active phasor output voltage regulation, which has been demonstrated to have fast response, high efficiency, and less than 1% regulation from zero to full load over an input voltage swing of 150-200 Vdc [4][5].

Referring to figure 2-1a, if the switch pair S1,S4 is turned-on, a sinusoidal current I_{L1} of resonant frequency $f_r=1/2\pi\sqrt{LC_r}$ will flow in the resonant L-C_r network as shown in figure 2-2. Switches S1 and S4 commutate when I_{L1} reverses direction and flows through the flyback diodes of S1 and S4. If switches S2 and S3 are turned-on while I_{L1} is negative, the current of I_{L2} results. The currents I_{L1} and I_{L2} sum to give the resultant resonant tank current I_{tk} of frequency f_s, the switching frequency of the S1,S4 and S2,S3 switch pairs. Since each switch pair is turned on while the current of the opposite pair is negative, the switching frequency is always lower than the resonant frequency. The resonant capacitor C_r integrates the current I_{tk} to obtain the sinusoidal voltage of V_C. The load Z_L is placed in parallel with the resonant capacitor via the output transformer, either with or without the series capacitor C_s.

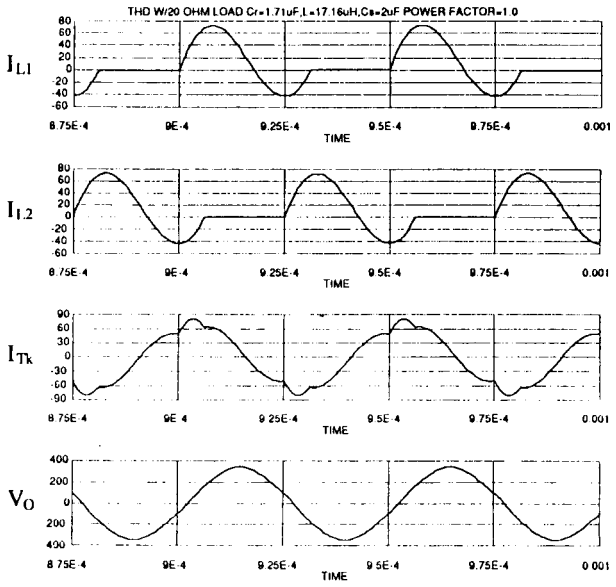


Figure 2-2. Typical Mapham inverter inductor currents, tank current, and output voltage waveforms under load.

3. EFFECTS OF f_{sn} ON INVERTER OUTPUT VOLTAGE DISTORTION

To investigate the output voltage distortion of the Mapham inverter, the EASY5 Engineering Analysis System [9] was employed. The EASY5 Mapham inverter model was originally developed by Virginia Polytechnic Institute and State University, and was later modified by the NASA Lewis Research Center and the Rocketdyne Division of Rockwell International [10]. The inverter simulation circuit parameters were initially chosen to match the values of the Mapham inverter modules located in the NASA Lewis Research Center 25kW, 20kHz Power System Testbed, developed by General Dynamics [4]. The testbed inverter modules each have a power output capability between 6kW and 12kW at 160 Vdc input, depending on series capacitor value and operating point definition. After some preliminary simulations were complete, the circuit model inductance value was increased slightly to realize minimum output voltage distortion at a 20kHz switching frequency. The circuit model transformer leakage and magnetizing inductance values were the same as measured on the testbed. The EASY5 inverter circuit and testbed inverter circuit parameters were as follows:

PARAMETER	EASY5	TESTBED
E_{in}	160 Vdc	160Vdc
L	17.16 µH	16.0µH
C_r	1.71 µF	1.71µF
C_s	2.0 µF	2.0µF
L_m (magnetizing)	1.3 mH	0.9 -1.3 mH
L_{leak} (leakage)	1.89 µH	1.8 µH

The relationship between the inverter normalized switching frequency and its output voltage distortion was investigated by varying the switching frequency f_s in the simulations while keeping the circuit parameters fixed. The inverter resonant frequency was calculated from Mapham's defining relationship of equation (1) below. The switching frequency was normalized by dividing it by the resonant frequency according to equation (2) below. The resultant inverter output voltage distortion was obtained from a Virginia Polytechnic Institute developed macro for EASY5.

$$f_r \equiv \text{resonant frequency} = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad (1)$$

$f_s \equiv$ switching frequency

$$f_{sn} \equiv \text{normalized switching frequency} = \frac{f_s}{f_r} \qquad (2)$$

$f_{sn\,min} \equiv f_{sn}$ for minimum THD

3.1 Unloaded Inverter Distortion

The unloaded Mapham inverter output voltage and inductor currents for normalized switching frequency values f_{sn} of 0.493, 0.684, and 0.863 are shown in figure 3-1. As can be seen from the figure, the f_{sn} value of 0.684 results in the lowest distortion.

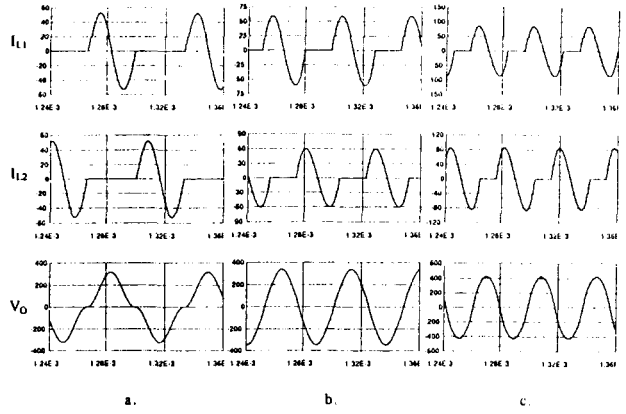


Figure 3-1. Unloaded Mapham inverter inductor currents (top two rows) and output voltage (bottom row) for f_{sn} values of: (a) 0.493, (b) 0.684, (c) 0.863.

In figure 3-2a, a plot of Total Harmonic Distortion (THD) as a function of f_{sn} shows a more quantitative picture of the THD vs. f_{sn} function. The graph reveals a distinct minimum output voltage distortion point which results in less than 1.5% THD. This minimum distortion point occurs at a normalized switching frequency $f_{sn\,min}$ of 0.68. The $f_{sn\,min}$ value of 0.68 is slightly lower than the value of 0.74 reported by Mapham [3], and lowers the open circuit THD from 2.9% to the minimum value of 1.5%.

To confirm the results of the EASY5 simulations on the unloaded Mapham inverter, hardware testing was performed using one of the testbed Mapham inverter modules. The switching frequency was varied with the circuit parameters fixed, as in the EASY5 simulations. The hardware results are also plotted in figure 3-2a and show excellent agreement with the circuit simulation results.

The existence of an optimum open circuit f_{sn} value from a distortion point of view suggests that for constant frequency applications such as high frequency AC distribution systems, the Mapham inverter resonant frequency should be chosen to realize a switching-to-resonant frequency ratio of 0.68. Resonant

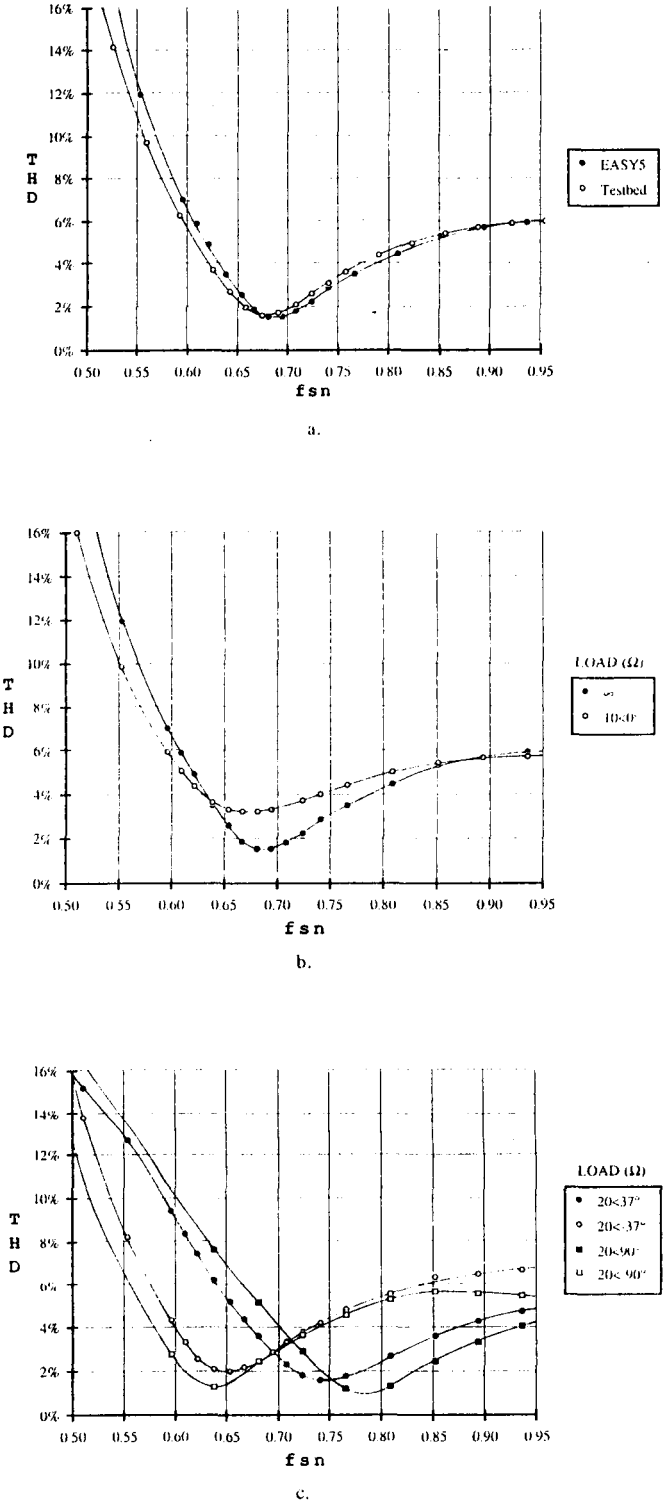
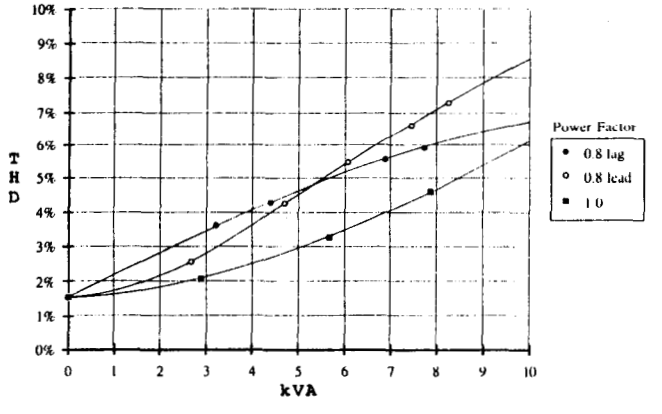


Figure 3-2. Mapham inverter output voltage Total Harmonic Distortion (THD) as a function of its switching-to-resonant frequency ratio f_{sn} from the EASY5 simulations: (a) Open circuit with testbed data, (b) No load and 10 ohm resistive load, (c) 0.8 and 0.0 power factor reactive loads.

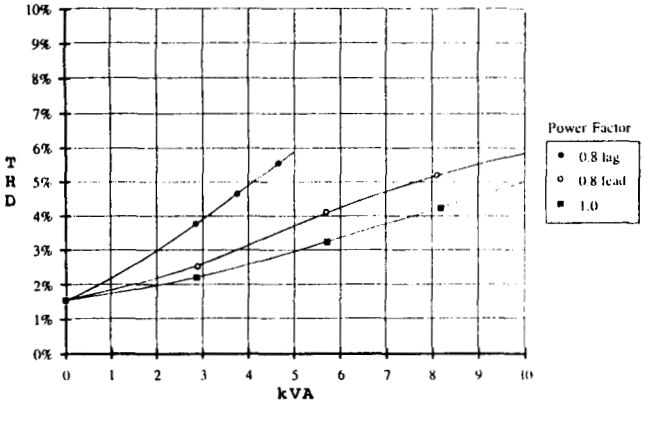
frequencies either higher or lower than f_{sn}=0.68 will unnecessarily increase the system distortion and radiated EMI. The f_{sn} value of 0.68 is also a good practical value, because it allows inverter to be loaded to near the critical damping point. This results in maximum efficiency, because the flyback diode current is near zero which reduces losses.

3.2 Load Effects on THD

It has been determined that both load magnitude and power factor increase the Mapham inverter output voltage distortion [6][8][11]. THD as a function of load kVA was characterized for our inverter model with $f_{sn} = f_{sn\ min} = 0.68$, and C_s=2.0μF and 3.5μF. Figure 3-3 shows a plot of THD vs load kVA at 1.0, 0.8 leading, and 0.8 lagging power factors. It can be seen that non-unity power factor loads increase the inverter distortion more than resistive loads. This is because the reactive component combines with the resonant capacitor C_r and changes the inverter resonant frequency, thereby de-tuning $f_{sn\ min}$ from the 0.68 value determined in the no load case. Such an effect should produce a new $f_{sn\ min}$ value different from 0.68 for reactive loads.



a. - 2.0 μF series capacitor



b. - 3.5 μF series capacitor

Figure 3-3. Mapham inverter output voltage distortion vs. load kVA for series capacitor values of: (a) 2.0μF, (b) 3.5μF.

3.3 Load Effects on $f_{sn\ min}$

To determine whether load has an effect on the THD vs. f_{sn} function, the simulations were repeated for the inverter loaded with resistive, capacitive, and inductive loads. The load impedances, load power factors, inverter kVA outputs (S_o) at f_{sn}=0.68 (f_s=20kHz), $f_{sn\ min}$, and THD values are listed below:

LOAD	p.f.	S_o @ f_{sn}=0.68	$f_{sn\ min}$	THD @ $f_{sn\ min}$
∞ Ω	--	0.0 kVA	0.68	1.53%
10 Ω	1.0	5.7 kW	0.67	3.23%
20 Ω	0.8 lead	2.6 kVA	0.65	2.01%
20 Ω	0.8 lag	3.2 kVA	0.74	1.60%
20 Ω	0.0 lead	2.4 kVA	0.63	1.25%
20 Ω	0.0 lag	3.5 kVA	0.77	1.20%

Figure 3-2b shows a plot of inverter THD vs f_{sn} for open-circuit and 10 ohm resistive loads. As can be seen from the figure, the resistance increases the minimum distortion value and also desensitizes the effect of f_{sn} on THD. Minimum distortion still occurs at f_{sn} = 0.68, but the curve is flat for f_{sn} values between 0.65 and 0.70. This result suggests that for systems with well-controlled power factors, the f_{sn} value of 0.68 is not as critical, but still achieves minimum distortion.

Figure 3-2c shows plots of THD vs f_{sn} for the 0.8 and 0.0 power factor load cases. Note that the pure reactive loads slightly decrease the minimum THD. In contrast to the resistive load case, pure reactive loads also shift $f_{sn\ min}$. Inductive loads increase $f_{sn\ min}$, while capacitive loads decrease it. This effect is as predicted: the reactive load elements de-tune the switching-to-resonant frequency ratio by combining with the resonant capacitor C_r and effectively changing the inverter resonant frequency.

The 0.8 power factor loads of figure 3-2c both shift $f_{sn\ min}$ and slightly increase the minimum THD value. It appears reasonable that the resistive portion of the load increases the distortion, while the reactive portion of the load shifts the $f_{sn\ min}$ point.

The results in figures 3-2b and 3-2c were obtained with a series capacitor value of 2.0μF because it was the value used in the testbed inverters, and also because frequency domain analysis predicted a 2.0μF capacitor would realize the lowest inverter output impedance and best inherent regulation [7]. As is discussed in section 4, the series capacitor affects the THD under load, so the loaded inverter THD vs f_{sn} results presented in this section will be slightly different for other series capacitor values. However, since the load impedances used resulted in moderate inverter loading and since the series capacitor effects become more pronounced at higher kVA levels, the difference is small. Some simulations were repeated using a 3.5μF series capacitor, and the results were nearly identical with the 2.0μF capacitor results.

4. SERIES CAPACITOR EFFECTS ON INVERTER PERFORMANCE

4.1 Series Capacitor Effects on Regulation

As noted in the introduction, the series capacitor C_s lowers the inverter output impedance. Referring to the frequency domain Mapham inverter model of figure 4-1a and neglecting the leakage inductance and magnetizing inductance, the output impedance Z_o at the switching frequency $\omega_s = 2\pi f_s$ is given by:

$$\bar{Z}_o = jZ_o = \frac{j\omega_s L}{1 - \omega_{sn}^2} \qquad (3)$$

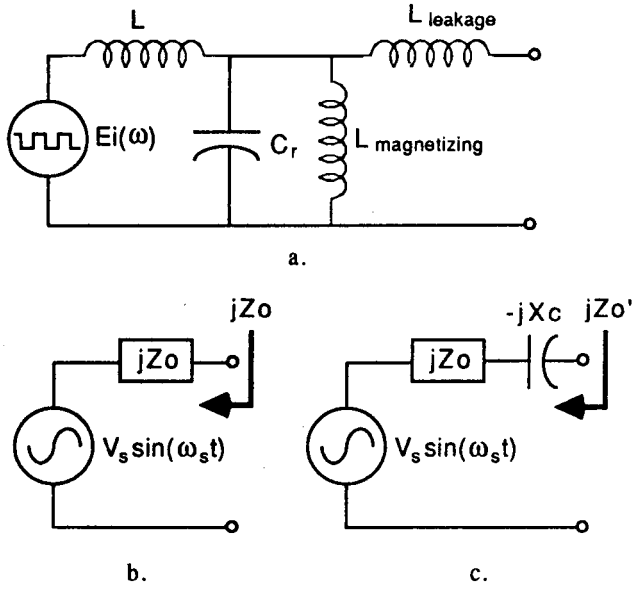


Figure 4-1. Mapham inverter simplified frequency domain model (a), equivalent Thevenin circuit at 20kHz (b), equivalent Thevenin circuit with series capacitor compensation (c).

Since ω_{sn} ($=f_{sn}$) is less than 1 in a Mapham inverter (0.68 for our EASY5 inverter model), equation (3) is positive and jZ_o is inductive. Figure 4-1b represents a simplified Thevenin voltage source equivalent circuit at the switching frequency ω_s. jZ_o represents the inductive source impedance given by equation (3). To cancel the inductance, a negative impedance $-jX_c$ equal in magnitude to jZ_o can be introduced in series with the inverter to form a new source impedance jZ_o', as shown in figure 4-1c. The value of series capacitor has been determined by Oruganti [7], and is derived as follows:

$$-jX_c = -j\frac{1}{\omega_s C_s} \qquad (4)$$

$$jZ_o' = jZ_o - jX_c = \frac{j\omega_s L}{1-\omega_{sn}^2} - j\frac{1}{\omega_s C_s} \qquad (5)$$

$$C_s(jZ_o'=0) = \frac{1-\omega_{sn}^2}{\omega_s^2 L} = \frac{1-\omega_{sn}^2}{\omega_{sn}^2} C_r \qquad (6)$$

For our optimized inverter with ω_{sn}=0.68 and C_r=1.71μF, the series capacitor $C_s(jZ_o'=0)$ was calculated from equation (6) to be almost exactly 2.0μF. Therefore, for C_s=2.0μF, equations (5) and (6) predict that the inverter output impedance should be near zero which should yield the best load regulation. This follows from approximate voltage drop analysis for an AC system with a source impedance of jZ_o' and a load impedance of $R_L + jX_L$:

$$\bar{V}_L = \bar{V}_s \frac{(R_L + jX_L)}{(R_L + jX_L) + jZ_o'}$$

$$|\bar{V}_L| = |\bar{V}_s| \frac{\sqrt{R_L^2 + X_L^2}}{\sqrt{R_L^2 + (X_L + Z_o')^2}} \qquad (7)$$

If $Z_o'=0$, then $|V_L| = |V_s|$. However, if $Z_o' \neq 0$, then equation (7) predicts either a load voltage drop or rise, depending on the respective signs of Z_o' and X_L. If X_L and Z_o' are the same sign in equation (7), then $(X_L + Z_o')^2 > X_L^2$ and $|V_L| < |V_s|$ resulting in a load voltage drop. If X_L and Z_o' are of opposite sign, then $(X_L + Z_o')^2 < X_L^2$ and $|V_L| > |V_s|$, resulting in a load voltage rise. For $C_s > C_s(jZ_o'=0)$, the impedance jX_c introduced by C_s in equation (4) is smaller than the inductive inverter output impedance jZ_o, and jZ_o' will be positive or inductive from equation (5). Conversely, if the series capacitor C_s is smaller than $C_s(jZ_o'=0)$, the impedance jX_c of equation (4) will be larger than jZ_o, and jZ_o' will be negative or capacitive.

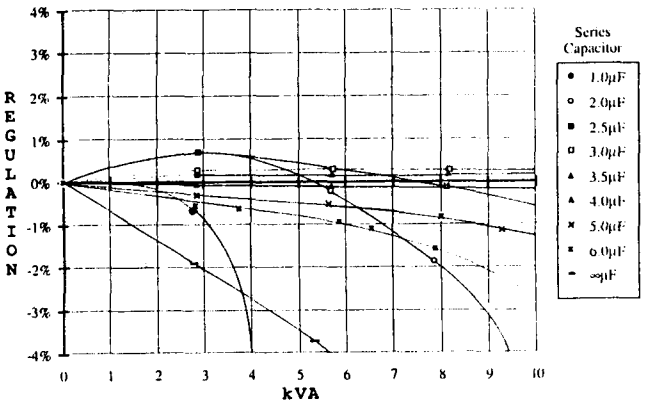
To verify the prediction of equations (3-7), circuit simulations were performed using a range of series capacitor values at 1.0, 0.8 leading, and 0.8 lagging power factor load impedances. Figure 4-2 shows plots of inherent inverter output voltage regulation vs. output kVA. The inductive impedance jZ_o of the uncompensated Mapham inverter is verified when $C_s=\infty$ (no series capacitor) or 6μF (jX_c is small). Inductive loads cause a voltage drop (figure 4-2c), while capacitive loads cause a voltage rise (figure 4-2b). For $C_s < C_s(jZ_o'=0)$, the inverter impedance is overcompensated and turns capacitive, as can be verified for the C_s = 1.0μF case. Inductive loads now result in a voltage rise while capacitive loads result in a voltage drop. These effects are as predicted by equation (7).

It can also be seen from figure 4-2 that near perfect load regulation is achieved for series capacitor values around 3.5μF at all power factors. The voltage regulation curve is within 2.5% up to 6 kVA for the resistive, capacitive, and inductive loads. Thus, the value of $C_s(jZ_o'=0)$ determined from the simulations is close to 3.5μF, and jZ_o' does appear to be close to zero. However, the 3.5μF value of $C_s(jZ_o'=0)$ does not agree with the predictions of equation (6), which gave a value of $C_s(jZ_o'=0)$ = 2.0μF. Tsai and Lee [8] used a value of L/2 in place of L in equation (5) and (6), which gives a value of $C_s(jZ_o'=0)$ = 5.7μF for our inverter model, which also does not agree with the simulation results. Since the 3.5μF value of $C_s(jZ_o'=0)$ falls in between both values calculated from the Mapham inverter simplified frequency domain model, it can be concluded that neither L nor L/2 is the proper frequency domain circuit inductance value. A closer look into the inverter operation is necessary to determine why the analysis does not accurately predict the inverter impedance, and what corrections, if any, can be made to the frequency domain inverter model of figure 4-1a to improve its accuracy.

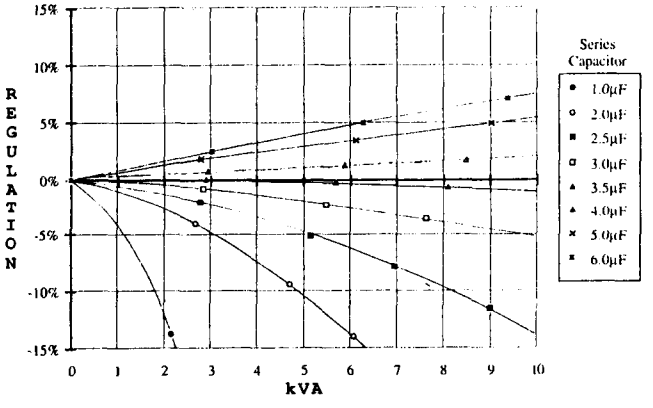
Effective Inductance

One explanation for the shortcomings of equation (6) is that the equivalent inverter inductance is not equal to L or L/2. A look into the three inverter conduction mode states will illustrate this point. Referring to figure 4-3, the three inverter conduction modes M1, M2, M1' are shown. During steady-state operation, the inverter passes through the sequence M2-M1-M2-M1' during each cycle. During conduction mode M2, the two inductors on either side of the resonant capacitor C_r are effectively in parallel, and the circuit inductance is L/2. During conduction modes M1 and M1', the circuit inductance is equal to L. Thus, the circuit inductance alternates between L and L/2 during every half-cycle. The equivalent or effective inductance will therefore be a complex average of L and L/2, and varies as a function of f_{sn} and load.

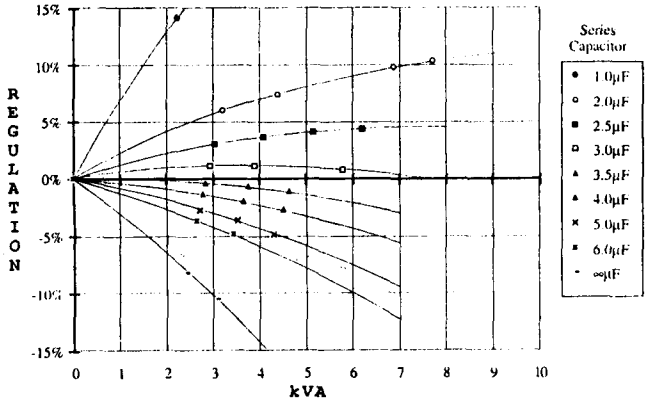
The dependence of the effective inductance on f_{sn} caused the steady-state resonant inductor conduction period T_{rss} to vary with f_{sn}. Defining the equivalent or effective inductance L_{eff} as the value of inductance that resonates with the inverter capacitor C_r at a period of T_{rss}, the following equation results:



a. - 1.0 power factor



b. - 0.8 leading power factor



c. - 0.8 lagging power factor

Figure 4-2. Mapham inverter inherent voltage regulation vs output kVA for different series capacitor values at: (a) unity p.f., (b) 0.8 leading p.f., (c) 0.8 lagging p.f.

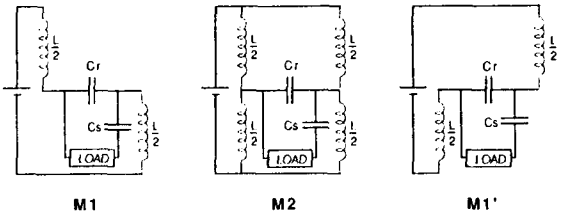


Figure 4-3. Normal conduction modes of the Mapham inverter.

$$L_{eff} = \frac{T_{rss}^2}{(2\pi)^2 C_r} \qquad (8)$$

Equation (8) is only valid at no load. A detailed discussion of L_{eff} and the load effects on L_{eff} can be found in reference [12].

4.2 Series Capacitor Effects on THD

The distortion effects of the series capacitor were also investigated, at unity, 0.8 leading, and 0.8 lagging power factor loads. Figure 4-4 shows plots of THD vs. load kVA for series capacitor values between 1.0μF and ∞μF (no series capacitor). For the unity power factor loads in 4-4a, series capacitor values between 2.5μF and 4.0μF reduce THD. However, the difference in THD between 2.0μF and ∞μF series capacitors is small. Thus for resistive loads, the effect of the series capacitor on THD is not very significant.

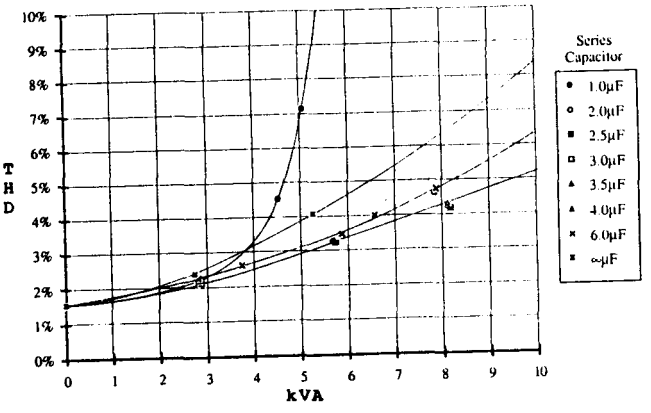
For 0.8 leading power factor loads, as shown in 4-4b, the series capacitor increases distortion. However, for large series capacitor values including $C_s(jZ_o'=0) = 3.5\mu F$, the increase in THD is insignificant. The value $C_s(jZ_o'=0) = 3.5\mu F$ results in a THD value of about 4.2% at 6kVA, which is close to the minimum THD value at 6kVA of 4.0% for the 6.0μF capacitor.

For 0.8 lagging power factor loads, the series capacitor decreases distortion, but the actual THD is higher at a given kVA than for leading power factor loads. For $C_s(jZ_o'=0) = 3.5\mu F$, the distortion at 6kVA was about 7% -- almost 3% higher than for a 6kVA leading 0.8 power factor load. A more significant benefit of the series capacitor is that it increases the kVA output capability of the inverter for lagging power factor loads.

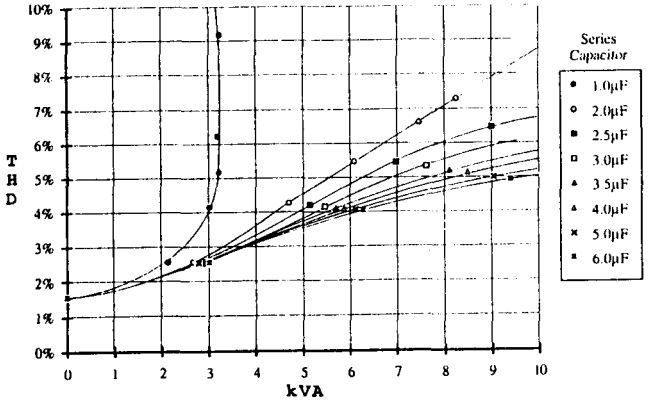
Despite the benefits of the series capacitor in improving regulation, additional output filtering may be required, depending on the THD requirements of the 20kHz system. The current flight design for the Space Station MIU replaces the series capacitor with a more complex filter to further reduce THD. The additional output filter can also be designed to eliminate the harmonic circulating currents in paralleled inverters, which result from the high frequency impedance zero due to the series combination of the output transformer leakage inductance and the series and resonant capacitors [12].

4.3 Series Capacitor Effects on Short Circuit Operation

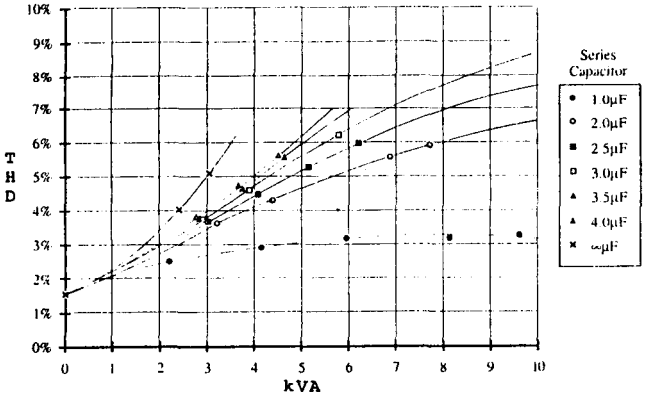
One disadvantage of the 3.5μF series capacitor is that the inverter will not inherently run into a short circuit, as it will for small series capacitor values as reported by Mapham [3]. Additional fault protection circuitry will therefore be required to limit the semiconductor switch current into the resonant tank/load network in the event of a load fault. One fault protection scheme is to utilize clamped mode operation. Upon



a. - 1.0 power factor



b. - 0.8 leading power factor



c. - 0.8 lagging power factor

Figure 4-4. Mapham inverter output voltage THD vs. output kVA for different series capacitor values at: (a) unity p.f., (b) 0.8 leading p.f., (c) 0.8 lagging p.f.

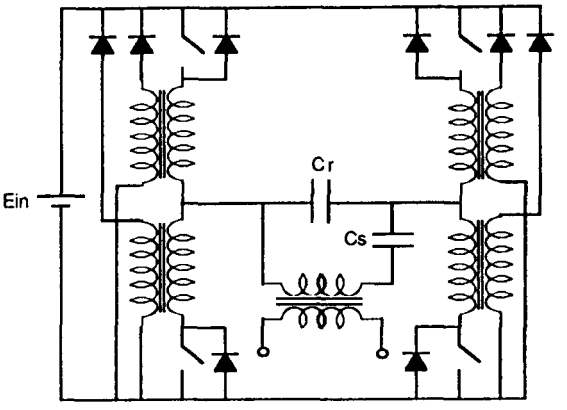


Figure 4-5. The Mapham inverter can be modified to drive a short-circuit by using turn-off switches and incorporating a secondary winding to return the stored inductor energy to the power supply during forced switch commutation.

detection of a fault, the switch on time is controlled to limit the current into the resonant tank. This method also actively limits the inverter short circuit output current.

To implement clamped mode operation in a Mapham inverter, forced switch commutation is required while the inductor is carrying current. This will produce large voltage transients across the semiconductor switches which can destroy the devices. To eliminate this potential problem, a secondary winding on the resonant inductors can be employed to return the stored inductor energy to the power supply, as shown in figure 4-5. If the voltage across the inductor exceeds the power supply voltage, the secondary winding diodes turn on and the stored magnetizing energy is returned to the supply.

5. CONCLUSIONS

- The EASY5 total harmonic distortion analysis agreed with hardware test results, and proved useful as a tool for characterizing the distortion of a Mapham inverter.
- A switching-to-resonant frequency ratio of 0.68 results in minimum output voltage distortion for an unloaded Mapham inverter.
- The minimum distortion switching-to-resonant frequency ratio was found to change with reactive loads. This is because the reactive component of the load combines with the resonant capacitor and changes the inverter resonant frequency.
- Selection of proper series capacitor can improve the inherent load regulation of a Mapham inverter to better than 3% for 0.8 leading to 0.8 lagging power factor loads up to 6kVA.
- Frequency domain analysis using an effective inverter inductance equal to either L or L/2 does not accurately predict optimum series capacitor for regulation.
- An effective resonant inductance, L_{eff} was proposed to improve the accuracy of the frequency domain Mapham Inverter model. L_{eff} results from a complex averaging of the three inverter conduction modes.

- Overall, the series capacitor results in a small improvement in THD, but more significantly increases the kVA output for lagging power factor loads. Additional filtering should be used to reduce THD.

- A Mapham inverter can be modified to operate into a short circuit if clamped mode operation is used. Additional windings on the inductors are required to return the stored inductor energy to the power supply during forced switch commutation.

6. REFERENCES

[1] "In Space, it's 20-kHz AC Power," J. Mildice, Powertechnics Magazine, February, 1989.

[2] "Space Station 20kHz Power Management and Distribution System," I.G. Hansen and G.R. Sundberg, PESC Conference Record, June, 1986.

[3] "An SCR Inverter with Good Regulation and Sine-Wave Output," N. Mapham, IEEE Transactions on Industry and General Applications, MAR/APR, 1967.

[4] "AC Power System Testbed, Final Report," J. Mildice and R. Sundberg, NASA CR 175068, November, 1988.

[5] "Development and Testing of a 20kHz Component Testbed," R. Button, A. Brush, and R. Sundberg, 24th IECEC Conference Record, August, 1989.

[6] "Main Inverter Unit (MIU) Efficiency Test Report - Phase II" R. Sundberg, General Dynamics Space Systems Division Rpt # 8721-88-021, May, 1988.

[7] "A Filter Approach to the AC Bus Systems," R. Oruganti, EE6400 Project Report, Virginia Polytechnic Institute and State University, June, 1985.

[8] "Effects of Load on the Performance of a Mapham Resonant Inverter," F. Tsai and F. Lee, Virginia Polytechnic Institute and State University, 23rd IECEC Conference Record, September, 1988.

[9] "EASY5 Engineering Analysis System User's Guide," Boeing Computer Services Company, April, 1983.

[10] "Computer Modeling and Simulation of a 20kHz AC Distribution System for Space Station," F. Tsai and F. Lee, 22nd IECEC Proceedings, 1987.

[11] "Main Inverter Unit (MIU) Distortion Test Report," R. Sundberg, A. Brush, and A. Patterson, NASA PIR 220, November, 1988.

[12] "Frequency Domain Model for Analysis of Paralleled, Series-Output Connected Mapham Inverter Pairs," A. Brush, R. Sundberg, and R. Button, 24th IECEC Conference Record, August, 1989.

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15. Supplementary Notes

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16. Abstract

Output voltage total harmonic distortion (THD) of a 20kHz, 6kVA Mapham resonant inverter is characterized as a function of its switching-to-resonant frequency ratio, f_s/f_r, using the EASY5 Engineering Analysis System. EASY5 circuit simulation results are compared with hardware test results to verify the accuracy of the simulations. The effects of load on the THD versus f_s/f_r ratio is investigated for resistive, leading, and lagging power factor load impedances. The effect of the series output capacitor on the Mapham inverter output voltage distortion and inherent load regulation is characterized under loads of various power factors and magnitudes. An optimum series capacitor value which improves the inherent load regulation to better than 3% is identified. The optimum series capacitor value is different than the value predicted from a modeled frequency domain analysis. An explanation is proposed which takes into account the conduction overlap in the inductor pairs during steady-state inverter operation, which decreases the effective inductance of a Mapham inverter. A fault protection and current limit method is discussed which allows the Mapham inverter to operate into a short circuit, even when the inverter resonant circuit becomes overdamped.

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