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Advanced Modulation Technology Development for Earth Station Demodulator Applications

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INTRODUCTION

This report is prepared by Harris Government Communications Systems Division for NASA Lewis Research Center under contract NAS3-24681. This report is written in response to SOW paragraph 3.7.3, Final Report. The purpose of this document is to provide a summary of the entire contractual efforts, pertinent results, and a compilation of the task reports.

1.0 Task I Report

The Task I Report describes the refinement of the proposed downlink modulation system design concept. It develops in detail the specific modulation scheme used, the conceptual design for the Earth station demodulator hardware implementation, and an assessment of the impact of future technology on system performance.

2.0 Task III Breadboard Evaluation Report

This report describes the test results for the A/D converter breadboard developed during Task III and was written in response to SOW paragraph 2.3.5. Task III was the breadboard development phase of the program.

3.0 Task V Design Review Package

This section contains the material presented at the Task V final design review. This material is in vu-graph format and describes the POC Model Demodulator and the Special Test Equipment (STE) detailed design. Included are descriptions of the design and layout, functional performance, size, weight, power, and results of functional performance analyses.

4.0 Coded 16-ary CPFSK Coherent Demodulator Paper

This section contains a paper which was published in the Proceedings of the Mobile Satellite Conference, sponsored by the Jet Propulsion Laboratory. It is a summary of the conceptual design and design implementation for the modulation system developed in response to the requirements of this contract.

5 0 Task VII Report

The Task VII Report provides the results of POC Model Testing and Analyses. The purpose of this document is to present the results of the tests conducted in accordance with the POC Model Test Plan and Procedure developed in response to SOW subtask 2.5.3. The POC Model Test Plan and Procedure is included in the Task VII Report. This report also provides recommendations for the development of an engineering model demodulator using further advanced implementation technology, based on analyses of test results.

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NAS3-24681

ADVANCED MODULATION TECHNOLOGY DEVELOPMENT

TASK I REPORT

APRIL 4, 1986

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1. DETAILED DEVELOPMENT OF THE MODULATION SCHEME

This section of the task one report details the development of the modulation scheme chosen to fulfill the requirements given in the Statement of Work (SOW).

1.1 Modulation Scheme Comparisons

The selection of the modulation/coding scheme proposed by Harris, and the corresponding implementation thereof has been based primarily on:

1. Demodulator simplicity
2. Achieving a transmitted spectral shape whose power outside of the .5 bit rate point is 20 dB down from the desired signal power
3. Achieving a 5×10^{-7} bit error rate performance with the required Eb/No as close as feasibly possible to that of QPSK
4. Operating through a non-linear TWT
5. Utilizing a coding scheme that creates minimal spectral spreading and yet is powerful enough to meet the 5×10^{-7} bit error rate

Careful attention has been paid to perform proper tradeoffs based on these criteria that would substantiate the proposed modulation/coding scheme and its implementation. The intent of this section is to summarize the most important of these tradeoffs.

A wide assortment of bandwidth efficient modulation techniques exist within the industry [1]. Some of these, like Minimum Shift Keying (MSK), have been developed [2] within the industry in general whereas others like Continuous Phase Frequency Shift Keying (CPFSK) have been specifically developed at Harris [3].

The first categorization of these techniques occurs when considering the envelope variations of the transmitted waveform. Techniques that impart

data onto a carrier through its phase or frequency, are constant envelope signals whereas a signaling scheme that imparts data onto the carrier amplitude clearly exhibits envelope variations. A candidate in the latter category is M-ary Quadrature Amplitude Modulation (MQAM) which has been shown [3] to have greater power efficiency than schemes such as CPFSK or M-ary Phase Shift Keying (MPSK) which are in the constant envelope category. However, time-varying envelope signals require a linear RF channel which proves to be power inefficient in a satellite TWT that must be backed-off to provide such linearity. In this present TDMA downlink the minimization of signal distortion may require a 10 dB backoff which in our opinion is too great a price to pay in lost link margin for the increased bandwidth efficiency. Therefore this first tradeoff concluded that only constant envelope signals would be acceptable because of the power inefficiencies caused by the TWT backoff.

Another technique that was considered is to generate a constant envelope signal that is amplified by the transmit TWT and then filtered to shape the spectrum. The modulation scheme shown in Figure 1.1-1 was considered relative to the Statement of Work (SOW) requirements. As shown, a 200 Mb/s QPSK constant envelope modulation is employed through the power amplifier (PA) so that the nonlinear AM/AM and AM/PM characteristics given in the SOW can be tolerated.

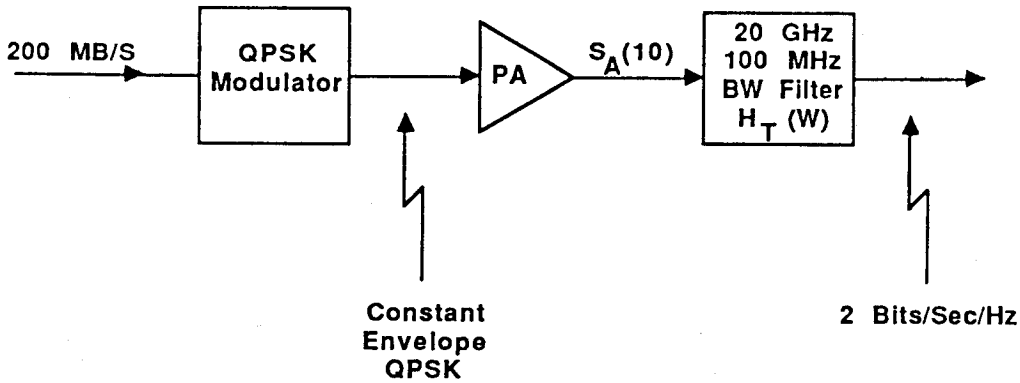


Figure 1.1-1 An Alternative Modulator Approach

After the amplifier, the spectrum is of course still that of QPSK, i.e.,

$$S_A(w) = \frac{\sin(2\pi f/ f_B)}{2\pi f/f_B} \tag{1}$$

where, f = frequency removed from the carrier

f_B = Bit rate = 200 Mb/s

The first nulls of this spectrum are at ± .5 Bit rate, i.e., in the center of the adjacent channel and consequently the main lobe will cause too much adjacent channel interference. Thus, additional filtering is required after the PA.

An approach that is attractive at first glance is to duobinary shape the spectrum after the amplifier. There are several ways of performing this spectral shaping. Irregardless of how it is done, the overall combination of transmit and receiver filtering must result in a net filter of:

$$H_{dB}(w) = \cos 2\pi \frac{f}{f_B}, \quad |f| < .25 f_B \tag{2}$$

$$= 0 \quad , \quad \text{elsewhere}$$

One way to perform the filtering is to do the full duobinary shaping at the transmitter, i.e., squeeze the spectrum of eq. (1) to give $H_{dB}(w)$ in eq. (2). This requires a transmit waveguide filter after the PA with the transfer function:

$$H_T(w) = \frac{2\pi(f/f_B)}{\sin(2\pi f/f_B)} \cos(2\pi f/f_B) \ , \quad |f| < .25f_B \tag{3}$$

$$= \qquad 0 \qquad , \quad \text{elsewhere}$$

The transmit filter in eq. (3) causes 3 dB of power loss just due to spectral truncation of the (sinx)/x spectrum out of the PA. In addition, there is power loss due to midband insertion loss of the filter. The sum of the 3 dB spectral loss and the insertion loss is a loss in link margin and reduces the efficiency of prime power consumption that can be critical in the satellite environment.

In addition, if the full duobinary shaping is done at the transmitter, the receive filter theoretically must have an ideal sharp cutoff at $\pm$ .25 f_B with a flat response across the band. Consequently, the effects, on performance and on adjacent channel interference rejection, of a more realistic receiver filter needs to be carefully considered.

Another approach to obtaining the duobinary shaping after the PA is to equally divide the filtering between the transmitter and the receiver. This leads to a transmit filter of,

$$H_T(w) = \frac{2\pi(f/f_B)}{\sin(2\pi f/f_B)} [\cos(2\pi f/f_B)]^{1/2} \ , \quad |f| < .25f_B \tag{4}$$

and a receive filter of:

$$H_R(w) = [\cos(2\pi f/f_B)]^{1/2} \ , \quad |f| < .25f_B \tag{5}$$

With the transmit filter of eq. (4), 2 dB of spectral truncation loss occurs, plus the filter midband insertion loss.

If well-known duobinary precoding techniques are used and simple "slicer" receivers are used to receive the duobinary signal created at the receiver, 3 dB of theoretical performance loss occurs relative to QPSK occurs with full duobinary shaping at the transmitter (given one can build a reasonable approximation to the ideal sharp cutoff filter required at the receiver without much additional loss). The performance loss for the equal filter division case with the simple slicer receiver is 2.2 dB theoretical.

Making use of Viterbi algorithm demodulation concepts, it is possible to recoup most of the performance losses relative to QPSK (3 dB and 2.2 dB in the full and equal filter division cases, respectively). Such an approach would involve building two 100 MHz (= symbol rate) 2-state Viterbi processors (one for each of the quadrature detector outputs).

Table 1.1 shows the summarizing data concerning the performance of employing duobinary signaling to meet the SOW objectives. From the columns showing degradation in received signal-to-noise ratio (SNR) requirement relative to QPSK, the simpler slicer receivers do not provide the needed performance. This leaves the Viterbi receivers, which obtain the required performance, but require 100 Mb/s 2-state Viterbi demodulators on each of the quadrature detector outputs. The 100 Mb/s high rate may be a bit of an implementation problem, but the 2-state Viterbi demodulator is not conceptually complex.

Table 1.1 Duobinary Summary Data

Duobinary Filter Division	S_T Spectral Truncation Loss, dB	L_I Filter Insertion Loss, dB	S_T+L_I Net Link Margin Loss, dB	RCVR Type	Theory: QPSK Degrad. Loss, dB
Full Xmit	3	1-2	4-5	Viterbi	-0
Full Xmit	3	1-2	4-5	Slicer	-3
Equal Xmit/RCVR	2	1-2	3-4	Viterbi	-0
Equal Xmit/RCVR	2	1-2	3-4	Slicer	-2.2

The desirability of this constant envelope QPSK through the PA followed by tight filtering reduces to consideration of the importance of these factors:

1. At best, 3 to 5 dB of link margin will be lost due to the transmit filters.
2. The modulator required is a 200 Mb/s QPSK modulator.
3. The demodulator is a 100 MHz symbol rate quadrature demodulator followed by 100 Mb/s 2-state decoders on each rail.
4. Additional filters are required at the downlink modulators.

Other such filtering techniques can be done, but based on link margin losses, these techniques do not meet the objectives of power efficiency and thus our efforts are directed to constant envelope modulation waveform signals.

Based on this constant envelope decision, attention was then focused on those signaling schemes that modulate data unto the phase or frequency of a carrier. One of the more widely used forms of modulation is Phase Shift Keying (PSK). It's utility arises in power limited channels where binary PSK provides good Eb/No performance for a given bit error probability. However it's capability in bandlimited channels is remarkably poor because the first sidelobe, which peaks at 1.5 x bit rate, is only 13 dB down from the main lobe. In order to achieve the spectrum requirement of 20 dB down power outside of the .5 x bit rate point, an M-ary PSK scheme with $M > 32$ would be required. Assuming no intersymbol interference, signal power efficiency would drop some 18 dB from QPSK if $M = 64$. This power efficiency loss is deemed too severe, and thus eliminates PSK from further consideration. Attention was then turned toward Frequency Shift Keying (FSK) signaling schemes.

Conventional FSK signaling (conventional in that the tonal separation is equal to an integer multiple of the symbol rate) is by itself not a spectrally efficient modulation scheme. However, two modifications to the conventional FSK scheme can be made to minimize this inefficiency. The first is to reduce the tonal separation, or frequency deviation, thus compressing the spectrum and necessitating a coherent receiver. Secondly, instead of permitting phase jumps at the symbol transitions, phase may be forced to be continuous across the transition boundary. The latter modification produces what is well known to be continuous phase FSK, or CPFSK. A subset of this class of signaling schemes is MSK which is merely binary CPFSK with a frequency deviation ratio of .5. As seen in Figure 1.1-2 the only M-ary CPFSK schemes that have a chance of meeting the out-of-band requirements is one where $M \geq 16$. Both 8-ary CPFSK and 4-ary CPFSK (otherwise known as

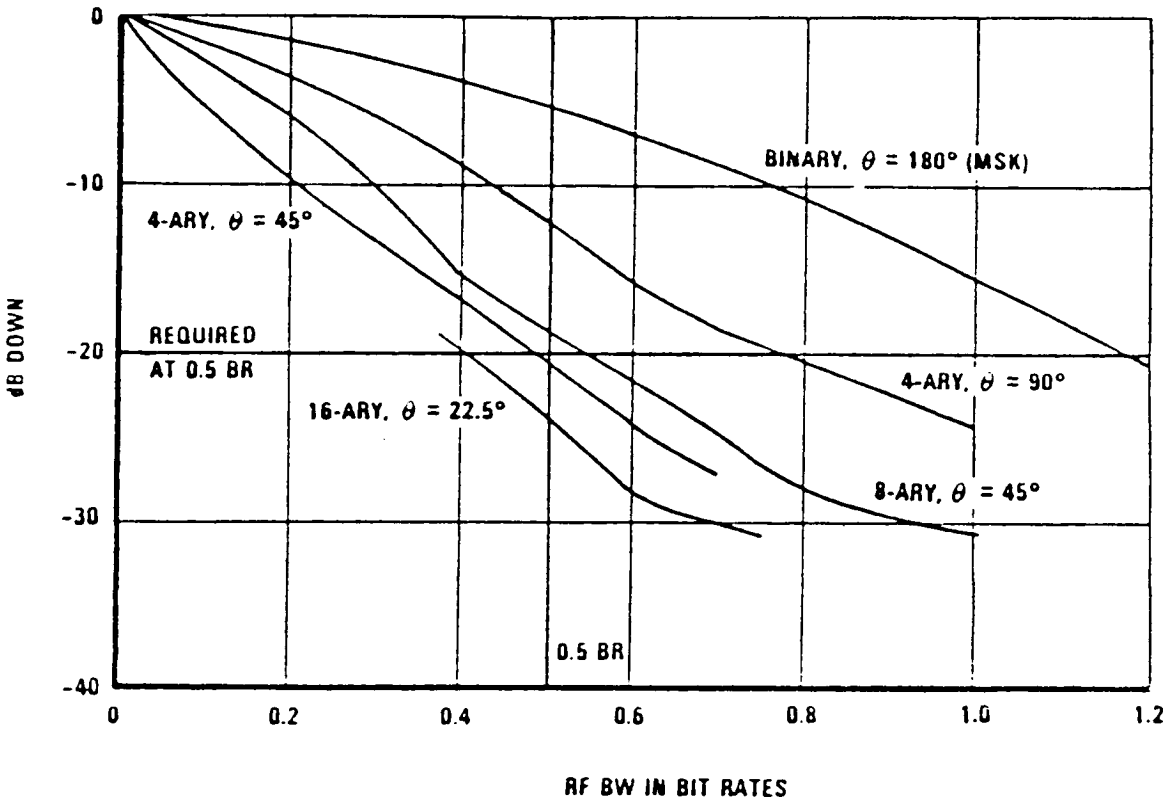


FIGURE 1.1-2 Spectral Characteristic of Uncoded CPESK

MSK/2) have out-of-band powers greater than the required 20 dB down from the desired signal power. Excluding intersymbol interference, the power efficiency loss relative to QPSK performance for 16-ary CPFSK is 13 dB. In comparison to PSK, CPFSK achieves the spectral requirement without filters but does so with a smaller power efficiency. Therefore, 16-ary CPFSK was chosen as the most likely signaling scheme capable of successfully meeting the QPSK performance when coding is added.

It is unfortunate that when forward error correcting coding is required in many systems, it is applied only as an afterthought by appending it to an already defined modulation format. For instance, the application of a rate 1/2 convolutional code, which is quite common, to an 8-ary FSK modulation format, seems congenial on the surface. However, each FSK symbol contains 3 coded bits thus making soft decision generation somewhat unhandy. On the other hand if a rate 1/3 code where used, the soft decision generation is now quite straight-forward, and if desired, more powerful symbol decoding could be performed in the decoder. This latter case is an example of a conscious marrying of a coding technique to a modulation format. Applying such a conscious effort to the bandlimited/power limited channel is an extremely high priority design focus. In fact we believe it is one of the most novel approaches toward consciously marrying modulation and coding in that we do not waste precious bandwidth to squeeze out tenths of dB's in performance. On the contrary, we use a moderate amount of coding (33% band spreading) but place it in that part of the modulation waveform where it is going to yield the greatest coding gain. This novel and Harris-patented (License rights owned by the Government) approach codes only the LSB's of a CPFSK symbol since errors are usually made to nearby signals in the signal space. Any coding to correct extremely low probability noise events (those

that cause errors in distant signals in the signal space) is a waste of bandwidth. An additional benefit of this coding technique is the hardware savings it provides by not requiring a decoder sync since symbol timing coincides with the decoder timing.

The coding technique which we developed on the 1979 RADC-sponsored Study [5] is almost identical to that investigated by researchers at the University of Virginia [6,7] in conjunction with M-PSK modulation on a study sponsored by NASA/LeRC. Unlike the MPSK schemes, however, our approach using coded 16-CPFSK modulation requires no additional spectrum shaping filters to achieve 2 bits/sec/Hz adjacent channel operation. In addition, the shaped spectrum signal of our coded 16-CPFSK modulation is of constant envelope, and thus avoids all nonlinear amplifier problems.

For the same number of coder states, the coded 16-PSK approach is theoretically 2 dB more power efficient than our coded 16-CPFSK approach solely on the basis of received SNR. However (and this is very important) the 16-PSK scheme will have to use post amplifier filtering to trim the (sinx)/x spectrum to meet the adjacent channel operability requirements of the SOW. If pre-amplifier filtering is proposed with the coded 16-PSK signal, the backoff required to prevent sidelobe restoration after the nonlinear PA will be excessive from a link power efficiency standpoint. Even with post amplifier filtering, the 2 dB theoretical advantage of the coded 16-PSK approach will be offset by the insertion loss of the required filter. We believe our constant envelope coded 16-CPFSK approach, in requiring no filtering, is the better approach from the overall link power efficiency and equipment simplicity standpoints and thus will be adopted as our baseline.

The final trade-off area to be discussed is the demodulator implementation. When using CPFSK it is possible to perform data detection

over multiple symbols because of the memory introduced into the waveform by forcing phase continuity during symbol transitions. While this multiple-symbol detection provides greater power efficiency [8], it carries along with it the necessity to perform a large number of matched filter correlations in a Viterbi-like, maximum-likelihood, sequence estimator algorithm [9]. For 16-ary CPFSK with a detection over just 2 symbols, 256 (16^2) individual correlations would need to be performed. This is contrary to the objective of demodulator simplicity and furthermore it only gains about 2 dB at an uncoded error rate of 10%. Therefore we have chosen to perform a simpler multi-symbol observation phase detection. Now, once we made this decision we further discovered that we could use a simple, Harris proven [10] technique of phase sampling and thus eliminate the need for 16 separate matched filters. A negligible performance difference at low error rates further enhances this phase sampling technique over the matched filter approach.

Listed below is a summarization of what these major tradeoffs have produced:

1. 16-ary CPFSK is the least complex, bandwidth efficient modulation format capable of meeting the out-of-band power requirement.
2. Multiple symbol detection with a Viterbi-like, maximum likelihood sequence estimator is not warranted from a complexity viewpoint although it does slightly increase power efficiency.
3. Multi-symbol observation detection is performed with a simple, and Harris proven, phase detector technique.
4. A Harris patented, bandwidth efficient coding technique has been creatively matched with 16-ary CPFSK to provide coding gain where it is needed most.

1.2 Rationale for the Scheme Selected

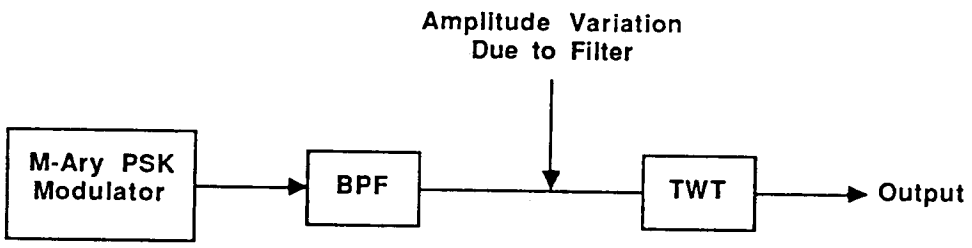
The selection of our approach was driven by key factors from both the SOW and the evaluation of system requirements for optimizing overall modulation technique performance. The key considerations in the selection of the signaling scheme are given below.

1. Constant envelope signaling provides maximum transmit TWT efficiency
2. Any filter at the satellite will dissipate power by spectral truncation and insertion losses, and will thus reduce link margin since the TWT is peak limited
3. Coding gain is necessary, but must be applied efficiently
4. Hardware simplicity is critical for cost effective implementations in the 1990's

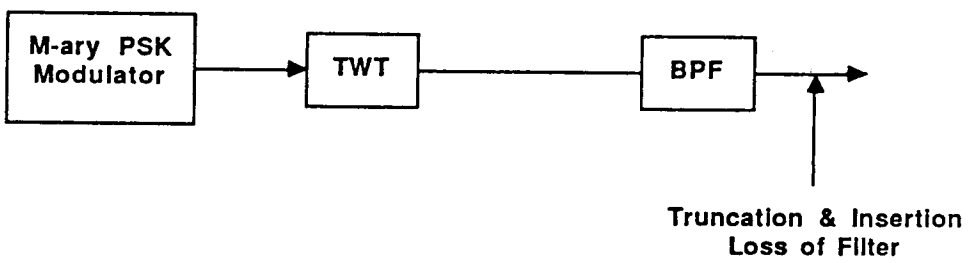
Any combination amplitude and phase modulation scheme will require backoff of the TWT from its saturation point and will decrease the overall link efficiency. Therefore, the only parameters left for the modulation are the phase and/or frequency of the signal.

M-ary PSK has been considered by Harris and other researchers [6] for applications such as this. With proper coding, near-QPSK level performance can be attained. The difficulty with PSK is that the rapid changes in phase result in bandspreading of the energy which must then be filtered for adjacent channel performance. The energy loss of the required filtering process is directly applied to link margin and must be considered when evaluating the modulation scheme. To illustrate this consider Figure 1.2-1. In A the signal is filtered prior to the input to the TWT. However, the signal now has amplitude variation due to the filter and the TWT must operate in the linear region (i.e., backoff from saturation) which decreases the average power and efficiency of the satellite output. In B the input to

the TWT is a constant envelope signal; the filtering is accomplished at the output. The filter truncates the spectrum and dissipates the power from insertion losses. In either case A or B, the power transmitted from the satellite is reduced by several dB and the overall system link margin is decreased.



A. Filtering Prior to TWT



B. Filtering After TWT

Figure 1.2-1 Transmit Filtering

The bandwidth problem of PSK is solved by utilizing a CPFSK approach. As shown in Figure 1.1-2, the modulated spectrum is adequate for transmission with no filter and the only remaining selection is the size of the transmit alphabet for bandwidth compression. Additionally, a unique

constraint of the phase progression of the signal resulted in a powerful coding gain for system performance.

Knowledge of the good spectral properties of our proposed CPFSK signaling is, of course, not unique to Harris. Many efforts have been directed here and elsewhere at trying to improve the performance obtainable with CPFSK modulation. These efforts have involved attempts to shape the phase trajectories and an exploitation of the coding-like gains available with multisymbol observation optimum receivers. Multisymbol observation is available with CPFSK because of the continuity of RF phase in the transmitted waveform that makes the present time symbol depend on previously transmitted symbols. Impressive, tantalizing performances are obtained for some of the CPFSK schemes. Their only drawback is the complexity of the optimum Viterbi algorithm demodulators required to get at the performance.

The uniqueness of the Harris demodulation approach resides primarily in the way we have managed to sidestep the complexity of the optimum demodulator, yet still retain most of its performance. We have done this by developing a multisymbol observation phase detection receiver that is simple, yet obtains performance within 2 dB of the optimum multisymbol observation Viterbi type of demodulator. Our simple phase detector approach (see the Harris proprietary addendum) allows relatively narrowband filtering (1/2 bit rate BW) ahead of the phase detector, and needs no intersymbol interference corrector to obtain its impressive performance relative to the complicated optimum receiver. Thus our coherent phase detector technique exploits the coding-like gains inherently available in the CPFSK signaling format.

The way in which we apply coding with low (33%) bandspreading, yet still obtain impressive coding gain is another unique feature of our

approach. We developed this coding strategy on a 1979 study for RADC [5]. Essentially the same coding approach in connection with M-ary PSK modulation is proposed in 1982 [6] and 1984 [11] papers by researchers at the University of Virginia. Their work was at least in part sponsored by NASA/LeRC. We prefer our coded 16-CPFSK approach over a coded 16-PSK approach for reasons detailed in paragraph 1.1.

Conceptually, we believe our approach of overlaying coding on the spectrally compact CPFSK signal to improve its performance is a practically important and enlightened one. Unlike some other ongoing research efforts that attempt to circumvent the limitations of simple CPFSK through the choice of more complicated phase trajectories (multimod index, cosine shaping instead of linear shaping of the trajectories, partial response shaping on the trajectories, etc.), our approach simply lives with the distance structure inherent in standard CPFSK and then improves it with coding. From the implementation standpoint, we believe our approach is superior.

1.3 Detailed Description of the Modulation Scheme Developed

The technique for accomplishing the performance requirements of the SOW is a modulation scheme pioneered by Harris and known as Continuous Phase Frequency Shift Keying (CPFSK). The scheme is a refinement of the well-known Frequency Shift Keying (FSK). CPFSK is a modification of FSK which provides spectral efficiency by reducing the frequency deviation and constraining the phase to be continuous across symbol transition boundaries. At the beginning of a symbol, the transmitted frequency is chosen at the modulator to be 1 of 16 possible transmit frequencies (for 16-CPFSK). This resulting frequency is transmitted for the duration of the symbol and the process is repeated for

each symbol transmitted. Because of the memory induced into the waveform by forcing the phase continuity, a mapping function that relates the modulator four bit (1 of 16) input to the transmitted phase value at the end of a symbol time can be generated. By computing a running count on phase, the modulator can project what frequency must be transmitted to force the output phase to exactly hit the desired phase node (value) at the end of a symbol time. This frequency is then sent across the link and a demodulated phase constellation such as shown in Figure 1.3-1 is generated. This variation on the transmit frequency selection is transparent to the overall performance of 16-ary CPFSK but is the key to the application of coding for performance improvement.

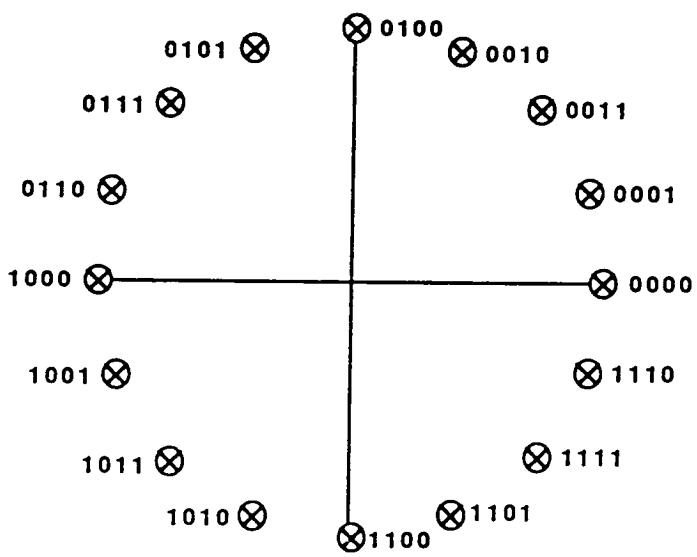


Figure 1.3-1 Demodulated Phase Constellation

The input data stream is demultiplexed, in the modulator, into three data streams (see Figure 1.3-2) in which the Least Significant Bit (LSB) is convolutionally encoded R=1/2, K=7. The corresponding four bit output

determines the frequency that will be sent by computing the necessary frequency deviation to arrive at the desired phase node. From this, it can be seen that the two Most Significant Bits (MSB's) determine the quadrant of the transmitted phase (at the end of a symbol) and the LSB's determine the position within a quadrant. For the bit assignments shown in Figure 1.3-1, any group of 4 adjacent phases contain all possible combinations for the two bits from the coder (i.e., LSB's). Further, within the set of any four adjacent phases, antipodal code branches (e.g., 00 and 11, or 10 and 01) produce phases differing by 45° and orthogonal branches (e.g., 00 and 01, or 10 and 11) produce phases differing by at least 22.5°. These properties are used in the Harris approach to provide coding gain that results in near QPSK performance.

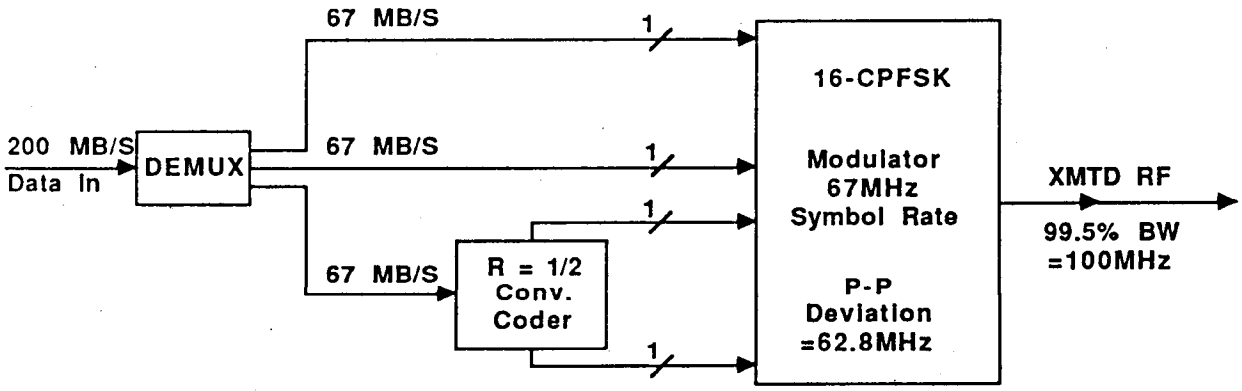


Figure 1.3-2 CPFSK Modulator

The spectral output power density versus bandwidth is shown in Figure 1.1-2 for 4-ary (also known as MSK/2), 8-ary, and 16-ary CPFSK. From the SOW, it can be derived that adjacent and co-channel interference requirements equate to a spectrum shaping requirement that the energy outside of the 0.5 bit rate bandwidth, be -20 dB relative to the total

signal power. As can be seen in Figure 1.1-2, 16-ary will provide the spectral shaping performance without transmit filtering. In addition, the 16-ary exceeds this requirement by a sufficient amount to allow 20-30% bandspreading to accommodate coding for overall system performance gain.

The combination of information coding in both the transmitted frequency and the phase state at the end of a symbol time, results in a signal that makes maximum use of the occupied system bandwidth. This unique spectral efficiency also supports maximum system power efficiency in two aspects. First, the resulting signal is constant envelope and thus the transmit TWT can be saturated for peak performance. Secondly, the transmit spectral shaping is inherent in the scheme and requires no filter which conserves power that would be lost in filtered spectrum truncation and insertion losses. This holds true whether the transmit filters are incorporated before or after the TWT since peak power available determines the link margin.

If baseband pulse shaping is incorporated into the modulator, further increases in spectral efficiency may be achieved at the modulator output without spectral filtering of the IF. In figure 1.3-3 we show the spectra produced at the modulator output for different choices of the modulator baseband pulse shaping filter. The curve for square pulses corresponds to standard 16-CPFSK signalling with 16 equispaced frequencies at a spacing of 1/16 of the symbol rate. The other curves are for various alphas on a square root of Nyquist filter with a raised cosine frequency characteristic. The far sidelobes are significantly reduced with the non-square pulse shaping baseband filters. The adjacent channel is located at 1.5 symbol rates from center (or .5 bit rate for our 3 information-bit/symbol scheme). We are contemplating the use of an $\alpha = .25$ baseband filter to control adjacent channel interference.

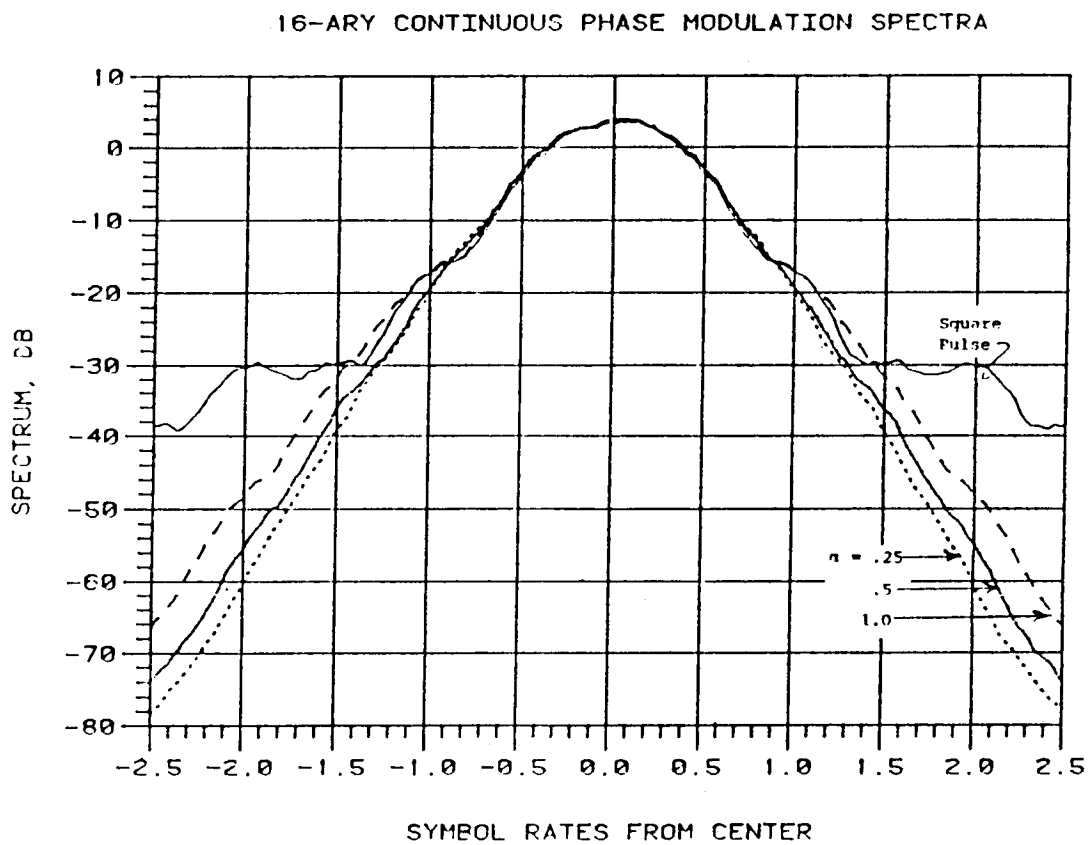


Figure 1.3-3 16-ary CPFSK Modulation Spectra for Various Baseband Filters

1.4 A Description of the Method and Estimated Speed of Independent Burst Acquisitions

Here we will provide answers to the TDMA burst acquisition problems. The problems to be addressed are as follows:

1. How is the coherent phase detector circuitry jammed to the correct value at the beginning of a burst?
2. What are the effects of frequency offsets on the acquisition strategy?
3. How is the symbol timing derived for each burst?
4. How is the 1msec. TDMA frame timing derived?

Figure 1.4-1 illustrates our concept of a single TDMA burst (a TDMA frame, which lasts 1 msec. in time, may consist of one or more bursts). As can be seen by Figure 1.4-1 a single TDMA burst consists of three components; a preamble (32 symbols = 96 bits), a unique word (6 symbols = 18 bits), and data ($\geq$ 32 symbols). The answers to the above questions all hinge on the special preamble we are considering to support all the timing functions.

PREAMBLE	UNIQUE WORD	DATA
32 Symbols	6 Symbols	≥ 32 Symbols
96 Bits	18 Bits	≥ 96 Bits

Figure 1.4-1 A Single TDMA Burst

The preamble must provide for initial phase acquisition, and initial symbol timing. In the following paragraphs we will address the methods by which phase and timing are acquired.

Figure 1.4-2 shows the phase modulation applied during the preamble we have selected. As shown, the preamble corresponds to an alternating frequency modulation between $\pm$ peak deviation = $\pm$ 15/32 symbol rate. The dotted line shows the rise that will occur for the center frequency input with no frequency offset. We will simply sum the 32 samples of this phase error over the preamble and divide by 32 to get the average phase error relative to the lowest frequency reference.

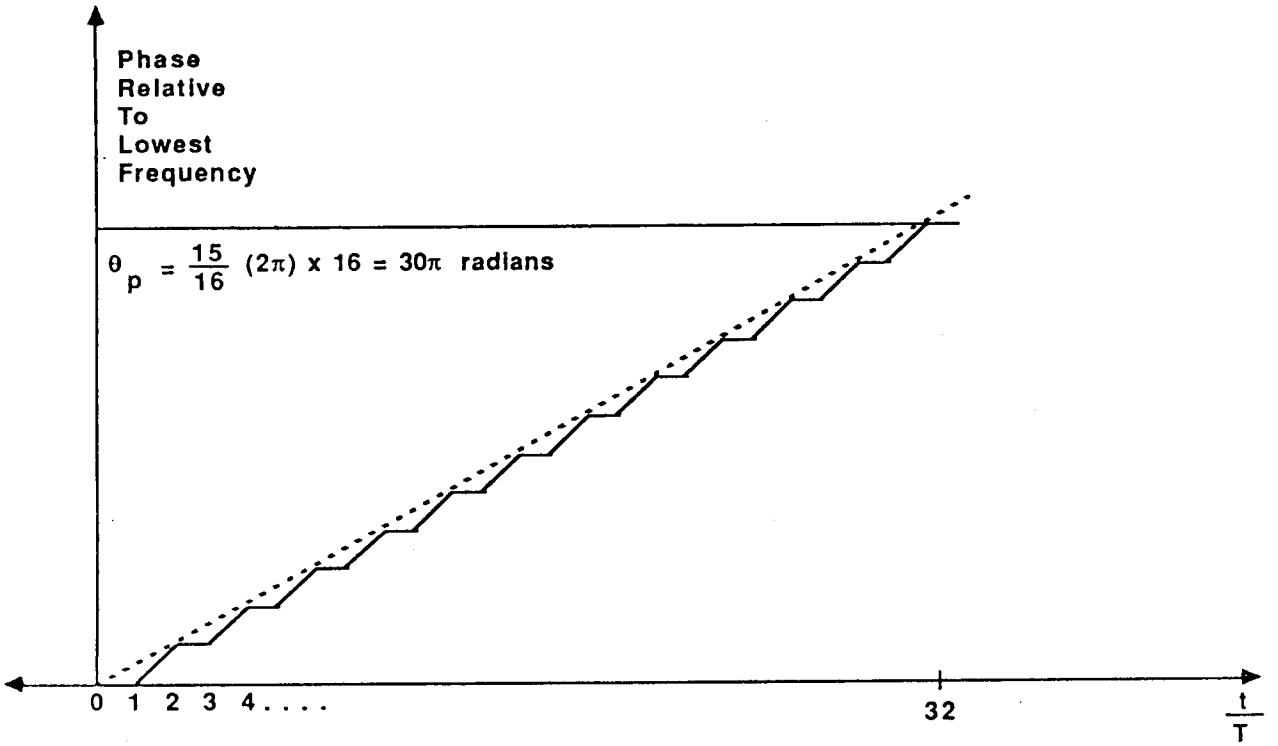


Figure 1.4-2 Phase Modulation During Preamble

There remain questions about how well does this "phase jam" strategy work in the face of noise and initial frequency offset. First, how accurately can the initial phase be acquired in the face of channel noise? Since we are averaging 32 samples to arrive at an estimate of initial phase error, the variance of the phase jitter on the estimate is 1/32 of the variance on each of the individual phase measurements over the preamble. Thus the phase jam procedure will have only a small impact on overall performance, causing about 10 $\text{Log}_{10}(1 + 1/32)$ = .13 dB degradation in noise performance. Secondly, what is the impact of initial IF frequency offset on the phase jam strategy? For a 30 GHz uplink, 10 GHz satellite translation, a 20 GHz downlink, and negligible doppler, assuming 5×10^{-7} L.O. stabilities everywhere, the initial frequency offset is:

$$F = (30 + 10 + 20) \times 10^9 \times 5 \times 10^{-7} = 30 \text{ kHz.}$$

The effect of this 30 kHz offset is to cause the preamble phase given by Figure 1.4-2 to ramp linearly up (or down, depending on the sign of the offset) over the 480 nsec. preamble, from zero to:

$$\Delta\theta = 30 \times 10^3 \times 480 \times 10^{-9} = .0144 \text{ cycle} = 5.2^\circ$$

Since the phase error increases linearly from 0 to 5.2°, the average of phase over the preamble is changed by 2.6°. This means that when peak frequency offset occurs, our phase jam is 2.6° in error. Whether or not this is of concern depends on which SNR at which we are operating. At 12 dB Eb/No, the SNR in the half-bit rate IF is 15 dB. The noise caused phase jitter on our signal at that point is:

$$\theta_s^2 = \frac{1}{2(\text{SNR})} = \frac{1}{2(31.6)} = .0158 \text{ rad.}^2$$

or $\theta_s = 7.2^\circ$ RMS.

Thus, 2.6° of error in the phase jam due to frequency offset is not negligible, but should be tolerable with no more than about .5 dB degradation before the baseband loop removes it, which for a 1 MHz loop bandwidth or more, takes less than lusec., or < 64 symbols.

We have already described above a technique for acquiring initial phase for our loop during the special preamble. However, that technique does not acquire initial frequency offset, which is approximately 30 kHz. Therefore, the second order phase lock loop is left with the task of acquiring this 30 kHz frequency offset after the phase is jammed by the procedure described above. We will make use of Figure 1.4-3 to specify a loop bandwidth, F_N, that will acquire the 30 kHz of frequency offset with little phase pull during such acquisition.

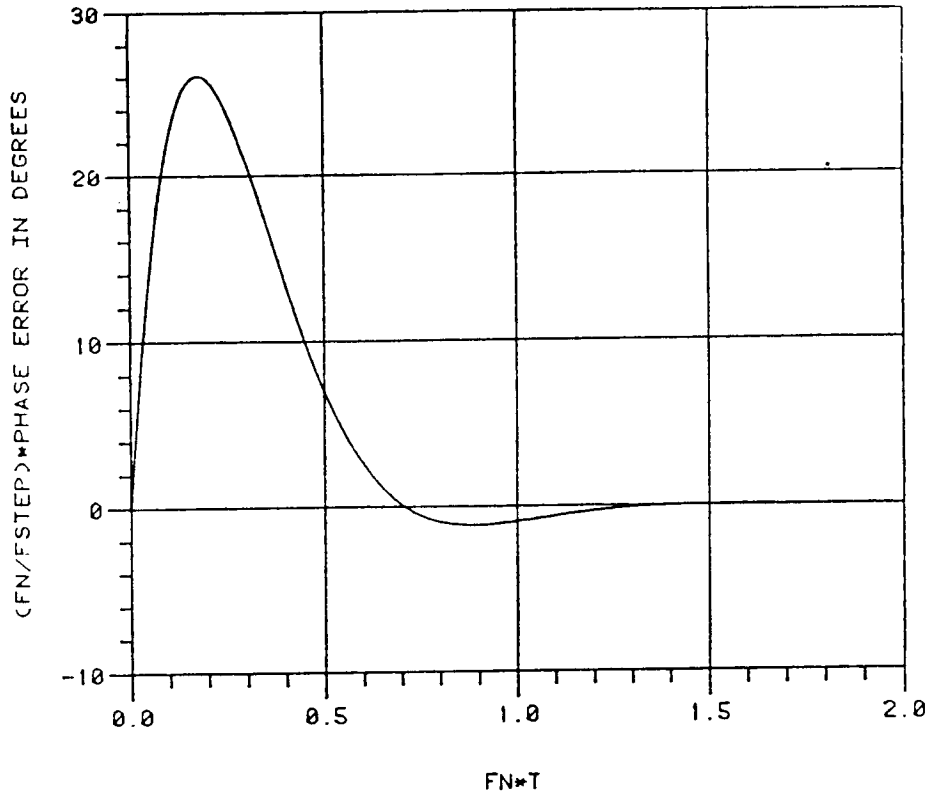


Figure 1.4-3 Transient Phase Error for a Frequency Step In Versus FN*T for a Second Order PLL with Zeta = .707

As shown in Figure 1.4-3, the peak phase error induced by the offset, F_{STEP}, in a ξ = .707, natural frequency = F_N loop is described by:

$$\frac{F_N}{F_{STEP}} \theta_{e,pk} = 26^o \tag{6}$$

From eq. (6), it can be seen that the key to holding peak phase error, $\theta_{e,pk}$, to a small value is to choose F_N large relative to F_{STEP}. If we choose, during the acquisition of a 30 kHz frequency offset, to hold peak phase error to 1° (which will have a negligible impact on the performance of our modem), then F_N must be:

$$F_N = \frac{F_{STEP}}{\theta_{e,pk}} \times 26^o = \frac{30 \times 26}{1} \text{ kHz} = 780 \text{ kHz} \tag{7}$$

As a baseline, we will assume an F_N = 1 MHz. Of course, the wider the loop bandwidth, the larger the channel noise induced phase jitter. The noise bandwidth of a second order loop is given by:

$$B_L = \frac{W_N}{2}\left(\xi + \frac{1}{4\xi}\right) = \frac{W_N}{2}\left(.707 + \frac{1}{4(.707)}\right) = 3.33\ F_N$$

where, F_N = natural frequency of the loop (Hz)

ξ = loop damping factor

The loop signal-to-noise ratio SNR_L, is:

$$SNR_L = SNR_{if}\ \frac{BW_{if}}{B_L} \tag{8}$$

where, SNR_{if} = IF signal-to-noise ratio

BW_{if} = IF bandwidth

B_L = loop equivalent noise bandwidth

In our system, for

BW_{if} = 0.5 x bit rate = 100 MHz & F_N = 1 MHz,

Then eq. (3) yeilds

$$SNR_L = SNR_{if}\ \left(\frac{100}{3.33}\right)$$

$$SNR_L = 30.0(SNR_{if}) \tag{9}$$

The variance of phase jitter due to channel noise in the loop is,

$$\theta_L^2 = 0.5/(SNR_L) \quad (rad^2), \tag{10}$$

and on the signal in the IF is,

$$\theta_{if}^2 = 0.5/SNR_{if} \quad (rad^2). \tag{11}$$

From eqs. (9), (10), and (11) one obtains

$$\left(\frac{\theta_L^2}{\theta_{if}^2}\right)^2 = \frac{1}{30.0} = .033 \tag{12}$$

Equation (12) shows that for a 1 MHz loop, the reference loop jitter is negligible relative to the IF signal jitter. Performance loss with the loop jitter given by eq. (12) would be:

$$\text{Loss} = 10\ \text{Log}_{10}\left[1 + \left(\frac{\theta_L^2}{\theta_{if}^2}\right)^2\right]$$

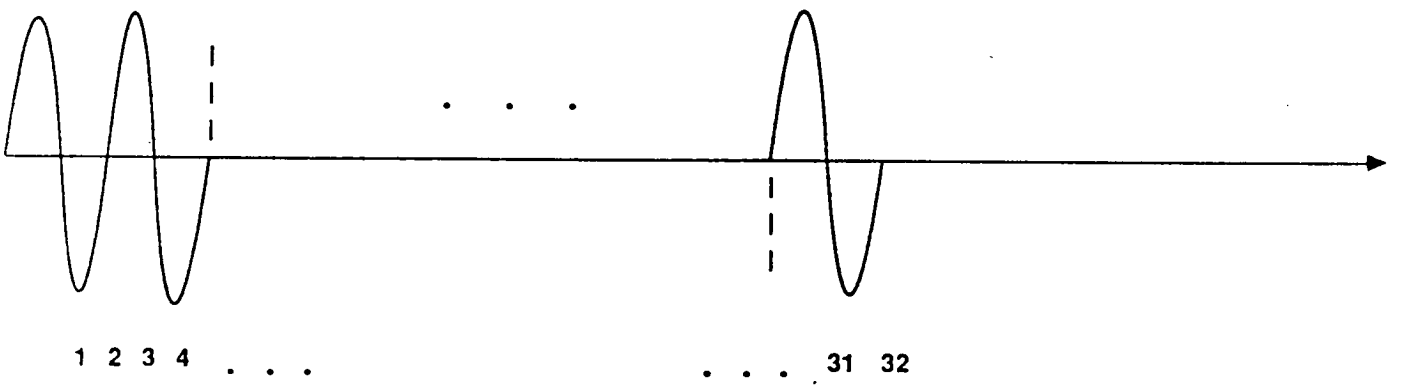
$$= 10\ \text{Log}_{10}(1.033)$$

$$\text{Loss} = .14\ \text{dB}$$

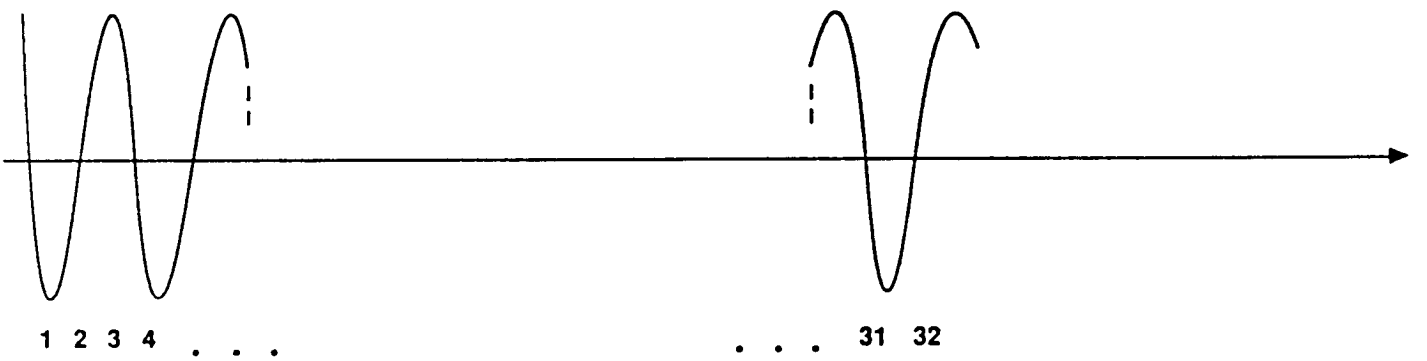
From this analysis, we have concluded that a loop bandwidth of approximately one (1) MHz should be considered. Since we contemplate a digital loop filter implementation, loop filter bandwidth changes will be easy to experiment with.

Now we will describe the method whereby symbol timing is derived for the independent burst transmissions. The symbol timing function must be performed by observing the preamble and must provide around 1% of symbol time setting accuracy at the end of the preamble time.

The frequency modulation applied during the preamble, as shown in Figure 1.4-4 (a), alternates between + peak deviation and - peak deviation. The peak deviation is (15/32) SR, where SR is the symbol rate. We propose here a scheme that observes the frequency detector output during the preamble time with a correlator (probably a surface acoustic wave device) with an impulse response equivalent to that shown in Figure 1.4-4 (b). The frequency response of this correlator is passband centered around half symbol rate = 33.33 MHz with noise bandwidth of (symbol rate)/32 = 2.08 MHz.



(a) Frequency Modulation During the Preamble



(b) Correlator Impulse Response

Figure 1.4-4 Symbol Timing Waveforms

The noise out of the frequency measuring circuit has a parabolic spectral density given by:

$$N(f) = \frac{(f)^2}{2(SNR_{if})BW_{if}} \tag{13}$$

The spectral density at the center frequency (half symbol rate) of the correlator is, therefore:

$$N(SR/2) = \frac{(SR)^2}{8(SNR_{if})BW_{if}} \tag{14}$$

The noise over the 2.08 MHz noise bandwidth of the correlator is, for all practical purposes, constant at the density given by eq. (14). Therefore, the noise power out of the correlator is:

$$N_c = \frac{(SR)^2(2.08\ MHz)}{8(SNR_{if})BW_{if}} \tag{15}$$

Since for our system, BW_{if} = 100 MHz, we have from (15):

$$N_c = \frac{(SR)^2(2.08)}{8(SNR_{if})(100)} = \frac{.0026(SR)^2}{SNR_{if}} \tag{16}$$

The SR/2 clock signal has peak deviation = (15/32) SR or signal power out of the correlator when the preamble fills it, of:

$$S_c = (\frac{15}{32}\ SR)^2/2 \tag{17}$$

From eqs. (16) and (17) we obtain a correlator signal-to-noise ratio (SNR_c), of:

$$SNR_c = \frac{S_c}{N_c} = \frac{(15/32)^2/2}{.0026}(SNR_{if}) = 42.3(SNR_{if}) \tag{18}$$

The jitter on the SR/2 clock has variance

$$\theta_j^2 = \frac{1}{2(SNR_c)} = \frac{1}{84.5(SNR_{if})} \tag{19}$$

and for Eb/No = 12 dB, SNR_{if} = 15 dB in our half bit rate IF. Since 15 dB = power ratio of 31.6, eq. (19) yeilds:

$$\theta_j^2 = \frac{1}{84.5(31.6)} = .00037$$

or

$$\theta_j = .019 \quad \text{radians} \tag{20}$$

Since pi radians of the SR/2 clock represents one symbol time, T, from eq. (20) we may obtain the RMS timing jitter from the correlator as

$$t_j = \frac{\theta_j}{\pi} T = \frac{.019}{\pi} T = .62\%(T)$$

Thus we meet out objective of better than 1% of T capability of jamming symbol timing phase at the end of the preamble.

This symbol timing strategy is not affected by DC offsets out of the frequency measuring circuit (since the correlator has no DC response). This procedure is also unaffected by AGC error. Thus the symbol timing is unaffected by either of the other two burst acquisition problems. Once the initial symbol timing phase is acquired, we will track it with a narrow band loop, observing the output of the frequency measuring device during the duration of the burst.

The following discussion will detail the sequence of events in acquiring access to the TDMA satellite network.

Our assumption is that the TDMA network is active when a new station desires entry onto the network. The TDMA channel has a master control station (MCT) burst interleaved with some number of other bursts from ground stations which have already gained entry on the network. Since the new station cannot even request service of the network until it acquires the MCT burst, a crucial task is to acquire the MCT burst.

As given above, the preamble correlator detects each preamble of a burst as it arrives. Upon burst detection, the 66.7 MHz symbol timing loop is jammed to the phase indicated by the next zero crossing after burst detect from the preamble correlator. After jamming the symbol phase, the loop develops a tracking signal as detailed in a previous discussion. The modem timing and control function now distributes symbol clock and timing signals required to sample the preamble-length delayed signal as well as direct the digital loop to perform burst acquisition and tracking functions as described previously. The coherent phase measurements made, within a burst interval but after the preamble, are delivered to the K=7 Viterbi decoder which performs the decoding of data as described in our proposal. By scanning the decoder output bit stream, we can detect the MCT unique word,

thereby providing our modem with the synchronized TDMA downlink 1 msec. frame timing. At this point, after no more than one (1) frame of TDMA reception, we will know all necessary information to gain access to the TDMA network.

For a fully operational TDMA satellite system, we have described the conceptual capability for our modem to perform all necessary acquisition and network synchronization functions. We have shown adequate capability to perform the following functions for independent bursts in the TDMA downlink:

1. Burst Detection
2. Symbol Timing Acquisition
3. Symbol Timing Tracking
4. Coherent Phase Acquisition
5. Coherent Phase Tracking
6. MCT Synchronization to allow synchronization of our uplink bursts into the uplink TDMA format

On the proof-of-concept (POC) modem, all functions except number 6. will be provided. Indeed, we cannot do 6. since that implies knowledge of network access protocols which are still under development.

However, we will provide a modem that can interface with equipment implementing any network access assignment and control protocols. Figure 1.4-5 shows the overall block diagram for our POC modem along with its inputs and outputs which will interface with the evaluation test beds at NASA/LeRC.

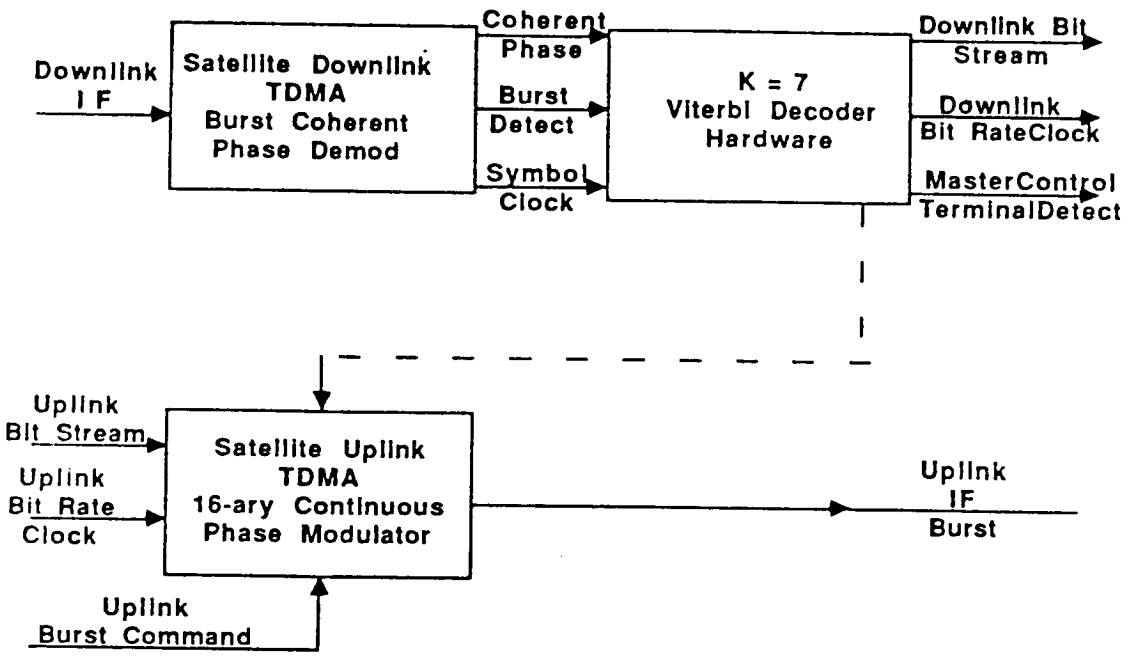


Figure 1.4-5 Overall Satellite TDMA Modem Block Diagram

The dotted line for the MCT detect pulse, which is necessary in an operational modem for timing and control circuitry in the modulator to synchronize uplink bursts into the satellite, will not be provided. Rather, as we understand it, the test bed will perform that function. The test bed is assumed to provide the signal "Uplink Burst Command" to trigger transmission of an uplink burst. Other inputs to the uplink modulator from the test bed include uplink bit stream and uplink bit clock. The uplink IF signal is output from the modulator to the test bed.

On the demodulator side, downlink IF is provided from the test bed to the demodulator. Coherent phase measurements along with burst detect and symbol clock signals are provided to our K=7 Viterbi error correction decoder per our proposal. Outputs from our demodulator to the test bed are thus; downlink bit stream, downlink bit rate clock, and MCT detect.

Therefore, the test bed at NASA/LeRC can use this modem for evaluation purposes, implementing any desired TDMA network access, assignment, and control protocols.

2. CONCEPTUAL DESIGN OF THE DOWNLINK MODULATION HARDWARE

In this section of the task one report the conceptual design of the demodulator hardware is presented along with simulation results. Some of the detailed hardware configurations are considered to be Harris proprietary and therefore, the reader will be referred to the proprietary addendum when appropriate. In addition to the topics given above, this section of the report will also discuss issues pertaining to producibility, reliability, maintainability, recurring costs, and special test equipment.

2.1 Downlink Modulation System Conceptual Design

Harris originally proposed a coded 16-CPFSK signalling scheme to meet the requirements for the NASA/TDMA satellite downlink. The coded 16-CPFSK signal was to be demodulated by a coherent phase measurement receiver using a phase-locked loop (PLL) IF implementation. During our task one investigations, we have still been considering the conceptually equivalent modulation and demodulation technique, i.e. a 16-ary continuous phase frequency shift keying modulator coupled with coherent phase measurement demodulation. However, our present baseline implementation approach is quite different. Also, there are some detail differences between our present approach and the proposed approach; primarily in the area of baseband waveshaping filters at the modulator and demodulator (see Figure 1.3-3). These detail differences have some advantage over our proposed approach and are available only because of our present implementation approach.

The most significant difference between our proposed implementation approach and our current baseline approach, lies in our implementation of coherent phase detection at the demodulator. Our current baseline uses a Harris-proprietary technique for coherent phase detection. Reasons for considering this approach include; (1) hardware simplification, (2) single rail processing as opposed to in-phase and quadrature (I & Q) dual-rail processing required in the proposed approach, (3) one high speed (67 Msample/sec.) A/D is required, (4) the coherent phase measurement is available directly from the single rail with no necessity for conversion from I and Q rail samples to phase as in our proposed quadrature demodulator, (5) baseband filter techniques at the demodulator, not available with the proposed approach, are applicable to the current approach, and (6) requirement for a 3 GHz IF PLL is eliminated by using our current baseline approach.

We believe that our current baseline approach offers the potential for significantly reduced hardware complexity relative to our proposed approach. We also believe that this technology is unique to Harris (We have never seen in the technical literature that our current baseline approach to obtaining coherent phase measurements is known elsewhere, and thus the need for the Harris proprietary addendum). By achieving our goals on this contract, this modem will represent a significant advance in modem technology.

Since our current baseline modem involves a departure from prior coherent phase measurement receivers, it is necessary to give a clear conceptual picture of our technique. Figure 2.1-1 illustrates our current baseline conceptual hardware design. The input to the modulator is a data stream, a bit rate clock, and a burst command. The output from the demodulator is a demodulated data stream, a bit rate clock, and 1msec.

timing marks. Thus, our modem may be used to implement any desired TDMA network access, assignment, or control protocols. The mathematical derivations of how we obtain coherent phase measurements from our current baseline approach, equivalent to an I and Q demodulator, is given in the proprietary addendum. Detailed block diagrams of the modem signal processing functions are also given in the proprietary addendum.

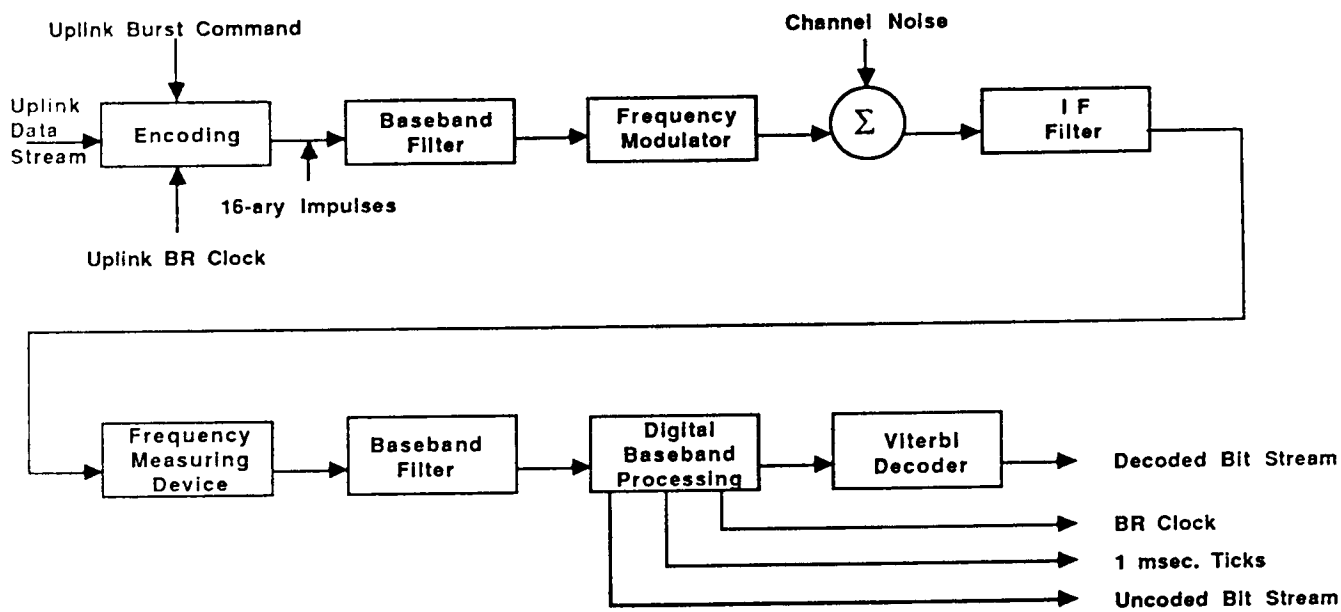


Figure 2.1-1 Current Baseline Conceptual Modem Hardware Block Diagram

2.2 Theoretical Performance Characteristics and Operating Conditions of the Downlink Modulation System Design Concept

In this section we present results obtained by computer simulations for the TDMA modem we have described conceptually in prior sections. These simulations were undertaken to evaluate the impact of several practical imperfections on our baseline modem. Some of these practical imperfections are not easily evaluated analytically, so the simulation results are necessary and valuable in assessing whether our unique coherent phase-measurement implementation technique leads to viable hardware.

Some of the effects we have investigated include; (1) the intersymbol interference caused by the bandlimiting IF filter, (2) effect of the A/D quantizing error in our baseband signal processing, (3) VCO modulation nonlinearity, (4) filter group delay distortion, and (5) the effect on performance of symbol timing offset.

2.2.1 Bandwidth Efficiency

In Figure 2.2.1-1 we show the spectra produced by our modem for different choices of the modulator baseband filter. The curve for square pulse signalling corresponds to standard 16-CPFSK signalling using 16 equispaced frequencies with spacing = 1/16 symbol rate. The other curves are for various alphas on a square root Nyquist filter with raised cosine frequency transfer characteristics. The far sidelobes are significantly reduced with non-square baseband filters. The adjacent channel is located at 1.5 symbol rates from center (or .5 bit rate for our 3 information bit/symbol scheme). We are contemplating the use of an alpha = .25 baseband filter to control adjacent channel interference.

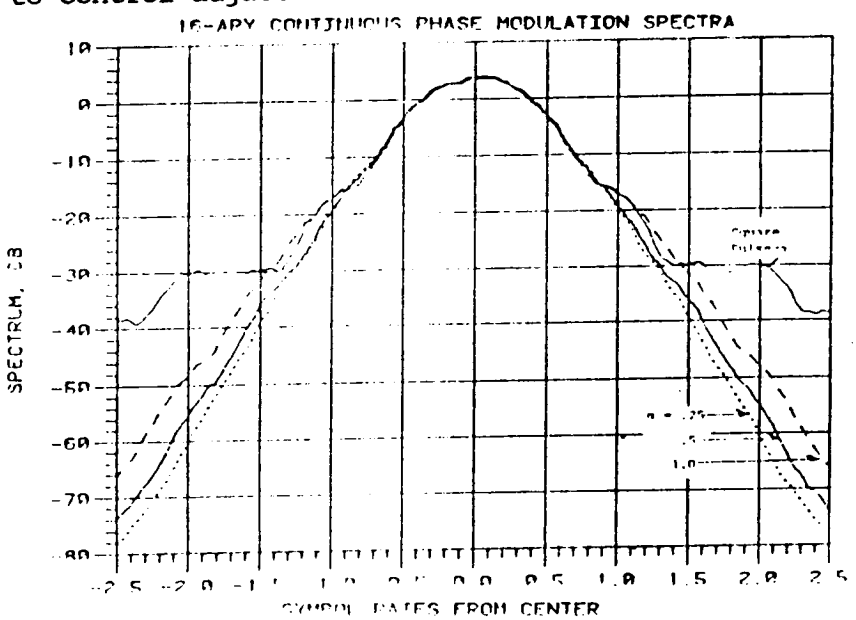


Figure 2.2.1-1 16-ary Continuous Phase FSK Modulation Spectra

Figure 2.2.1-2 shows the IF filter characteristic we are using. This filter has a -6 dB BW = 1.5 symbol rate = .5 bit rate = 100 MHz. We are currently investigating an implementation approach that will allow the use of a SAW device for the IF filter. Such SAW filters have desirable low group delay distortion, coupled with steep skirt selectivity.

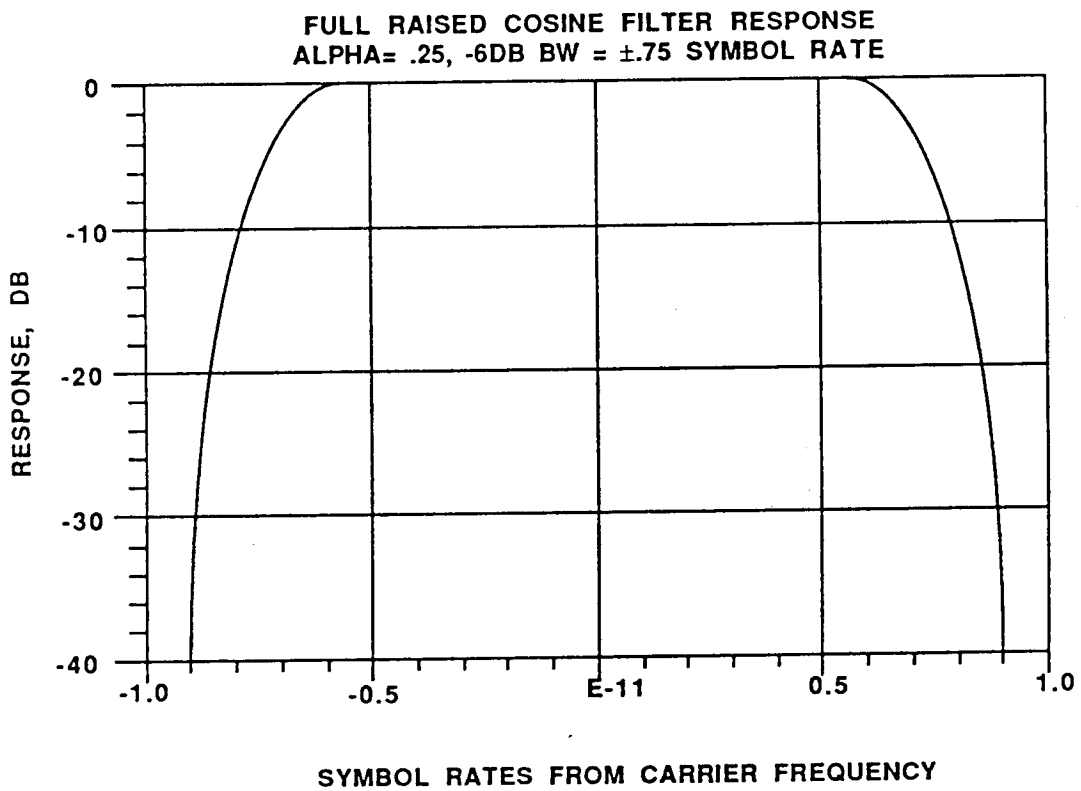


Figure 2.2.1-2 IF Filter Characteristics

2.2.2 Power Efficiency

Any filter at the satellite will dissipate power by spectral truncation and insertion losses, and will thus reduce link margin since the TWT is peak limited. Since our modulation scheme is constant envelope, the TWT may be operated at peak efficiency (saturation). In addition, our modulation scheme, as previously described, requires no transmit filtering and thus there are no spectral truncation or insertion losses at the satellite. For the same number of coder states, the coded 16-PSK approach is theoretically

2 dB more power efficient than our coded 16-CPFSK approach solely on the basis of received signal-to-noise ratio. However, the 16-PSK scheme will have to use post amplifier filtering to trim the (sinx)/x spectrum to meet adjacent channel operability requirements of the SOW. IF pre-amplifier filtering is used with the 16-PSK signal, the backoff required to prevent sidelobe restoration after the nonlinear PA will be excessive. If post amplifier filtering is used, the 2 dB theoretical advantage of the coded 16-PSK approach is offset by the insertion loss of the required filter. Therefore, we believe our constant envelope coded 16-CPFSK approach, in requiring no filtering makes highly efficient use of overall link power.

2.2.3 Bit Error Rate Performance

In this section of the report, bit error rate versus Eb/No will be given to illustrate the practical effects of various hardware elements, for both coded and uncoded operation.

Figure 2.2.3-1 shows a comparison of the uncoded error rate curves of our proposal and our new approach using the square root of Nyquist baseband filter and the IF filter given by Figure 2.2.1-2. The proposed scheme used square pulse 16-CPFSK and experienced large intersymbol interference (ISI) due to the bandlimiting IF filter. This necessitated, in our proposed scheme, the use of ISI correction circuitry to handle up to $\pm 22.5^{\circ}$ of phase error introduced by the IF filter. Because of the baseband pulse shaping filter, ISI is considerably reduced (without requiring ISI correction circuitry), and the performance curve labeled "New Scheme" in Figure 2.2.3-1 is obtained. From this work, we concluded that the ISI correction circuitry of our proposal could be eliminated, resulting in simpler hardware.

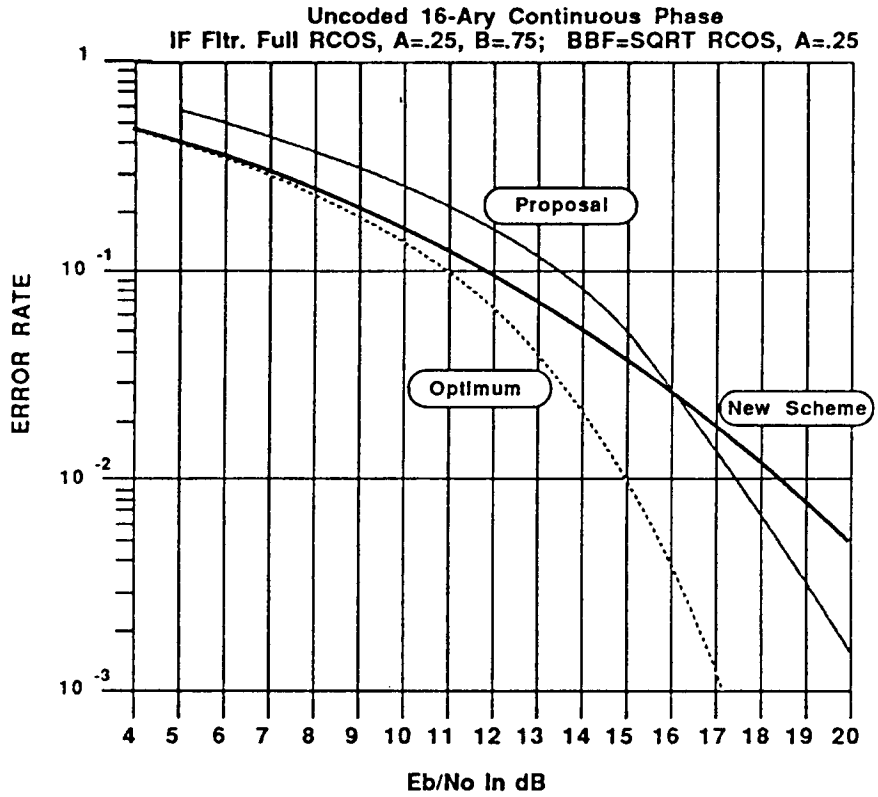


Figure 2.2.3-1 Performance Curve for the New Scheme Versus the Proposal

Figure 2.2.3-2 shows the result of a Monte-Carlo simulation of the uncoded error rate performance for a hardware implementation of our modem. The dotted curve is performance of an optimum Viterbi algorithm demodulator for 16-CPFSK. The solid curve is the analytical performance prediction for our modem. The dots are Monte-Carlo simulation points. Through computer modeling, the entire modulator/demodulator was simulated. Many sequences of data were sent for each value of Eb/No. Symbol errors were counted and the error rate computed by dividing the total errors by the total symbols sent. Important hardware parameters for the simulation were; (1) 8-bit A/D quantization assumed, (2) the linearity of the frequency measuring device was approximately .4%, (3) the phase jam strategy, described in section 1.4, was modeled, (4) the loops had a damping factor, zeta = .707.

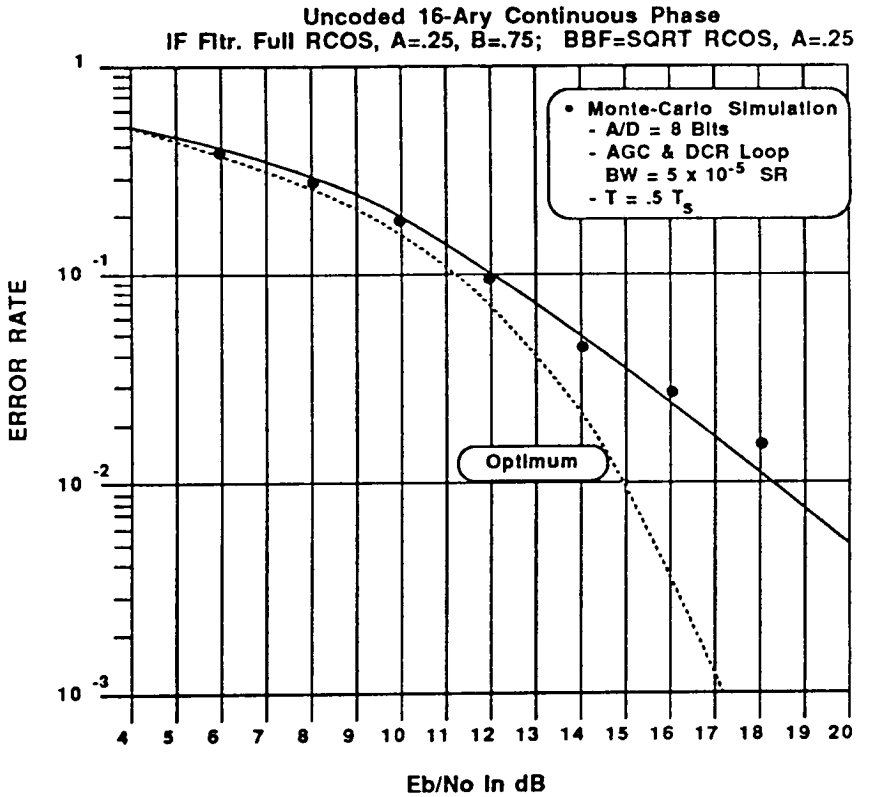


Figure 2.2.3-2 Uncoded Performance Derived from a Monte-Carlo Simulation

The results given in Figure 2.2.3-2 were encouraging and indicated that our new coherent phase measurement implementation could be achieved with realistic hardware. The close comparison between analytical results and Monte-Carlo simulation results also validated the analytical prediction.

We next produced the analytical performance prediction for the coded system using a K=7 rate 1/2 convolutional code in the fashion described in our proposal. The result is shown in Figure 2.2.3-3, where our proposal prediction assuming no ISI, our current baseline system with ISI, and QPSK performances are all plotted for comparison. We note that the prediction for the current baseline is within 2.7 dB of QPSK at 5×10^{-7} bit error rate. But it is approximately 1.4 dB worse than our proposal's prediction assuming no ISI. The loss is apparently due to the residual ISI. Perhaps some of the 1.4 dB loss relative to the proposal prediction can be recovered by careful

equalization of the baseband receiver filter. This remains under investigation.

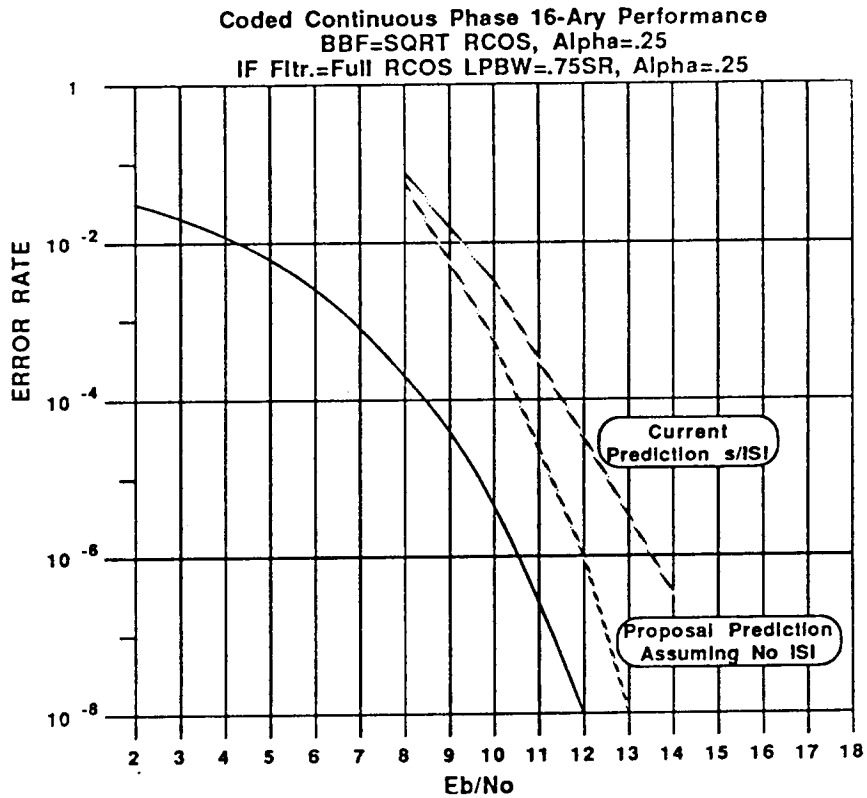


Figure 2.2.3-3 Coded Performance Prediction

2.3 "Ility" Data

In this section of the task one report several subjects will be discussed that have the "ility" suffix such as; producibility (including an estimate of recurring costs), reliability, and maintainability.

2.3.1 Producibility - Special Features for Lowering Costs When Produced in in Quantity

There are several hardware design features of our modem that can reduce the cost of producing it when large quantities are purchased. The most notable features are; the extensive use of digital circuits in the baseband processing, the use of surface acoustic wave (SAW) technology for filtering

applications, and the use of monolithic microwave integrated circuits (MMIC) for the IF signal processing.

Digital technology has and still is evolving at an incredible pace. Because of shrinking geometries, integration at the chip level is increasing while the gate capacitance is decreasing, leading to lower propagation delays. Also, the cost of producing complex parts keeps falling due to greater percentage yeilds over time and a ever increasingly competitive market. It is for these reasons that we have strived to construct a major portion of our modem using digital technology. In the POC model we will use standard ECL parts to implement a majority of the baseband signal processing functions. However, we envision either gate array and/or custom VLSI circuits to be used in the production models, both of which have great potential for low cost when quantity purchases are made. Even VHSIC technology, which could be used to implement the K=7 Viterbi decoder, will drop significantly in quantity prices over the next several years as that technology matures (see section 2.3.2 for detailed cost estimations). Finally, the use of digital technology in implementing our modem will eliminate many adjustments that would have to be performed during the production and test cycles which are labor intensive and costly.

We are considering the use of SAW technology to implement the IF filter, the preamble correlator, and a delay line. Because SAW devices are fabricated from a mask (in much the same way as digital devices), the filters, correlators, and delay lines built using SAW technology are very repeatable from device to device. That is, the characteristics, of a filter for example, remain very consistent between various runs of the device. In addition to repeatability, once the mask for a SAW device has been designed,

the fabrication process is very automated (non labor intensive) which leads to low cost per unit if the NRE is spread over a large quantity of units.

Monolithic microwave integrated circuits (MMIC) is a young technology that is maturing quickly. Currently, companies such as Pacific Monolithics are offering circuits such as a downconvertor on a chip that has an RF input range of 3 to 6 GHz and an IF output in the range of 50 to 2000 MHz. Each chip (part# - PM-CO0601-A) contains numerous components, such as RF and IF amplifiers, a local oscillator, an LO buffer amplifier, and a double-balanced mixer. This specific device is used as an example because we are considering it's use in the POC model and because it represents what type of circuits are available now in quantities for a cost a low as $20 per unit. Other functions are also available, including AGC amplifiers, limiting amplifiers, phase shifters, phase modulators, etc., all of which operate in the GHz regions. Since such powerful devices are currently available, it is not difficult to predict further integration levels, thus enabling even more complex MMICs to be fabricated. We anticipate that by the 1990's, the entire front-end IF chain of our modem will consist of one MMIC chip and one SAW filter on the corner of a PC board.

2.3.2 An Estimate of Recurring Costs

The recurring cost estimate is based on the conceptual design, built in quantity, in a manufacturing environment. No nonrecurring engineering costs are included.

Table 2.3.2 shows three costs: first the design using present discrete components, second the design using gate arrays presently available, and third the design using 1990's technologies.

Cost data was gathered from vendor quotes, current program costs with similar complexity designs, and Harris's VHSIC operations. Gate array performance was established using current issues of VLSI magazine (esp. December, 1985), and gate array development ongoing at Harris.

Table 2.3.2

Estimation of the recurring cost of the TDMA Demod in the 1990's:

FUNCTION	PRESENT	$	GATE ARRAY PRESENT	$	1990'S	$
Chassis	1	$ 600	Chassis	$ 600	1 Card	$ 300
Input RF	1 Card	$ 2,000	1 Card	$ 2,000	1 MMIC, 2 Saw	$750
Bit Sync	1 Card	$ 2,500	1 Saw, 1 VLSI(ECL, ASIC)	$ 500	1 Saw, 1 VHSIC	$650
Phase Detector	1 Card	$ 2,000	1 VLSI (ECL, ASIC)	$ 250	Part of Above	
Decoder	1 Card, 7 VHSIC IC's	$30,000	1 Card, 7 VHSIC IC's	$30,000	1 VHSIC	$400
		$37,100		$33,350		$2,100

2.3.3 Reliability

The reliability of our modem will be insured by several factors. The first factor to be considered is the parts that make up the whole, i.e., the components. To ensure component reliability, our preference for parts selection will be for those parts that have a proven reliable performance history, or for those parts similar to parts with a proven reliable history. In addition our preference will be toward those components that are multiple sourced. Finally, we will choose components that are capable of satisfactory performance over time and temperature, and are not stressed by the application, either thermally, electrically, or otherwise.

The second factor to be considered from a reliability standpoint is at the chassis level. First, the reliability of the overall box will be insured by a design that does not allow circuit damage due to improper control settings. Secondly, a thermal cutoff capability will be designed into the chassis. Finally, forced air circulation will be used to keep components well away from degrading or damaging temperature conditions.

2.3.4 Maintainability

The maintainability of our modem will be insured through thoughtful system level design considerations. Features that have already been "flagged" as important design considerations for the easy maintenance of our modem are items such as; status indicators, internal fault indicators, and easy access test points. In addition, thoughtful chassis layout in conjunction with connectorized cards will allow easy access to both cards and modules. Finally, chassis inputs and outputs will be designed for easy chassis interchange.

2.4 Overview of Special Test Equipment

The special test equipment that will be required for testing our modem is of the type that can be designed and fabricated "in-house". Figure 2.4-1 illustrates the system level concept of a test bed. The test bed consists of three modulators, a signal-to-noise ratio combiner, and a demodulator. The three modulators may be configured as co-channel or adjacent channel modulators which in either case share a common design. They may be operated in a CW or burst mode, with a fixed burst rate and a variable burst length. Each modulator will have internal data generators, and the ability to operate with external clock, data, and uplink burst enable signals.

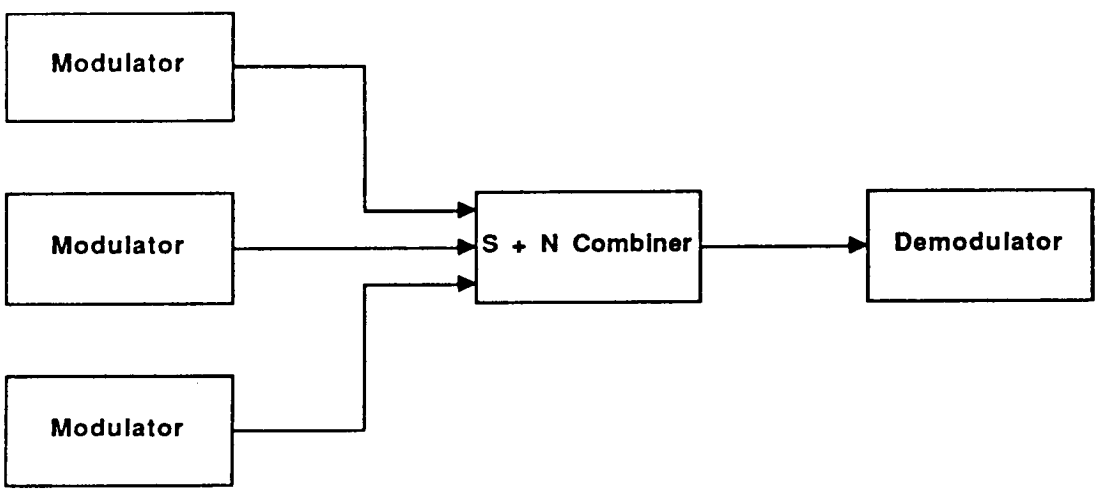


Figure 2.4-1 System Level Block Diagram

Figure 2.4-2 shows a block diagram of the signal to noise combiner. The signal-to-noise ratio combiner features; an internal noise source, variable signal attenuators, signal and noise combiner, burst rate and frame clocks.

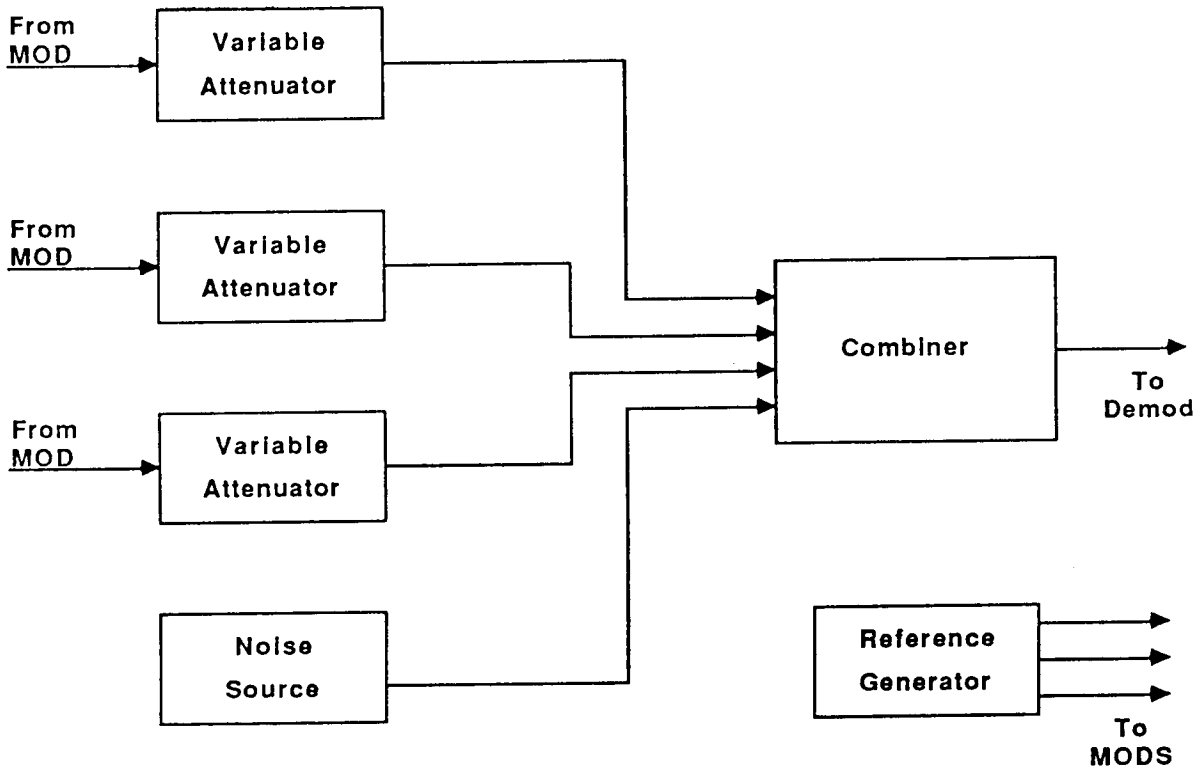


FIGURE 2.4-2 Signal to Noise Combiner Block Diagram

3. TECHNOLOGY ASSESSMENT AND DESIGN IMPACT

In this section of the task one report we will discuss the impact of technology on the design of our modem.

3.1 Current Versus Future Technology

Virtually all of the circuitry required to implement our modem is available now, except for the high rate K=7 Viterbi decoder. The question is, what form, or what type of technology will be utilized in the

construction of these circuits? For example, we propose using an analog VCO to switch frequencies with no abrupt change in phase at the symbol boundaries. However, in the future it will be possible (and advantageous as discussed later in this report) to perform the frequency modulation using a direct digital synthesis technique (i.e., NCO). In addition, baseband processing circuits that are now accomplished with SSI and/or MSI ECL devices may, in the future, be implemented in either VHSIC(.5u CMOS), VLSI(ECL gate arrays), or digital GaAs circuits with a high degree of integration at the chip level, enabling many functions to be performed by one device. The improvements that are realized by the future technology may be in performance (as in the case of the NCO implementation of the VCO), in reliability (as in the case of the SSI to VLSI transition), and/or in cost. To summarize the key technologies used in the modem and their current or future implementation strategies, respectively, see Table 3.1.

Table 3.1 Current Versus Future Implementation of Key Technology Items

TECHNOLOGY ITEM	CURRENT IMPLEMENTATION	FUTURE IMPLEMENTATION
Frequency Modulator	Analog VCO	Digital NCO
Frequency Detector	Bulk Analog	MMIC/SAW
IF Filter	SAW	SAW
Baseband Processing	SSI & MSI ECL	VHSIC, VLSI
Viterbi Decoder	Low Rate - SSI/MSI	High Rate - VHSIC

3.2 Hardware Techniques which Represent an Advancement in the State-of-the-Art in Modulation Technology

There are various hardware techniques incorporated into our modem which represent an advancement of the state-of-the-art in modem technology, some of which are listed in the proprietary adendum. Others include a high speed Op Amp, high speed A/D converter, high speed D/A converter, IF input filter, and 1/2 Nyquist lowpass filter. The Op Amp represents advanced technology in that a true differential amplifier is required that has a very large bandwidth and a very short settling time. The state-of-the-art in wideband Op Amps is defined by an amplifier with a -3 dB bandwidth of DC to 200 MHz, a settling time (to .02%) of roughly 10 nsec., and a slew rate of 7000V/usec. The A/D and D/A convertors represent the state of the art in conversion technology, again because of the high speed and large bandwidth requirements of our system. The present state-of-the-art in A/D conversion is a 100 Msample 6-bit A/D. The present state-of-the-art in D/A conversion is a 100 MHz 8-bit D/A. The IF filter represents an advance in technology in that conflicting specifications, such as very steep skirt selectivity coupled with almost absolute linear phase, must be met in one filter. The 1/2 Nyquist baseband filter advances modulation technology in that it reduces the sidelobe levels of the non-filtered CPFSK spectrum at the output of the TWT. For a more thorough description of hardware techniques that represent an advancement of modulation technology, the reader is referred to the Harris proprietary adendum.

3.3 The Impact of Technology on System Performance

There are a few technology areas that impact the performance of our modem. That is, as the technology progresses, we will be able to take advantage of the new technology, not only to decrease the cost of our modem, but to increase (slightly) it's performance relative to the current (POC) implementation. Listed in the following paragraph are the technologies that may affect system performance. Included in this discussion is the specific area of performance affected as well as the contributor.

The linearity of the frequency detector will impact the BER versus Eb/No performance of our modem. Our goal for the frequency linearity is 1 percent. As technology progresses, linearities of less than 1% may easily be realizable. The VCO linearity may also affect the BER performance of our modem. However, as technology allows an NCO to be implemented at the frequencies of interest, linearity will be of no concern in that an NCO is inherently linear. The VCO output power variation with frequency may impact BER performance. Our goal is to keep the power variation to within .25 dB, but again, an NCO would alleviate this problem. The ability to correlate with the preamble and quickly jam the symbol timing along with the RF phase will impact acquisition. As the ultimate speed of digital technology increases, the criticality of this timing issue is diminished. The large number of interconnections required in the baseband processing section with the use of SSI and MSI technology may impact reliability. However, as the implementation transitions from SSI/MSI to VHSIC and VLSI, the number of interconnections between parts as well as the total parts count will decrease, which will increase the reliability of the modem.

3.4 Advantages and Disadvantages of Implementation Technologies

In this section the advantages as well as the disadvantages of the previously mentioned technology is outlined. These technology items are; the frequency measurement circuit, the VCO, the NCO, and the baseband signal processing functions.

The advantage of using a frequency measuring circuit in the implementation of the demodulator is that it reduces the overall hardware design complexity of the demodulator. Thus, by reducing circuit complexity, a cost savings is realized both in the design effort (POC) and in future production runs (EDMs and beyond). The only disadvantage to the frequency measuring approach is the possible degradation (slight) in BER performance due to nonlinearities. Although, there are methods in which to linearize a frequency measuring device, of which we are currently pursuing to ameliorate the linearity problem.

The advantage of using a VCO as the continuous phase frequency modulator is that a VCO is presently available has suitable dynamic characteristics. The disadvantage of the VCO technology is the nonlinearity of voltage to frequency conversion (goal is < 1% nonlinearity) and the long term frequency drift of the VCO. An NCO, as previously touted, is inherently linear and it's frequency stability is as good as it's reference. However, an NCO is not currently available with an output center frequency capability of 3.373 GHz, and probably will not be available for some 2 to 5 years. Hence, the only disadvantage of the NCO technology is the availability of that technology.

The baseband signal processing functions are implemented using digital technology and therefore realize all the advantages that are inherent to threshold logic. These advantages include; stability over time and

temperature, a high degree of integration at the chip level, immunity to small cross-talk and noise signals, and finally, digital circuits lend themselves to all kinds of automated processes which reduce production, test, and maintenance costs. The only disadvantage of using digital circuits to implement the baseband processing functions of our demodulator are the high processing speeds at which we must operate (the sample rate = symbol rate = 67 MHz). This leads to technology such as ECL or GaAs to accomplish the required processing under worst case conditions with margin.

TECHNICAL REFERENCES

1. J. D. Oetting, "A Comparison of Modulation Techniques for Digital Radio", IEEE Transactions on Communications, Vol. COM-27, No. 12, Dec. 1979, pp. 1752-1762.

2. C. R. Ryan, A. R. Hambley, and D. E. Vogt, "760 Mbps Serial MSK Microwave Modem", IEEE Transactions on Communications, Vol. COM-28, May 1980, pp. 771-777.

3. Robert C. Davis, "An Experimental 4-ary CPFSK Modem for Line-of-Sight Microwave Digital Data Transmission," EASCON 1978, pp. 674-682.

4. P. R. Hartman, "Digital Radio Technology: Present and Future", IEEE Communications Magazine, Vol. 19, No. 4, July 1981, pp. 10-14.

5. Final Technical Report, RADC-TR-79-56, "Linear Modulation Techniques for Digital Microwave," Robert C. Davis, Harris Corporation, Study for Rome Air Development Center, August 1979.

6. S. G. Wilson, H. A. Sleeper, II, P. J. Schottler, M. T. Lyons, "Rate 3/4 Convolutional Coding of 16-PSK: Code Design and Performance Study", IEEE Tran. of Comm., Vol. COM-32, pp. 1308-1314, Dec. 1984.

7. Stephen G. Wilson, Paul J. Schottler, and Harry A. Sleeper, "Rate 3/4 10-PSK Phase Codes," ICC 1982, pp. 6 F.1.1-6F.1.5.

8. T. A. Schonhoff, "Symbol Error Probabilities for M-ary CPFSK: Coherent and Non Coherent Detection", IEEE Transactions of Communications, Vol. COM-24, No. 6, June 1976, pp. 644-652.

9. G. David Forney, Jr., "The Viterbi Algorithm" Proceedings of the IEEE, Vol. 61, No. 3, March 1973, pp. 268-277.

10. M. G. Palchat, R. C. Davis, and M. B. Luntz, Harris Corporation, "Coherent Demodulation of Continuous Phase Binary FSK Signals," in Proc. Int. Telemetry Conf. (Washington, D.C., 1971).

11. Joe Grabowski and Robert C. Davis, "An Experimental M-QAM Modem Amplifier Linearization and Baseband Equalization Techniques," National Telesystems Conference Record, November 1982, Galveston, TX., pp. E3.2.1 - E3.2.6.

NAS3-24681

ADVANCED MODULATION TECHNOLOGY DEVELOPMENT

HIGH SPEED A/D CONVERTER

BREADBOARD EVALUATION REPORT

SUBMITTED BY:

JAMES F. ROESCH, JR.

HARRIS GCSD

PREPARED FOR:

NASA LeRC

2.3.1 Breadboard Development Definition

2.3.1(a) The high speed quantizer (A/D) was a recommended breadboard item as presented at NASA LeRC during the Task II review.

2.3.1(b) Rationale supporting the need for breadboarding.

The high speed 8-bit flash A/D technology is very young. Only three 8-bit, 100 MHz converters are known to exist, with one of the three not yet a reality. Utilizing such new technology in such a critical function in our system, it was deemed necessary to evaluate and verify the performance of the technology relative to vendor specifications. In so doing, valuable information as to the proper utilization of the technology could be inferred for use in the detail design phase of the POC model.

2.3.1(c) A description of the objectives and approaches for breadboarding.

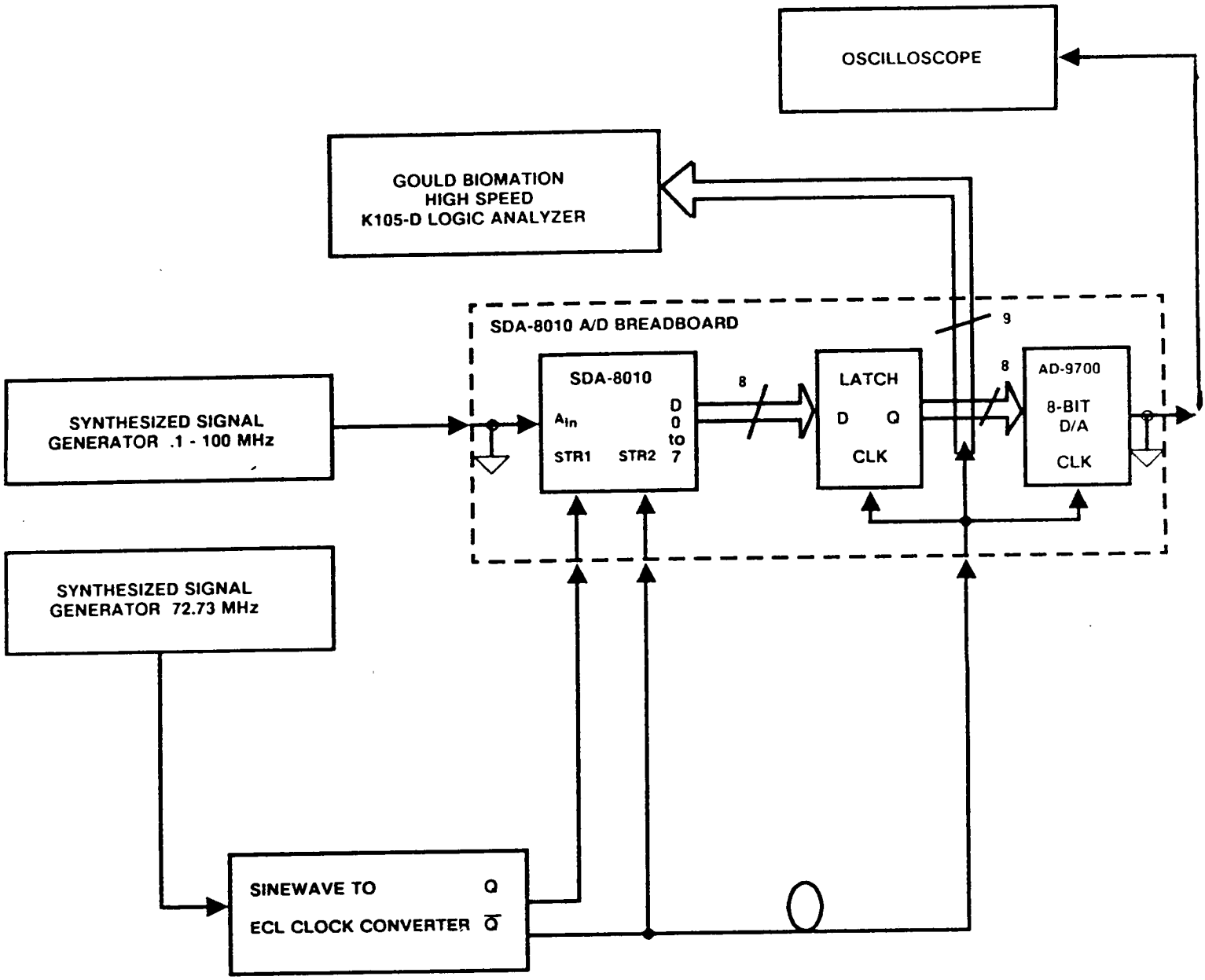
The objectives of the A/D breadboard phase are quite straightforward. They are:

(1) To verify accurate 8-bit resolution (1/2 LSB linearity) digitization of frequencies between DC to 50 MHz, at a sampling rate of 72.73 MHz.
(2) To verify the input bandwidth of the device.
(3) To experiment with the clocking scheme of the Siemens SDA-8010 A/D and verify accurate sampling with STR1 = CLK and STR2 = $\overline{CLK}$.

The approach taken to verify the above objectives is also quite straightforward. All necessary hardware will be built and tests conducted, as given in Section 2.3.2, to verify the major objectives outlined above.

Tests will also be performed as necessary to verify minor objectives pursuant to the major objectives.

A block diagram of the test bed including the SDA-8010 A/D breadboard is given in Figure 2.3.1.



A/D/0107X

Figure 2.3.1. SDA-8010 A/D Test Bed

2.3.1(d) Functional Requirements of the SDA-8010 A/D Breadboard.

The functional requirements of the SDA-8010 A/D breadboard as pertaining to the performance of the A/D itself may be found in Section 2.3.1(c). Other, more general functional requirements, pertain to interface and testability requirements. These requirements include separate inputs for the analog voltage input, the two clock inputs of the A/D (Strobe 1 and Strobe 2), and the system clock input that clocks the data latch and the D/A converter. Each of these inputs are connected via SMA connectors, and have the appropriate device pins terminated in the characteristic impedance of the stripline (50 ohms). A 50 ohm terminated analog output voltage is supplied via an SMA connector, while a digital representation of the input waveform is available directly at the output pins (Q or $\overline{Q}$) of the data latch.

2.3.1(e) Material Requirements.

SDA-8010 A/D Breadboard Parts List

Part Number	Qty	Description	Vendor
SDA-8010	1	8-Bit 100 MHz A/D	Siemens
AD9700BD	1	8-Bit 125 MHz D/A	Analog Devices
F100151	2	Hex D Flip Flop	Fairchild
--	5	SMA Connector	
OP07A	2	Op Amp	PMI
LM313	2	Bandgap Voltage Ref.	National Semi
VK-200	11	Low Freq. RF Choke	
M39018/01-0653M	8	4.7 F Elec. Cap	
CDR04BX104AKSM	25	0.1 F Chip Cap	
CDR04BXB92AKSM	10	3900 pF Chip Cap	
CMR03C100DOCM	2	10 pF Capacitor	
IN4149	3	Diode	
RNC55H2400FM	3	240 Ohm Res.	
RNC55H1002FM	2	10K Ohm Res.	

SDA-8010 A/D Breadboard Parts List (Continued)

Part Number	Qty	Description	Vendor
RNC55H4020FM	1	402 Ohm Res.	
RNC55H1000FM	8	100 Ohm Res.	
RNC55H49R9FM	13	49.9 Ohm Res.	
M39015/1-004WM	2	1K Ohm Pot.	
M39015/1-003WM	2	500 Ohm Pot.	
RNC55H1800FM	2	180 Ohm Res.	

2.3.2 Breadboard Test Plan and Test Procedures

2.3.2.1(a) Test Type.

Clock timing adjustment.

2.3.2.1(b) Objective of the Test.

The objective of the clock timing adjustment test is to find which pulse timing relationship for Strobe 1 and Strobe 2, hereafter referred to as STR1 and STR2, yields the best dynamic performance of the A/D. The goal will be to establish a simple relationship between STR1 and STR2 of CLK and $\overline{CLK}$. To provide a background on the strobe timing relationships of the Siemens SDA-8010 A/D, an excerpt from the SDA-8010 Technical Description will be given below.

2.3.2.1(c) Range of Test Parameters.

The range of test parameters associated with the clock timing adjustment are units of time measured in nanoseconds. There is probably an infinite number of ways that the clock signals STR1, STR2, and CLKL could be adjusted both in duty cycle and in relative delay between rising edges; however, only a few should be and will be considered. These are the pulse diagram of Figure 9, and that of setting STR1 = CLK and STR2 = CLKL = $\overline{CLK}$.

2.3 Clock circuitry

SDA 8010 is driven by two ECL clock signals Str 1 and Str 2 **(figure 9)**. The internal CLK1 and $\overline{CLK1}$ signals driving the first comparator stage are derived from Str 1. The pulse width of Str 1 affects the conversion characteristics. A duty cycle of 1:1 is recommended under normal 100-MHz operating conditions; for particulars refer to **chapter 4**.

The second signal Str 2 delivering CLK2 and $\overline{CLK2}$ is responsible for regeneration of the digital signals in the second comparator latches and influences the pulse shape of the output signals. The internal signals are latched during hold time $t_{H\,1}$ and $t_{H\,2}$ respectively. Thus the positive transition of Str 1 causes sampling of the analog signal after an aperture delay of approx. 3 ns. The output-signal transitions are determined by the rising edge of Str 2. The signal transition time $t_{d,Q}$ marks the time interval between the positive transition of Str 2 and the beginning of the data valid range $t_{V,Q}$ of the output signal. The data valid range in turn is related to the pulse width $t_{H\,2}$.

The duty cycle of Str 1 is limited by two effects. If the strobe time $t_{Str\,1}$ (see **figure 9**) is too small, the first comparator stage cannot settle to the new analog voltage in time and conversion errors increase. The upper limit of $t_{Str\,1}$ is dictated by the smallest hold time required to pass information to the second comparator latch. The setting of $t_{Str\,1}$ is not particularly critical, the limits being shown in **table 1**.

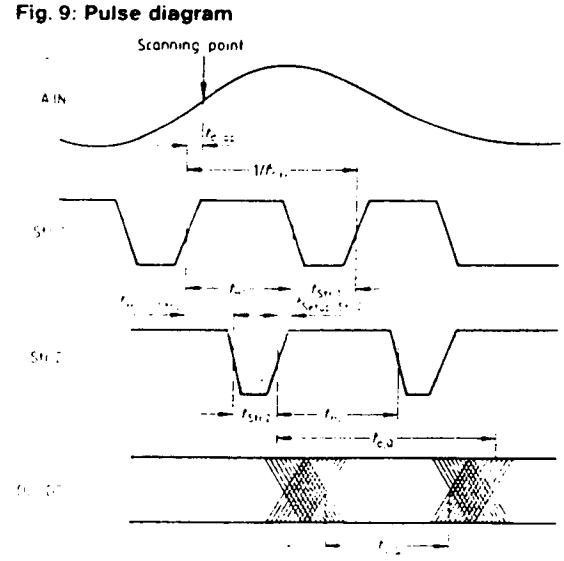
Table 1 Range of clock settings for operation over the whole temperature range. Characterization measurements were performed with typical settings.

	min	typ[1)]	max	
$t_{Str\,1}$	3.5	5	6.5	ns
$t_{Str\,2}$	4.0[2)]	3.5	4.5	ns
$t_{Setup,\,Str\,2}$	0	−1.5	−2.5	ns
$t_{Hold,\,Str\,2}$	1	3		ns

[1)] Recommended for normal operation at room temperature
[2)] At room temperature the minimum strobe width is 3 ns

In the digital section, accurate clock timing ensures easy handling of the 100-MHz output data stream. **Figure 13** gives recommended settings of the converter clocks together with the resulting output signals at junction temperatures of 30, 90 and 125 °C. Additionally the latch clock CLK_L for the external output register is shown. Valid data are assumed if the conversion of a 30-MHz/2-V_{pp} signal yields an *SNR* of greater than 40 dB at a conversion rate of 100 MHz. To achieve proper operation over the whole temperature range, latching of data into the output register must occur between 10.5 ns and 13 ns after the rising edge of Str 2. This can be achieved using ECL 100 K latches (e.g. 100150). If a larger range of valid data is required, temperature dependence has to be given to the latch clock CLK_L corresponding to the temperature dependence of the signal transition time $t_{d,Q}$ shown in **figure 10**.

Fig. 9: Pulse diagram



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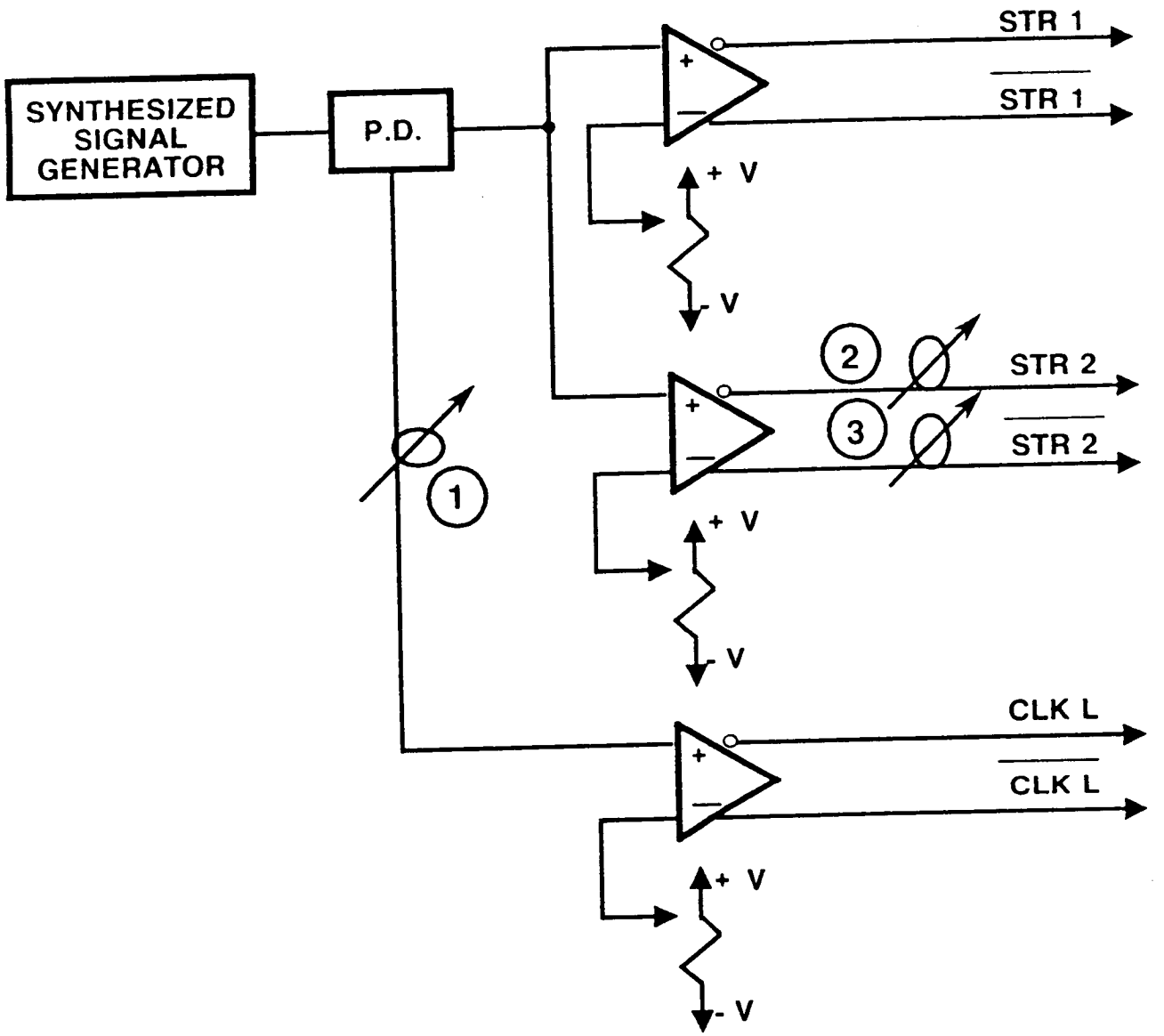

Figure 2.3.2.1. Clock Generator Block Diagram

2.3.2.1(d) Test Procedure

To find the optimum clocking scheme for the SDA-8010, a flexible clock generator circuit must be provided. A detailed block diagram of the circuit used to generate and adjust the clocks is given in Figure 2.3.2.1.

As given by Figure 2.3.2.1, the 100K ECL clock signals are derived from a single sinewave source by three separate comparator circuits. Each comparator has its own threshold reference so that the duty cycle of each clock may be independently adjusted. Also, a delay (trombone) line is added in the signal path leading to the CLKL comparator so that its rising edge may be adjusted relative to STR1 and STR2. Delays 2

and 3 depicted in Figure 2.3.2.1 are implemented by adjusting the length of coaxial cables, and function to adjust the rising edge of STR2 relative to Strobe 1.

The testing procedure will be to adjust the clocking signals STR1, STR2 and CLKL for various timing relationships, and simply observe the dynamic behavior of the A/D via a high speed logic analyzer. Timing relationships will be searched until good dynamic A/D outputs result such as; no missing or erroneous codes, and low waveform distortion (relates to good dynamic linearity).

2.3.2.2(a) Test Type.

Static Nonlinearity

2.3.2.2(b) Objectives of the Test.

The objective of the static nonlinearity test is to verify the vendor specification of $\pm 1/2$ LSB linearity error.

2.3.2.2(c) Range of Test Parameters.

With the positive and negative voltage references set at a magnitude of 0.75 VDC, the LSB weighting of,

$$\frac{+Vref + |-Vref|}{256} = 5.86 \text{ mV/LSB}$$

results.

Thus, the expected range of data points (in volts) between bit transitions is;

LSB weighting $\pm$ 1/2 LSB
= 5.86 mV $\pm$2.93 mV or
2.93 mV < expected data < 8.79 mV

2.3.2.2(d) Test Procedure.

The static linearity of the SDA-8010 will be measured by first accurately setting the positive and negative voltage references of the A/D to +0.75 and -0.75 DC respectively, to establish an LSB weighting in mV/LSB. Then a DC voltage will be applied to the analog voltage input of the A/D, taking note of the voltage value for which a stable numerical output results. This process will be laboriously repeated for the numerical outputs of zero to 255. The data taken can then be analyzed to verify the 1/2 LSB nonlinearity (or linearity error) specification given by the vendor.

2.3.2.3(a) Test Type.

Amplitude response of SDA-8010.

2.3.2.3(b) Objectives of the Test.

The objective of the amplitude response test of the SDA-8010 is verify the input bandwidth of the device.

2.3.2.3(c) Range of Test Parameters.

The output (numbers) of the A/D should fall off no more than approximately 0.2 dB over the input frequency range of DC to 45 MHz, for proper operation in our system. The baseband square root of Nyquist filter is down roughly 6 dB at 36.4 MHz, and falls off very rapidly beyond that frequency. The A/D frequency response remaining flat to 45 MHz ensures that the cascaded response of the baseband filter with the A/D (filter) is essentially that of the baseband filter.

2.3.2.3(d) Test Procedure.

The amplitude response of the SDA-8010 will be measured by three separate techniques.

2.3.2.3.1 The first technique will be that of keeping the voltage constant at the input to the device over the measured range in frequency. The response will be measured by measuring the numerical positive and negative peaks with a logic analyzer. These peaks will be recorded for several frequencies so that the frequency response of the SDA-8010 can be determined. A block diagram of the test setup is given below.

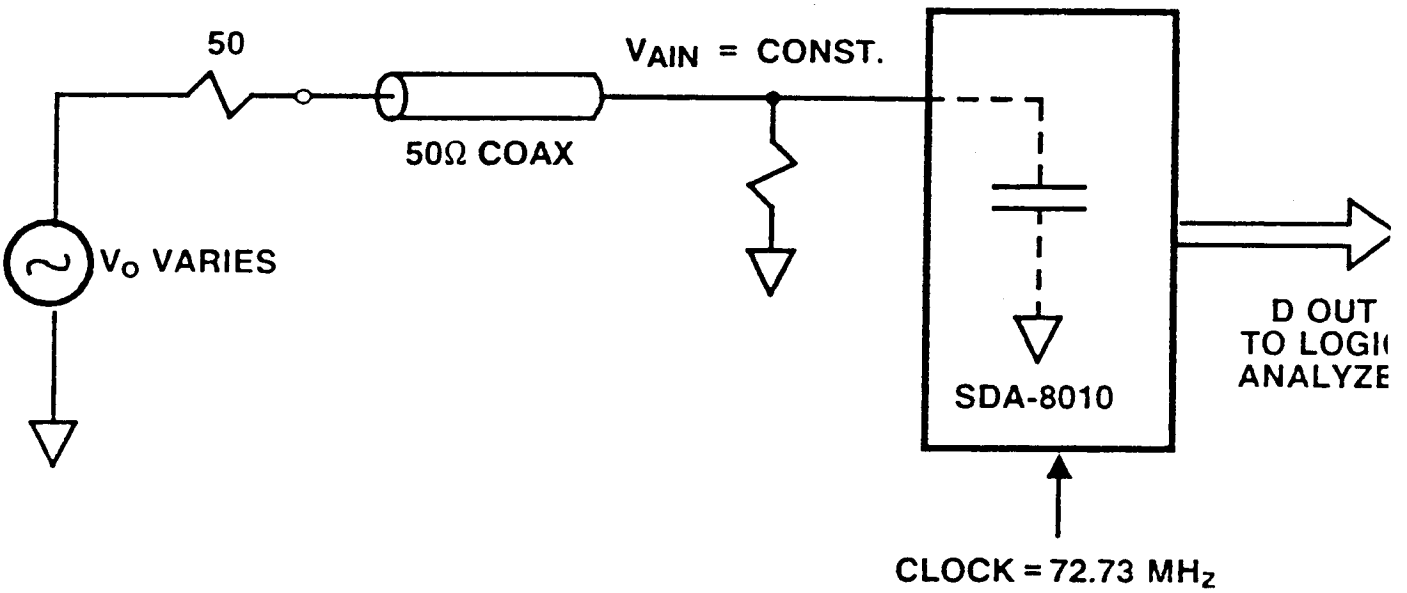

Figure 2.3.2.3.1. Amplitude Response (50 ohm System)
Test Setup Block Diagram

In this first test, V_{AIN} is held constant, and therefore any filtering action at the input to the A/D is not accounted for in the digital measurements.

2.3.2.3.2 The second technique, will be that of holding the source power constant over the entire frequency spectrum of interest. In this test V_{AIN} will vary somewhat due to filtering at the input of the A/D. This filtering action is mainly due to an internal capacitance and an external resistance setting up an RC time constant. Therefore, a minimum loss network will be added at the input of the A/D so that the

A/D "sees" a lower source impedance of 25 ohms while the signal source "sees" a characteristic impedance of 50 ohms. A block diagram of the test setup is given by Figure 2.3.2.3.2.

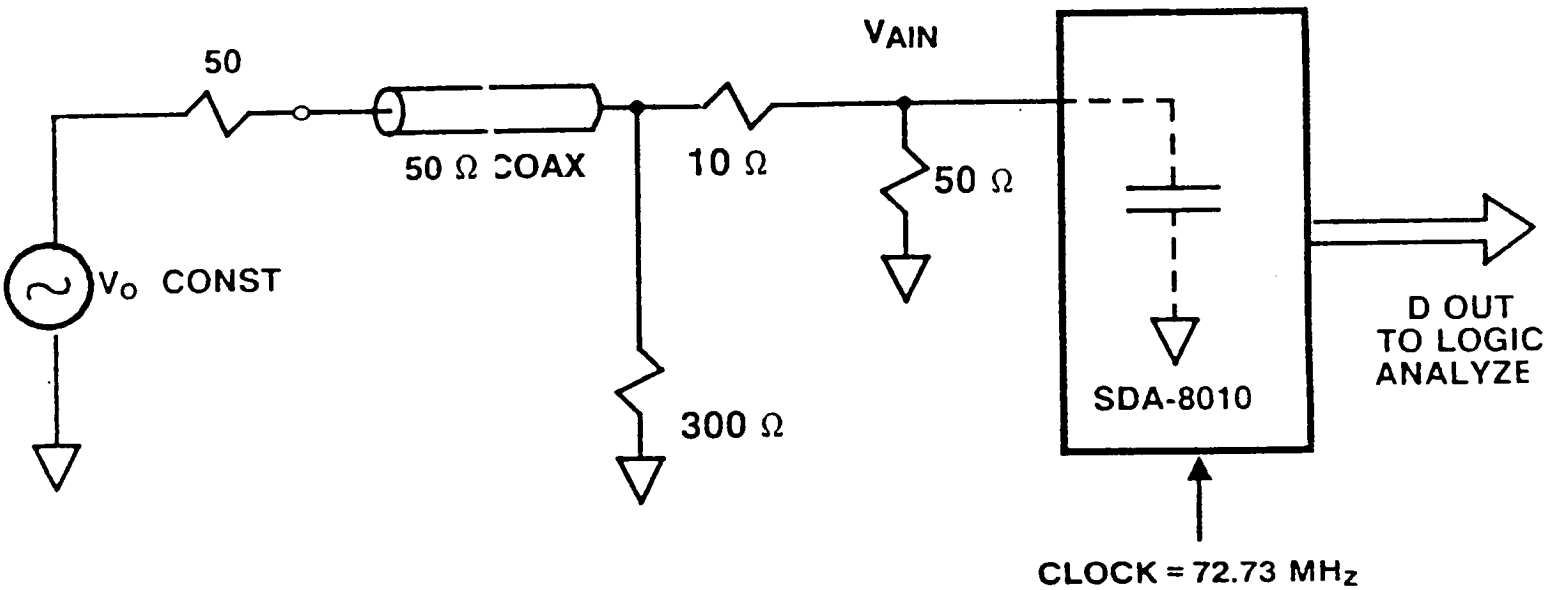

Figure 2.3.2.3.2. Amplitude Response Test Setup Block Diagram

The frequency response will be measured at the A/D output by measuring the numerical positive and negative peaks (of the sinewave) with a logic analyzer. These peak values will be recorded for several different input frequencies so that the amplitude response at the output can be determined.

2.3.2.3.3 The third amplitude response measurement technique involves the use of a low output impedance amplifier at the input of the A/D. A block diagram of the test setup is given by Figure 2.3.2.3.3.

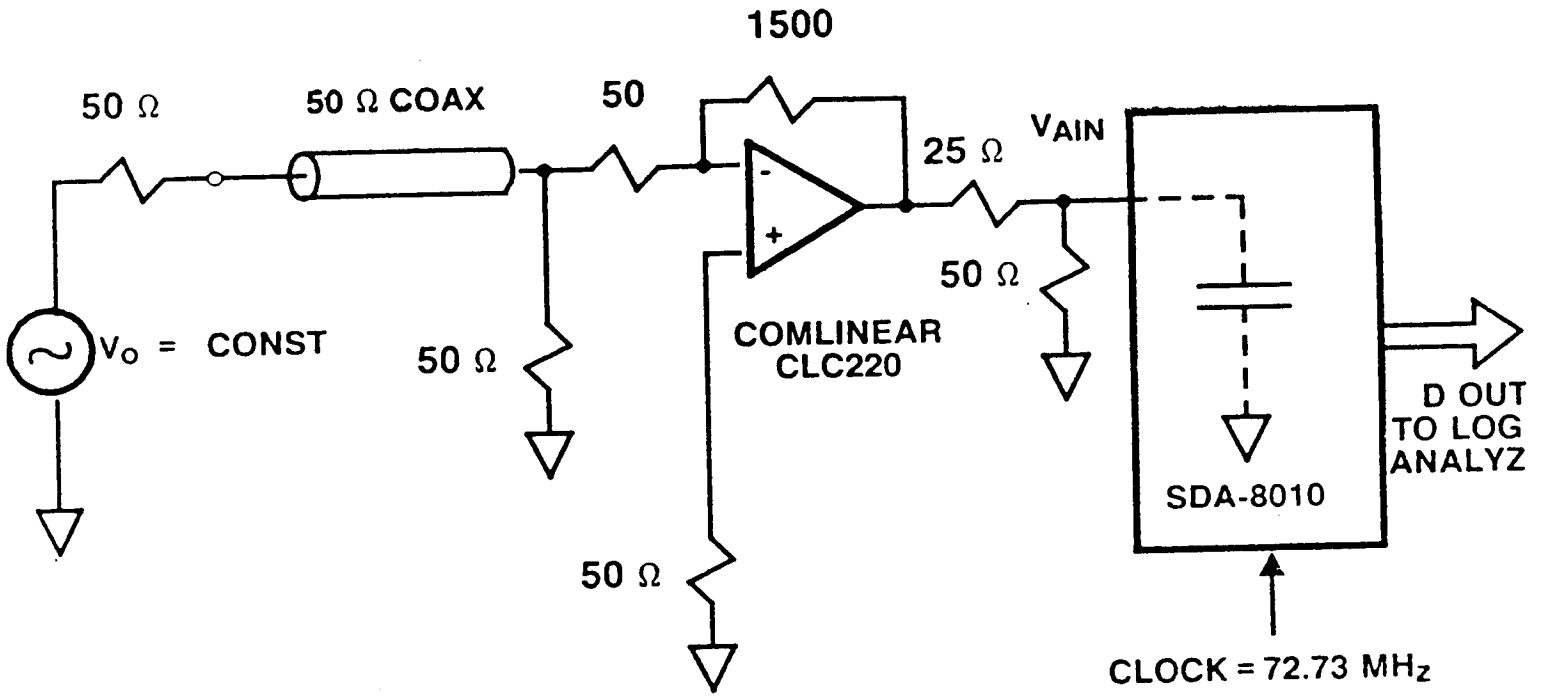

Figure 2.3.2.3.3. Amplitude Response Test Setup Using a Buffer Amplifier

The measurement of amplitude response will be measured directly at the A/D output as previously detailed in Sections 2.3.2.3.1 and 2.3.2.3.2.

2.3.3 Breadboard Design

See Schematic Diagram of the SDA-8010 Breadboard.

2.3.4 Breadboard Fabrication

See color photographs of the SDA-8010 Breadboard

2.3.5 Breadboard Testing

2.3.5.1 Clock Timing Adjustment

Dynamic Response of the A/D was insensitive to the duty cycle of STR1. Very good dynamic behavior resulted when the simple CLK, $\overline{CLK}$ scheme was applied to the A/D, and therefore no further testing was performed in this area. Remember, the goal was to achieve good dynamic behavior using STR1 = CLK, STR2 = $\overline{CLK}$, as stated in Section 2.3.2.1(b).

A pulse diagram of the clocking scheme used to clock the SDA-8010 and the 100151 flip-flops following the A/D is given in Figure 2.3.5.1.

The output of the SDA-8010 A/D for 1.4 volt peak-peak sinewave inputs of 1 MHz, 36 MHz, and 70 MHz were recorded by photographing the K105 logic analyzer display. The clocking scheme used to produce all photographs was that given by Figure 2.3.5.1, with a clock frequency of 72.73 MHz.

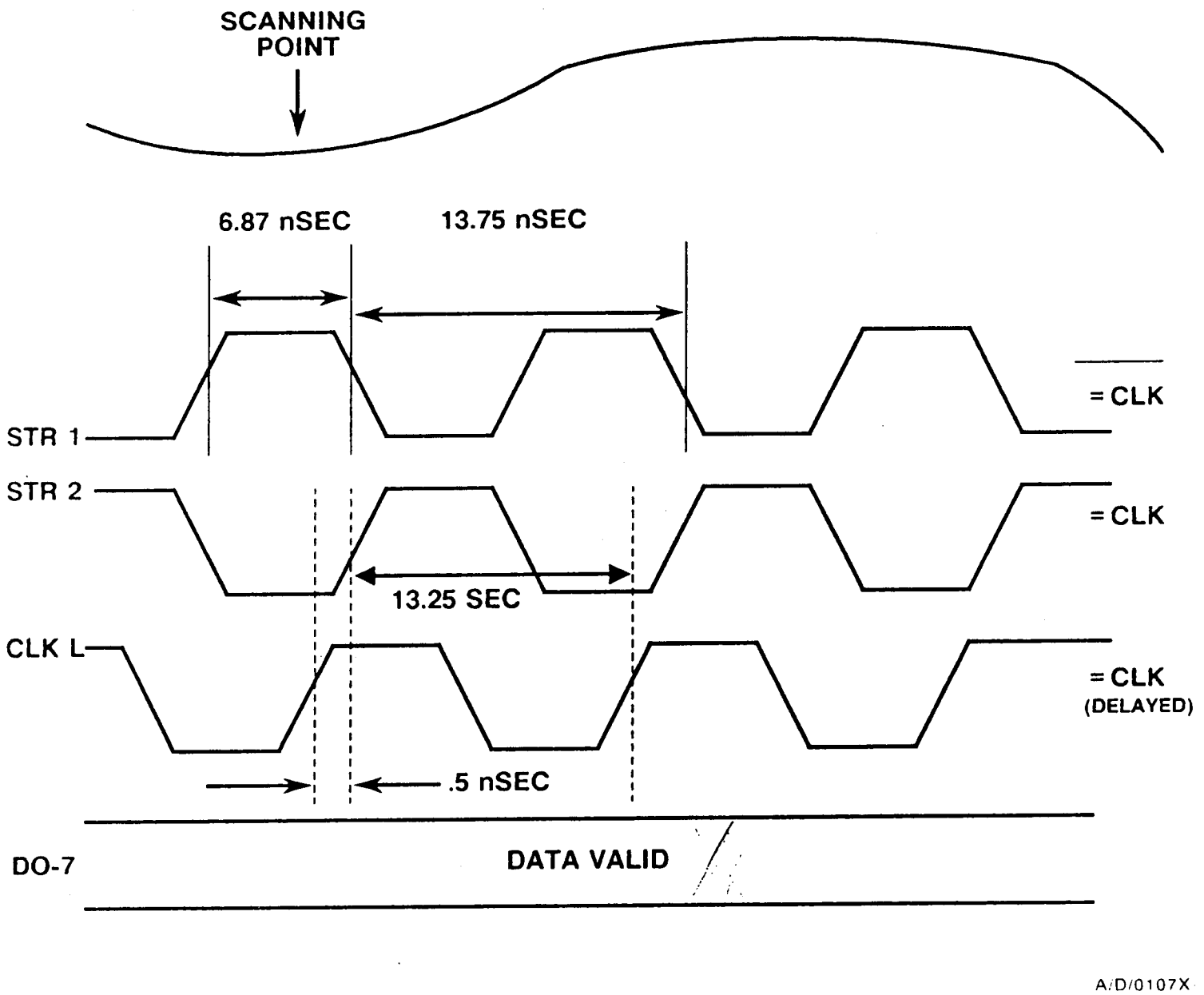

Figure 2.3.5.1(a). Timing of Clocking Scheme Used With SDA-8010 A/D. Clock Frequency is 72.73 MHz

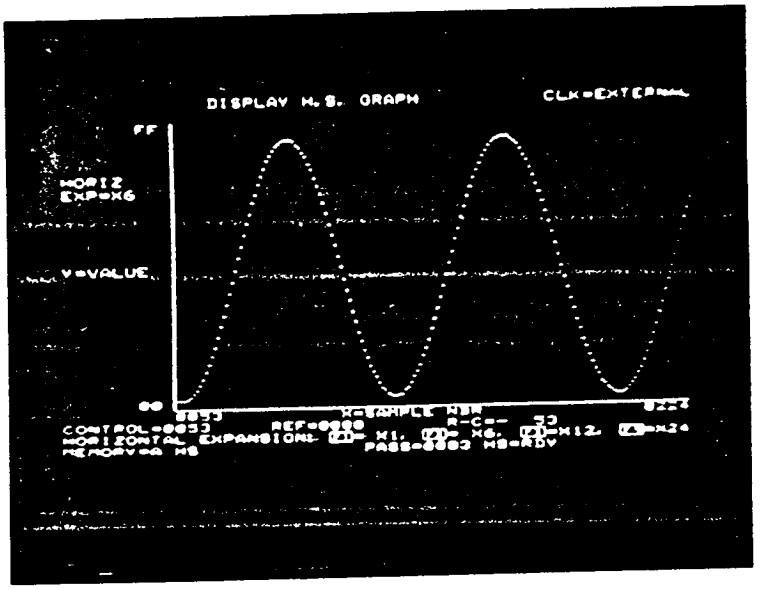

Figure 2.3.5.1(b). SDA-8010 Output for an Almost Full Scale 1 MHz Sinewave Input; STR1 = $\overline{CLK}$, STR2 = CLK, Clock Freq. = 72.73 MHz

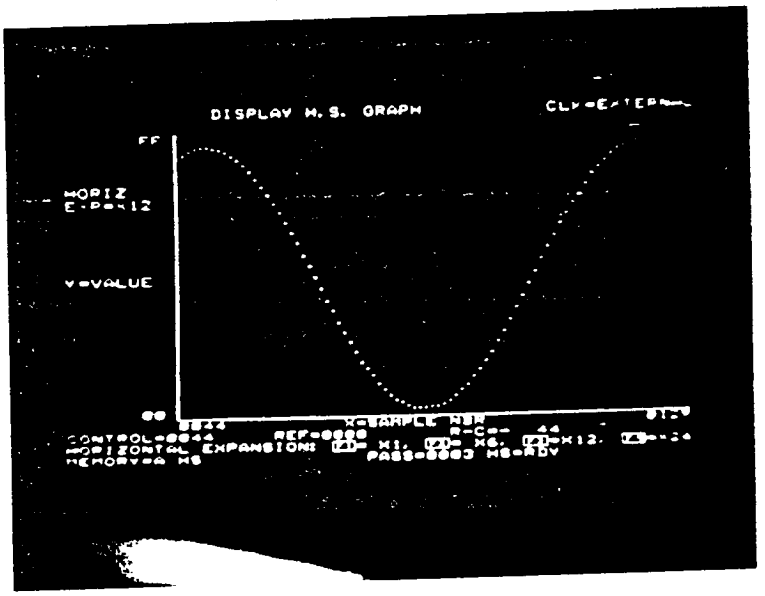

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Figure 2.3.5.1(c). Horizontal Expansion of Figure 2.3.5.1(b) to Show More Detail

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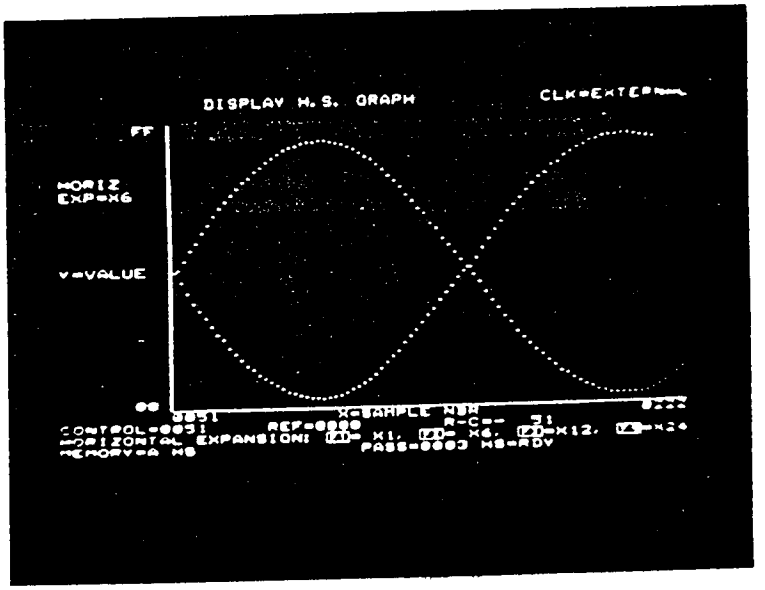


Figure 2.3.5.1(d). SDA-8010 Output for an Almost Full Scale 36 MHz Sinewave Input. STR1 = CLK, STR2 = $\overline{\text{CLK}}$, Clock Frequency = 72.73 MHz

Note the 365 kHz beatnote frequency produced by sampling a 36 MHz sinewave with a 72.73 MHz clock. Sampling a 36 MHz tone with a 72.73 MHz clock, maximally stresses the A/D because each adjacent sample has opposite polarity, and therefore each successive sample has an MSB transition. Note that there are no missing codes and the dynamic linearity seems to be "good."

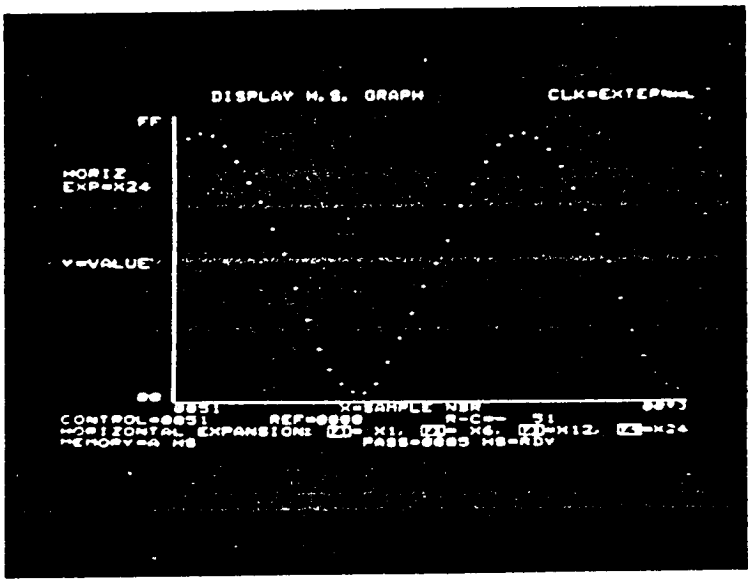


Figure 2.3.5.1(e). SDA-8010 Output for an Almost Full Scale 70 MHz Sinewave Input. STR1 = CLK, STR2 = CLK, Clock Frequency = 72.73 MHz

The sinewave of Figure 2.3.5.1(e) is slightly distorted. The distortion, however, is a result of the source, not the conversion process. The frequency of the displayed sinewave is the difference between the sample frequency (72.73 MHz) and the input frequency 70 MHz) which is 2.73 MHz.

2.3.5.2 Static Nonlinearity

The static linearity error was measured as described by Section 2.3.2.2(d). The measured data is given on the following pages.

Static Linearity (+Vref = .750V, -Vref = -.750V)

Code	Voltage	Code	Voltage
00000000	-.750	00100010	-.548
00000001	-.744	00100011	-.542
00000010	-.737	00100100	-.537
00000011	-.731	00100101	-.532
00000100	-.725	00100110	-.525
00000101	-.720	00100111	-.520
00000110	-.713	00101000	-.513
00000111	-.708	00101001	-.507
00001000	-.702	00101010	-.501
00001001	-.696	00101011	-.495
00001010	-.690	00101100	-.489
00001011	-.685	00101101	-.483
00001100	-.679	00101110	-.478
00001101	-.673	00101111	-.472
00001110	-.667	00110000	-.467
00001111	-.661	00110001	-.460
00010000	-.655	00110010	-.455
00010001	-.650	00110011	-.449
00010010	-.645	00110100	-.443
00010011	-.638	00110101	-.436
00010100	-.631	00110110	-.430
00010101	-.625	00110111	-.425
00010110	-.619	00111000	-.419
00010111	-.614	00111001	-.413
00011000	-.608	00111010	-.407
00011001	-.603	00111011	-.401
00011010	-.596	00111100	-.395
00011011	-.591	00111101	-.389
00011100	-.584	00111110	-.383
00011101	-.579	00111111	-.377
00011110	-.572	01000000	-.370
00011111	-.567	01000001	-.365
00100000	-.560	01000010	-.360
00100001	-.554	01000011	-.355

Static Linearity (+Vref = .750V, -Vref = -.750V) (Continued)

Code	Voltage	Code	Voltage
01000100	-.350	01100110	-.152
01000101	-.344	01100111	-.145
01000110	-.338	01101000	-.139
01000111	-.333	01101001	-.134
01001000	-.326	01101010	-.129
01001001	-.321	01101011	-.124
01001010	-.314	01101100	-.117
01001011	-.309	01101101	-.112
01001100	-.302	01101110	-.107
01001101	-.297	01101111	-.101
01001110	-.292	01110000	-.095
01001111	-.285	01110001	-.088
01010000	-.279	01110010	-.083
01010001	-.274	01110011	-.077
01010010	-.268	01110100	-.072
01010011	-.263	01110101	-.065
01010100	-.256	01110110	-.060
01010101	-.251	01110111	-.054
01010110	-.245	01111000	-.048
01010111	-.239	01111001	-.043
01011000	-.234	01111010	-.037
01011001	-.228	01111011	-.030
01011010	-.222	01111100	-.025
01011011	-.217	01111101	-.020
01011100	-.209	01111110	-.014
01011101	-.204	01111111	-.007
01011110	-.198	10000000	-.001
01011111	-.192	10000001	+.005
01100000	-.187	10000010	+.009
01100001	-.182	10000011	+.015
01100010	-.175	10000100	+.021
01100011	-.169	10000101	+.027
01100100	-.164	10000110	+.033
01100101	-.158	10000111	+.039

Static Linearity (+Vref = .750V, -Vref = -.750V) (Continued)

Code	Voltage	Code	Voltage
10001000	+.044	10101011	+.249
10001001	+.050	10101100	+.255
10001010	+.056	10101101	+.261
10001011	+.063	10101110	+.267
10001100	+.068	10101111	+.273
10001101	+.075	10110000	+.279
10001110	+.080	10110001	+.285
10001111	+.085	10110010	+.291
10010000	+.091	10110011	+.295
10010001	+.097	10110100	+.302
10010010	+.103	10110101	+.308
10010100	+.114	10110110	+.314
10010101	+.120	10110111	+.321
10010110	+.126	10111000	+.327
10010111	+.131	10111001	+.332
10011000	+.136	10111010	+.337
10011001	+.143	10111011	+.343
10011010	+.150	10111100	+.350
10011011	+.155	10111101	+.355
10011100	+.161	10111110	+.361
10011101	+.166	10111111	+.367
10011110	+.172	11000000	+.374
10011111	+.179	11000001	+.382
10100000	+.184	11000010	+.390
10100001	+.190	11000011	+.394
10100010	+.196	11000100	+.399
10100011	+.201	11000101	+.405
10100100	+.207	11000110	+.412
10100101	+.213	11000111	+.417
10100110	+.219	11001000	+.424
10100111	+.225	11001001	+.429
10101000	+.231	11001010	+.434
10101001	+.237	11001011	+.441
10101010	+.243	11001100	+.448

Static Linearity (+Vref = .750V, -Vref = -.750V) (Continued)

Code	Voltage
11001101	+.453
11001110	+.459
11001111	+.464
11010000	+.470
11010001	+.477
11010010	+.483
11010011	+.488
11010100	+.493
11010101	+.500
11010110	+.505
11010111	+.512
11011000	+.519
11011001	+.524
11011010	+.530
11011011	+.535
11011100	+.542
11011101	+.547
11011110	+.554
11011111	+.559
11100000	+.565
11100001	+.570
11100010	+.576
11100011	+.583
11100100	+.588
11100101	+.594
11100110	+.601
11100111	+.607
11101000	+.612
11101001	+.619
11101010	+.625
11101011	+.632
11101100	+.637
11101101	+.642
11101110	+.647

Code	Voltage
1101111	+.653
11110000	+.659
11110001	+.666
11110010	+.672
11110011	+.677
11110100	+.683
11110101	+.690
11110110	+.696
11110111	+.701
11111000	+.708
11111001	+.713
11111010	+.720
11111011	+.725
11111100	+.731
11111101	+.737
11111110	+.742
11111111	+.750

A graph of the measured data is given in Figure 2.3.5.2(a).

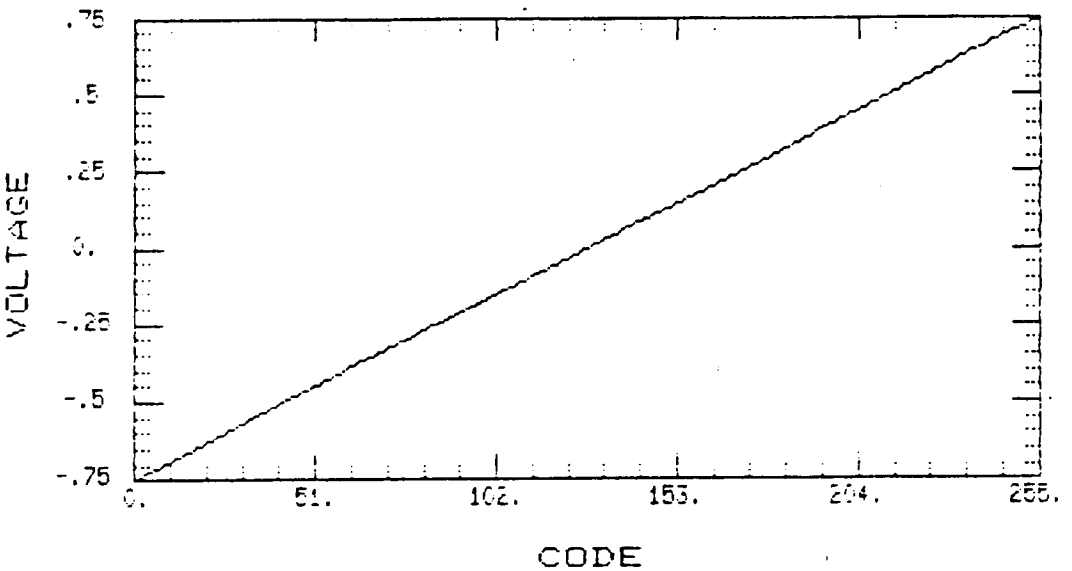


Figure 2.3.5.2(a). Voltage to Code Transfer Function of the SDA-8010

A graph of the differential linearity error is given in Figure 2.3.5.2(b). Differential linearity error of less than ±1/2 LSB, ensures no missing codes.

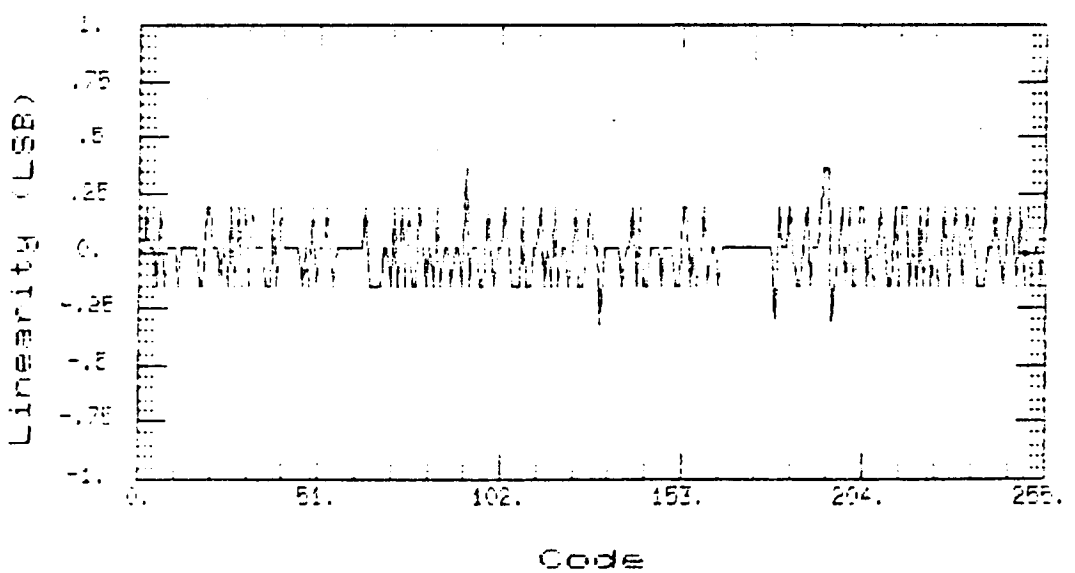


Figure 2.3.5.2(b). Differential Linearity Error Plot for the SDA-8010

In addition to the static linearity error tests performed, a crude dynamic linearity test was also performed. A $(72.73\ \text{MHz})^{-1} \times 256$ second long ramp was applied to the analog input of the SDA-8010. This ramp was not exactly linear and is shown in the photograph of Figure 2.3.5.2(c). The output response of the SDA-8010 to the ramp was then converted back to an analog voltage (Figure 2.3.5.2(d)). The output of the D/A was then subtracted from the input of the SDA-8010 to yield the photograph of Figure 2.3.5.2(e). The photograph of Figure 2.3.5.2(e) shows a straight line which indicates good dynamic linearity.

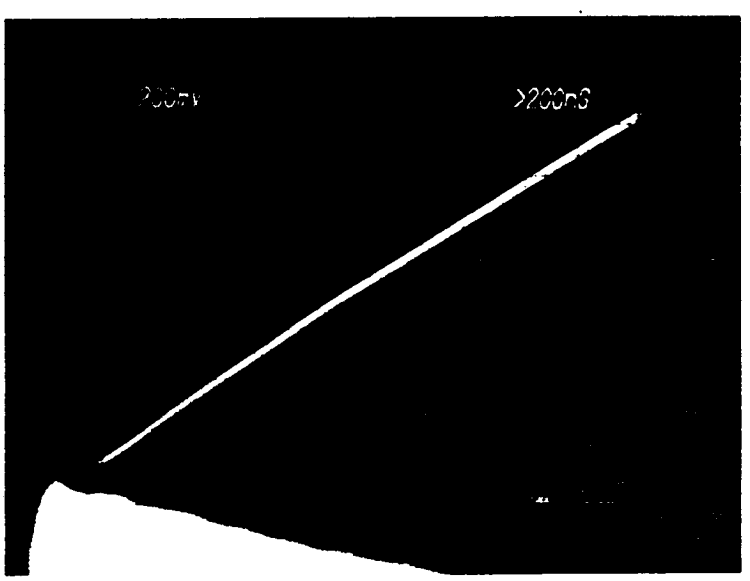


Figure 2.3.5.2(c). Ramp input to the SDA-8010 of Length 3.52 usec

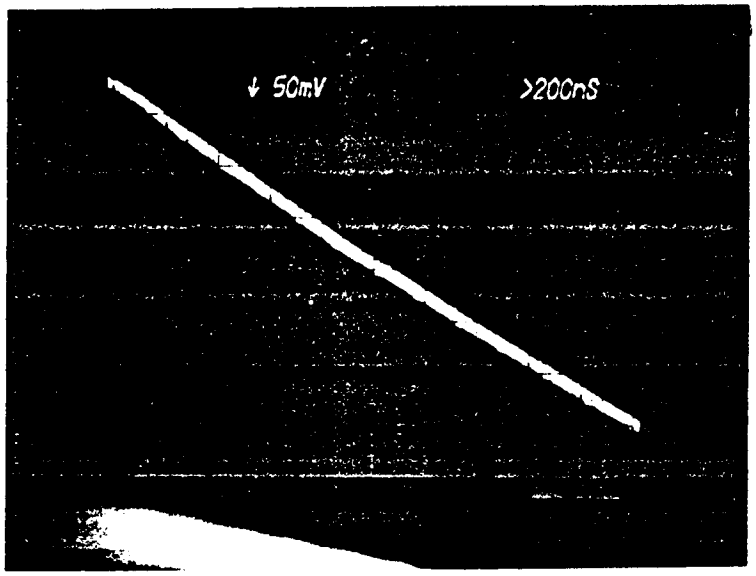


Figure 2.3.5.2(d). Ramp Output of the AD9700 D/A Converter

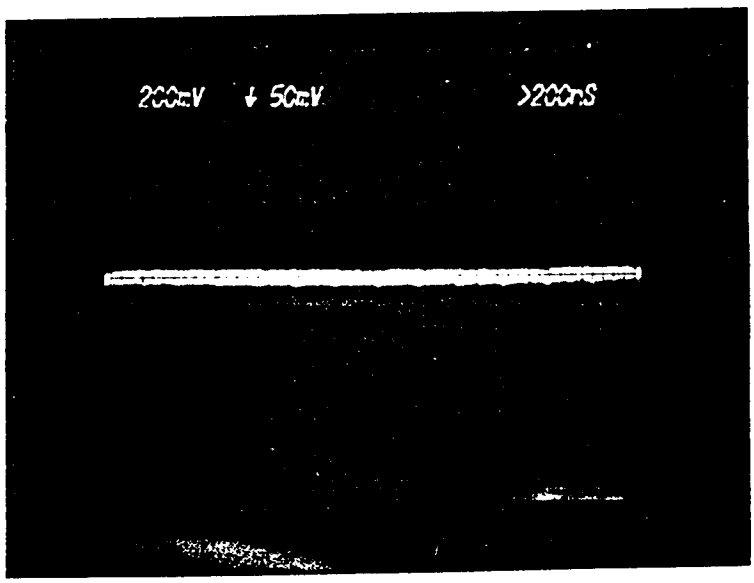


Figure 2.3.5.2(e). Difference Between the Ramp Input to the SDA-8010, and the Ramp Output of the AD9700 D/A, Which Represents the Cumulative Linearity Error of Both Devices

2.3.5.3 Amplitude Response of the SDA-8010

2.3.5.3.1 The amplitude response of the SDA-8010 was measured as given by the test procedure in Section 2.3.2.3.1 of this report.

SDA-8010 Amplitude Response, V_{AIN} = Const.

Binary Numbers Out

Input Frequency	Positive Peak	Negative Peak	dB, 1 MHz*
500 kHz	11110011	00001000	-0.18
1 MHz	11110101	00000101	0.0
5 MHz	11110100	00001000	-0.15
10 MHz	11110111	00001001	-0.07
20 MHz	11110110	00000100	+0.07
30 MHz	11110110	00000100	+0.07
40 MHz	11110111	00000011	+0.14
50 MHz	11110110	00000101	+0.04
60 MHz	11110101	00000110	-0.04
70 MHz	11110100	00001000	-0.15

$$* \text{ dB, 1 MHz} = 20 \log\left(\frac{\text{Positive - Negative Peak @ X MHz}}{\text{Positive - Negative Peak @ 1 MHz}}\right)$$

2.3.5.3.2 The amplitude response of the SDA-8010 was measured as outlined by the test procedure in Section 2.3.2.3.2.

SDA-8010 Amplitude Response, V_o = Const., R_s = 25 ohms

Binary Numbers Out

Input Frequency	Positive Peak	Negative Peak	dB, 1 MHz*
1 MHz	11010000	00101011	0.0
5 MHz	11010001	00101100	0.0
10 MHz	11010010	00101110	-0.05
20 MHz	11010001	00101110	-0.11
30 MHz	11010000	00101110	-0.16
40 MHz	11010000	00101110	-0.16
45 MHz	11001111	00101111	-0.27
50 MHz	11001110	00110000	-0.38
60 MHz	11001010	00110100	-0.83
70 MHz	11000011	00111011	-1.68

$$* \text{ dB, 1 MHz} = 20 \log\left(\frac{\text{Positive - Negative Peak @ X MHz}}{\text{Positive - Negative Peak @ 1 MHz}}\right)$$

2.3.5.3.3 The amplitude response of the SDA-8010 was measured as outlined by the test procedure in Section 2.3.2.3.3.

SDA-8010 Amplitude Response, V_o = Const.
Buffer Amp Used, R_s = 25 ohms

Binary Numbers Out

Input Frequency	Positive Peak	Negative Peak	dB, 1 MHz*
500 kHz	11101001	00010111	+0.04
1 MHz	11101000	00010111	0.0
5 MHz	11101001	00011000	0.0
10 MHz	11101001	00011010	-0.08
20 MHz	11101000	00011011	-0.16
30 MHz	11100111	00011010	-0.16
40 MHz	11101000	00010111	0.0
45 MHz	11101001	00010111	+0.4
50 MHz	11101010	00010101	+0.16
60 MHz	11101011	00010100	+0.25
70 MHz	11101010	00010110	+0.12

2.3.6 Test Evaluation

2.3.6(a) Results of the Evaluation.

Three test have been performed; the clock timing adjustment test, the linearity test, and the amplitude response test. The evaluation of the test data for these three tests follows.

The test data given in Section 2.3.5.1 indicates clearly, that a straightforward CLK, $\overline{CLK}$ clocking scheme may be used at the 72.73 MHz clock rate, even though vendor technical information indicates this clocking scheme is not optimal. This scheme will simplify the generation of timing by eliminating the need for voltage references (with their associated drifts) necessary in the comparator circuitry to generate other than CLK, $\overline{CLK}$ 50% duty cycle clocks.

The test data given in Section 2.3.5.2 indicates that linearity errors are less than $\pm 1/2$ LSB, and therefore, the device may be operated at the desired clock frequency with no missing codes at the output!

The test data given in Section 2.3.5.3 indicates that the amplitude response of the SDA-8010 is relatively flat, especially if the voltage right at the analog input can be held constant. An external source resistance with an internal (nonlinear) capacitance forms an RC time constant which will cause rolloff at the analog input. If, however, the source resistance is minimized the effect of the RC time constant can be "pushed" out to frequencies beyond the bandwidth of interest.

In other words, the -3 dB bandwidth of the RC filter can be made high enough in frequency that the amplitude rolloff over the bandwidth of interest (DC to 45 MHz in our design) is on the order of a few tenths of a dB.

2.3.6(b) Revisions Necessary or Recommended, from Breadboard Evaluation.

The revisions to the SDA-8010 evaluation breadboard based on test results are as follows.

Since the CLK, $\overline{CLK}$ clocking scheme will be used for the STR1, STR2 clock signals of the SDA-8010, it is recommended that a differential line receiver be used on the quantizing card to receive the clock signal. This provides common mode rejection between cards.

In addition, it is recommended that the circuit given by Figure 2.3.2.3.3 be used to "drive" the SDA-8010, in that it gives the best amplitude response. A lower gain buffer device designed specifically for driving Flash A/D converters (the Comlinear CLC231) is under consideration for replacing the CLC220, so that amplitude peaking (see Section 2.3.5.3.3) may be reduced to less than tenths of a dB.

NAS3-24681
ADVANCED MODULATION TECHNOLOGY DEVELOPMENT
TASK V REVIEW
JANUARY 28, 1987

HARRIS CORPORATION, GCSD
P.O. BOX 91000
MELBOURNE, FL. 32902

PRESENTED BY:
RICHARD D. CROWLEY
ROBERT C. DAVIS
JAMES A. GANN

PREPARED FOR:
NASA LEWIS RESEARCH CENTER
CLEVELAND, OH. 44135

ADVANCED MODULATION TECHNOLOGY DEVELOPMENT
TASK V REVIEW
AGENDA

9:00-9:10	Introduction	Rich Crowley
9:10-9-45	System Overview	Bob Davis
9:45-10:30	Modulator Design	
	Baseband	Rich Crowley
	RF	Jim Gann
10:30-10:45	Break	
10:45-12:00	Demodulator Design	
	RF	Jim Gann
	Coherent Demodulator (Phase Detector)	Jim Gann
	Bit Synchronizer	Jim Gann
	Baseband	Rich Crowley
12:00-1:00	Lunch	
1:00-1:45	Signal Combiner	
	Digital	Rich Crowley
	RF	Rich Crowley
1:45-2:00	Mechanical	Rich Crowley

NASA/TDMA:

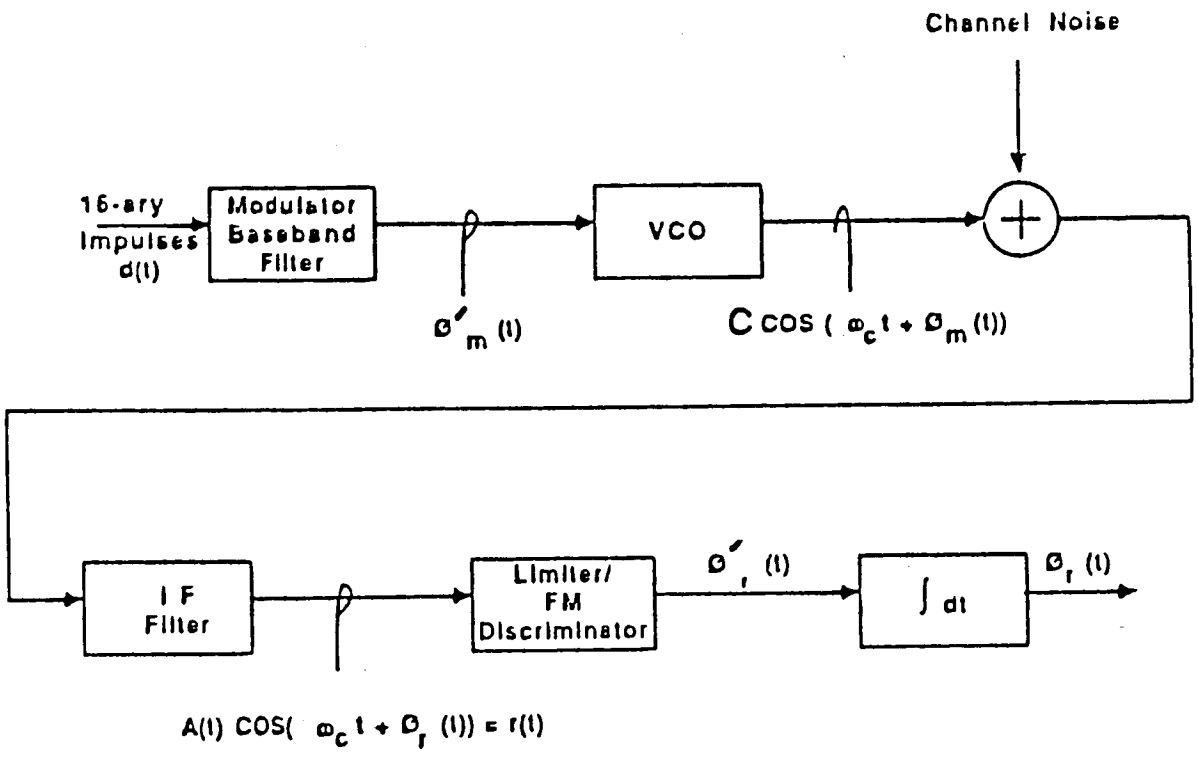
SYSTEM OVERVIEW

NASA Lewis Research Center
Cleveland, OH
January 28, 1987

Presented by:
Bob Davis
Harris Corporation
Advanced Technology Department

Viewgraph 1

This viewgraph shows the conceptual technique whereby Harris' TDMA modem produces coherent phase measurements using VCO modulation followed by discriminator detection. As shown, 16-ary impulses enter the modulator baseband filter. The output of this filter is instantaneous frequency produced by the VCO. The filter output consequently is labelled phi dot. The output of the VCO has phase modulation phi, which is the integral of the input instantaneous frequency. The output is passed over the noisy channel,filtered by an IF filter, and passed to a limiter/discriminator. The output of the discriminator is the instantaneousfrequency of the IF filtered signal. Next, the instantaneousfrequency is integrated to provide a measure of received signal phase.



Current Baseline Conceptual Modem Phase Measurement Technique

Viewgraph ^

This viewgraph shows conceptually how the integrator of the baseband signal from the discriminator is implemented. The integrator is basically implemented as an integrate and dump (baseband filter) followed by an accumulator. The accumulator rolls over modulo 2 pi. The accumulator output is observed and the error to the closest phase node is computed and passed to a "DC restore" loop filter. The output of the loop filter is subtracted from the discriminator output, closing a baseband loop. The action of this closed loop is such that coherent phase is acquired in the accumulator. The dynamic equations describing this baseband loop are exactlyy the same as for a standard IF phase lock loop.

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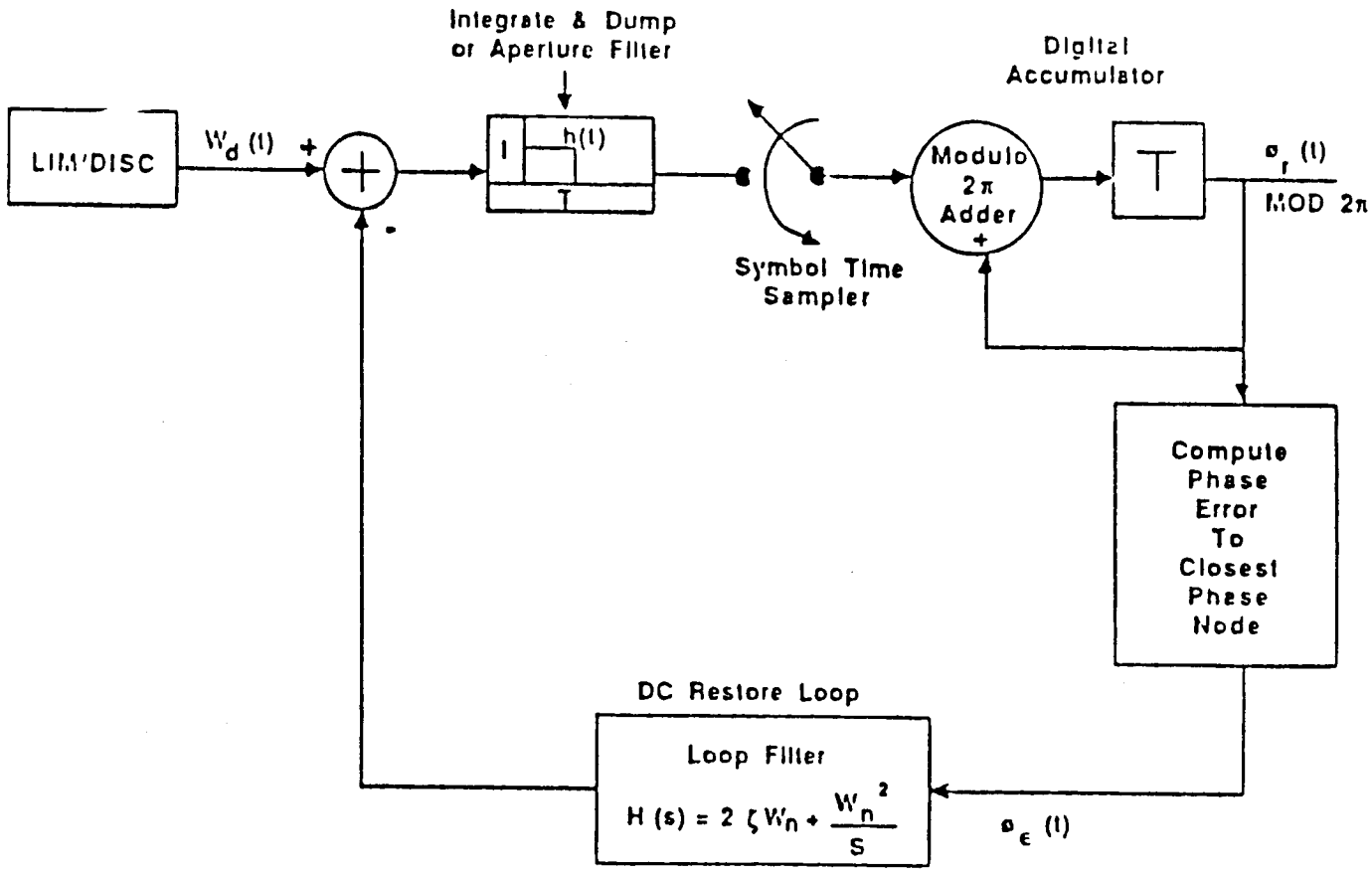

Baseband Processing to Obtain Coherent Phase Measurements
From Discriminator Output

Viewgraph 3

This viewgraph gives an overall conceptual block diagram for Harris' TDMA modem. Half Nyquist filtering is employed at the VCO baseband on the 16-ary pulses to produce the IF signal at the modulator. At the demodulator the IF signal is filtered and passed to the discriminator. The discriminator baseband signal is Half Nyquist filtered and sampled at the symbol rate by an eight bit A/D. The Half Nyquist filter at the discriminator baseband completes the pulse shaping begun at the VCO, producing an overall Nyquist response to the 16-ary impulses transmitted. The 8-bit A/D samples are passed to the baseband digital accumulator loop. The accumulator output is coherent received phase and it is passed at the symbol rate to the Viterbi decoder for demodulation of the original 3 information bits carried by the 16-ary symbol. These decoded bits are passed to the user.

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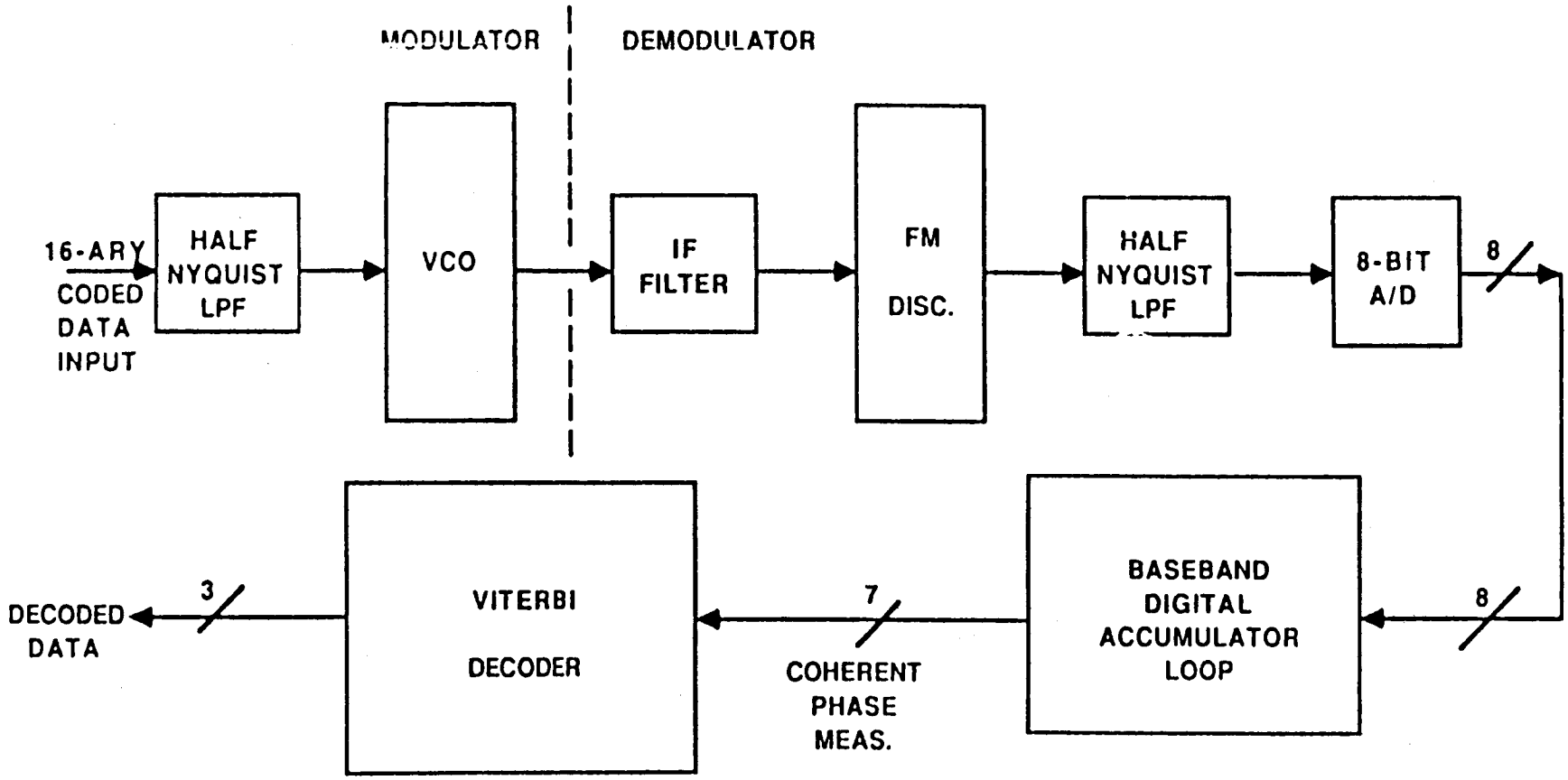
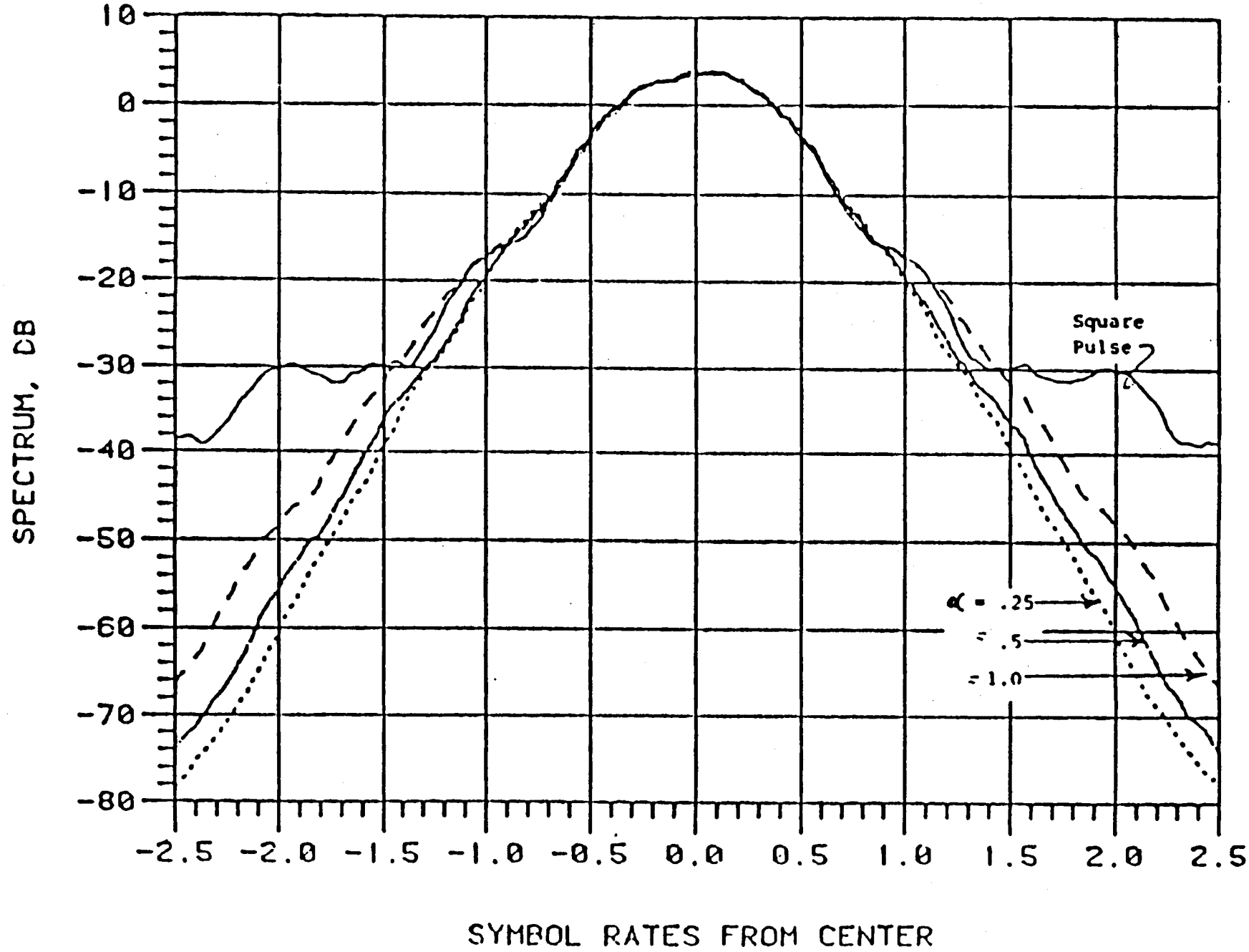
BASIC BLOCK DIAGRAM - NASA/TDMA



Viewgraph 4

This viewgraph shows the spectrum of the resultant VCO IF signal in comparison with standard 16-ary Continuous Phase FSK (CPFSK). The standard CPFSK is labelled Square Pulse signalling since the instantaneous VCO modulating signal in that case is square pulse 16-PAM signalling, as opposed to our baseband pulse shape dictated by the Half Nyquist filter used at the VCO baseband. We are using a Half Nyquist filter based on the raised cosine frequency response with rolloff parameter given by alpha=.25.

16-ARY CONTINUOUS PHASE MODULATION SPECTRA



Viewgraph 5

This viewgraph shows the manner in which coding is applied to the modulator. The incoming data is demuxed into three parallel bit streams. The 2 MSB's are passed uncoded to the MSB positions of the modulator. The LSB bit stream is coded by a rate 1/2 K=7 convolutional encoder, thus expanding the one LSB data bit into 2 encoded branch bits. These 2 branch bits are applied to the 2 LSB positions of the modulator. The total of 4 bits produced by this encoding process are applied at the symbol rate to dictate the appropriate one of 16 symbol-ending phases from the 16-CPFSK modulator as shown on the following viewgraph.

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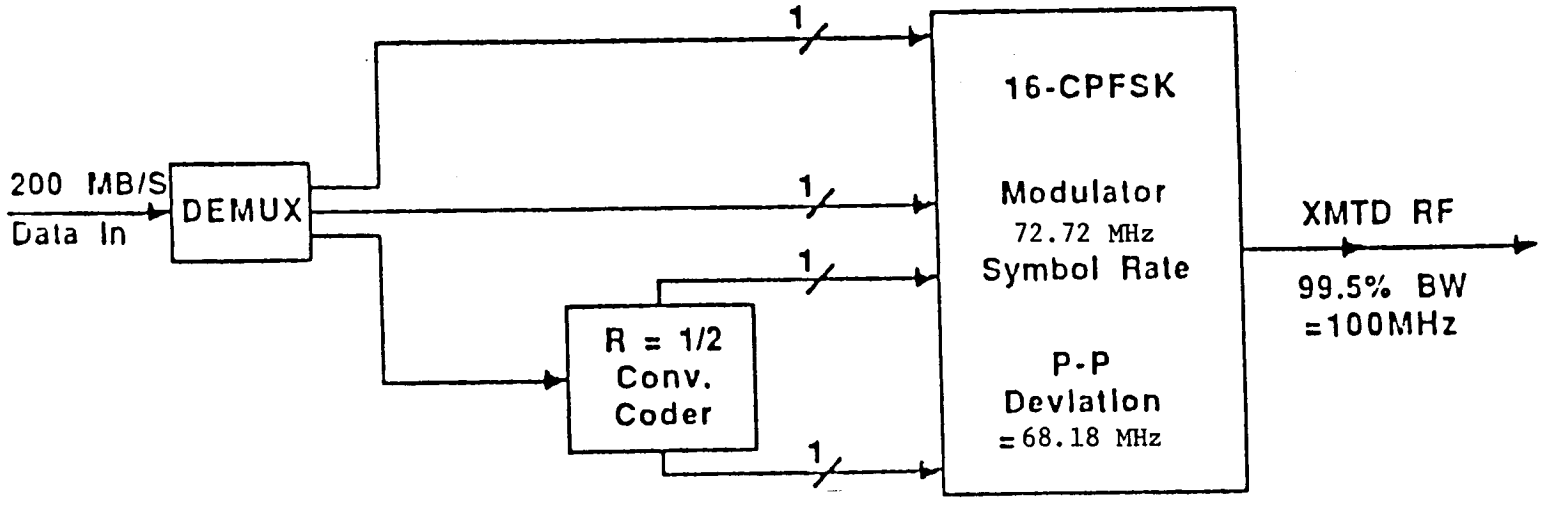

CPFSK Modulator

Viewgraph 6

This viewgraph shows the 16 symbol ending phases from the 16-ary CPFSK modulator along with the mapping of coded 4-bit groups onto them. These assignments were chosen for good code properties. You will note that any group of 4 succesive phases contain all rate 1/2 code branches (the 2 LSB's--see previous viewgraph). This forms the basis for our decoding strategy. The strategy, briefly, is to retain for consideration by the decoder only the four phase nodes nearest to the received phase. The Viterbi decoder then decides which of the four retained phases is most likely to have been transmitted. The 2 MSB's associated with the decoders decision are output as 2 of the decoded bits. The third bit decision is that information bit decision made by the decoder. These three bits make the total information bit stream output.

C-2

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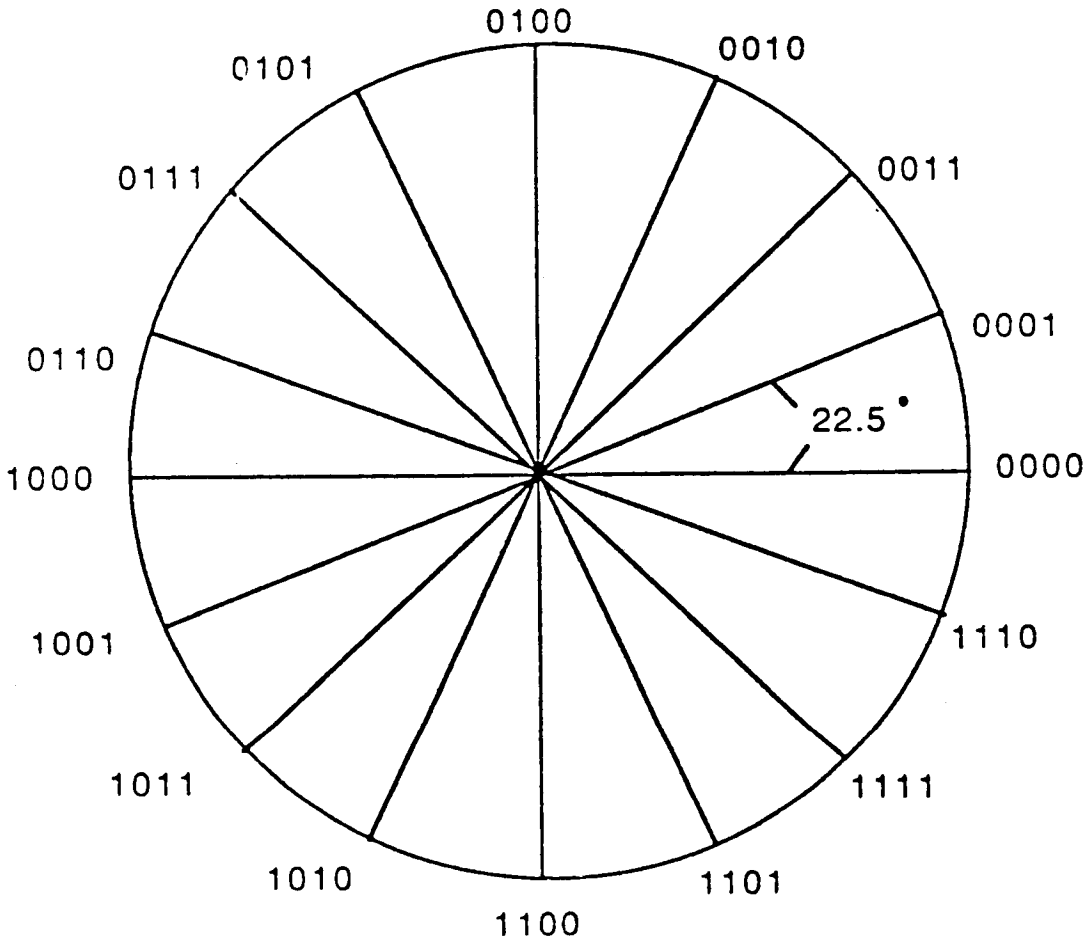
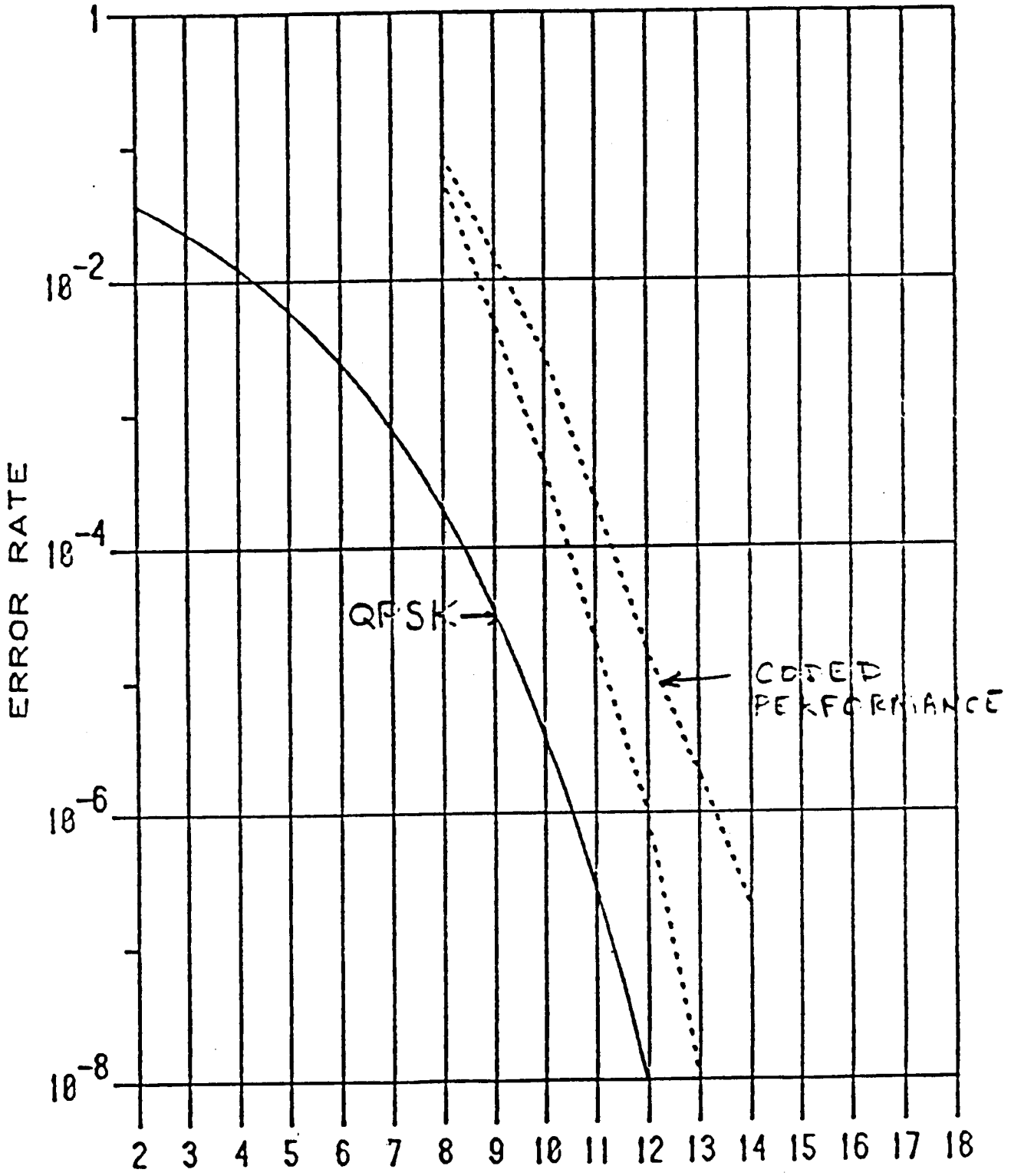
PHASE PLOT



Viewgraph 7

This viewgraph shows the performance predicted for the coded 16- CPFSK signal. Also shown for comparison is the performance for QPSK.

CODED CONTINUOUS PHASE 16-ARY PERFORMANCE
BBF=SQRT RCOS, ALPHA=.25
IF FLTR=FULL RCOS LPBW=.75SR, ALPHA=.25



Viewgraph 8

This viewgraph shows the time sequence of modulation symbols chosen for the Harris TDMA modem. This sequence has been selected to provide 90 degree separation between phases every fourth symbol time. This has been done to provide more reliable phase error signals to the baseband accumulator loop. The basic idea is that updating to the loop filter in the phase accumulator loop will be done only on the 90 degree spaced symbols occuring every fourth symbol time. This has necessitated only carrying 2 information bits on these every-fourth-symbol times, rather than 3 information bits as on the other 3 out of 4 symbols. This is accomplished at the modulator by not accepting an input bit into the coder shown in Viewgraph 5 every fourth symbol time and forcing the two branch bits from the encoder to be zeros. This has the effect of only transmitting one of four phases spaced by 90 degrees on these symbol times. Since the baseband loop filter is only driven by the phase error on these every-fourth-symbol time symbols, the phase errors are more reliable than if the phases were always spaced by only 22.5 degrees.

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Modem Engineering Section

MODIFIED SIGNALLING

	CYCLE 1				CYCLE 2			
	1	2	3	4	5	6	7	8
Info bits	3	3	3	2	3	3	3	2
Phase Spacing	22.5	22.5	22.5	90	22.5	22.5	22.5	90
M-ary Phase	16	16	16	4	16	16	16	4

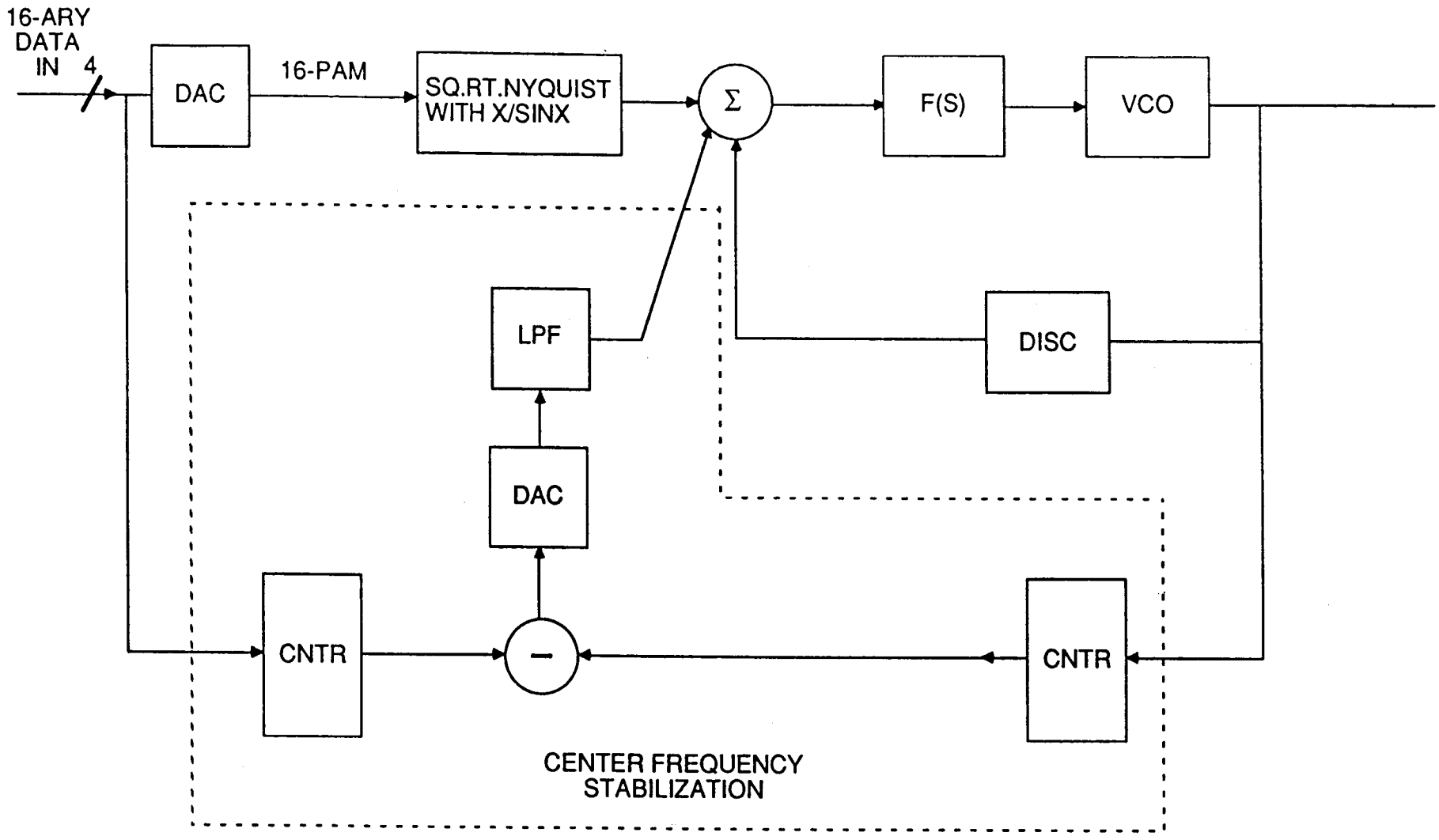
etc...

MODEM SYMBOL TIME

MODIFIED SIGNALLING DEVELOPED TO ELIMINATE DECISION DIRECTED ERROR PROBLEM.

Viewgraph 9

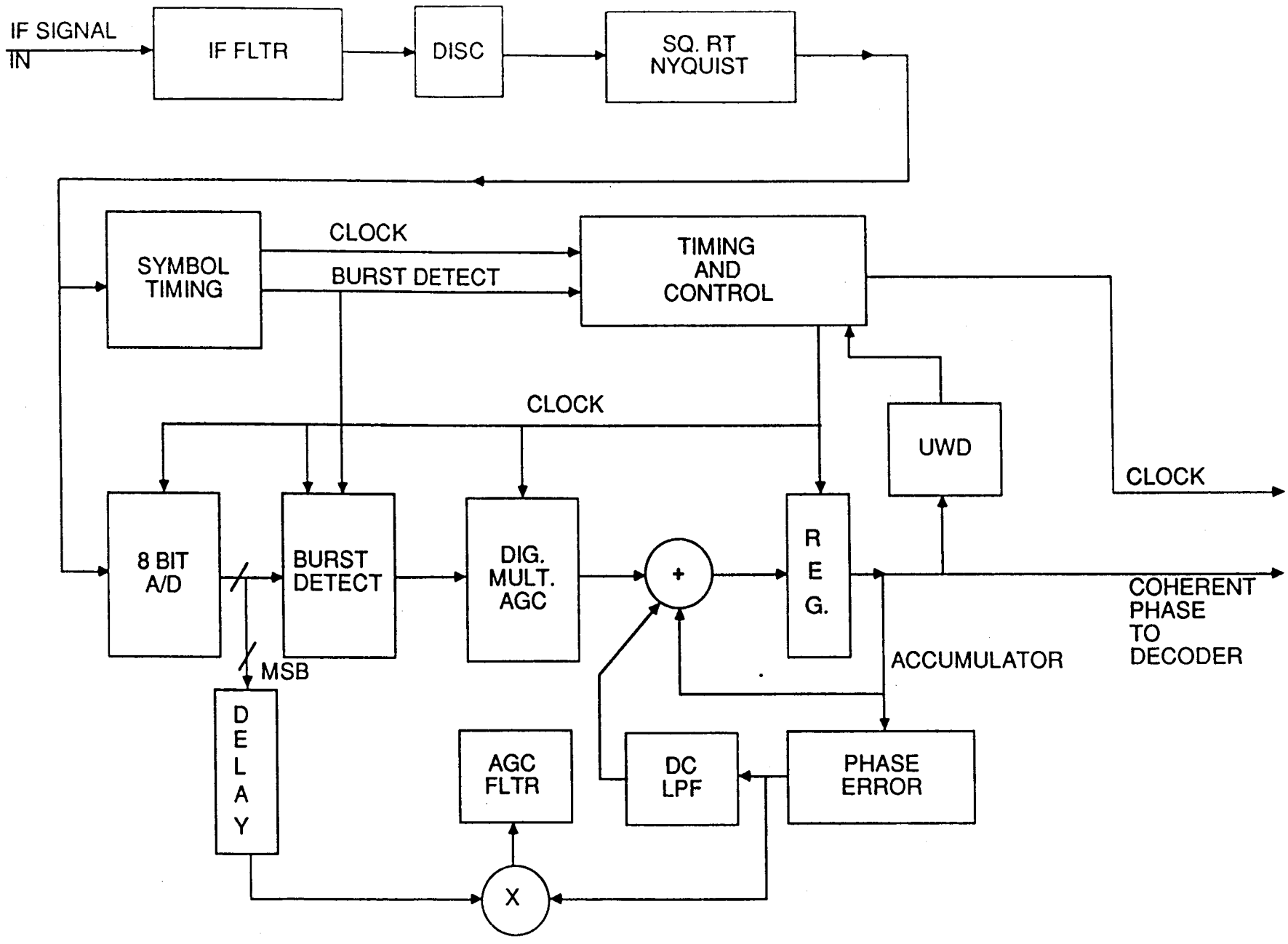
This viewgraph shows the modulator concept Harris is adopting for this NASA/TDMA modem. As shown, 16-ary (4-bit) data arrives and is D-to-A converted and applied to the Half Nyquist filter on the baseband VCO input. Since the pulse from the DAC are held for an entire symbol time, this implies sinx/x filtering of the input 16 -ary impulses--and consequently requires x/sinx correction in the VCO baseband filter. The baseband filter output is applied to the summer in the VCO closed loop. F(s) is a wideband loop filter in the VCO modulating loop. The output of the VCO is immediately converted back to a baseband signal by a discriminator (DISC) and the DISC output is subtracted in the summer from the baseband input modulating signal to generate an error signal for the closed loop. The basic idea is that the VCO is modulated such that there is no error between the baseband modulating signal and the output of the DISC. If the DISC characteristic in the modulator loop is identical to the DISC at the demod, this circuit at the modulator linearizes the signal path through the VCO and the demod DISC. It has been found at Harris that the stabilities of the delay line used to implement the DISC function is such that excessive center frequency drift is experienced without the circuit enclosed in dotted lines on the viewgraph. The purpose of this circuit is to stabilize the center frequency drifts of the VCO modulator without the circuit. The basic idea employed in this circuit is to compute the net phase change desired from the VCO over some many-symbol time interval by counting the instantaneous 4-bit frequency data from the input. Similarly, the phase change actually produced from the VCO is counted. The difference between the desired and the produced counts provides an error signal after D- to-A conversion that is filtered and used to correct for center frequency drift.



NASA/TDMA MODULATOR CONCEPT

Viewgraph 10

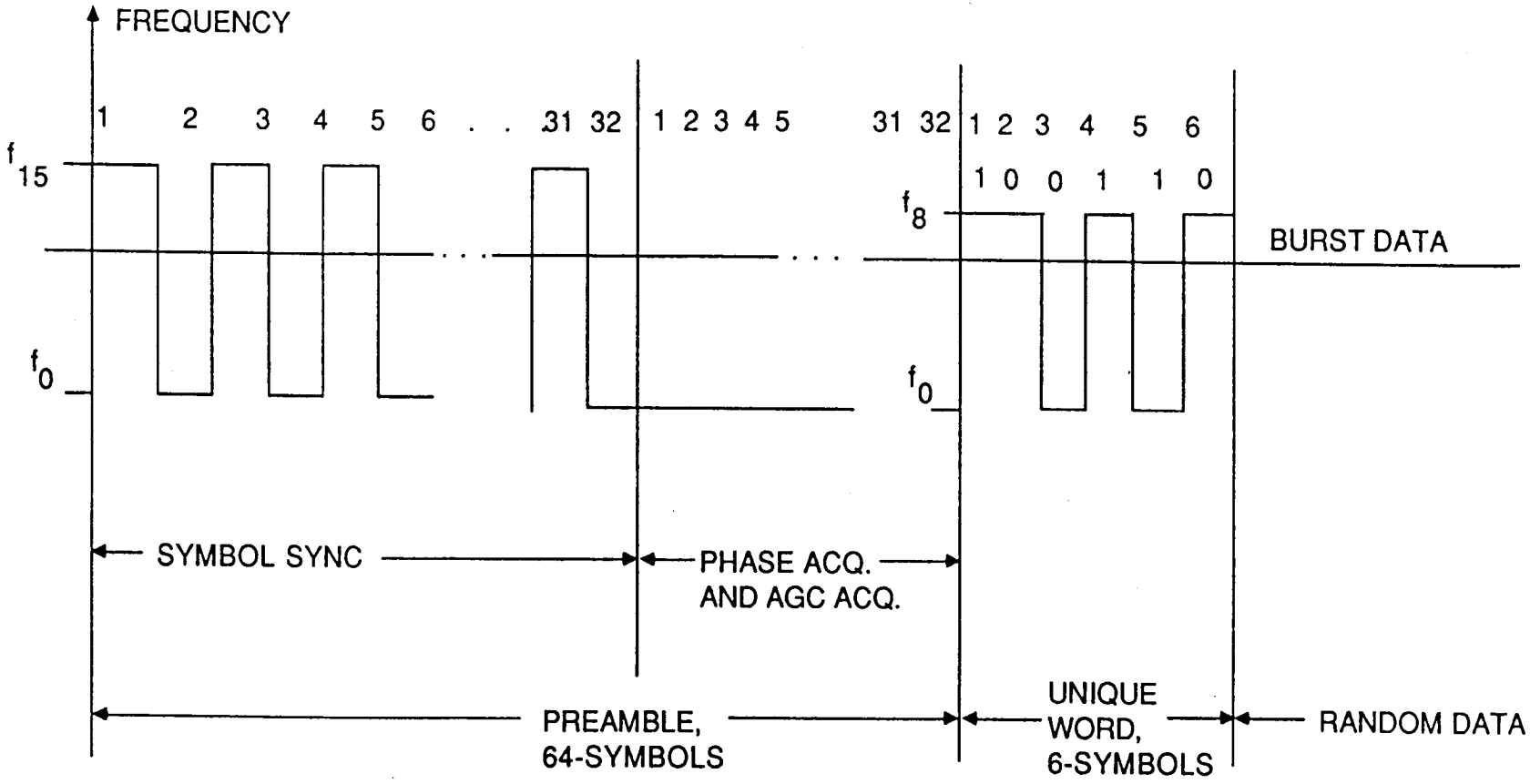
This viewgraph shows a conceptual block diagram for the demod coherent phase detector. As shown, the IF signal is IF filtered, discriminator detected, and square root Nyquist (i.e. Half Nyquist) filtered. The filtered output is passed to the symbol timing circuit and the A/D which drives the baseband loop providing coherent phase measurements. The symbol timing circuit works on the TDMA preamble pattern (described on the following viewgraph) to derive symbol clock as well as a coarse burst detect signal. This signal is provided to timing and control as well as to the block labelled "Burst Detect". The purpose of the "Burst Detect" block is to detect when the preamble has entered the constant f0 (lowest frequency) portion of the preamble by detecting 4 f0's in a row. When this happens, the 8-bit A/D words are passed to the AGC digital multiplier, and thence on to the accumulator loop previously discussed. The AGC loop adjusts gain on the digital baseband signal being fed to the accumulator loop and the DC restore loop acquires coherent phase in the accumulator. The Unique Word Detector observes 6 successive samples from the accumulator loop to detect the predetermined pattern of 0 and 180 degree phases in the accumulator. The detection of this Unique Word gives the t=0 indication for the received burst and coherent phases immediately following the Unique Word are freed to pass on to the decoder for the decoding of the random data portion of the burst.



NASA/TDMA DEMOD PHASE DETECTOR CONCEPT

Viewgraph 11

This viewgraph shows the preamble modulation employed on our modem. 32 symbols of alternating peak-peak deviation (f0 and f15) are employed for the purpose of synchronizing the symbol timing circuitry. 32 symbols of constant f0 (lowest frequency) follow and this portion allows acquisition of AGC and coherent phase in the baseband accumulator. Next follows 6 symbols of Unique Word signal. This UW will use f0 and f8 frequencies to swing the accumulator through the desired sequence of 0 and 180 degree phase in the accumulator. Random burst data follows on the heels of the Unique Word.

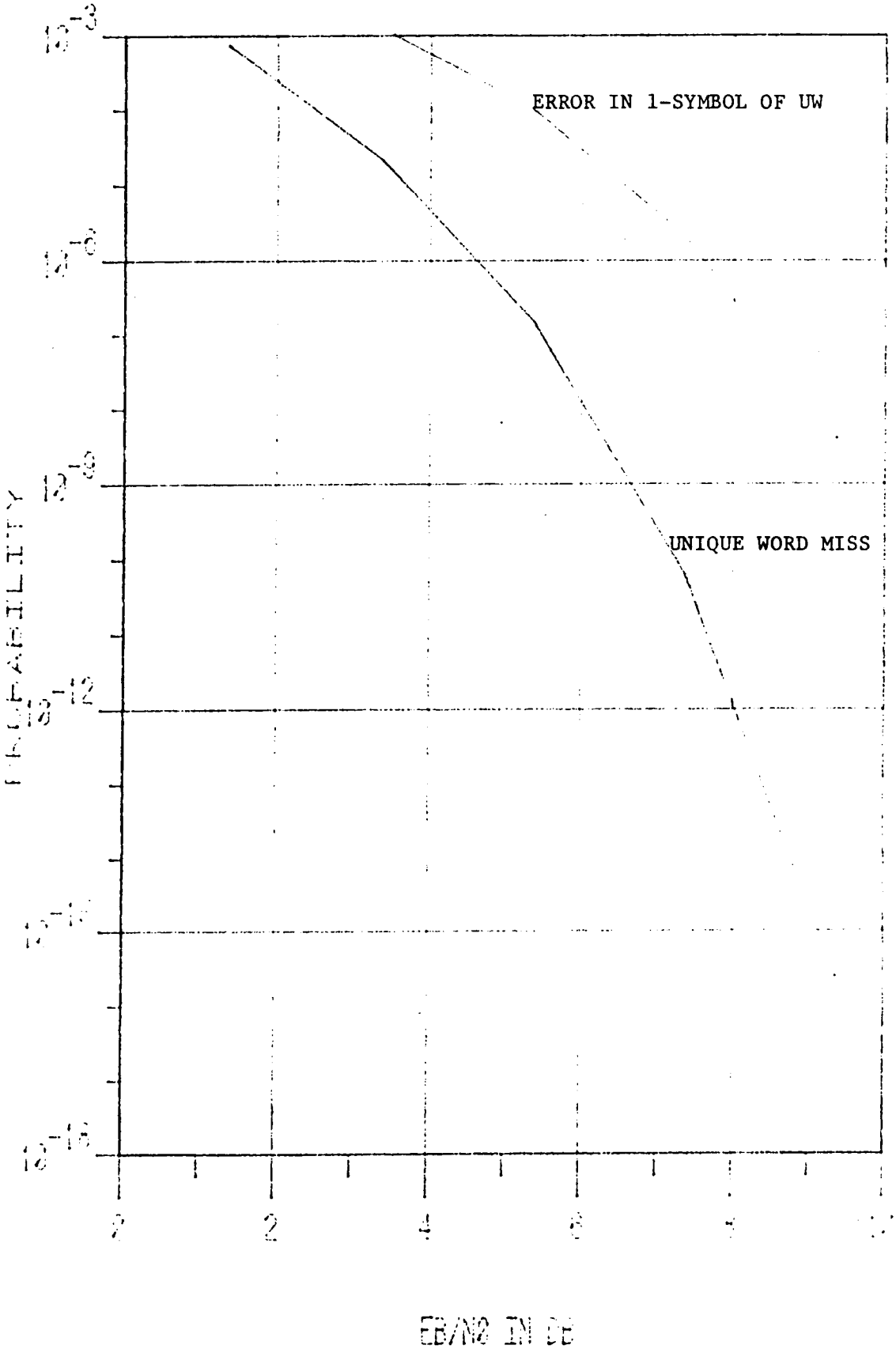


BURST STRUCTURE

Viewgraph 12

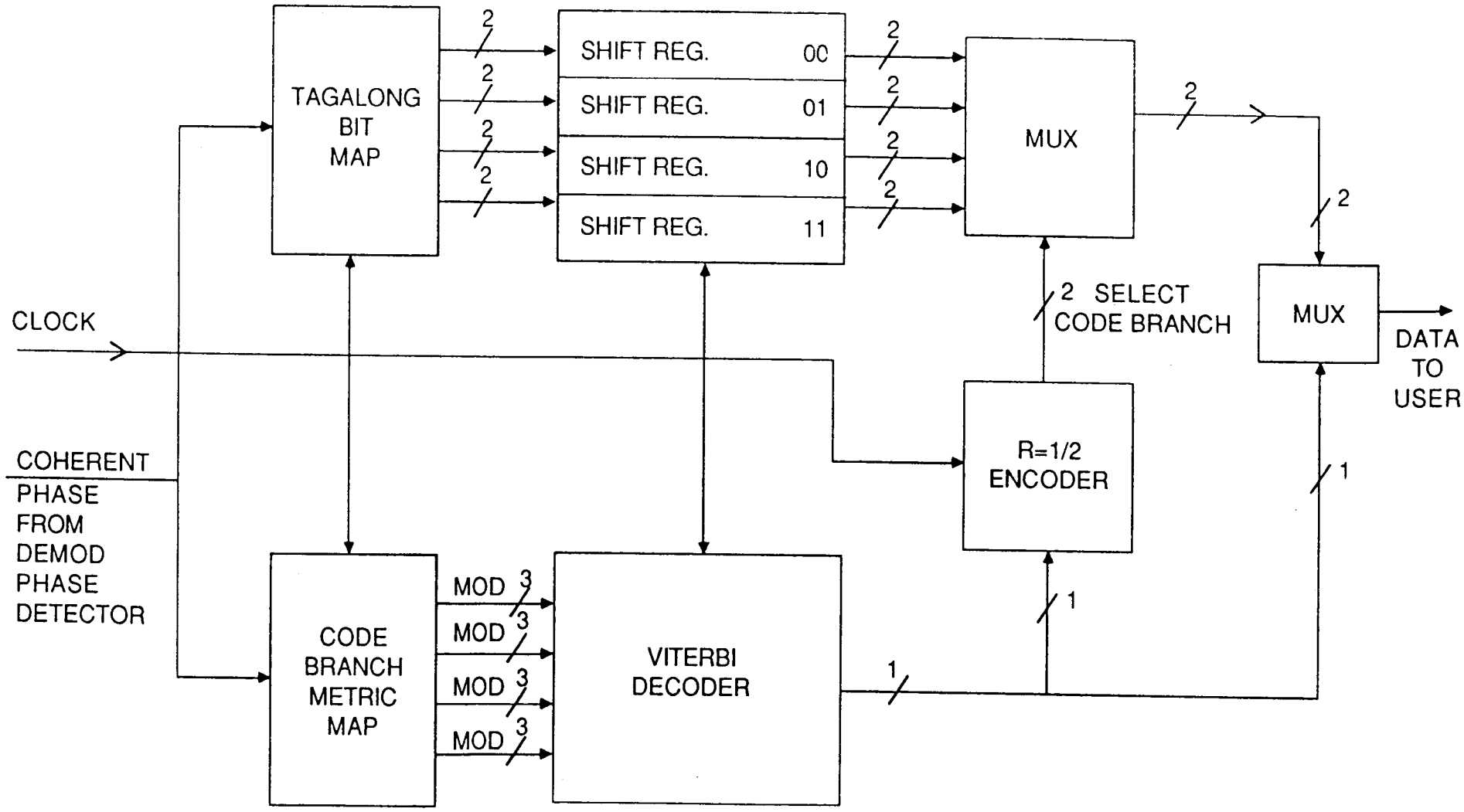
This viewgraph shos the probability of missing the 6-symbol Unique Word versus Eb/N0 when one symbol is allowed to be in error out of the 6 symbols of the Unique Word.

PROBABILITY OF MISSING UNIQUE WORD



Viewgraph 13

This viewgraph shows the fundamental manner in which the Viterbi decoder is employed to produce the decoded information bits from the coherent phase measurements provided by the coherent phase detector. As shown, coherent phases are input to the tagalong bit map and to the code branch metric map. The tagalong bit map provides the 2 tagalong bits for each of the 4 phases closest to the coherent phase measurement input. As previously mentioned in connection with Viewgraph 6, each of these pairs of tagalong bits will be associated with one of the four possible rate 1/2 code branches: 00, 01, 10, and 11. Consequently, as shown on Viewgraph 13, these four pairs of tagalong bits are output from the map into four 2-wide shift registers labelled 00, 01, 10, and 11 to correspond to the code branch with which the tagalong bits are associated. Simultaneous to this tagalong mapping operation, the coherent phase measurement is also observed by the code branch metric map, wherein a metric for each of the four code branches is accessed. The metric is proportional to the phase distance of the corresponding candidate code branch from the actually received phase measurement. These metrics, labelled M00, M01, M10, and M11 in Viewgraph 13, are processed by the Viterbi decoder where, after some decoder delay, a decoded information bit emerges. This is the bit originally input to the decoder at the modulator. This decoded bit is re-encoded to produce the decoded 2-bit branch. This 2-bit decoded code branch is used to select the appropriate one of the four tagalong bit pairs. The 2 tagalong bits, along with the decoded information bit, make up the total of three information bits originally input to the modulator. Consequently they are muxed together and passed to the user as shown in Viewgraph 13.



NASA/TDMA ERROR CORRECTION DECODER CONCEPT

TDMA ENCODER BLOCK DIAGRAM

Incoming (200 Mbps) data is serially shifted into a high speed register. After 11data bits are accumulated in the register, this data is then parallel loaded into another register and subsequently written to an ECL RAM data buffer. A BURST COMMAND signal is also sent with the incoming fast data. The rising edge of the signal indicates the beginning of valid data. The falling edge indicates the end of valid data and is also used as a request to process the data and transmit a burst.

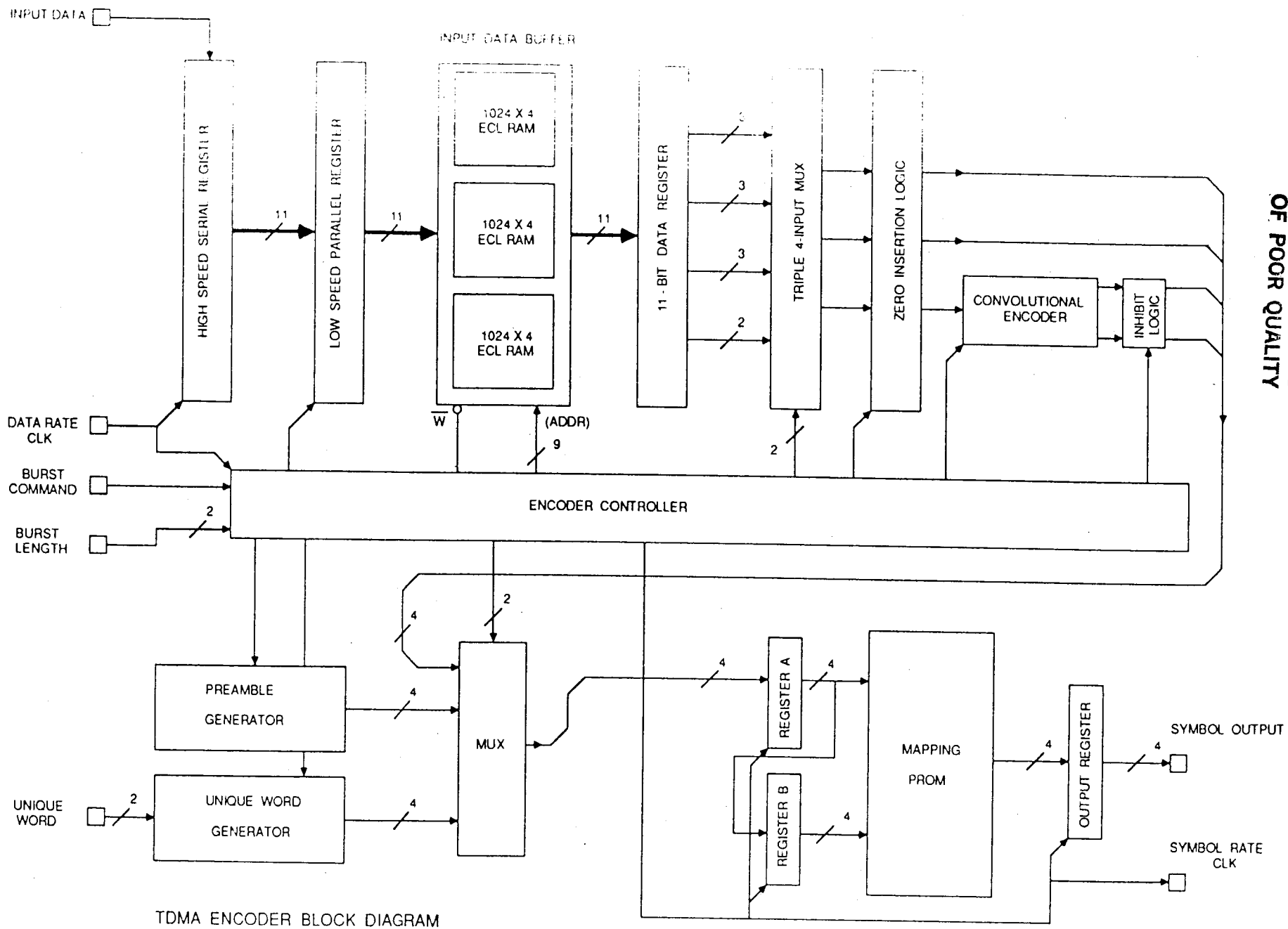
When the falling-edge burst command is initiated, the preamble generator is activated. This produces a 64-symbol preamble pattern. The first 32 symbols are alternating f_0 and f_{15} symbols. The next 32 are all f_0's. This pattern was chosen to aid in initial acquisition of the TDMA modem.

After the preamble is completed, the unique word generator is then invoked. This produces six more symbols that immediately follow the 64-symbol preamble. The unique word pattern is contained in a PROM (as is the preamble pattern). The current design is such that up to four different unique word symbol patterns can be selected via external control lines.

After the unique word has been generated, the RAM data buffer is then read and the resultant data is formed into symbols and sent to the modulator. Every time the RAM buffer is read, 11 data bits are accessed. These bits are grouped into three groups of 3 bits and one group of 2 bits. Two bits of the 3-bit groups are used directly as (MSB) data bits. The last bit in the 3-bit groups is sent to a K=7, rate 1/2 convolutional encoder and two (LSB) bits result. These two encoded bits are grouped with the two unencoded data bits to form a 4-bit modulator symbol. Every fourth symbol the remaining 2-bit group is combined with forced "00" bits that take the place of the encoded LSB bits. This operation is done to aid in maintaining lock at the demodulator.

The resultant 4-bit symbols are sent to the modulator via a "mapping function." The 4-bit symbols produce a 16-point phase constellation. To get from one 4-bit phase point to another, the modulator must send the "difference" in phase from the current point to the desired point. The mapping PROM shown in the block diagram performs this differencing function. Register A contains the current 4-bit symbol and register B contains the previous symbol. The mapping PROM calculates the required 4-bit modulator symbol to send. The calculated symbol is sent to the modulator via the output register shown in the diagram. A symbol rate clock is also provided to the modulator.

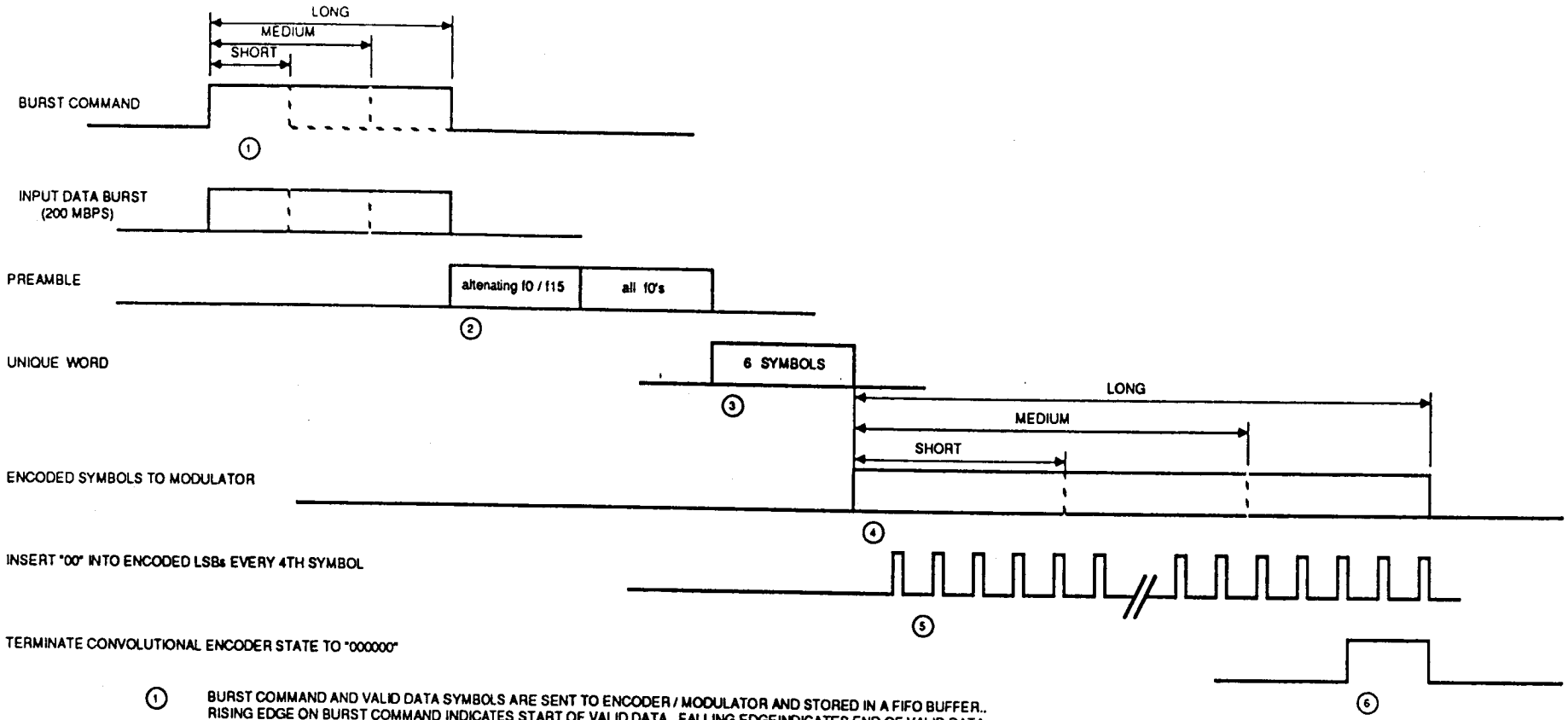
Towards the end of the valid data, the data bits read from the RAM input buffer are manipulated such that the last 16 bits are all "direct data bits" (i.e. no more data bits go into the convolutional encoder.) Instead, zeroes are fed into the convolutional encoder and the resultant bits are used to form the final symbols. This operation of feeding zeroes into the encoder is done so that the encoder state will end up at all zeroes (000000) when the last of the data is read from the RAM buffer. This results in the convolutional encoder always starting at 000000 and ending at 000000. It is beneficial to terminate the encoded sequence this way since we can take advantage of this a-priori knowledge at the demodulator/ decoder and gain a slight performance advantage. Once all the data in the RAM buffer has been read out and converted to modulator symbols, the TDMA ENCODER / MODULATOR logic is ready to receive another burst of data.



TDMA ENCODER BLOCK DIAGRAM

DEC. 15, 1986

TDMA ENCODER SEQUENCE OF EVENTS



1. BURST COMMAND AND VALID DATA SYMBOLS ARE SENT TO ENCODER / MODULATOR AND STORED IN A FIFO BUFFER.. RISING EDGE ON BURST COMMAND INDICATES START OF VALID DATA. FALLING EDGEINDICATES END OF VALID DATA AND IS A REQUEST TO BEGIN SENDING OUT AN ENCODED BURST OF SYMBOLS.

2. PREMABLE GENERATOR IS ACTIVATED, 64 SYMBOL PREAMBLE IS SENT OUT; 32 SYMBOLS ARE ALTERNATE F0 / F15. 32 MORE SYMBOLS ARE ALL F0 SYMBOLS.

3. WHEN PREAMBLE IS COMPLETE, UNIQUE WORD GENERATOR IS ACTIVATED. A 6 SYMBOL UNIQUE WORD IS GENERATED THAT IMMEDIATELY FOLLOWS THE PREAMBLE.

4. AFTER THE UNIQUE WORD IS COMPLETE, THE INPUT FIFO BUFFER IS READ OUT IN 11-BIT WORDS. THESE BITS ARE FORMATTED INTO FOUR SYMBOLS PER THE BLOCK DIAGRAM DESCRIPTION.

5. EVERY FOURTH SYMBOL THE CONVOLUTIONAL ENCODER IS PAUSED TO ALLOW THE INSERTION OF "00" BITS INTO THE LSBs OF THAT SYMBOL.

6. FOR THE LAST 16 BITS OF INPUT DATA, ALL BITS ARE USED AS "TAG-ALONG" BITS. ZEROES ARE CLOCKED INTO THE CONVOLUTIONAL ENCODER AND THE RESULTANT ENCODED DATA IS USED AS THE SYMBOL LSBs. THE CONVOLUTIONAL ENCODER STATE IS AT 000000 AT THE END OF THE VALID DATA FROM THE INPUT FIFO BUFFER.

DATA BIT MANIPULATION

The TDMA Encoder / Modulator reads an 11-bit wide word from the input data RAM buffer. It formats these into groups of 3, 3, 3, and 2 bits. Most of the time the 3-bit groups are partitioned such that the first 2 bits are used as "tag-along bits" (taken directly as MSBs of a modulator symbol). The remaining bit is processed by a R =1/2, K=7 convolutional encoder. The 2 bits resulting from this encoding (LSBs) are paired with the 2 tag-along bits (MSBs) to form the 4-bit modulator symbol. This action continues for the next two 3-bit groups.

The fourth group of bits taken from the 11-bit word contains only two data bits. These bits are used directly as tag-along bits. Two "zero" bits are placed in the location where the usual encoded LSB bits would have gone. During this fourth symbol time the encoder is paused one cycle to avoid losing any bits. No new bits are sent to the encoder nor are any bits used from the encoder during this fourth symbol time. This approach of forcing 00 in the modulator LSB locations every fourth symbol provides a 4-ary constellation (as opposed to 16-ary) which aids the demodulator in maintaining sync.

Towards the end of the data burst (during the last 16 data bits), the convolutional encoder state is terminated to 000000. The last 16 data bits from the RAM buffer are used to produce eight final modulator symbols. During eight symbol times, the encoder is paused twice (once every 4th symbol). This leaves just enough time to clock six zeroes into the convolutional encoder so that its end state is 000000.

Since the encoder is forced to 000000 at the end of data, it will start up at 000000 at the beginning of the next data burst. The demodulator / decoder can take advantage of this a-priori knowledge by initializing the Viterbi decoder accordingly thereby gaining a slight performance advantage.

The manipulation of the final 16 data bits deviates from the usual order of 3, 3, 3, and 2 because of the introduction of six zeroes into the convolutional encoder. As the block diagram shows, the first 2 bits of the first 3-bit group is used as before. However, the bit that would have been encoded is now used along with the first bit of the second 3-bit group to form the tag-along bits for the second symbol. The resultant output bits from the convolutional encoder are still used as the LSBs of the final modulator symbols.

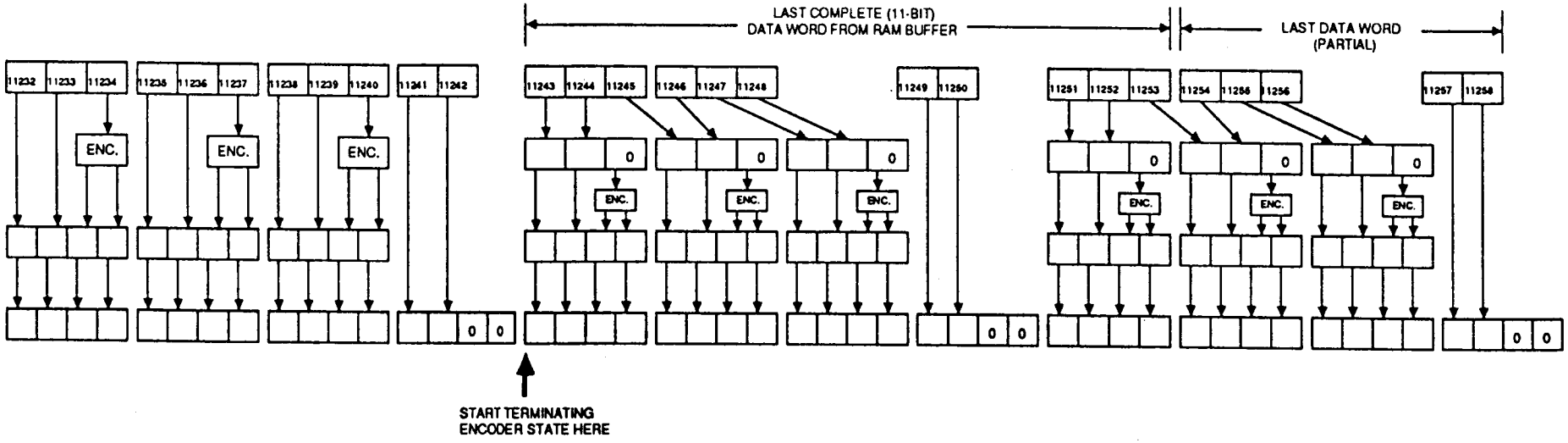
The MSBs for the third modulator symbol are formed from the NSB and LSB of the second 3-bit piece. In the fourth symbol the MSB and NSB of the third 3-bit group are used for the tag-along bits. The LSBs for the fourth symbol are forced to 00 and the convolutional encoder is paused.

The fifth modulator symbol is formed from the LSB of the third 3-bit group and the MSB of the following 2-bit group (to form the symbol MSBs) and the LSB outputs of the convolutional encoder.

Next, the LSB of the previous 2-bit data group and the MSB of the first 3-bit group in the final word read from the data buffer are used as MSBs for the sixth symbol. The NSB and LSB are used as the tag-along bits for the seventh symbol. The final zero is sent to the convolutional encoder and the resultant bits are used as LSBs for this symbol.

The final two remaining data bits are used as the final tag-along bits in the eighth and final symbol. The LSBs are forced to 00. This ends the modulator burst.

DATA BIT MANIPULATION ON TDMA ENCODER CIRCUITRY - NOV. 21, 1986



BURST LENGTH	No. SOURCE BITS	No. XMT'D SYMBOLS
LONG	11258	4096
MEDIUM	3734	1360
SHORT	170	64

RF MODULATOR

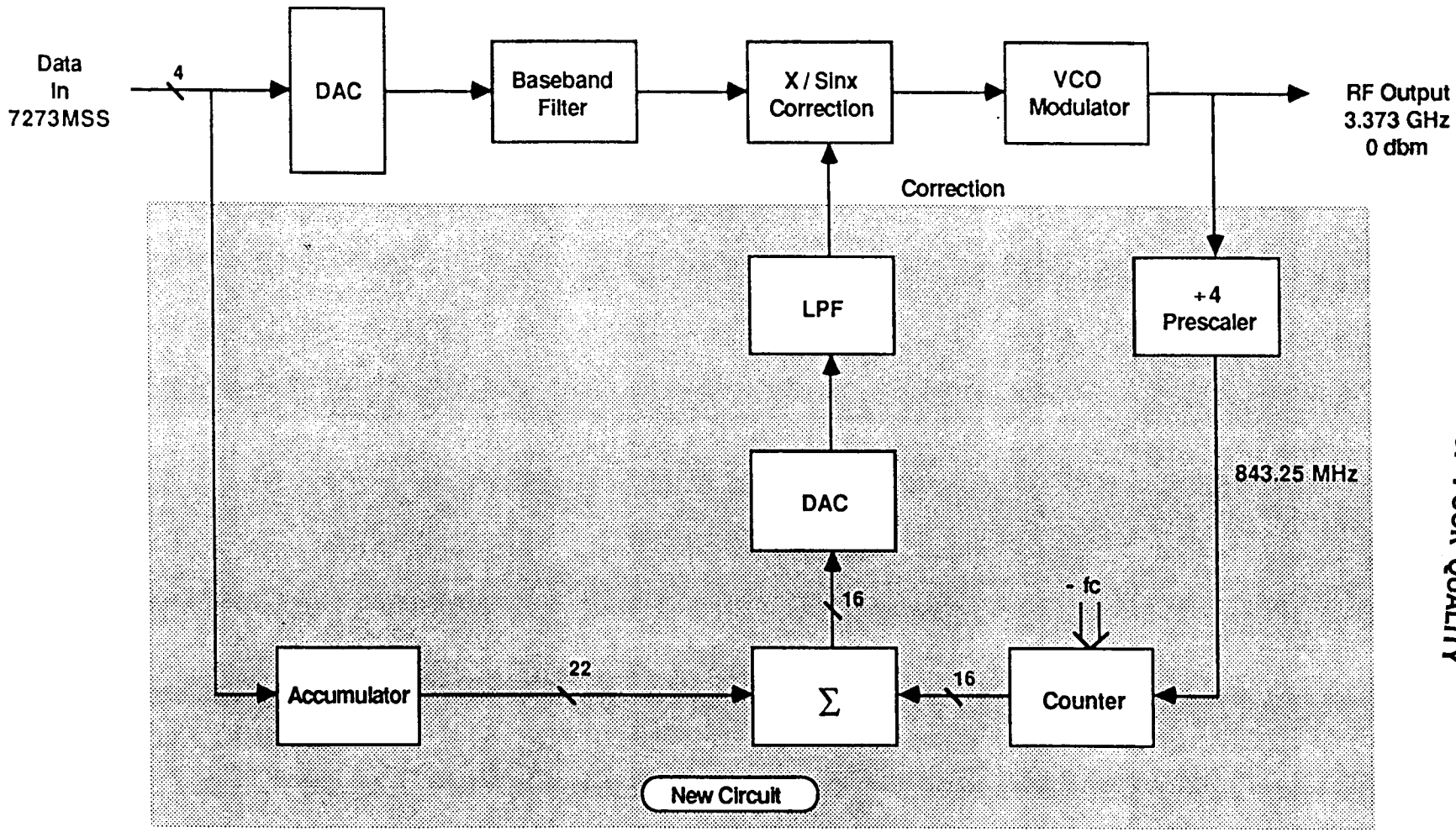
There have been several changes in the modulator design since the last review.

1) Based on the results of breadboard testing, the NE5539 VHF op amp used in the loop filter has proven inadequate. It has a time delay of about 6 nsec which is far in excess of what can be allowed. The time delay in the VCO loop due to all causes must be held to 2 or 3 nsec max.

2) The delay stability of the best known delay line used in the discriminator is inadequate to provide the desired frequency stability of the transmitted frequency even with an oven. An oven stabilized discriminator would produce output frequency errors of 20 to 40 KHz.

   To solve the frequency stability problem a low speed outer frequency stabilizing loop has been added.

   For a 256,000 symbol interval (≈ 3.5 msec) the output frequency is counted and the input data is accumulated. The data accumulation represents the average desired transmitted frequency and the count of the output represents the actual average output frequency and the difference between the two is the average frequency error. The frequency error is DA converted, filtered and applied to the VCO modulator as as a frequency correction. The frequency correction is performed at 284 Hz rate and is therefore able to track any time/temperature frequency variations. The resolution is 1136 Hz/bit in the frequency counter and 1136/64 or 17.75 Hz in the Data accumulator.



RF Modulator

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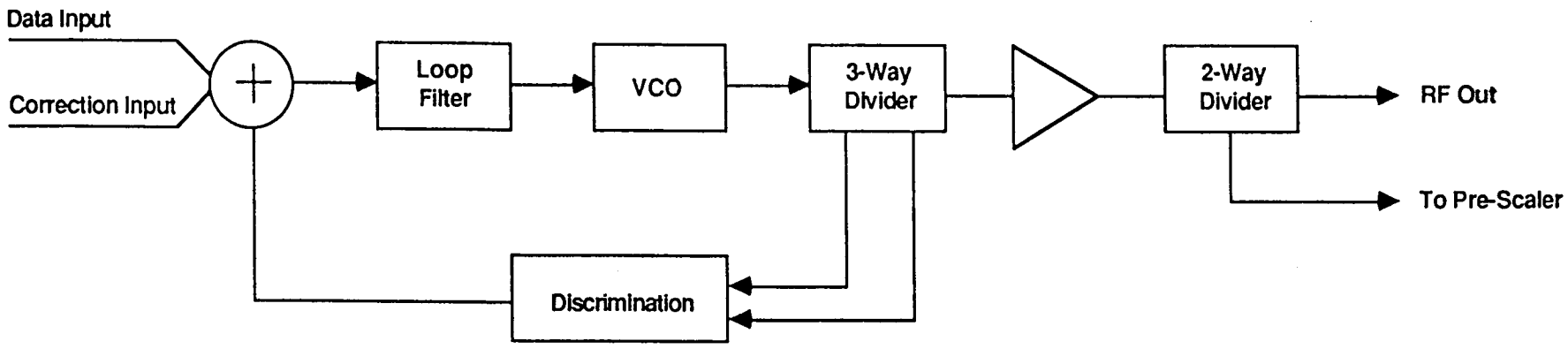
JAG.1(2)
1-23-87

VCO MODULATOR

The VCO Modulator has been redesigned based upon the results of Breadboard testing to minimize the total time delay around the loop.

The time delay problem in the breadboard was do to two major sources. First, the NE5539 op amp used in the loop filter had excessive (6-7 nsec) propagation delay, it has been replaced with a design using discrete transistors that has a propagation delay of about one nsec. Second, the physical layout and the use of connectorized components contributed significantly to the delay around the loop. To minimize this connectorized components are not being used and considerable effort was made in the PWB layout to minimize the loop delay.

The new loop is just beginning test now.



VCO Modulation

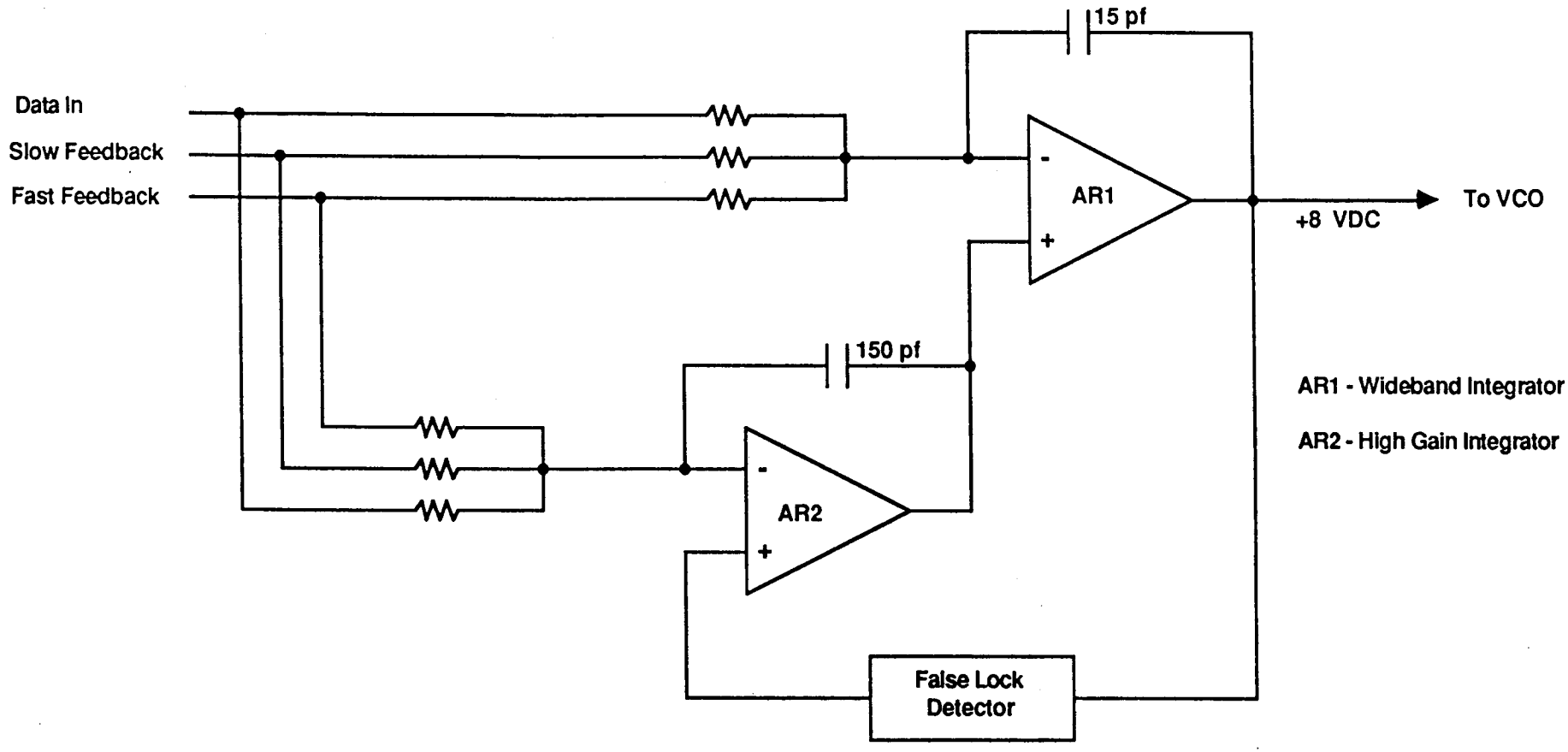
JAG.1(1)
1-23-87

LOOP FILTER

The loop filter needs to provide an integration function with a bandwidth of at least 100 MHz with a time delay of 1-2 nsec (the lower the better). The NE5539 could provide the bandwidth but the time delay was too great.

A Hybrid approach using a discrete transistor amplifier (ARI) for bandwidth and an IC OP AMP (AR2) for dc gain. The path thru the inverting input of ARI has a very wide bandwidth (>500 MHz) low gain and poor dc offset. The path thru ARI and AR2 has moderate bandwidth (≈ 10 MHz) very high dc gain and low dc offset. The output is a sum of the paths. As shown in the next viewgraph the circuit is dominated by AR2 below 500 KHz, by ARI above 10 MHz with a crossover region in between. In this way it is possible to get some of the benefits of a 2nd order loop without the additional time delay of a second cascaded amplifier.

During breadboard testing it was discovered that the loop was very prone to false locks. To prevent this a false lock detector was added. The false lock detector senses the average dc voltage at the VCO input and if in error drives it to the correct value.



Loop Filter

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LOOP FILTER BODE PLOT

Desired Loop Filter Bode Plot showing the effect of the High gain amplifier on the overall response.

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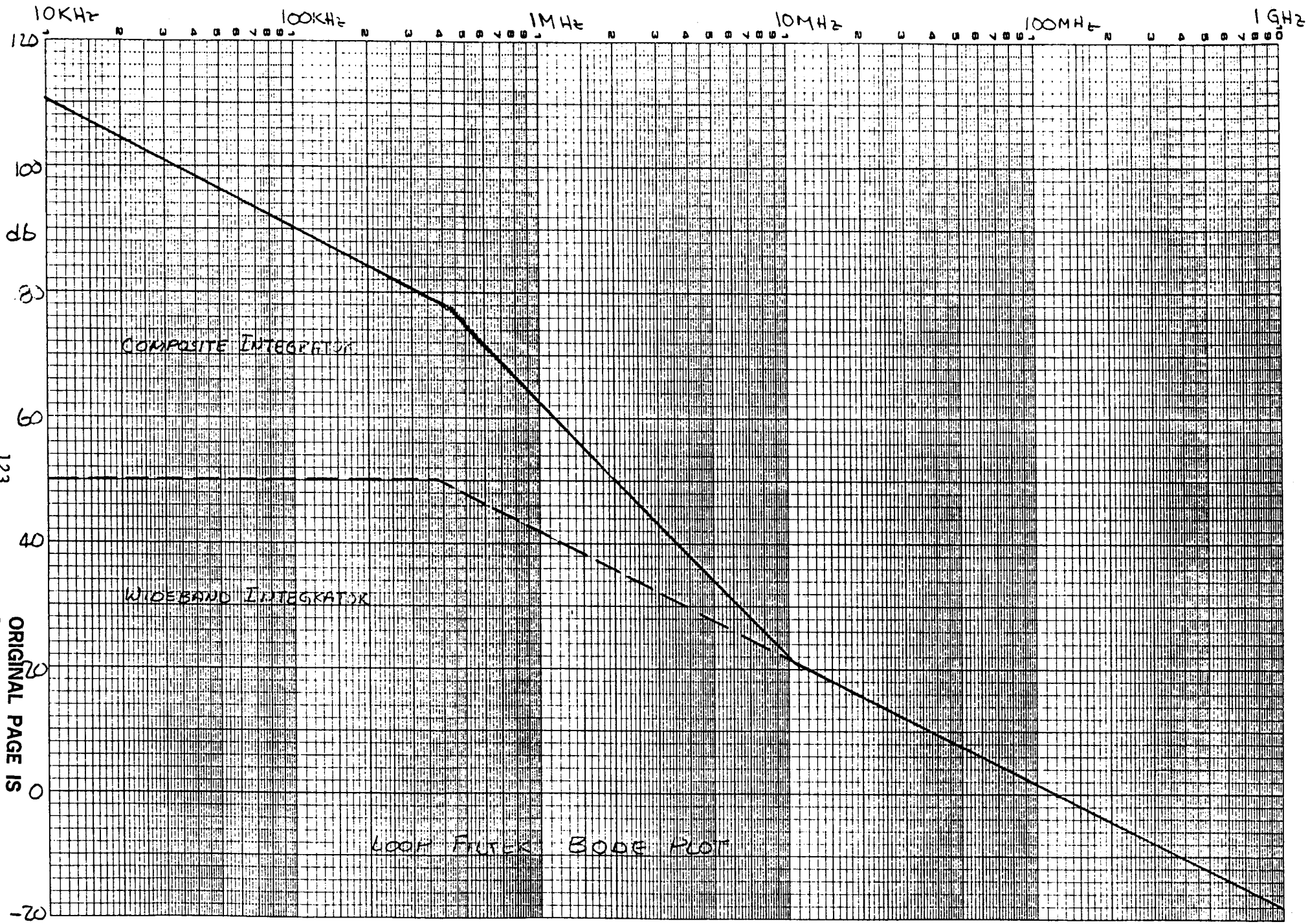
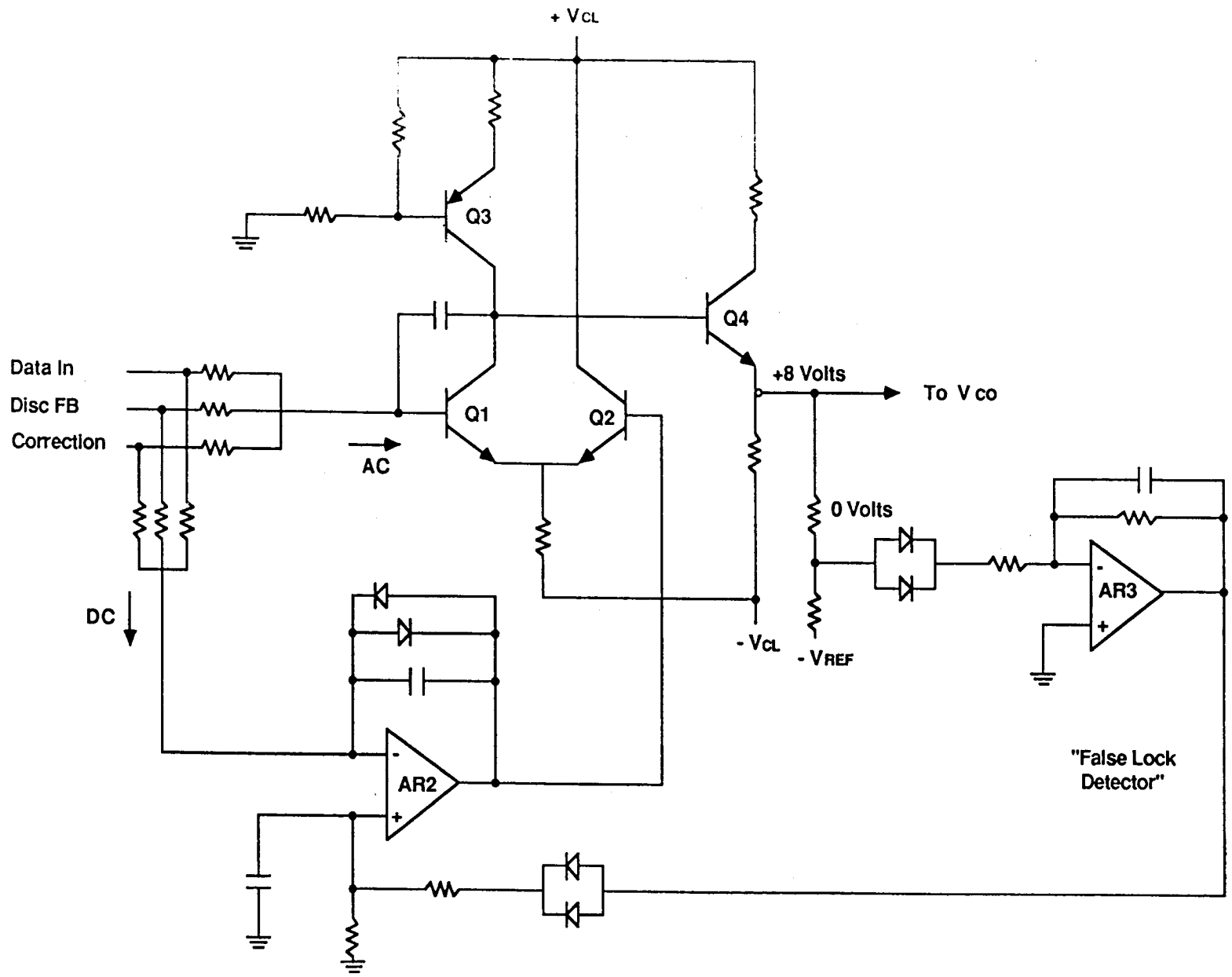


LOOP FILTER SCHEMATIC

The wideband Amplifier (ARI) is a single differential gain stage (Q1, Q2) with a emitter follower (Q4). To get high gain a current source (Q3) load is used for Q1. This topology gives a moderately high gain and a single pole frequency rolloff, just what is needed. Some breadboard test results are shown in the following viewgraphs.

AR2 and its associated components is the high gain path. The diodes is the feedback of AR2 limits the output voltage to prevent overdriving Q2.

AR3 and it's associated components is the false lock detector. The output voltage from Q4 (VCO input) is applied to a voltage divider to a negative reference voltage. When the VCO input is at the correct value (+8 V dc) the voltage divider output is zero volts. The voltage divider is applied to AR3 thru diodes to provide a dead zone of about ± 1 volt so that small errors do not activate the circuit. AR3, R18, R16, & C2 are a "leaky" Integrator with a dc gain of 100 and a time constant of 1 sec. If the average VCO input is in error by more than one volt AR3's output will begin to ramp either up or down until the threshold provided by D6 and D7 is exceeded at which time the loop filter is driven such that the false lock paint is abandoned and proper lock is achieved. The effect of the diodes in the input and output circuits of AR3 is that when not needed the false lock detector switches itself out of the circuit completely. During breadboard testing the false lock detector worked with 100% reliability.



Loop Filter

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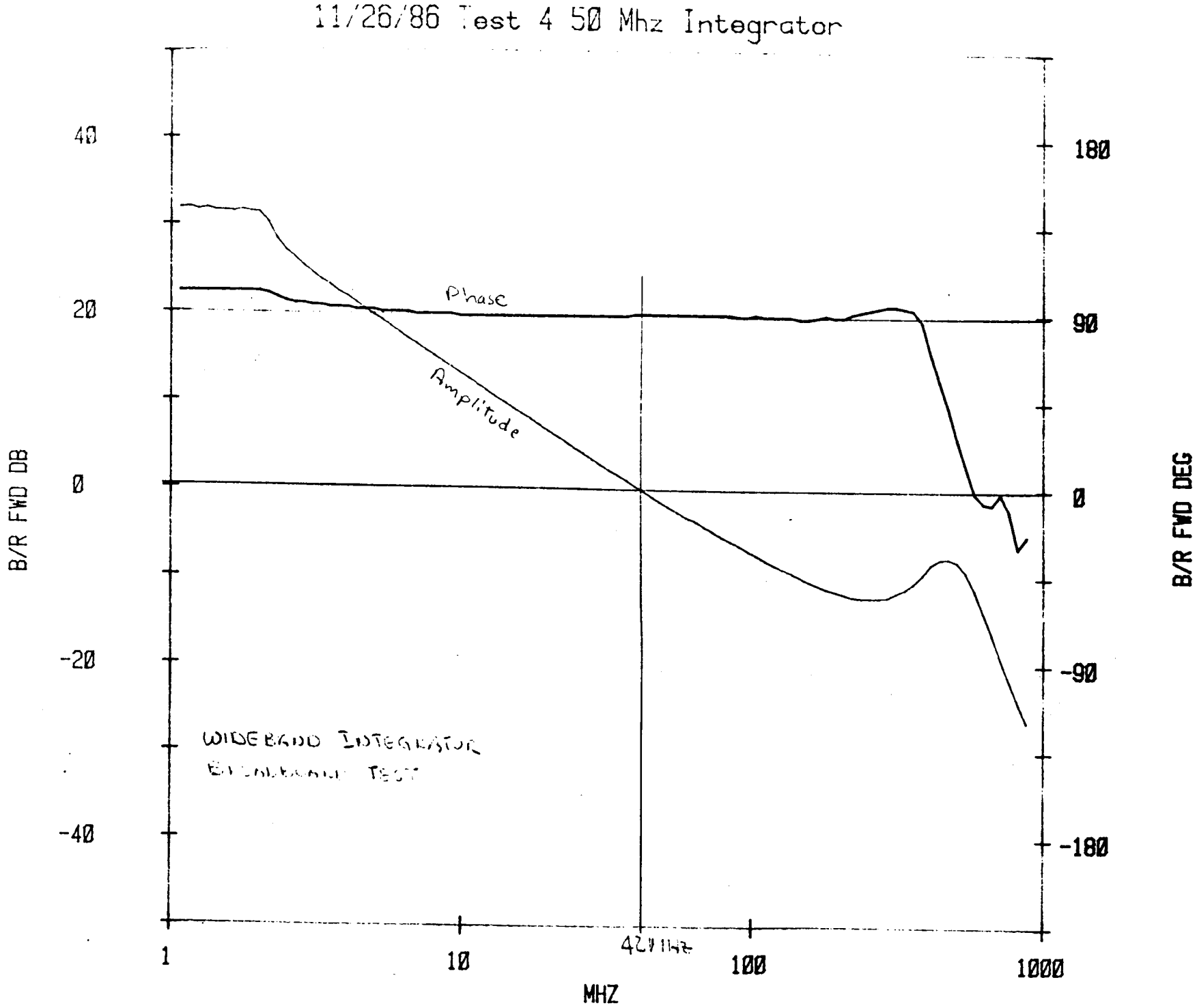
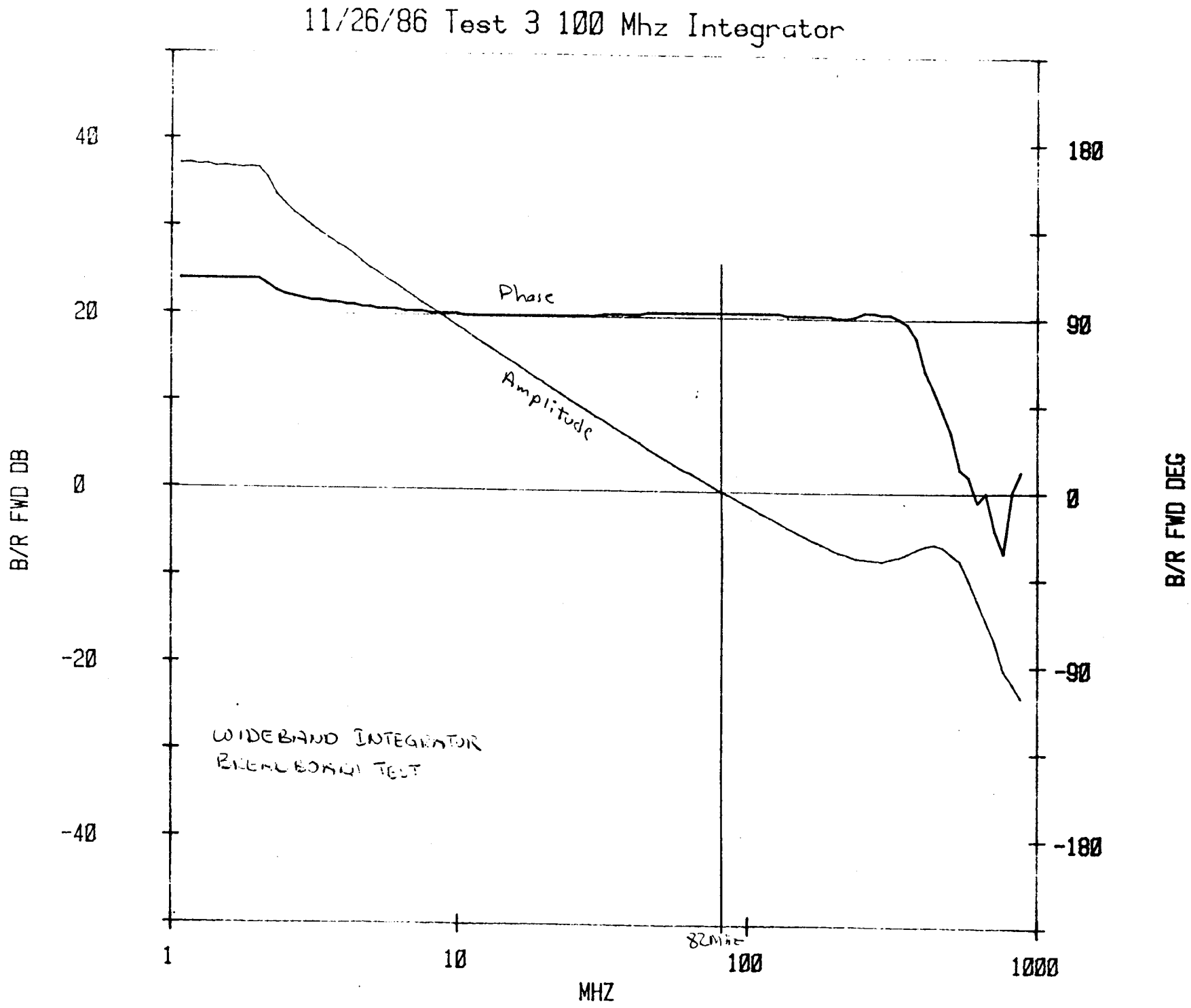
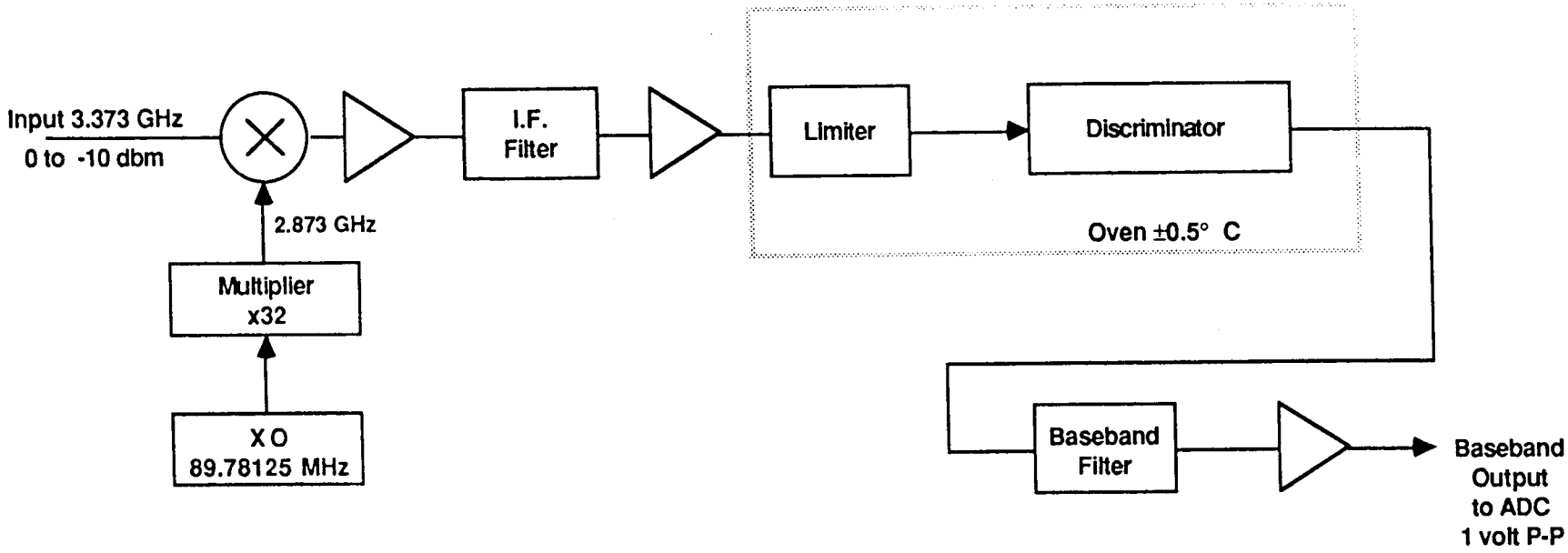




DEMODULATOR INPUT RF

The Input RF has not changed since the last review, except for some additional detail. The Input signal at 3.373 GHz is downconverted to 500 MHz and Bandpass Filtered to remove undesired sidebands and out of band noise. The Filtered signal is limited to maintain the signal level to ±0.1 db in amplitude. The Limited signal drives the frequency discriminator which is a wideband delay-line discriminator. The center frequency stability and sensitivity are very important and it is therefore necessary to ovenize the limiter and entire discriminator to insure adequate performance. The limiter, a WJ-L40 typically has an output level stability of ± 1db over a temperature range of from -55°C to +85°C or about 0.015 db/°C. With a ±0.5°C oven the limiter output should remain constant to within ±0.01 db or better. The discriminators most serious problems are dc offset in the mixer and delay variation of the delay line a delay line made from coax can be made with a delay variation of about ±5 ppm/°C over a temperature of from 0 to 120° F. With a ±0.5°C oven this represents a frequency stability of ±1250 Hz. The mixer DC offset stability vs temperature is not known at this time but is expected to produce errors of a similar to that due to delay variations or 1 to 2 KHz.



Demodulator Input RF

JAG.1(3)
1-23-87

PHASE DETECTOR TOP LEVEL DESCRIPTION

The phase detector block diagram depicts the major functional parts of the phase detector circuitry. It also divides the phase detector circuitry into four parts to facilitate a more detailed examination of the phase detector circuits. The input to the phase detector is a coherently sampled, and filtered 8-bit word. This signal must be integrated to yield coherent phase.

Several practical problems exist using this method of demodulation; 1) How does one know at t=0, what value to place in the baseband integrator? (this is tantamount to guaranteeing that the signal emerging from the integrator is truly coherent phase), 2) A normal phase detector has a modulo 2*pi characteristic. How can we make our integrator display the same characteristic? 3) How does one set the gain on the output of the discriminator so that exact, coherent phase, is truly measured? (an error here will cause severe walk off problems), 4) What about DC offset in the discriminator output? Such and offset will cause phase to walk away in the integrator, just like unaquired frequency offset does in a standard PLL. How is such offset tracked with the current approach? 5) Finally, with this coherent phase measurement technique, how are the TDMA burst acquisition problems solved? That is, the demodulator must be able to acquire all three parameters above, for independent user bursts, within a preamble length. The following circuits provide the answers to these questions.

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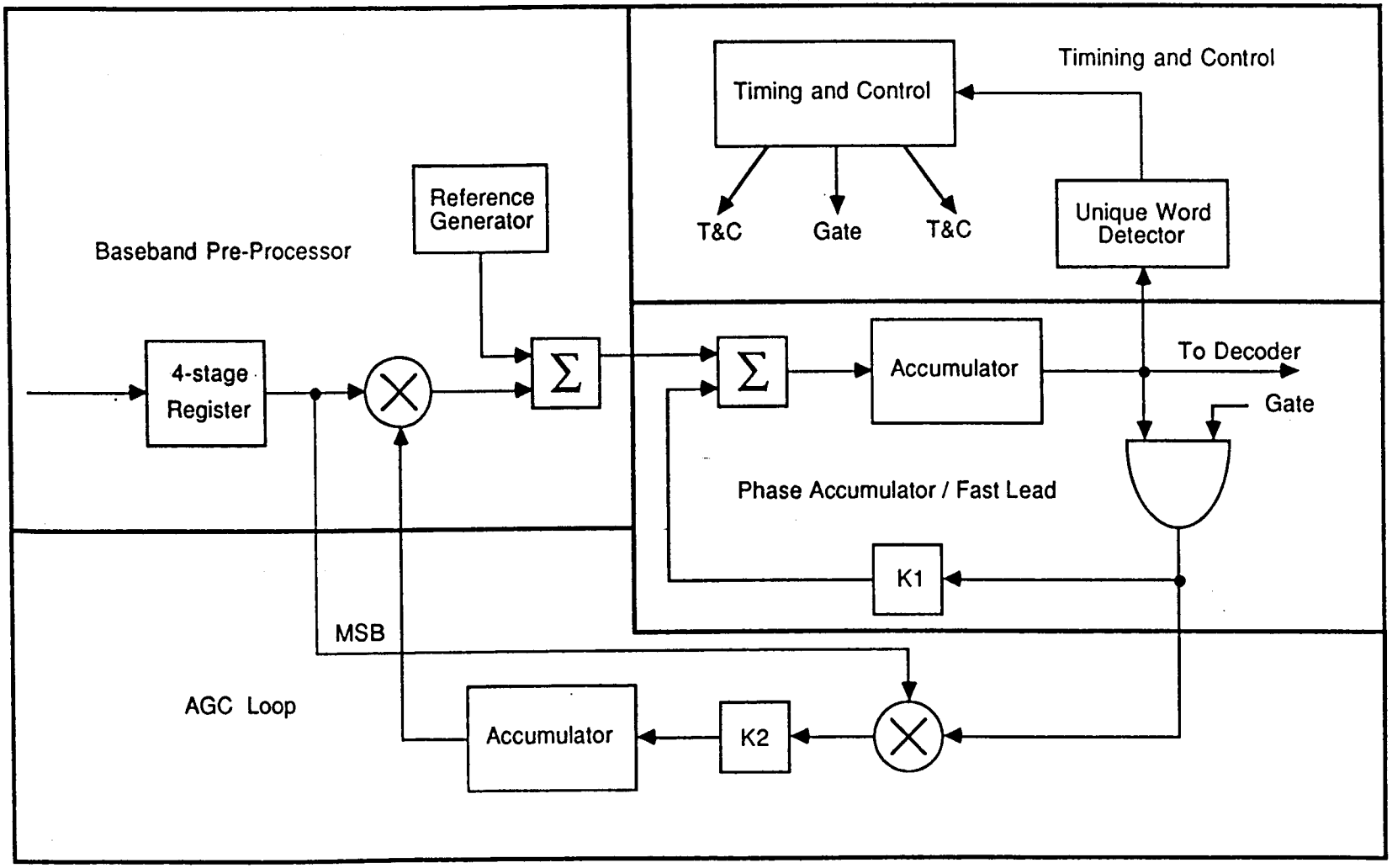
Phase Detector Block Diagram



Phase Detector Baseband Preprocessor

Eight bit samples (of the baseband filtered, discriminator output) are input to the phase detector at the symbol rate of 72.73 MHz, and sequentially stored in four registers. This facilitates the checking of data, to determine whether the "all fo's" portion of the preamble is being received. If it is, then the remaining registers in the phase detector circuitry are allowed to operate normally. If it is not, then the remaining registers are asynchronously held low. The output of the fourth register, along with a 16-Bit AGC correction factor, K, are input to a 16x16 ECL multiplier. This multiplier scales the incoming data by an amount proportional to an AGC error term (the generation of this error term will be discussed later). Thus, question number three (3) has been answered by this circuit. The gain at the output of the discriminator will be compensated for digitally, using a multiplier. Therefore, the integrator will not "walk-off" due to AGC missetting. This approach does however, rely on the discriminator output gain setting to be no more than ± 6.25% off, initially (which should be easily achievable). At the output of the multiplier, a binary number is added to the two's complement product such that, when fo is received "perfectly", then the result of the multiplication/addition is the number zero (0). This may be viewed as a reference generator.

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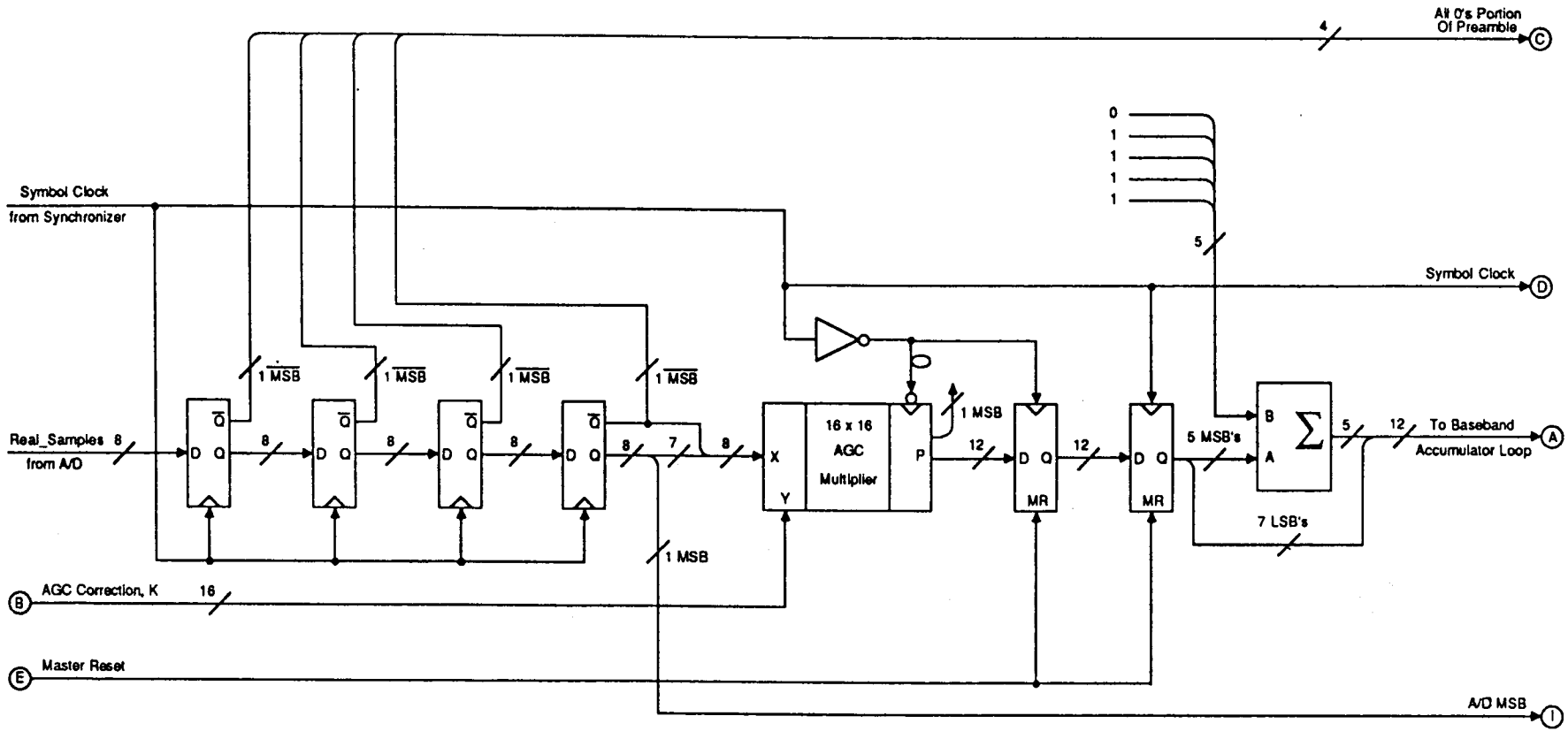
Baseband Pre-Processor



Baseband Accumulator Loop with Fast Lead Term

Twelve bit digital words are received from the baseband preprocessor at the symbol rate (72.73MHz). These 12-Bit words are added to an error term that represents DC offset in the discriminator output (which is equivalent to frequency offset in the IF). The "DC restored" value is then accumulated in a digital 12-Bit accumulator, completing the implemenatation of an integrator (which integrates $\phi r'(t)$ to yield $\phi r(t)$). The output of this accumulator represents coherent phase. Therefore, the value output from the accumulator represents 360 degrees of phase quantized to 12-Bits. This accumulator is allowed to rollover modulo 2**12 (which is modulo 2*pi), and thus question number two (2) has been answered. Unbounded accumulation of phase is prevented, and a modulo 2*pi phase detector characteristic is displayed by allowing the phase accumulator to rollover.

If the 12-Bit output of the accumulator represents phase modulo 360 degrees, then the 10 LSB's of the accumulator output represent phase modulo 90 degrees. If the transmitted phase constellation is restricetd to that of 4-ary signalling, then the 10 LSB's out of the accumulator represent directly, in binary two's complement form, the error in hitting a desired phase node on the constellation (error-to-node). To control DC offsets out of the discriminator, this error term is mutiplied by a constant, K1, and "fed" directly into a summing node. This is equivalent to a first order PLL correction, which is why the "Fast Lead Term" phrase was coined (a lead term only, in a PLL, results in a first order PLL). The constant that has been chosen for K1, is 1/4, which is implemented by dropping the 2 LSB's of the error term. Thus, through this DC restore approach, question number four (4) has been answered. That is, DC offsets in the discriminator output will be "tracked" out digitally by a first order control loop. During the tracking phase, (the data portion of a burst) the constellation will be restricted to be modulo 90 degrees every fourth symbol period, at which time the DC restore loop will be allowed to update. this has the effect of an additional 1/4 multiplicative term in the open loop gain. For a first order lcontrol loop, the loop noise equivalent bandwidth is defined as;

$$Bl = K/4 \text{ , where } K = \text{the open loop gain}$$

During tracking, the open loop gain is the symbol rate divided by 16, so that the loop bandwidth, Bl = 1.14 MHz.

Question number one (1) and part of question number five (5) are answered by considering acquisition, during the special preamble. First, the integrator is loaded with zero (0) at t=0. Because this value may not be correct, a preamble has been constructed that consists of 32 consecutive peak frequency deviation symbols (fo's). The DC restore loop is allowed to update every symbol period (providing mamximum loop gain, and thus a wide loop bandwidth) to "track-out" our ignorance of the integrator loading at t=0. This is identical to phase acquisition in a PLL. Since, the loop is allowed to update on every symbol, the loop gain is four times that of the "tracking" loop gain, and thus, Bl = 4.54 MHz.

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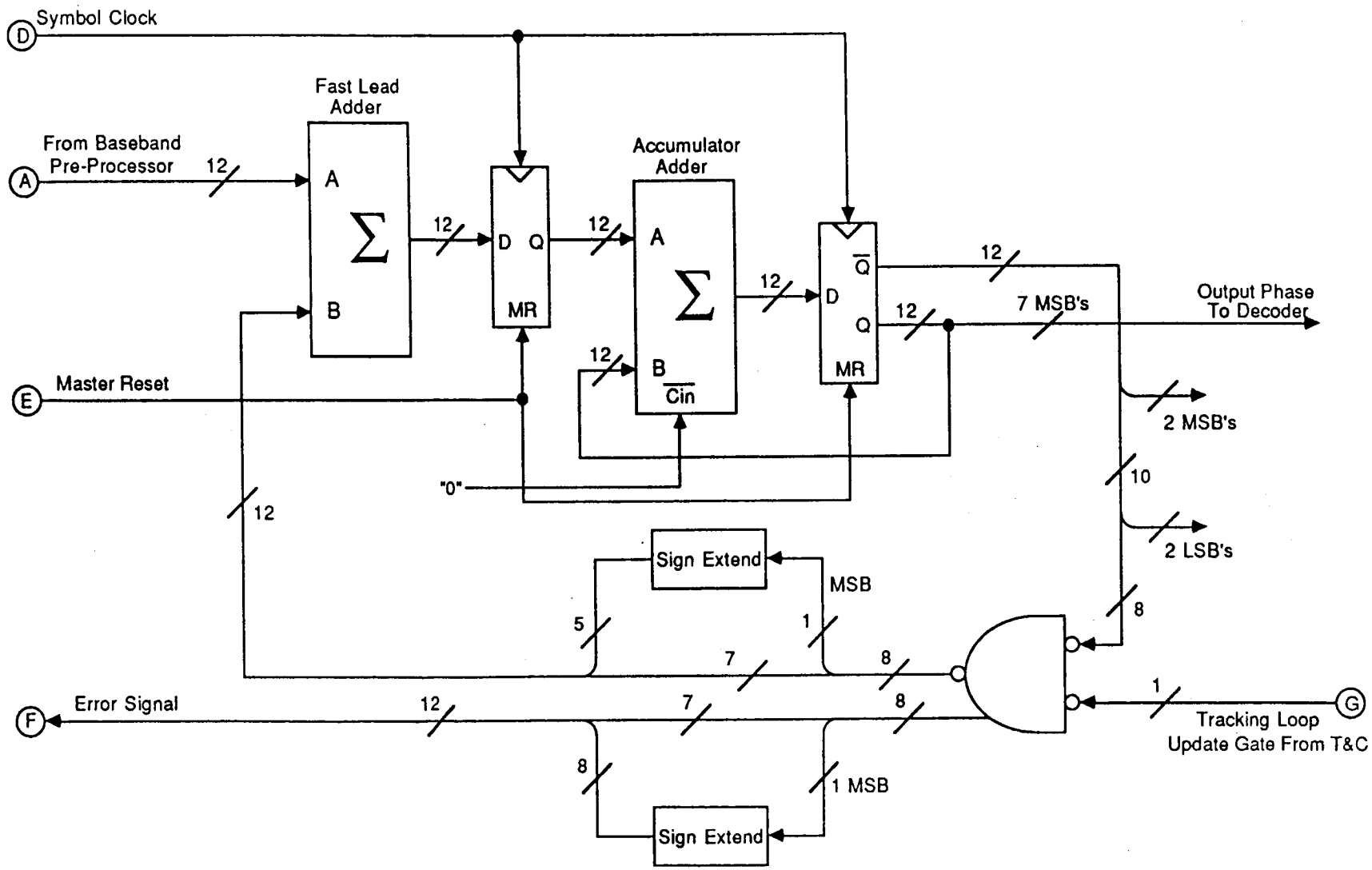
Baseband Accumulator Loop with Fast Lead Term



Baseband AGC Circuit

The baseband AGC circuit receives the 12-Bit error-to-node (12-Bits due to sign extension) signal from the phase accumulator. It cross-correlates this signal with a delayed version of the sampler sign output, to form an error signal proportional to gain misseting (see Task One report, proprietary addendum, for mathematical analysis of AGC error signal generation). The gain error is then accumulated, in a digital accumulator. The resultant output of the accumulator is added to the number one (1), such that the AGC correction factor, $1-.0625 < K < 1+.0625$. This correction factor is used to scale the incoming 8-Bit words, as explained in the section describing the baseband preprocessor. During tracking, which corresponds to the data portion of a burst, the AGC loop is allowed to update on every fourth symbol only, just like the DC restore loop. There is an additional gain factor of 1/4, implemented as a connection gain to the digital multiplier, in the AGC loop. Thus, during tracking, the AGC loop bandwidth, Bl = 284 kHz.

The remaining portion of question five (how is the AGC acquired for independent user bursts) is, again answered by considering AGC acquisition during the special preamble. The AGC loop, like the DC restore loop, is allowed to update every symbol interval during the peak frequency deviation (all fo) portion of the preamble. This increases the open loop gain by a factor of four over that of tracking. Thus, the loop bandwidth of the AGC loop during acquisition is, Bl = 1.14 MHz. It has been shown through computer simulations, that this loop bandwidth is sufficiently wide enough to acquire 4%, or less, of gain error within the 32 symbols of the preamble.

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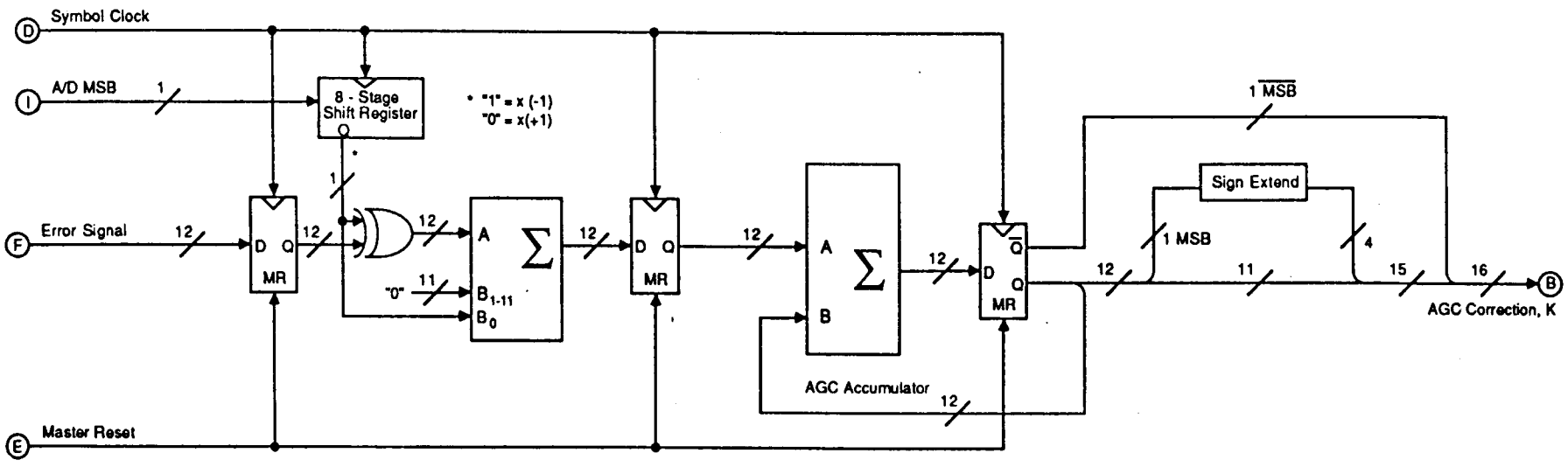
Baseband AGC Loop



Baseband Timing and Control

The baseband timing and control circuit is responsible for providing the necessary control signals to the remainder of the baseband phase detector circuitry. During a burst, the timing and control circuit receives stimuli and generates specific control signals based on the stimulus it receives, as well as what state the sequencer is in. The first external stimulus to the control circuit will be a power-up reset pulse, which will force several registers to known states, force Master Reset "high", and set the BDQ signal "high". After an initial power-up reset, the functions described above are initiated by an End-of Burst, EOB, pulse. The next external stimulus will be a Burst Detect pulse sent from the symbol synchronizer. This will initiate checking for the all fo's portion of the preamble. Once this has been detected in four consecutive registers, the burst counter is preset to a specific state (depending on the burst length), and the Master Reset line is forced "low", which allows the remaining registers in the phase detector circuitry to update on the symbol clock. The next main event that should occur is, detection of the unique word. If a unique word is not detected 64 symbol times after a Burst Detect occurs, then an EOB is automatically generated. Upon the detection of the unique word, the burst counter (12-Bits) is enabled to start counting. A gating signal, that allows the DC Restore, and the AGC loop to update every fourth symbol is generated by decoding repeating states of the burst counter. When the burst counter reaches the terminal count, an EOB pulse is generated which re-initializes the phase detector circuitry. Further action is dependent upon receiving a Burst Detect pulse.

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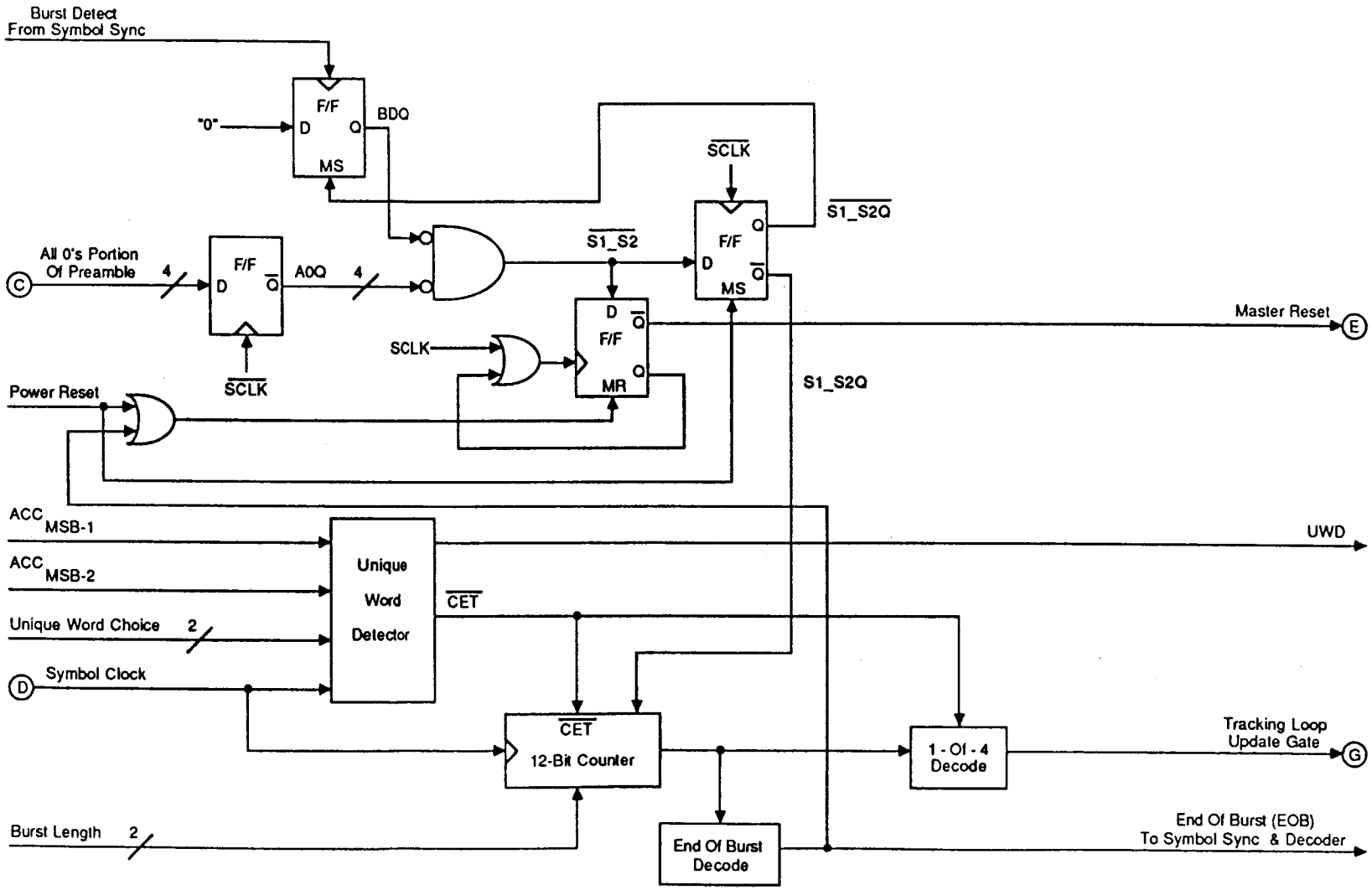
Baseband Timing And Control



SAMPLER CARD: Ref Figure #9

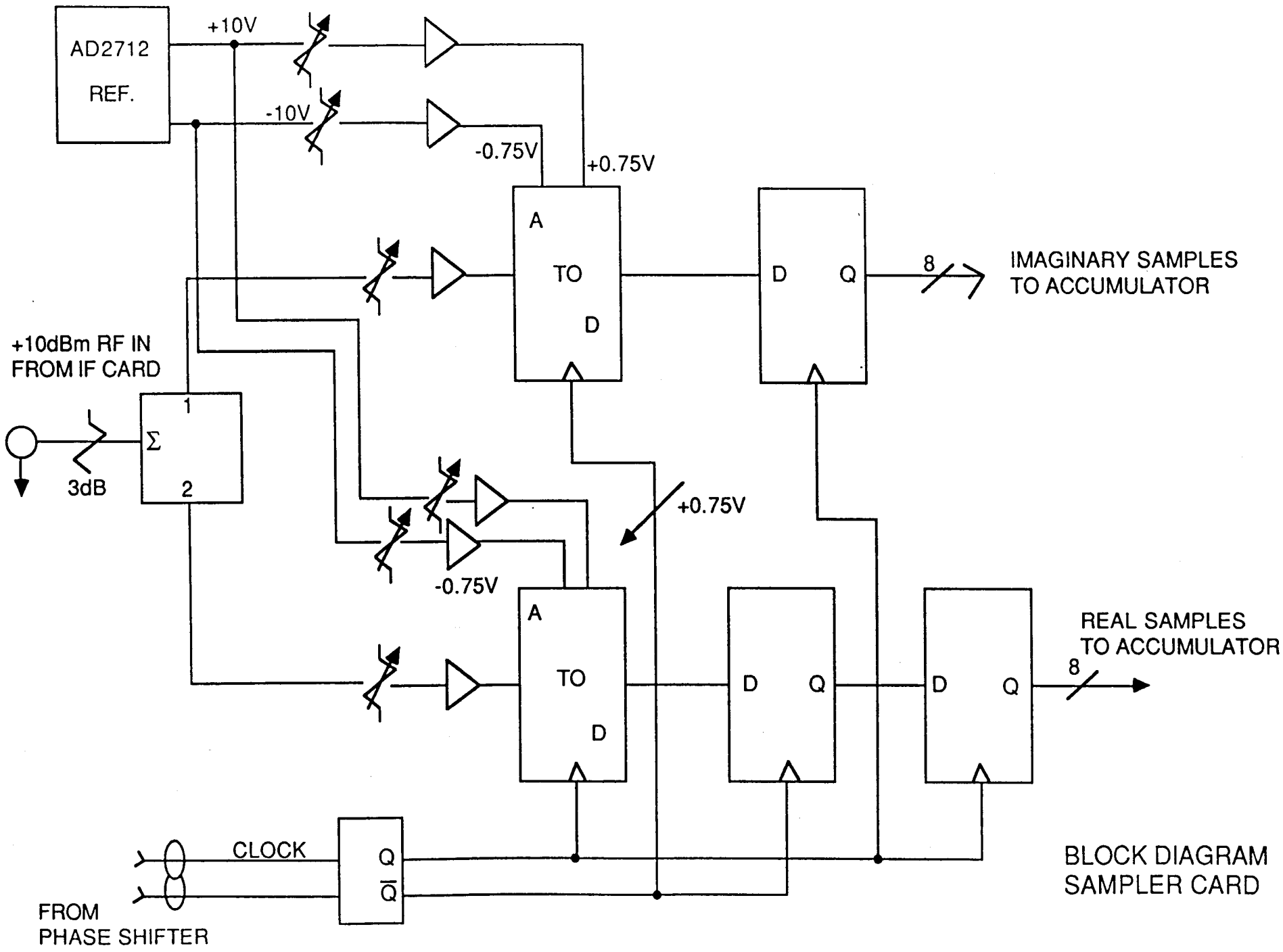
The Sampler Card generates the Real and Imaginary Samples used by the TDMA Demod. These samples are generated by two samplers, sampling the discriminator output from the RF card. Samples are taken on the rising and falling edge of the Symbol Rate Clock. The samples taken on the rising edge are called Real and the falling edge are called Imaginary.

A +10 dBm discriminator output is received through a 50 Ω transmission line. This signal is power split to the two A to D converters. The amplitude of these signals can trimmed ± 1 db. The sample time of each sampler can be shifted by a trim put on the reference of the comparator generating the clock signal.

A ±0.75 Volt reference is generated for both A to D's using a percision bipolar reference and a resistor divider. These signals can be independently trimmed ±4.0 millivolts.

The A to D outputs are latched providing sixteen differential signals, eight Real and eight Imaginary. The A to D outputs are latched using the inverted version of it's respective sample clock. The Real samples are latched one more time aligning all samples with the rising edge of the symbol rate clock. The samples are the sent off card to the Accumulator card.

FIGURE #9



BLOCK DIAGRAM
SAMPLER CARD

SYMBOL TIMING FUNCTIONAL DISCUSSION: Ref Figure #1

The Symbol Timing Recovery Circuits are contained on two cards. The Accumulator Card Assy # 460905-G01 and the Phase Shifter Card Assy #460910-G01. The accumulator card generates all error signals and the phase shifter card uses these signals to correct phase. These two cards are shown in Figure #1.

Eight bit Real and Imaginary signals are sent to the Accumulator Card from the Sampler Assy, #460900-G01. These samples are immediately stored in RAM. The incoming samples are also multiplied by plus or minus one and added to delayed samples stored in RAM. The delayed samples are also multiplied by plus and minus one. The multiplier for both signals is based on the mode of operation and is controlled by the timing and control circuits.

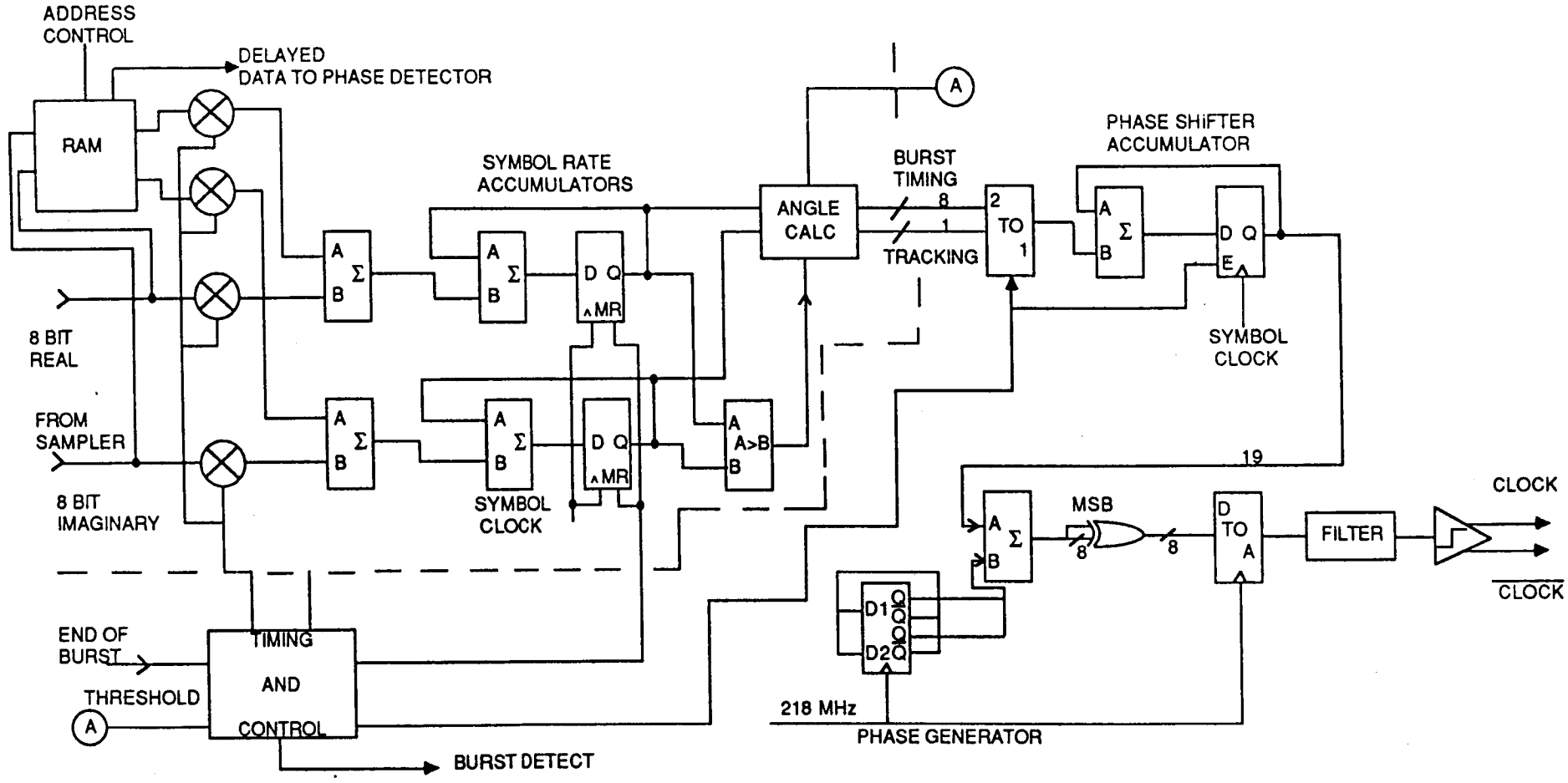
The result of these adds is then accumulated in two accumulators at the symbol rate. The values in these accumulators is monitored by the angle calculator circuits and by a digital comparator. Both of the monitoring circuits are fed off card to the phase shifter card.

The phase shifter card receives these signals through a two-to-one Mux. The select line of the Mux is controlled by the timing and control circuits. The output of the Mux then feeds an accumulator. This accumulator is also controlled by the timing and control circuits. If the signal selected by the Mux is from angle calculation circuits, the phase shifter accumulator is allowed to accumulate over sixteen initial symbol times. If the signal selected by the Mux comes from the comparator, the Phase Shifter Accumulator is allowed to accumulate once.

The output of the Phase Shift Accumulator is then added to the phase generator output to create a phase shifted binary signal. The phase generator generates binary phase at a 218 MHz rate. The add result is mapped from a binary phase to a binary amplitude and converted to an analog signal. The analog signal is filtered and a clock is generated using a comparator.

All card I.O. is sent and received using differential drivers and receivers. All logic is done using 100K ECL circuits. The timing and control circuits are controlled by the signals End Of Burst and Threshold. The data is delayed to Phase Detector Card so that the Signal Burst Detect generated by the timing circuits is coincident to the thirty-two F0's portion of the preamble.

FIGURE #1



BLOCK DIAGRAM SYMBOL TIMING RECOVERY

MULTIPLY AND STORE: Ref Figure #2

The eight bit Real and Imaginary samples are received by the accumulator through differential line receivers. The signals are immediately latched by the RAM Read Write Register File and a separate set of latches. The real Q data is also fed to a digital comparator. This comparator is used to control the multipliers during tracking. The signal Delay-32. Cont is used to control signals to the multipliers and the read address of the C port of the RAM. The RAM is a five port LSI device. This design uses one write port and two read ports. The D read port delays data to the Phase Detector Card. This delay aligns the burst detect signal, generated by the symbol tracking circuits with the start of the F0 portion of the preamble.

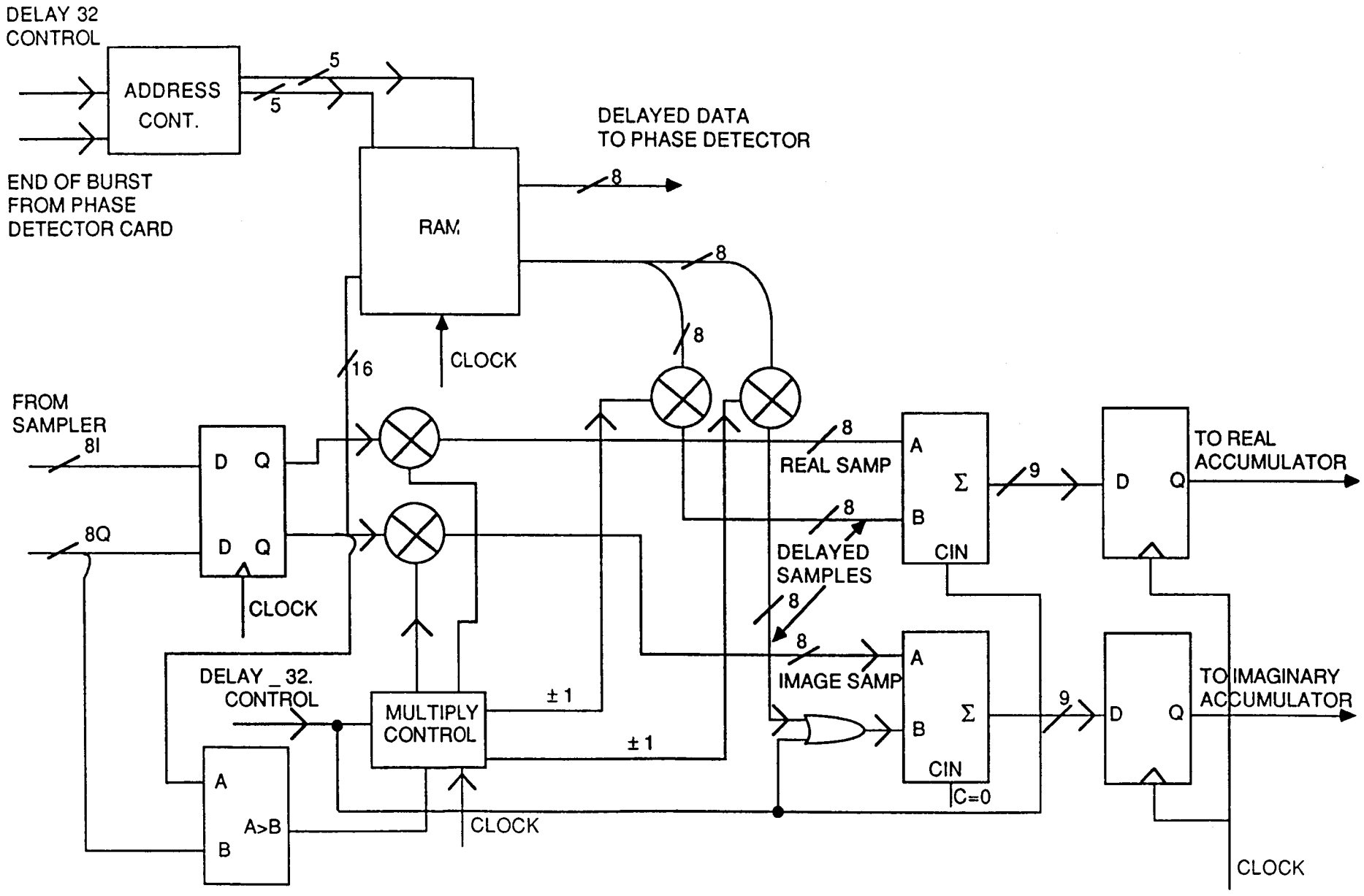
The signal End Of Burst sets the write address of the RAM to zero and zero's it's C port. Delay-32. Cont is forced low by the phase shifter card, causing the read address to write address minus 32. The adders are now adding zero to the incoming samples. Thirty-two symbol times later the RAM output is enabled and the adders begin subtracting. The B inputs to the adders is the minus of the A input thirty-two symbol times earlier. This creates the 32 sample sliding average.

In the correlation mode the multiply control circuitry generates an alternating plus minus one pattern. This causes the alternating F0, F15 portion of the preamble to look like a constant tone to both the real and imaginary accumulators and results in the integration of a constant. When a threshold is reached the Phase Shifter Card forces Delay-32.Cont high.

Delay-32. Cont going high configures the multipliers for tracking. The read address is now the write address, minus one. Control of the multipliers is transferred to the comparator and the delayed imaginary sample is zero'ed. The comparator is monitoring two adjacent real samples to determine the direction of the symbol transition. All samples are then multiplied by this value. This removes the effects of transition direction on the error signal, see tracking error analysis in Symbol Timing Design Review Package. The real adders are now adding two adjacent samples. These samples have been multiplied by plus or minus one depending on which one is greater. These samples will be averaged by the real accumulator to generate and estimate of the true zero crossing. The imaginary samples are the zero crossings. These samples are multiplied by the comparator value associated with it's two adjacent real samples. The imaginary accumulator averages these values to generate the measured zero crossing. A comparison of these two values results in the tracking error signal.

FIGURE #2

BLOCK DIAGRAM MULTIPLY AND STORE

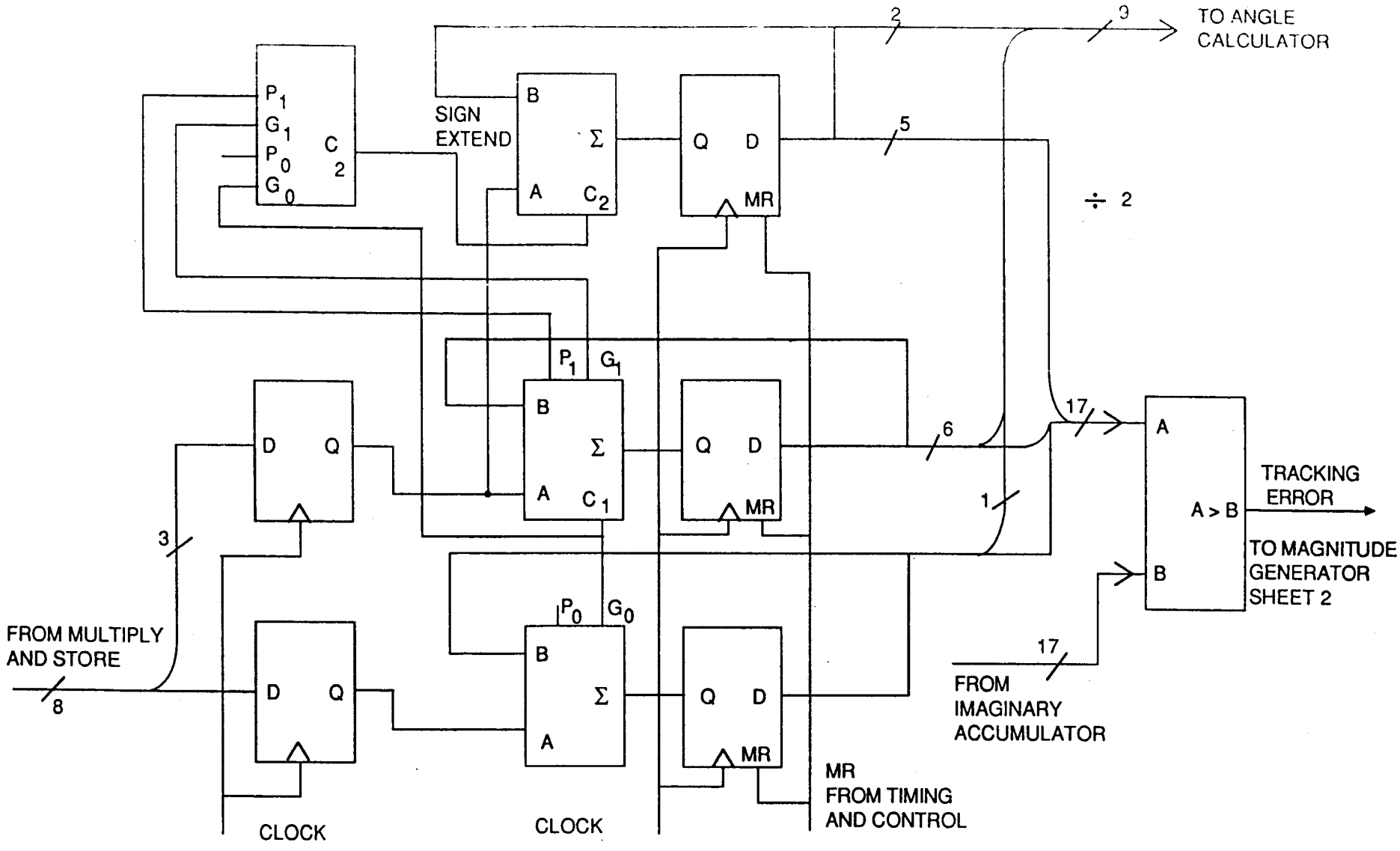


ACCUMULATOR: Ref Figure #3

The Real and Imaginary accumulators are identical. Data is clocked into the accumulators from the multipliers. Three six bit adders and three six bit latches are used to make one eighteen bit accumulator. The accumulators are clocked at symbol rate, a master reset line is used to clear the accumulators. This line is controlled by the timing and control circuitry on the phase detector card.

The outputs from these accumulators is continuously monitored by the tracking error comparators and the angle calculator circuits. The timing and control circuits of the Phase Detector Card determines which signal is used. There is a hard wired divide by two in the real accumulator signals to the tracking error comparator. This accommodates the divide by two required for the zero crossing estimate. See Tracking Error Analysis in Symbol Timing Design Review Package.

FIGURE #3



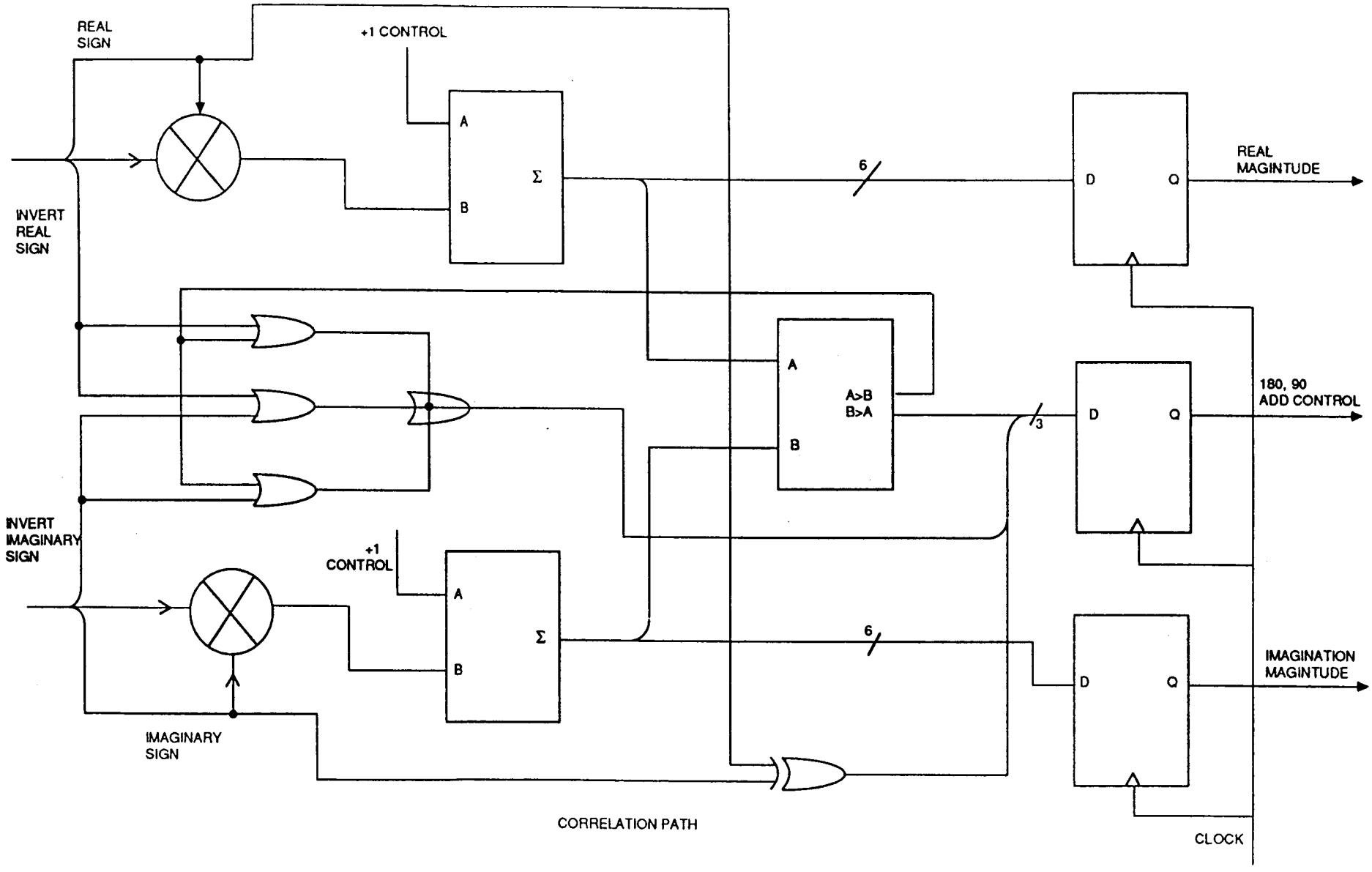
BLOCK DIAGRAM
ACCUMULATOR

MAGNITUDE GENERATOR: Ref Figure #4, 5

The Magnitude Generator circuits perform two functions. They generate three bits of octant information and convert the real and imaginary accumulator values to six bits of magnitude (straight binary). There is a hard wired divide by thirty-two on signals coming from the accumulators. These two functions are used to generate the angle sent to the phase detector as burst timing error.

The magnitude signals are generated by EX-OR'ing the accumulator values with their sign bit and adding one for a negative sign. The resulting seven bit number is rounded by adding the seventh bit to the sixth and latched. The rounding and adding of one, can be accommodated by one adder. The three octant bits are generated from the two sign bits and the comparator signal $|A| > |B|$ (see Angle Calculation Analysis Symbol Timing Design Review Package). These fifteen bits, 6 bits Real Mag, 6 bits Image Mag and 3 bits Octant are then latched. The signals then proceed to the angle calculation circuits.

FIGURE #4



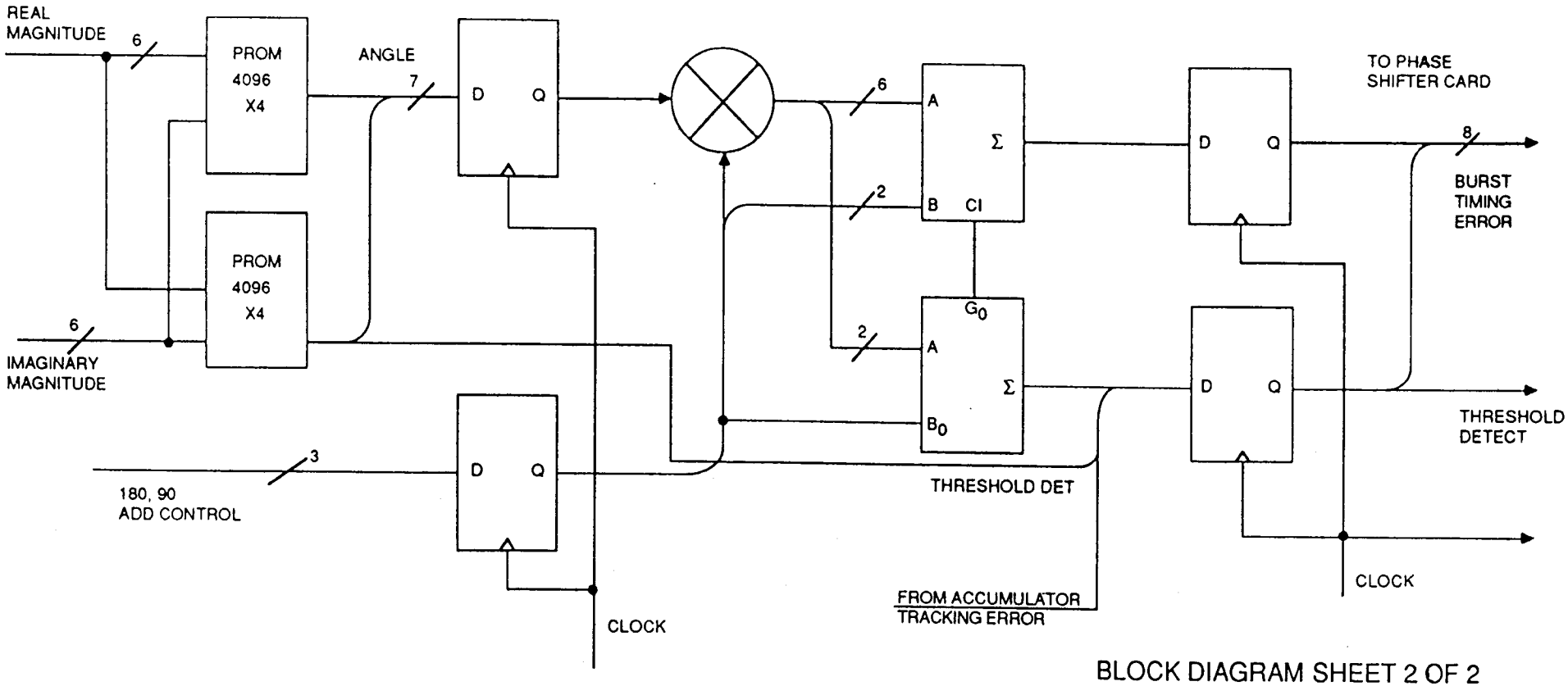
BLOCK DIAGRAM SHEET 1 OF 2
MAGINTUDE GENERATOR

ANGLE CALCULATION: Ref Figure #5

The Angle Calculation circuits use the signals real magnitude,imaginary magnitude, and octant to calculate the burst timing error and the signal threshold. Threshold is used to indicate a valid burst timing measurement.

The two magnitude signals are clocked into two 4096-bit PROM'S. The output of these PROM'S is seven bits phase and one bit threshold. The seven phase bits represents an angle between 0 and 45 degrees. The one threshold bit indicates $(\text{REAL MAG})^2 + (\text{IMAG.MAG})^2$ is above some threshold. The seven phase bits are then combined with the three octant bits using adders and ex-ors to generate ten bits of phase. A hard wired X2 on the output of the angle generator results in the final nine bits of phase. The signal threshold bypasses the PROM latches and goes directly to the output latches. This is done to accomodate a delay on the Phase Shifter Card. The tracking error signal is shown coming from the accumulator section to the output latches also. All signals to the Phase Shifter Card are sent diffential.

FIGURE #5



BLOCK DIAGRAM SHEET 2 OF 2
MAGNITUDE GENERATOR

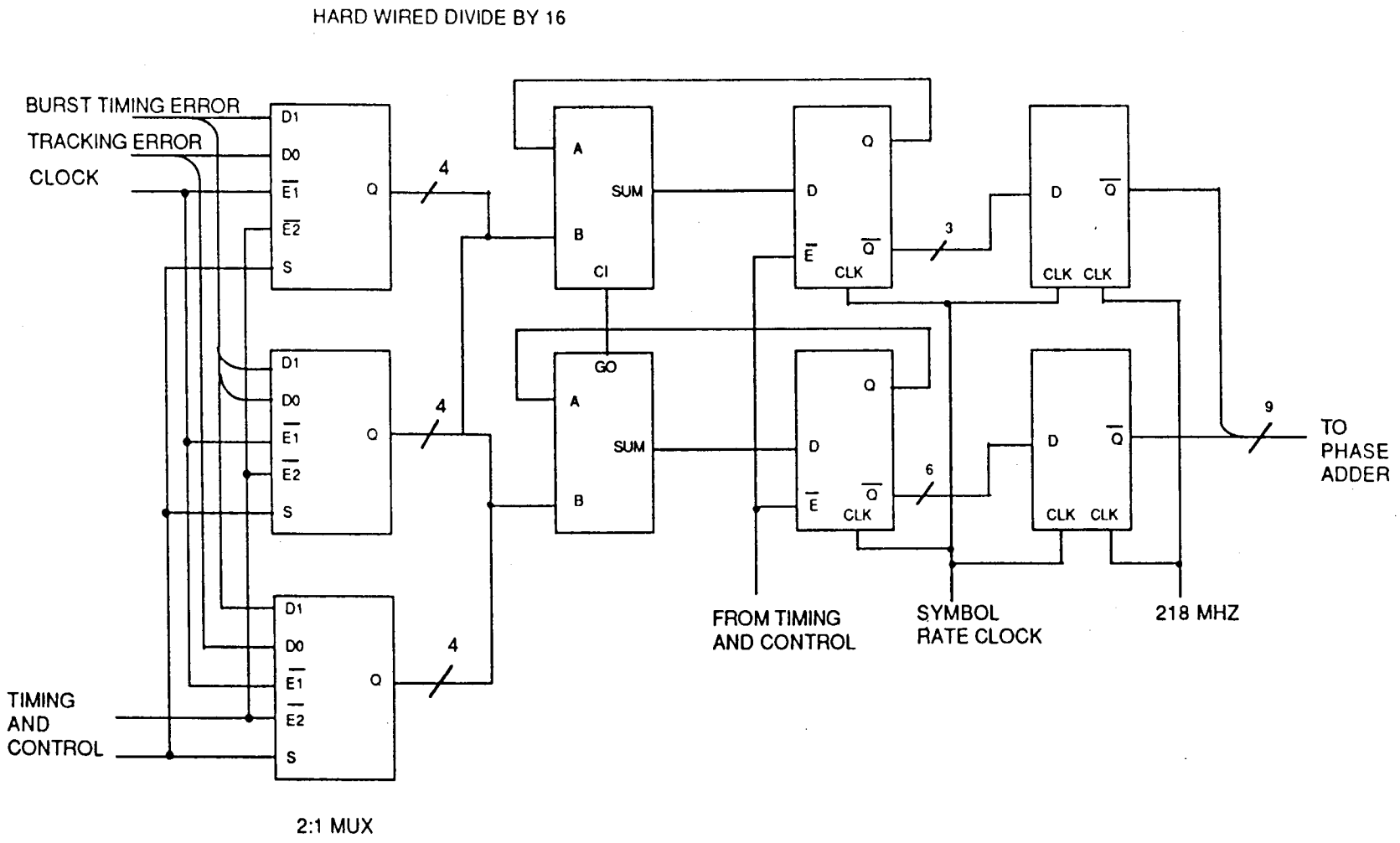
PHASE ACCUMULATOR: Ref Figure #6

The signals Burst Timing Error and Tracking Error are received using differential line receivers. These receivers drive the two-to-one Muxes of the Phase Accumulator. The timing and control circuits have configured the Muxes to select one of the two error signals. The accumulator is allowed to roll over through 2π.

When configured for correlation the Timing and Control circuits generate a pulse to the two-to-one Muxes one clock pulse after the threshold signal goes high. This strobes data into the accumulator. The burst timing error is divided by sixteen using a hard wire divide. One clock cycle after data is strobed into the accumulator the output latches are enabled. The latches remain enabled for sixteen counts. This compensates for the divide by sixteen and distributes the burst error correction over the next sixteen symbol times. This correction is distributed over the 32 F0's portion of the preamble.

After the burst timing correction has been made, the timing and control circuits select the tracking error signal as the Mux inputs. This signal is sampled once every 1025 symbol times by the Phase Accumulator Muxes. One clock pulse after the accumulator latches are enabled. This time the latch enable's remain low for one clock cycle only. The Muxes will continue to sample the Tracking Error Signal until the timing and control circuits receive and End Of Burst signal from the Phase Detector Card.

The remaining circuits on the Phase Detector Card are being clocked with a 218.18 MHz local clock. The final latches shown are used to strobe the Phase Accumulator output into the Phase Adder.

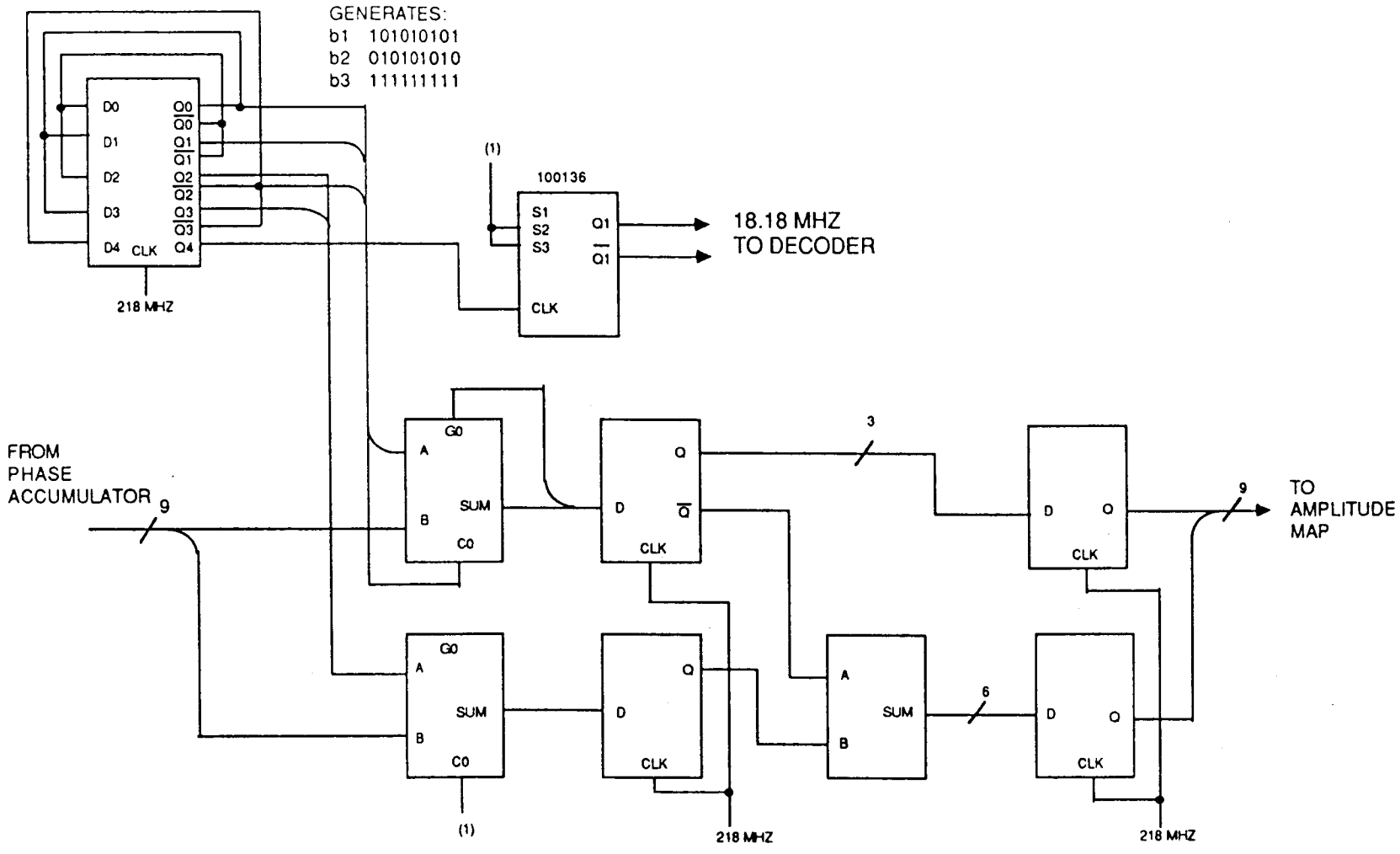


PHASE ACCUMULATOR
BIT SYNCHRONIZER

PHASE ADDER: Ref Figure #7

The Phase Adder adds the Phase Accumulator to the Phase Generator. Nine bits of the Phase Accumulator are added to nine bits of the Phase Generator. The Phase Generator generates three phases of a 72.73 MHz signal. The three phases are 0°, 120° and 240°. These phases are represented by the binary numbers 000···, 010101···, and 101010···. These numbers are generated by a latch clocking at 218.18 MHz.

The result of this addition results in three phases of a 72.73 MHz signal phase shifted by the phase accumulator value. The add is broken into two six bit adds and takes two 218.18 MHz clock cycles to complete, the throughput rate remains 218.18 MHz as the adds are pipelined. The resulting binary phases are latched. These digital words are phase amplitudes of the generated clock signal.

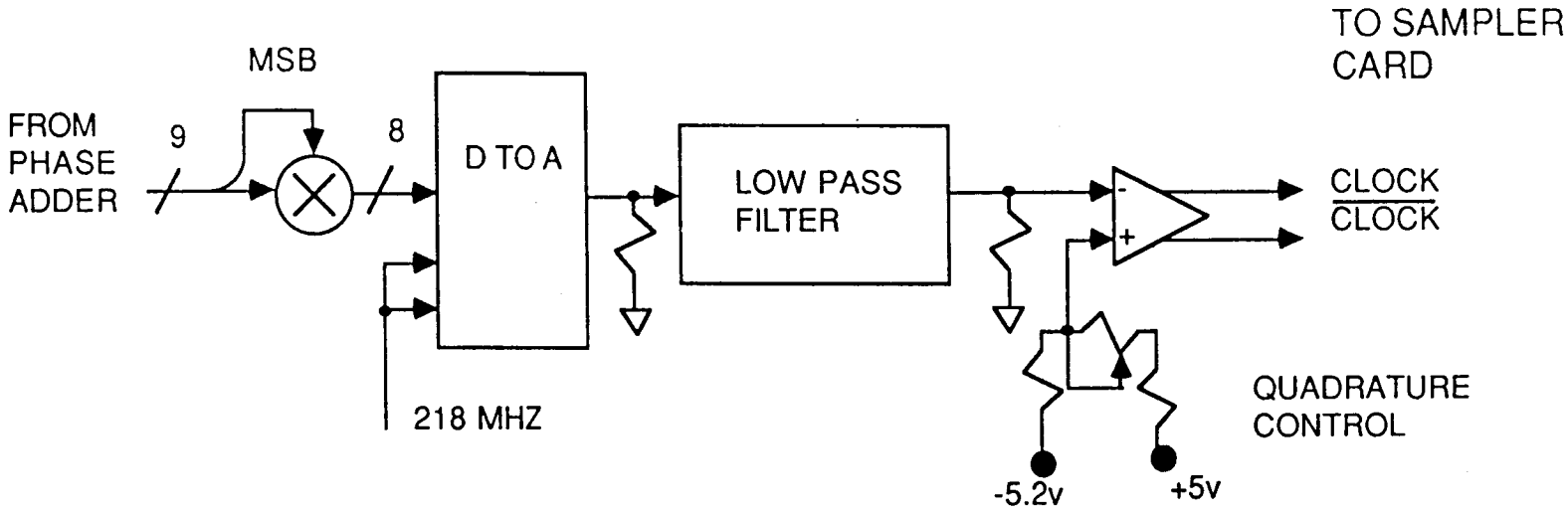


PHASE ADDER
BIT SYNCHRONIZER

AMPLITUDE MAP: Ref Figure #8

The Amplitude Map circuits take the binary phase generated by the phase adder circuits and map it into a sampled waveform. The simplest waveform mapping is from Linear Phase to a traingle. The triangle is generated by multiplying the MSB of the phase signal with remaining nine bits. This is done with EX-OR's.

The result is then D to A converted with a video D to A converter and filtered. The filter selects the 72.73 MHz component and a comparator converts it to a clock. An offset trim is used on the comparator to guarantee a 50% duty cycle. The clock signal is sent to the sampler card.



PHASE TO AMPLITUDE MAP
BIT SYNCHRONIZER

Decoder Block Diagram

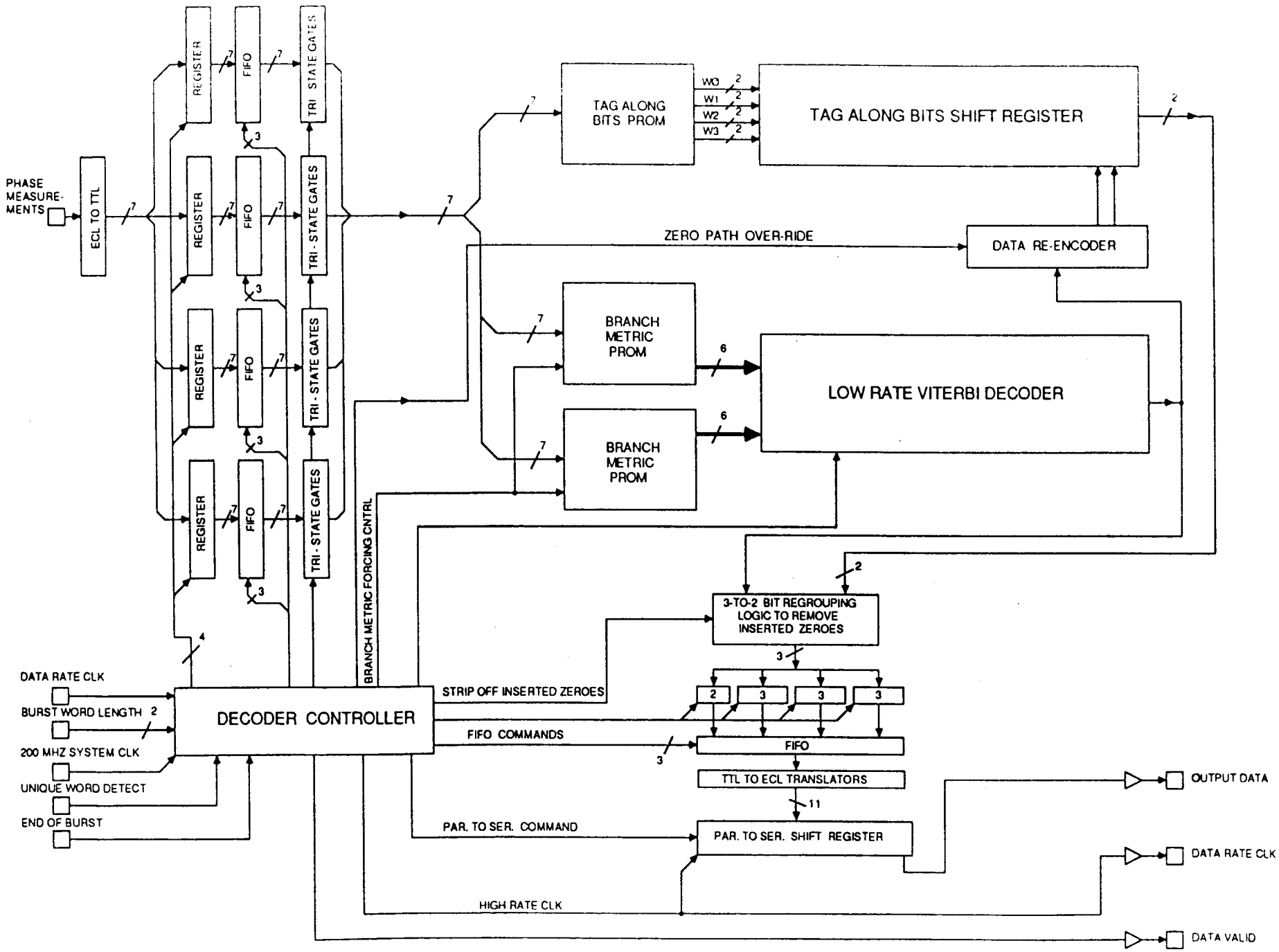
The decoder circuitry receives 7-bit phase measurements at a 72.73 Mhz rate from the demodulator accumulator and stores these in FIFO data buffers. This implementation has the capability to receive, buffer, decode and distribute up to three bursts containing up to 3740 bits of data per burst within a frame. Alternately one burst of 11258 bits of data could be received within a frame.

A *unique word detect detect* (UWD) signal to the decoder indicates the begining of valid data and initiates the storing of the 7-bit phase measurements. The length of the data burst into the input data buffer is defined by the length from the UWD signal to the *end of burst* (EOB) signal. Once data is buffered in the input FIFO, the FIFO data is then read out and sent to processing PROMs. The two unencoded MSB bits are processed by the "tag-along bits" PROM. These tag-along bits are then sent through a FIFO that matches the delay of the Viterbi decoder.

The Viterbi decoder receives the R=1/2 encoded data from the LSBs of the modulated symbol through the action of the branch metric PROMs processing the buffered 7-bit phase data. Decoded data LSB bits out of the Viterbi decoder are re-encoded to now produce an error-corrected version of the convolutionally encoded bits. These error-corrected bits are then used to select the correct MSB (tag-along) bits and are grouped with the decoded data bit out of the Viterbi decoder to form the 3-bit symbol groups.

The Viterbi decoder processing is paused every fourth symbol to account for the forced 00 LSB bits inserted by the encoder / modulator. In addition, the action of re-grouping the final 16 bits (due to 000000 termination of the encoder) is also performed.

These recovered symbols are then stored in an output data buffer (another FIFO). Once the buffer is full, the stored data is read out and translated in speed so as to present a 200 Mbps data stream to the output.



DECODER BLOCK DIAGRAM NOV. 20, 1986

1. UNIQUE WORD DETECT SIGNALS BEGINING OF VALID 200 Mbps DATA TO DEMOD / DECODER

2. EOB COMMAND SIGNALS THE END OF VALID DATA TO THE DEMOD / DECODER

3. INPUT DATA BURSTED TO DEMOD / DECODER AT 200 Mbps. SHORT BURST = 170 BITS. MEDIUM BURST = 3734, LONG BURST = 11258 BITS. INPUT DATA IS STORED IN FIFO BUFFER REGISTERS.

4. AT COMPLETION OF INPUT DATA BURST, FIFO DATA IS READ AND SENT TO TAG-ALONG BITS PROM AND BRANCH METRIC PROMS. CALCULATED TAG-ALONG BITS ARE STORED IN ANOTHER FIFO REGISTER. BRANCH METRICS ARE SENT TO VITERBI DECODER.

5. EVERY 4TH SYMBOL INPUT TO VITERBI DECODER (AND EVERY 4TH BIT DECODED BY VITERBI DECODER) IS PAUSED ONE SYMBOL TIME TO COMPENSATE FOR THE ACTION OF THE ENCODER.

6. DECODED DATA BITS BECOME VALID AT THE OUTPUT OF THE VITERBI DECODER AFTER A FULL TRACEBACK NUMBER OF BIT TIMES HAS OCCURED.

7. AT THE END OF VALID DATA INTO THE VITERBI DECODER, THE ENCODER STATE HAS BEEN FORCED TO 000000. THE INPUT (BRANCH METRICS) TO THE VITERBI DECODER ARE NOW BIASED TOWARD THE ZERO STATE (SEE BLOCK DIAGRAM DESCRIPTION). THIS ALSO PROVIDES INPUT DATA AND CLOCK WITH WHICH TO TRACEBACK THROUGH AND OUTPUT THE FINAL VALID DECODED DATA BITS.

8. TOWARDS THE END OF VALID DATA , THE SIX ZEROES INSERTED INTO THE ENCODER WILL APPEAR AT THE OUTPUT OF THE VITERBI DECODER. THESE ZEROES ARE NOT VALID DATA AND ARE REMOVED.

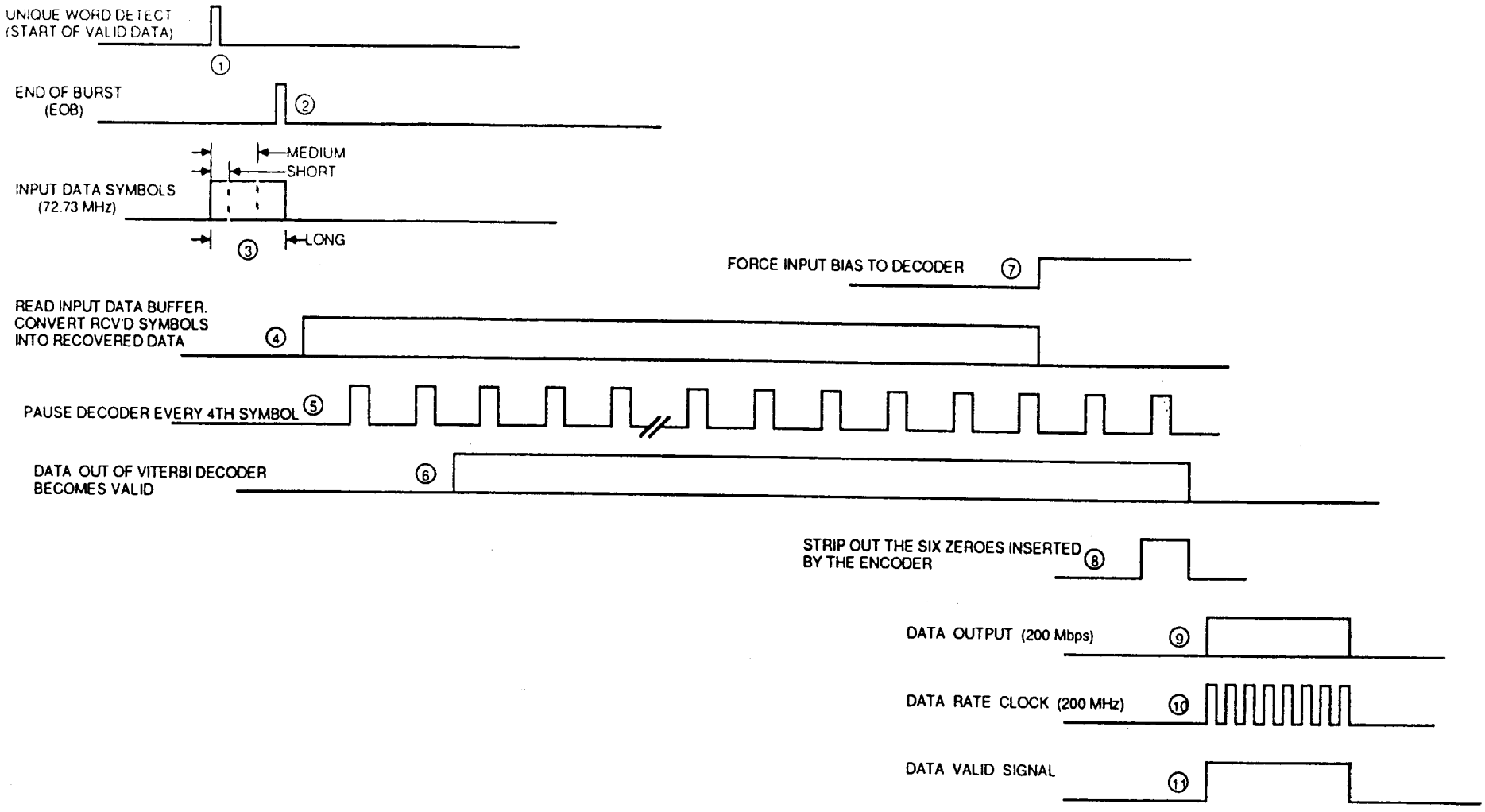
9. RECOVERED OUTPUT DATA HAS BEEN WRITTEN TO AN OUTPUT FIFO BUFFER. ONCE ALL VALID RECOVERED DATA IS IN THE FIFO, IT CAN THEN BE READ OUT, PARALLEL TO SERIAL CONVERTED, AND SENT OUT TO THE "DATA SINK."

10. A BIT RATE CLOCK (200 MHz) IS SENT OUT ALONG WITH THE RECOVERED / DECODED DATA.

11. A DATA VALID SIGNAL IS ALSO SENT OUT WHICH INDICATES THE BEGINING AND END OF VALID DATA IN THE OUTPUT BURST.

DECODER SEQUENCE OF EVENTS DESCRIPTION

TDMA DECODER SEQUENCE OF EVENTS



TDMA SIGNAL COMBINER DIGITAL INTERFACE TEST CONFIGURATION

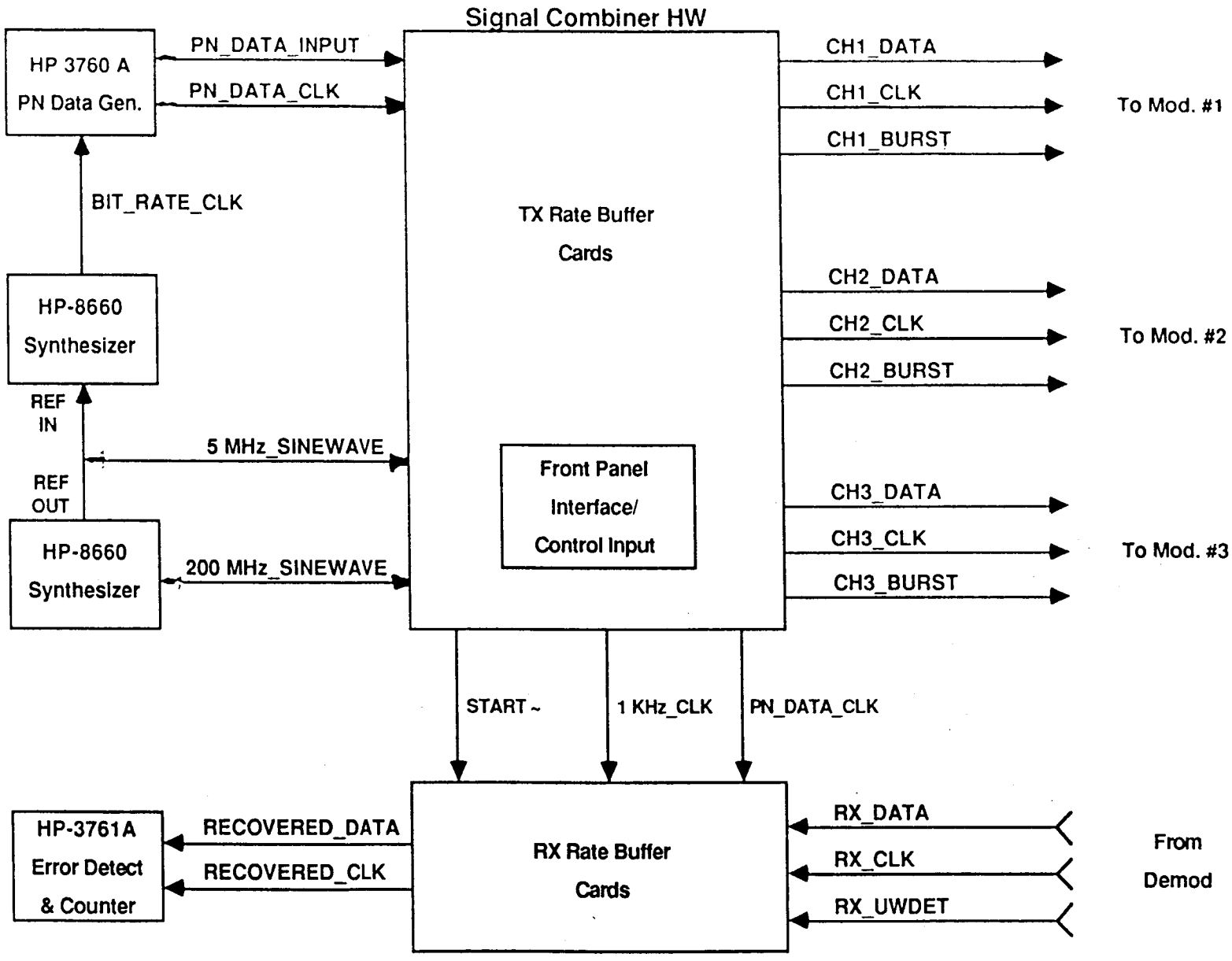
The function of the Tx Rate Buffer is to convert a serial low rate data stream into a high rate 200 Mbps bursted serial stream. The 200 Mbps data, along with the 200 Mbps clock, to which the data is rising edge aligned is supplied to the Modulator for bursting to the demodulator over the simulated channel. The 200 Mbps data with clock is accompanied by a burst command, which controls the bursting of the high rate data.

The Tx buffer receives serial data and clock from external test equipment, which is referenced to a 5 Mhz and 200 Mhz sine wave sources, which it also uses. The buffer stores this data in a 16-bit word format in preparation for the data to be bursted upon command.

The Tx buffer stores 1 msec of data every frame. A frame is defined as 1 msec time span. There are three data rates, 11.258 Mbps, 3.734 Mbps, and 0.170 Mbps. Data storage is accomplished for all test modes with the data rates given, except in the Test 2 case. In order to meet the Test 2 requirements, the data rate must be set to 3 times the normal rate.

Five different tests are selectable from the format panel. There are two main groups, defined by the number of bursts per frame (BPF). Test 2 requires 3 BPF while the other tests require 1 BPF in varying combinations of sequence length and number of modulators.

The Rx rate buffer receives bursted data from the demodulator. The rising edge of the unique word detect signal indicates data is present, the falling edge indicates data is over. the Rx buffer stores the data in a FIFO. The output of the FIFO is a serial data stream to the error detector. The transmit data clock is used to clock the data out. Signals from the Tx rate buffer are used to detect missed bursts.

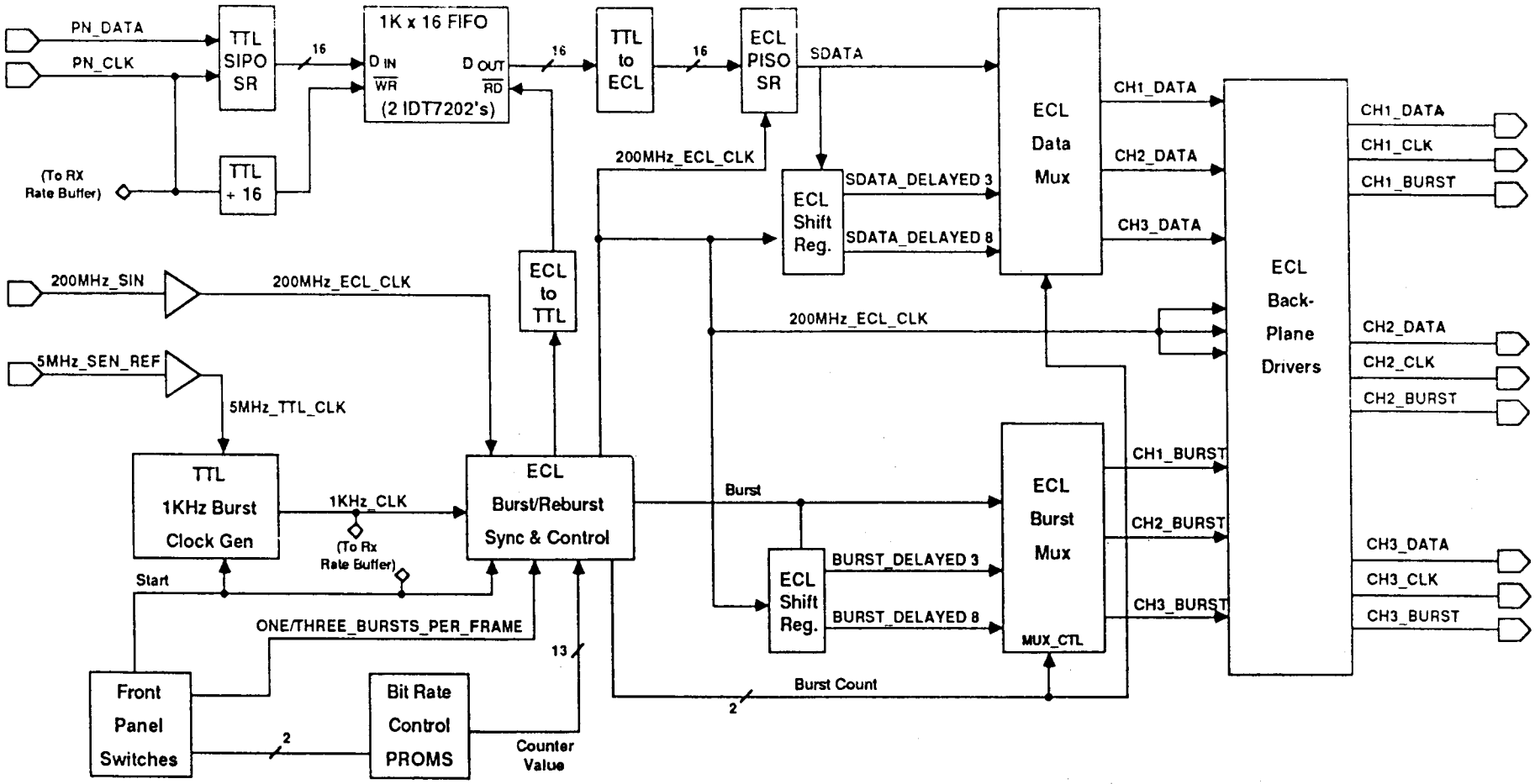


TDMA Signal Combiner Test Configuration

RC.1(3)
1-21-87

SIGNAL COMBINER Tx RATE BUFFER BLOCK DIAGRAM

This circuit accepts serial data and clock from an external data generator. It separates the data into 16 bit words, and loads the words into a 1kx16 FIFO. This FIFO is large enough to hold the longest burst (11258 bits) without overflowing. When the correct number of bits are in the FIFO, selected by the front panel, it is emptied at 200/16 MHz. Data is then parallel to serial converted, and sent to the modulators at the burst rate, 200 Mbps. The 200 MHz and 5 MHz clocks are phase aligned external to the Signal Combiner. The 5 MHz reference clock is counted down to determine the frame timing, in 1 msec increments. The 200 MHz clock is used to count the number of bits to be transmitted in a particular burst, selected by front panel control. Burst are sent either one or three bursts per frame. In the one burst per frame mode a 11258 bit or 170 bit burst may be selected. In the three bursts per frame mode, the bursts are sent to independent modulators with each modulator receiveing 3734 bits. Provision is also provided for sending delayed burst data to independent modulators, when testing adjacent channel performance. The circuit is enabled when the front panel start button is pushed, and the test continues until the reset button is pushed.



TX Rate Buffer Block Diagram

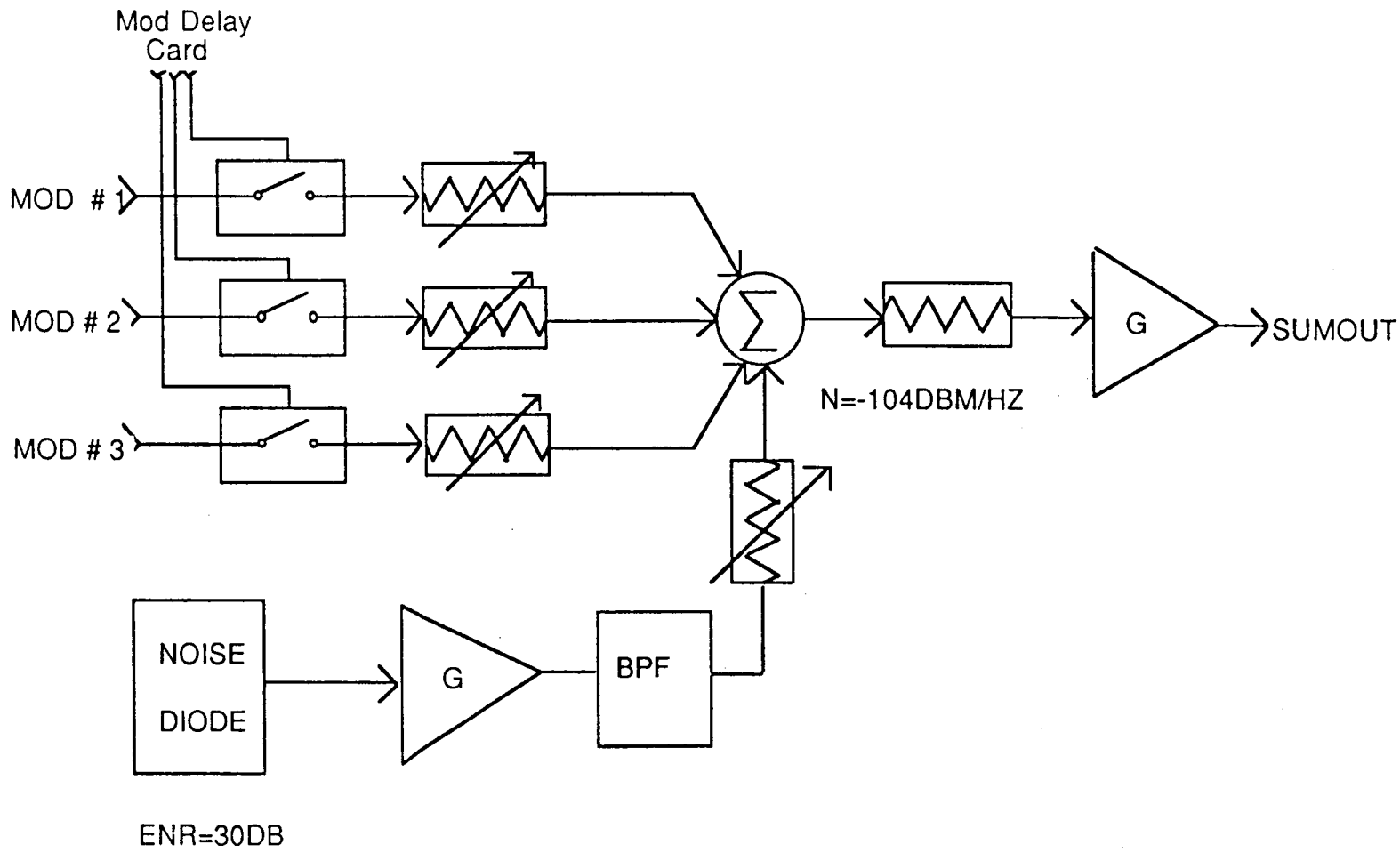
RC 1-4)
1-21-87

SIGNAL COMBINER RF BLOCK DIAGRAM

The RF circuits accept three modulated carriers, combines them, and adds noise to them. There are also amplitude controls on all signals. Each modulator's signal power is at about 0 dBm when they enter the combiner. They are then sent through a fast RF switch (Amer. Microwave SW-2183). This is the TDMA switch. We had Amer. Microwave characterized the switch for us, and the phase transients die out to an acceptable level in about 20 nsecs. The signals are then passed through attenuators to set up particular test conditions. The three signals are then added to wideband noise. The noise is generated with a noise diode with excess noise ratio of 30 dB. The noise power is then amplified (Avantek amplifiers are used) and bandpass filtered. The filter is required to set a known noise power level in the system. The noise bandwidth of the filter is 500 MHz centered at 3.373 GHz. An attenuator on the noise is used to set different Eb/N0 levels. The summed signal is then amplified to 0 dBm, and sent out of the unit.

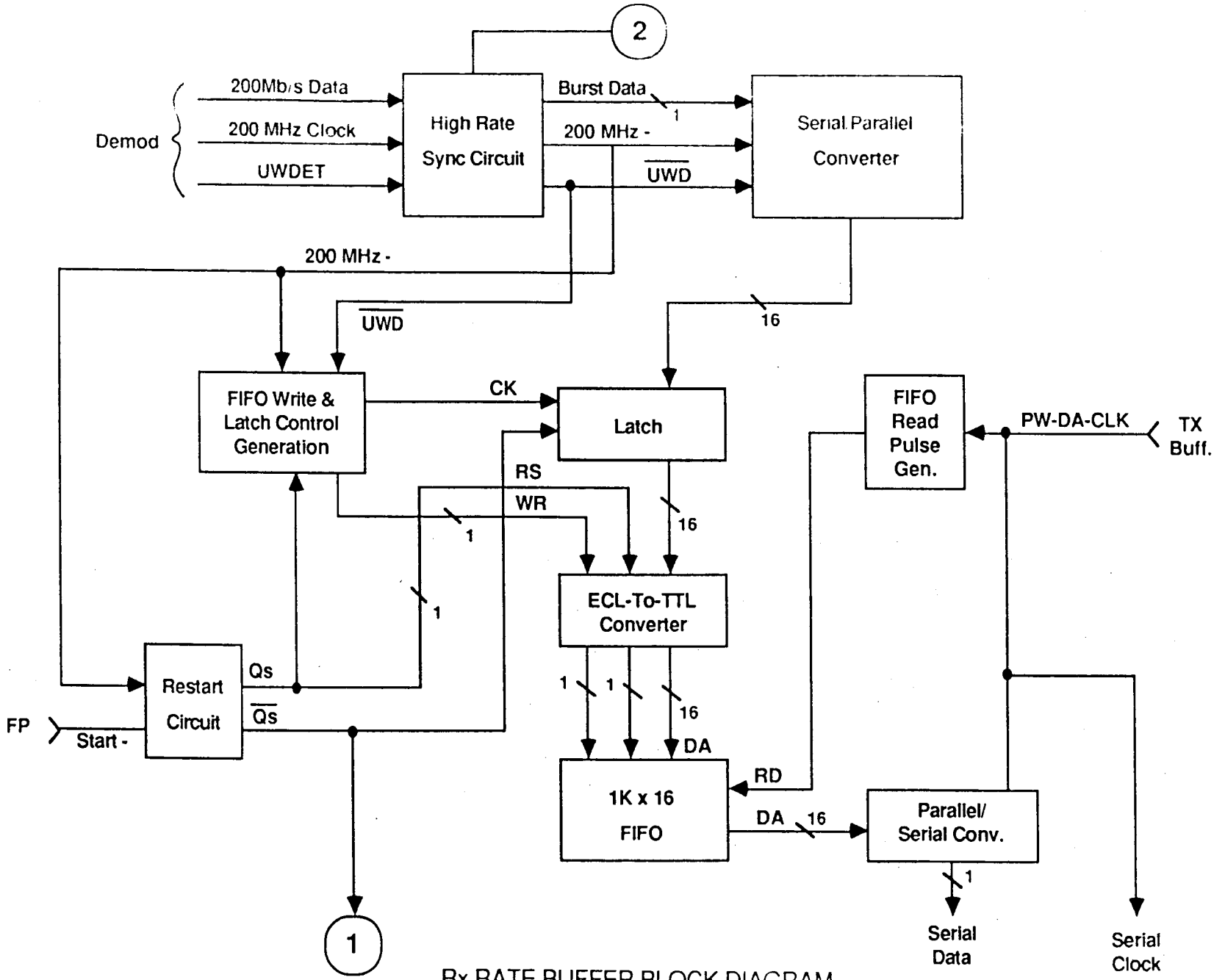
HARRIS
Government Communication Systems Division
Modem Engineering Section

SIGNAL COMBINER
RF CIRCUIT
BLOCK DIAGRAM



Rx RATE BUFFER

Data, clock, and unique word detect is received from the demodulator. These signals are 100K ECL levels, single ended. The data is serial to parallel converted, then ECL to TTL converted. The 16-bit words are stored in a FIFO. The FIFO is 1kx16. The FIFO is read with the Tx low rate data clock divided by 16. The data is then parallel to serial converted and sent to the external error detector. Operation is enables from the front panel with the start switch. The circuit also keeps track of the number of bursts sent. When a burst is missed the acquisition failure circuits detect and display this event.



Rx RATE BUFFER BLOCK DIAGRAM

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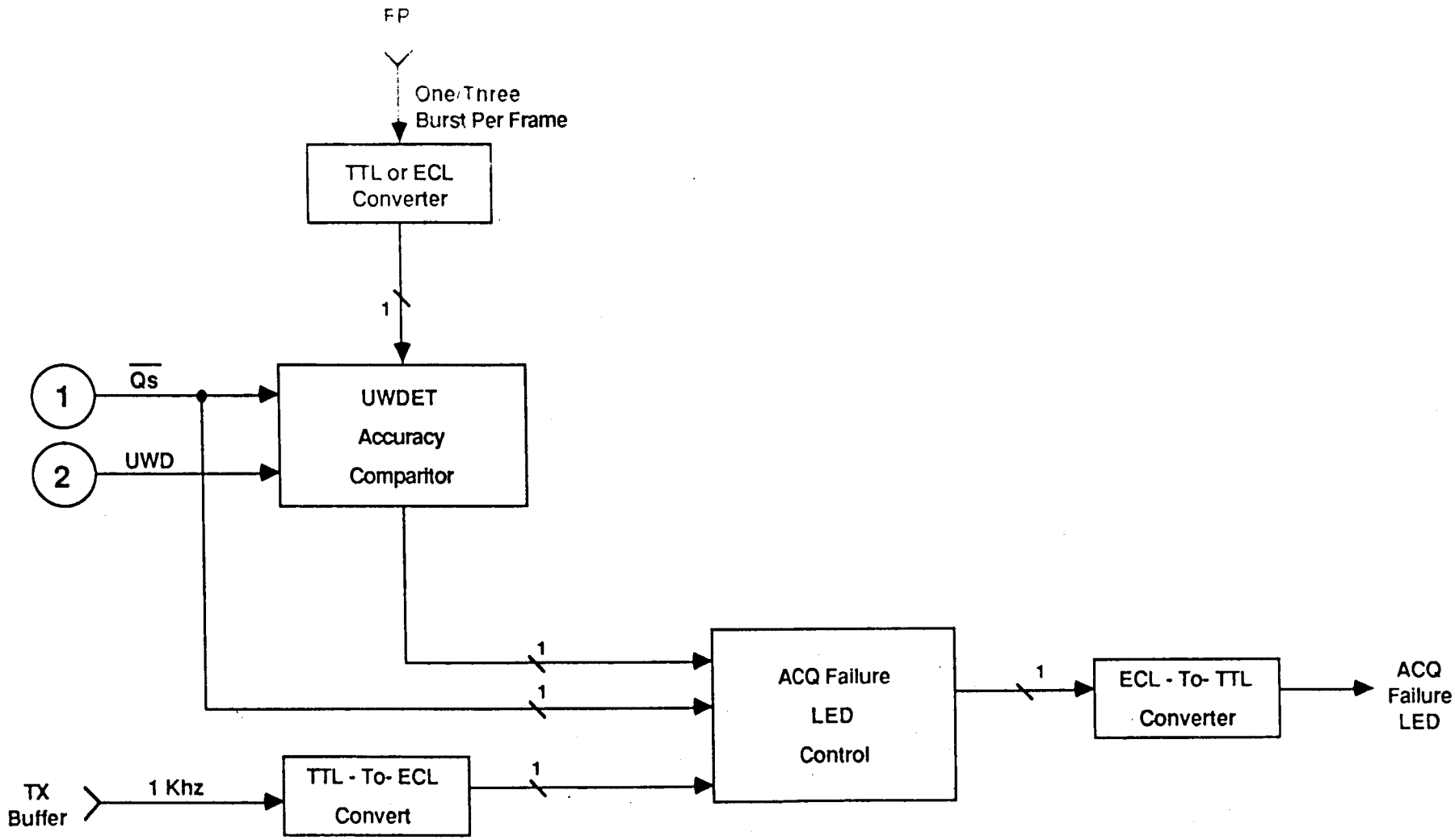


Rx RATE BUFFER BLOCK DIAGRAM

RC.1(2)
1-21-87

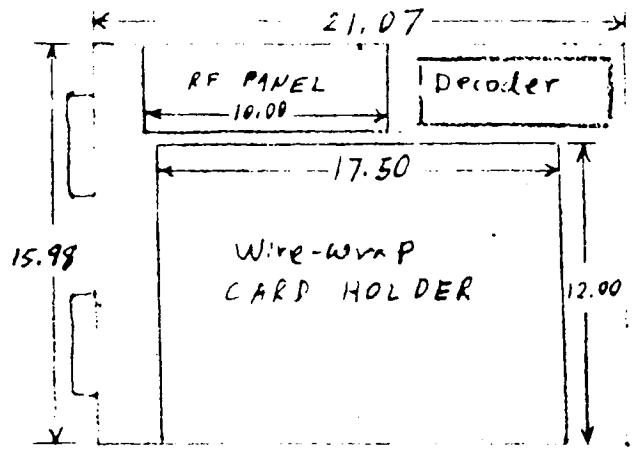
NASA/TDMA

MECHANICAL

DEMODULATOR CHASSIS

The demodulator chassis will contain the digital and RF circuits that transform the 3.373 GHz 16-ary CPFSK RF waveform to digital burst data. The RF circuits will be housed on an RF plate. The digital wire-wrap cards will be housed in a card file. There are four digital cards designed for this program, and four existing digital decoder cards. There will be three 72 DIP 100K ECL Augat wire-wrap cards and one universal TTL wire-wrap board the same physical size as the ECL boards. The card file holding the wire-wrap cards will pivot up and fan out for troubleshooting. The cards do not slide in and out of the card file. Two fans are provided for cooling. DC power is supplied from a separate unit (not shown). The chassis is a standard Zero enclosure. The power supplies are purchased from Lambda. All oscillators are purchased from Vectron.

DEMODULATOR CHASSIS



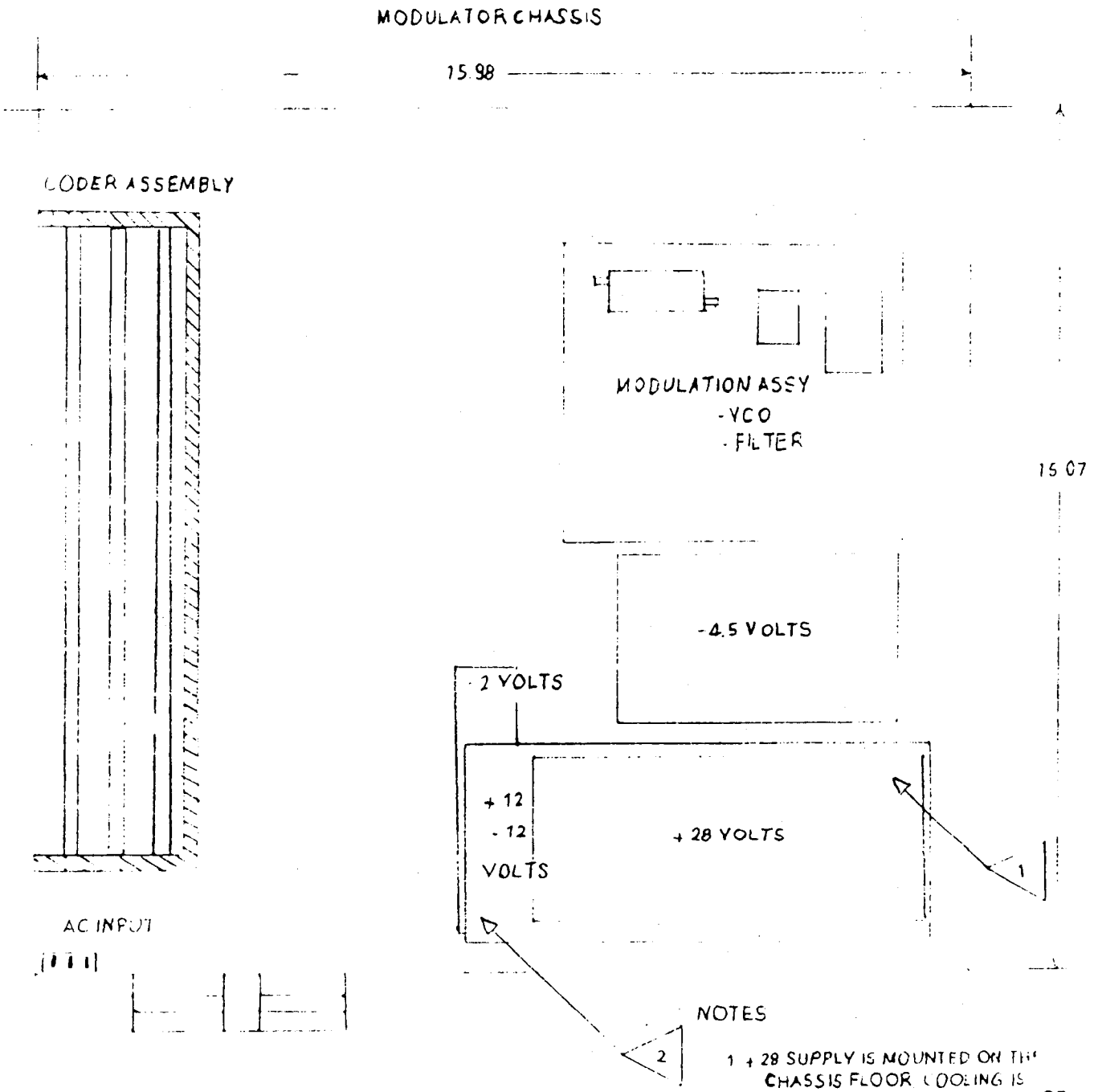
TOP INSIDE VIEW (USABLE PANEL)

CHASSIS INTERIOR CONSISTS OF CARD RACK (HOLDS FOUR CARDS), RF PANEL, Decoder cards, and two fans

MODULATOR CHASSIS

This chassis will house the modulator digital and RF circuits and the power supplies. There will be three 48 DIP 100K ECL Augat wire-wrap boards. They will be housed in a card file that will pivot and fan out for easy troubleshooting. The card file wiring will be from board connector to board connector, so they will not slide in and out. The RF hardware will be mounted on an aluminum plate. A fan is provided for cooling. Lambda power supplies are used. The chassis is a standard Zero enclosure. There will be three of these units built.

ORIGINAL PAGE IS OF POOR QUALITY



NOTES

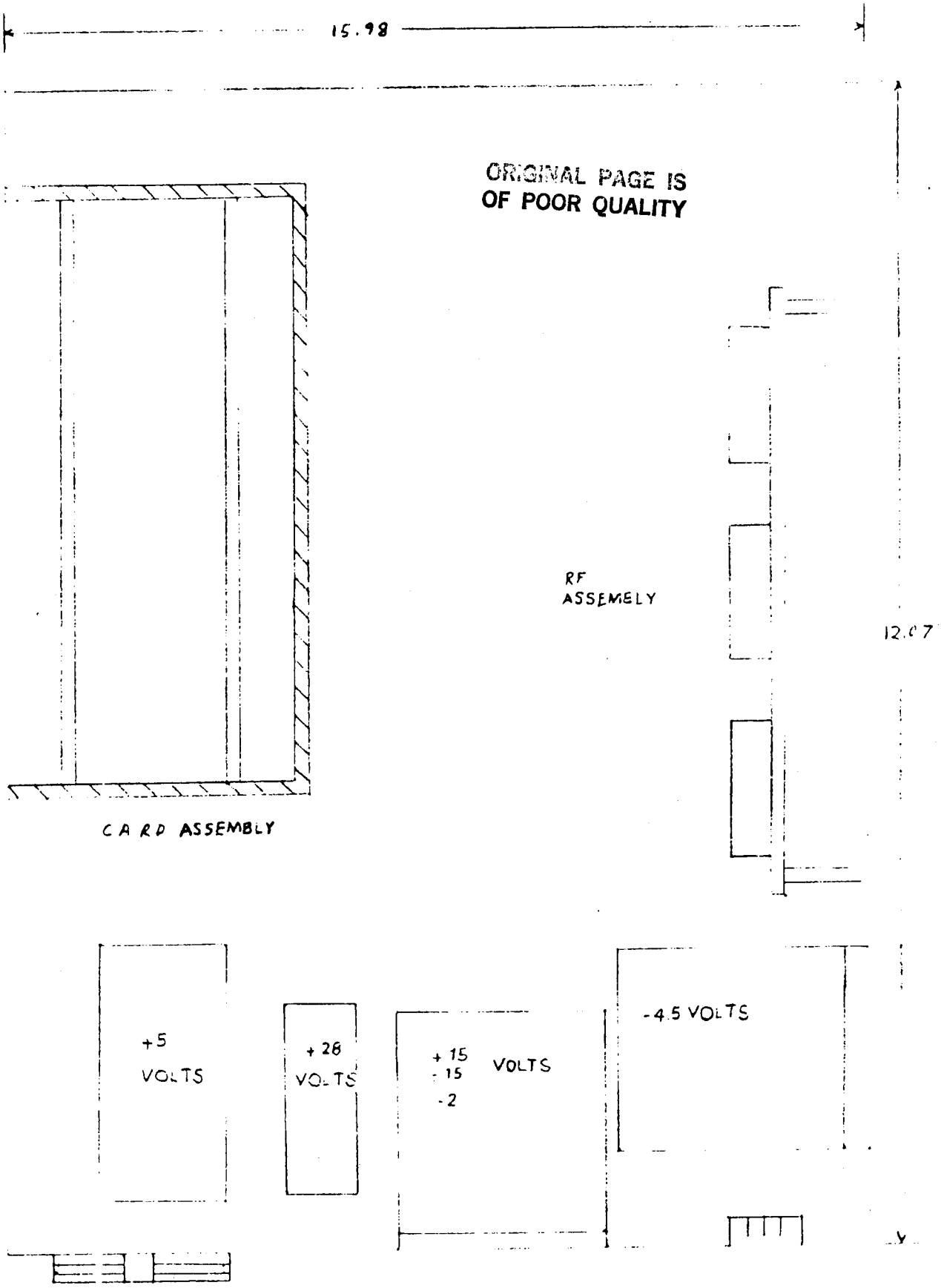
1. + 28 SUPPLY IS MOUNTED ON THE CHASSIS FLOOR COOLING IS THROUGH FRONT AND REAR OF UNIT.

2. + 12 AND - 12 SUPPLY IS MOUNTED ABOVE THE + 28 SUPPLY AND ON REAR PANEL COOLING IS THROUGH SIDE VENTS ON UNIT.

RF 9.00 x 6.00

SIGNAL COMBINER CHASSIS

This unit takes low rate serial data and generates burst data, clock, and control for up to three modulators. It accepts three modulated RF waveforms, sums them together and adds noise. It accepts receive bursts from the demodulator and reserializes the data. There are two wire-wrap cards housed in a card file. One 54 DIP 100K ECL Augat card, and a universal TTL Augat card of the same physical size. The card file will pivot and fan out for easy troubleshooting. The RF hardware is contained on an aluminum plate. Lambda power supplies are provided. A fan provides cooling. The chassis is a standard Zero enclosure.



SIGNAL COMBINER CHASSIS

DEVELOPMENT OF A CODED 16-ARY CPFSK COHERENT DEMODULATOR

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ABSTRACT

Theory and hardware are described for a proof-of-concept 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK) digital modem. The 16 frequencies are spaced every 1/16th baud rate for 2 bits/sec/Hz operation. Overall rate ¾ convolutional coding is incorporated. The demodulator differs significantly from typical quadrature phase detector approaches in that phase is coherently measured by processing the baseband output of a frequency discriminator. Baud rate phase samples from the baseband processor are decoded to yield the original data stream. The method of encoding onto the 16-ary phase nodes, together with convolutional coding gain, results in near QPSK performance. The modulated signal is of constant envelope; thus the power amplifier can be saturated for peak performance. The spectrum is inherently bandlimited and requires no RF filter.

MODEM OVERVIEW

We discuss a bandwidth efficient constant envelope modem: 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK). Error-correction coding is applied to reduce the performance disadvantage relative to AM schemes. The modem is designed for 200 mb/s TDMA application with 100 mHz adjacent channel spacing.

Theoretical Considerations

Two novel theoretical techniques are used in this 16-CPFSK modem: I) coherent phase measurements obtained by processing an FM discriminator baseband output; II) Modulation via a closed-loop linearized VCO. Refer to Figure 1 in the following discussion.

Obtaining coherent phase from a discriminator. A discriminator outputs $\phi'(t)$, where $\phi(t)$ is the signal's phase modulation. Integration of $\phi'(t)$ recovers the desired signal, $\phi(t)$. Implementation of the integration has several practical problems: 1) Integrator output can grow without bound; 2) Initial phase, $\phi(0)$, must be determined; 3) AGC is needed on the baseband signal. Regarding problem 1), fortunately, we need only know phase Mod-2π. Thus the growth problem is avoided by integrating Mod-2π. How can such an integrator be implemented? It is essential only that we obtain $\phi(nT)$, phase at baud time intervals. An integrator yielding $\phi(nT)$ can be implemented as a T-interval Integrate-and-Dump (I&D) sampled by an A/D which feeds a digital accumulator that rolls over Mod-2π. The I&D is actually a lowpass Half-Nyquist filter in this modem, but the conceptual picture remains useful.

Problem 2)--acquiring initial unknown phase, $\phi(0)$, is handled by first observing for each baud time, the phase error to the closest one of the 16-CPFSK phase nodes (Mod-2π) equally spaced in the accumulator. This phase error is filtered by a lowpass loop filter whose output is subtracted from the

accumulator input. The initial phase error, $\phi(0)$, appears as a DC component of the error and is eliminated by the baseband loop. Frequency offset (DC offset from the discriminator) also is eliminated by this baseband loop, the equations for which are identical to those for a PLL.

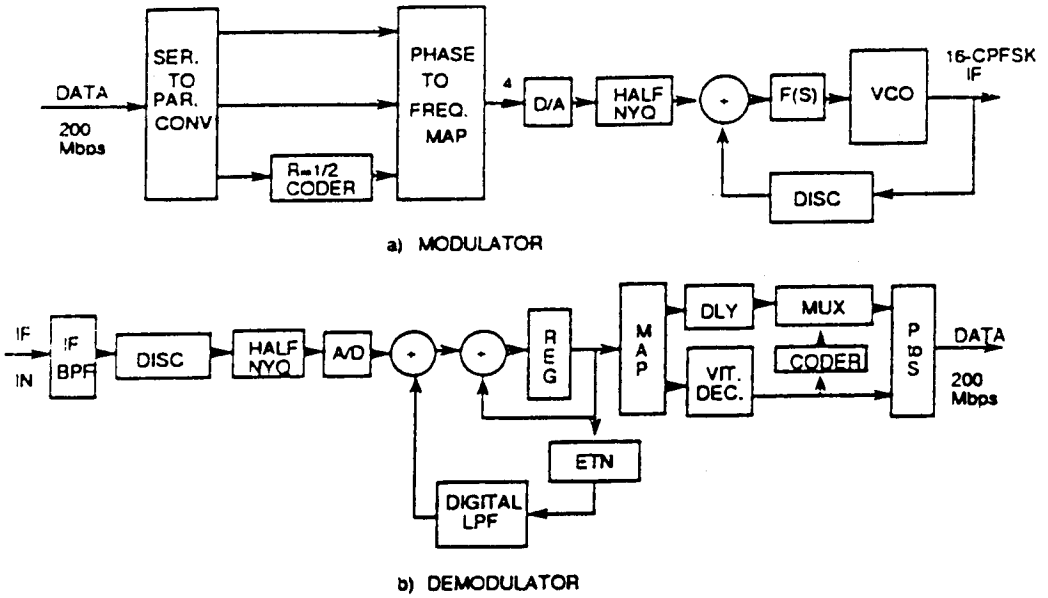

Fig. 1. Basic modem block diagram

Problem 3), AGC, is handled as shown in Figure 1. The accumulator phase error is correlated with input samples, and baseband gain is adjusted to zero the correlation.

Linearized VCO modulator. Figure 1 shows the closed-loop-linearized VCO modulator. The baseband filter output is applied through a feedback summer to the VCO. F(s) is a wideband loop filter. The output of the VCO is immediately converted back to baseband by the discriminator (DISC) and subtracted from the baseband input modulating signal to generate a correction signal in the closed loop. The VCO is thus modulated with small error between the baseband modulating signal and the output of the DISC. If the modulator DISC is identical to the demod DISC, this modulator linearizes the baseband signal path through the modem's VCO/DISC combination.

Brief Description of Modem Operation.

As shown in Figure 1, incoming data is split into 3 parallel bit streams. The 2 MSBs are passed unaltered to modulator MSB positions. The LSB bit stream is coded by a rate ½, K=7 convolutional encoder. The 2 resulting coded branch bits go to the 2 LSB positions of the modulator. The 4 bits produced by this encoding process specify one of 16 symbol-ending phases (Mod-2π) from the 16-CPFSK modulator. Half-Nyquist filtering is employed at the VCO baseband on 16-ary impulses to produce the IF signal at the modulator. At the demod the IF signal is filtered and passed to the DISC. The DISC baseband signal is Half-Nyquist filtered and sampled at symbol rate by an 8-bit A/D. The Half-Nyquist filter completes shaping begun at the VCO, producing an overall Nyquist response to 16-ary impulses. The A/D samples feed the accumulator, whose output is $\phi(nT)$. These phase samples feed a Viterbi decoder for demodulation of the original 3 data streams.

Figure 2 shows the 16-CPFSK phase nodes, along with the mapping of coded 4-bit groups onto them. Any set of 4 adjacent phases contains all 4 rate ½ code branches and has good distance structure. This fact forms the basis for our decoding strategy, to wit: retain only the 4 phase nodes nearest the received coherent phase measurement; then let the Viterbi decoder determine which of these 4 phases is most likely to have been transmitted. The 2 modulator MSBs associated with the decoder's decision are output as 2 of the decoded bits. The third bit decision is the data bit decision made by the decoder. These 3 bits form the total output data bit stream.

Figure 3 shows performance predicted for the coded 16-CPFSK modem.

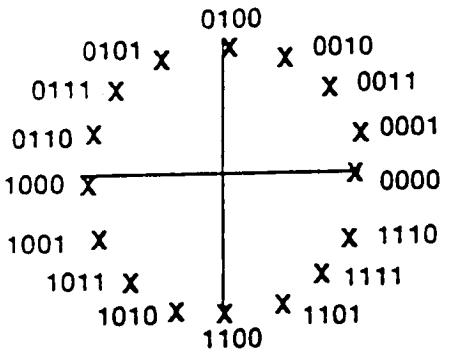

Fig. 2. 16-CPFSK phase nodes.

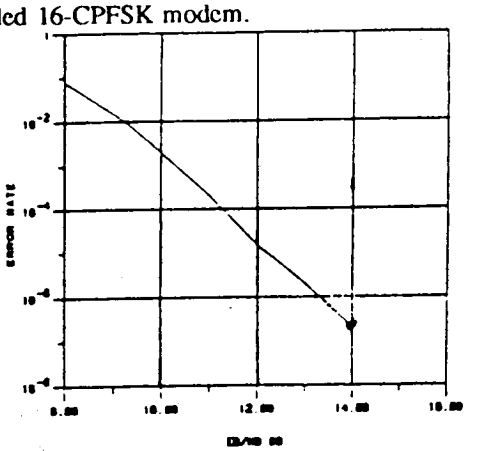

Fig. 3. Modem performance.

DIGITAL BASEBAND PROCESSING

We now discuss the Coherent Baseband Phase Detector (CBPD) hardware. Figure 4 depicts the four major functional portions of the CBPD circuitry: 1) Baseband Preprocessor, 2) Phase Accumulator/DC Restore Loop, 3) AGC Loop, and 4) Timing and Control.

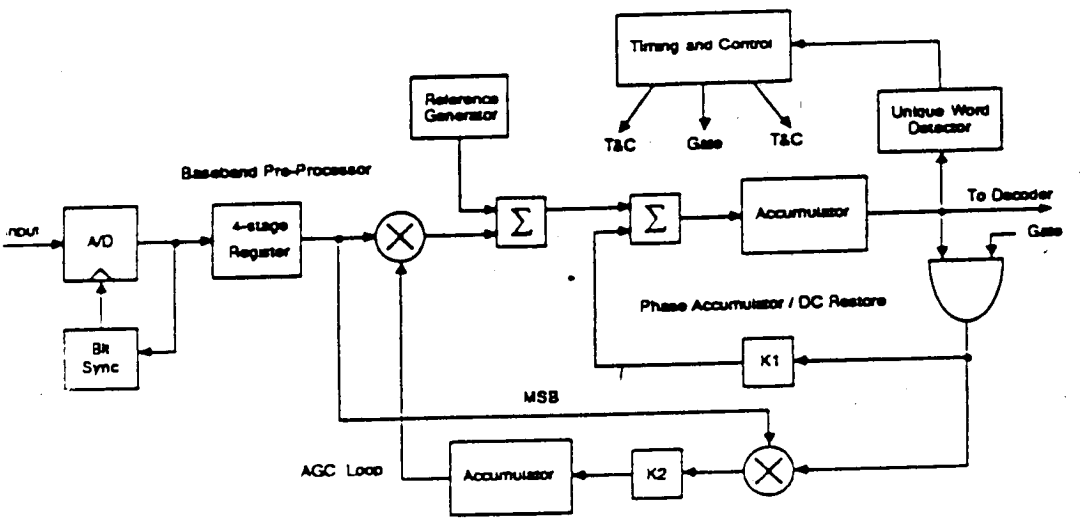

Fig. 4. Coherent Baseband Phase Detector.

Baseband Preprocessor

The filtered (Raised Cosine, 25% excess bandwidth) output of the frequency discriminator is sampled at symbol rate by an 8-bit A/D converter. The samples are sequentially stored in 4 registers to allow detection of an "all f_0's" portion of the TDMA preamble. If detected, the remaining registers in the phase detector circuitry operate normally; otherwise, these registers are asynchronously held low. The output of the fourth register, along with a 16-bit attenuation factor, K, are input to a 16 × 16 ECL multiplier, which provides AGC on any gain variation at the output of the limiter/discriminator (± 6.25% max.). At the output of the multiplier, a binary number is added to the 12-bit two's complement product such that when an f_0 is received, zero is output to the phase accumulator circuit.

Phase Accumulator/DC Restore Loop

An error term, proportional to DC offset in the discriminator output (which results from frequency offset in the IF), is subtracted from the 12-bit number output from the baseband preprocessor. The "DC restored" value is then accumulated by a 12-bit accumulator, completing the implementation of an integrator. The output of the 12-bit accumulator represents 360° of coherent phase (Mod-2π).

The DC restore loop is constructed in the following fashion. During the data portion of a burst (following the preamble and unique word), the transmitted phase constellation is restricted to that of 4-ary signalling (90° spacing) on every fourth transmitted symbol (called a "tracking" symbol). During the tracking symbols, the 10 LSBs, of the accumulator output, directly represent the error in hitting a phase node (error-to-node). Thus, a modulo 90° (±45°) phase detector characteristic is displayed by the 10 LSBs of accumulator output during the tracking symbol. To control DC offsets out of the discriminator, the error-to-node is multiplied by a gain factor, KL, and subtracted from the input to the coherent phase accumulator. This processing is equivalent to a 1st-order PLL correction. For a 1st order control loop with open loop gain, K, the loop noise equivalent bandwidth is given by: $B_L = K/4$ (Gardner, 1979). During the data portion of a burst, with KL = 1/4, and corrections being applied to the loop on every fourth symbol, $B_L = R_S/64$ MHz, where R_S = the symbol rate.

Phase acquisition for independent bursts is accomplished during the all-f_0's portion of the preamble. Initially, the phase accumulator is zeroed. After the all-f_0's portion of the preamble has been detected by the Baseband Preprocessor, the DC restore loop is allowed to update during every symbol interval (providing maximum loop gain, and thus wide loop bandwidth). This processing acquires $\phi(0)$ and initial DC offset at the discriminator output. Since the loop corrects on every symbol, the loop gain is four times that of the "tracking" loop gain, and thus, $B_L = R_S/16$ MHz. Transport delay in the digital control loop is minimized to maintain stable closed loop response for wide loop bandwidths.

AGC Loop

An error term, proportional to gain missetting, is derived by correlating a delayed version of the discriminator sign output with the error-to-node signal. The gain error is filtered by a digital accumulator, and a detector bias (1.0) is added at the accumulator output. The resulting AGC correction factor, KA, is 1 ± 0.0625. The input to the CBPD circuit is scaled by KA using a 16×16 ECL multiplier. Thus, fine decision-directed AGC is provided, which prevents "walkoff" of the coherent phase accumulator.

The loop bandwidth of the AGC loop is given by; $B_L = K/4$, where K = Open Loop Gain. During the all-f_0's portion of the preamble, the AGC loop updates on every symbol and the open loop gain is $R_S/16$. Like the DC Restore loop, the AGC loop updates on every fourth symbol during tracking, so that the open loop gain is ¼ that of acquisition. Thus, $B_L = R_S/64$ during acquisition and $B_L = R_S/256$ during tracking.

Timing and Control

The major portion of the baseband timing control circuit is the Unique Word (UW) detector. The UW consists of six unique symbols immediately following the preamble. The UW is detected when the 6 symbols fill the UW detector correlator cells, allowing one symbol error. The UW, when detected, establishes a second level time tick for burst processing (first level is symbol synchronization). The UW detector establishes the gating clock used to update the control loops on every fourth symbol during the data portion of a burst.

BASEBAND ENCODER/MODULATOR

In the baseband encoder, the data stream (at 200 Mbps) is partitioned into 3-bit symbols. The two MSBs are used directly, and the LSB is rate ½, K=7 convolutionally encoded to produce a 4-bit symbol. This overall rate ¾ code, combined with the CPFSK characteristic, promotes good bandwidth efficiency.

With 3-bit symbols, the symbol rate is reduced to 1/3 the 200 Mbps data bit rate, allowing use of off-the-shelf ECL and eliminating need for custom ICs or GaAs technology.

Figure 5 shows a block diagram of the encoder/modulator. The input data buffer translates the 200 Mbps serial data stream into a parallel 11-bit word, allowing the input data RAM to operate at 1/11th of the input bit rate. The ECL RAM input buffer is configured as a FIFO. After buffering, the data is read out of the FIFO and partitioned into three, 3-bit groups, and one 2-bit group. Each 3-bit group is operated on as previously described (2 MSBs unaltered; LSB R=½ encoded) to produce 4-bit coded symbols. The remaining 2 bits are treated as MSBs and two zero bits are appended to form the fourth 4-bit symbol. This is done as previously described to aid the demodulator in maintaining carrier lock.

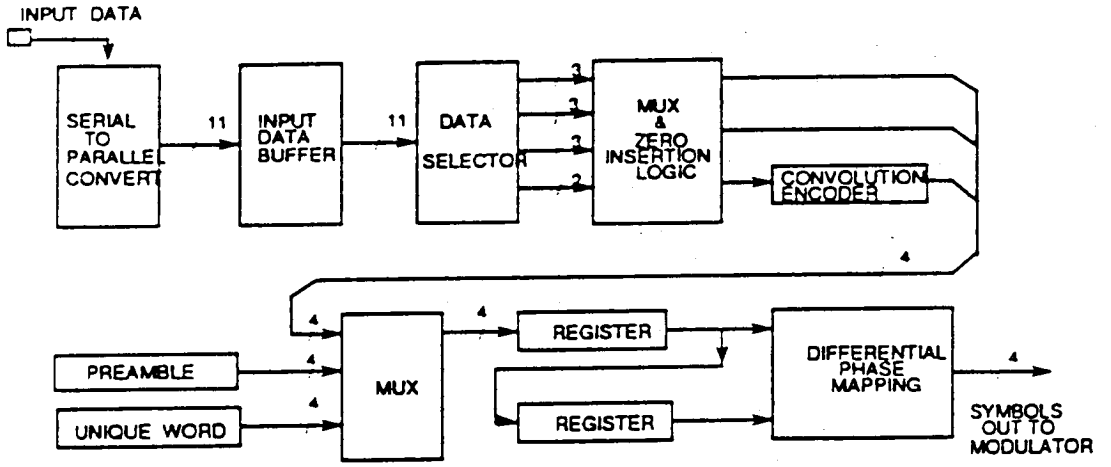

Fig. 5. Encoder block diagram.

Preamble/Unique Word

Prior to sending data, a TDMA preamble is sent. The preamble is a 32-symbol pattern alternating between the two peak frequencies of the 16-CPFSK signal, followed by 32 symbols of lowest frequency, which allows symbol synchronization and coherent phase acquisition.

A 6-symbol unique word to flag start-of-data follows the preamble. Encoded data symbols immediately follow the unique word. The preamble, unique word, and encoded data are all selected via the mux function shown in Figure 5.

Symbol Mapping

With CPFSK, transmitted frequency symbols convey "differential" phase information rather than absolute phase. For example, if the previous encoded 4-bit symbol produced a phase value of Φ_5 and the next 4-bit symbol represented phase Φ_{10}, then the modulated frequency sent out for the current symbol time is that needed to swing phase from Φ_5 to Φ_{10}. The mapping function shown in Figure 5 provides this operation. Two registers address the mapping PROM. One contains the previous 4-bit encoded symbol and the other contains the current 4-bit symbol. This provides the mapping PROM with sufficient information to determine the required frequency to transmit such that the received phase point will be that specified by the current 4-bit symbol.

Encoder Termination Sequence

At the end of the input buffered data, six zeroes are appended to the data stream sent to the convolutional encoder. This forces the encoder to start and end in state 000000 each TDMA burst. At the receiver, the Viterbi decoder function exploits this *a priori* knowledge by forcing the decoder to begin in state 000000 on every burst.

BASEBAND DEMODULATOR

Major baseband demodulator functions are highlighted in Figure 6 The 7-bit phase measurements, as received from the CBPD, are rate buffered and sent to the mapping function, which determines the 4 signal phase points closest to each demodulated value. This homes in on a quadrant of adjacent phase points retained as likely decision candidates.

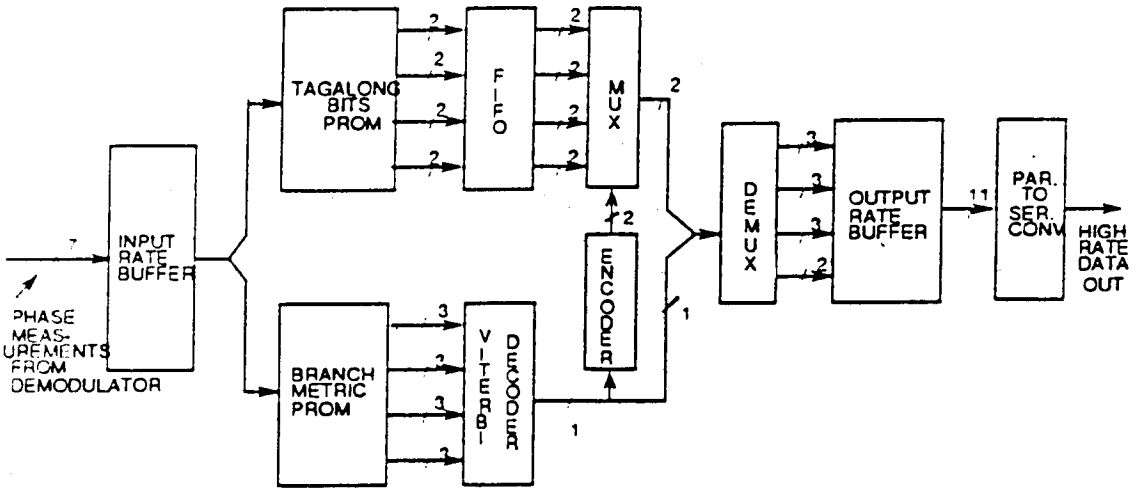

Fig. 6. Decoder block diagram.

The phase distances of these 4 candidate nodes from a given demodulated phase point serve as branch metrics to the Viterbi decoder for the four (00, 01, 10, 11) LSB R=½ code-branch bit pairs. The decoder uses these metrics directly to determine which of the four candidates was most likely transmitted.

As noted already, ANY four consecutive nodes in the signal constellation always contain the values 00, 01, 10, an 11 for the encoded LSB portion; and the two unencoded MSBs simply "tag along" with the respective encoded LSB values. These MSB tag-along bits are sent to a FIFO buffer whose length equals the throughput delay of the Viterbi decoder.

Viterbi Decoder

The four candidate branch metrics described above are fed directly into a R=½, K=7 Viterbi decoder to recover the coded third of the total data bit stream. The decoder output data is then re-encoded to produce an error-corrected 2-bit symbol pair (code branch). This pair selects the corresponding tag-along MSB bit pair from the tag-along FIFO. These tag-along MSB bits are regrouped with the corresponding output data bit from the Viterbi decoder to form the recovered 3-bit data group.

Final Processing

The recovered 3-bit data groups are collected. On every fourth group, only two tag-along bits are recovered (because the LSBs were forced to 00 back at the encoder to support phase tracking). In addition, the 000000 coder termination sequence is removed from the recovered data bit sequence.

The recovered data bits are then rate buffered in another FIFO whose output is then parallel-to-serial converted. This reconstructs the original data stream at the original high speed data bit rate (200 Mbps).

Parallelism in the design of the encoder/modulator and decoder/demodulator allows the use of lower speed, lower cost technology for most internal processing operations. High data rate parts are limited to the encoder/modulator input and to the decoder/demodulator output.

REFERENCES

Gardner, F.M. 1979. Phaselock Techniques. John Wiley & Sans, New York, New York.

TASK VII REPORT

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prepared for
NASA Lewis Research Center
Contract number NAS3-24681

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1.0 INTRODUCTION

This report is prepared by Harris Government Communications Systems Division for NASA Lewis Research Center under contract NAS3-24681. This report is written in response to SOW paragraph 2.7, Task VII Proof-of-Concept (POC) Testing and Analyses. The purpose of this document is to present the results of the tests conducted in accordance with the POC Model Test Plan and Procedure developed in response to SOW subtask 2.5.3 and which covers in detail all of the categories of the top level test plan generated under subtask 2.4.4.

1.1 Reason for Test

The purpose of the POC Model Test is to verify the ability of the POC model to meet the performance requirements of SOW sections 3.1 and 3.2, and to provide a quantitative measure of the required electrical and performance parameters. Additionally, the purpose of the POC Model Test is to produce recommendations for the development of an engineering model demodulator using further advanced implementation technology, based on analyses of test results.

1.2 Description of Unit Under Test (UUT)

The UUT is the POC model demodulator which is comprised of the Demodulator chassis and the Demodulator Power Supply chassis. The Demodulator chassis contains the RF and digital circuits that transform the 3.373 GHz 16-ary CPFSK RF waveform to digital burst data. The Demodulator Power Supply chassis houses the DC power supplies that provide power to the Demodulator chassis. The chassis are standard Zero enclosures.

1.3 Applicable Documents

- Contract NAS3-24681 Statement of Work (SOW)
- POC Model Performance Specification, Rev. A, November 1986
- POC Model Test Plan and Procedure

The POC Model Test Plan and Procedure document is attached as Appendix A to this report. Section 2.0 contains the POC Model Test Plan, Section 3.0 contains the POC Model Test Procedure, and Section 4.0 contains the POC Model Test Data Sheets.

2.0 PROOF-OF-CONCEPT MODEL TEST RESULTS

Regrettably, contract funds were exhausted before the POC Model Test could be performed. Certain technical problems with the POC model hardware prevented the desired BER performance from being achieved. As a result, no meaningful data could be derived by performing the formal POC model test procedure. We believe that conceptually the modulation approach we selected is sound and that the problems with the POC model hardware implementation can be resolved. The following paragraphs serve to document the known problems and explain their effect on system performance.

2.1 System Noise

A noise floor exists within the POC Model Demodulator and Special Test Equipment (STE) that establishes an error floor which prevents the system from operating error free. One of the functions of the Signal Combiner Chassis is to allow noise to be summed with the desired signal for the purpose of measuring BER performance versus E_b/N_0. Even when no noise from the internal noise source is summed with the desired signal, a significant amount of unexpected noise can be measured at the demodulator. The exact origin of the unwanted noise is unknown but switching power supply pick up, amplifier noise figures, and coupling from the internal noise source are all suspected to be potential contributors. The purpose of this discussion is to document the amount of noise present and project its effect on system BER performance.

Figure 2.1.1 shows a spectrum analyzer plot at the discriminator output of the demodulator. The single carrier shown at 36.36 MHz was produced by alternately transmitting f_0 f_{15} tones. These tones represent the maximum FSK tone spacing available in our modulation scheme and are spaced 15/16*symbol rate, or 68.18 MHz apart. Since these tones alternate at a period equal to 2 symbols, their fundamental frequency is 1/(2*symbol period), or 36.36 MHz. They are shown as a reference point since the number of LSBs for the maximum f_0 f_{15} peak to peak frequency deviation is known to be 120 LSBs. Since this f_0 f_{15} signalling is sinusoidal, the RMS value of the signal in LSBs can be computed by the following:

$$\frac{120 \text{ LSBs p-p}}{2\sqrt{2}} = 42.43 \text{ LSBs}$$

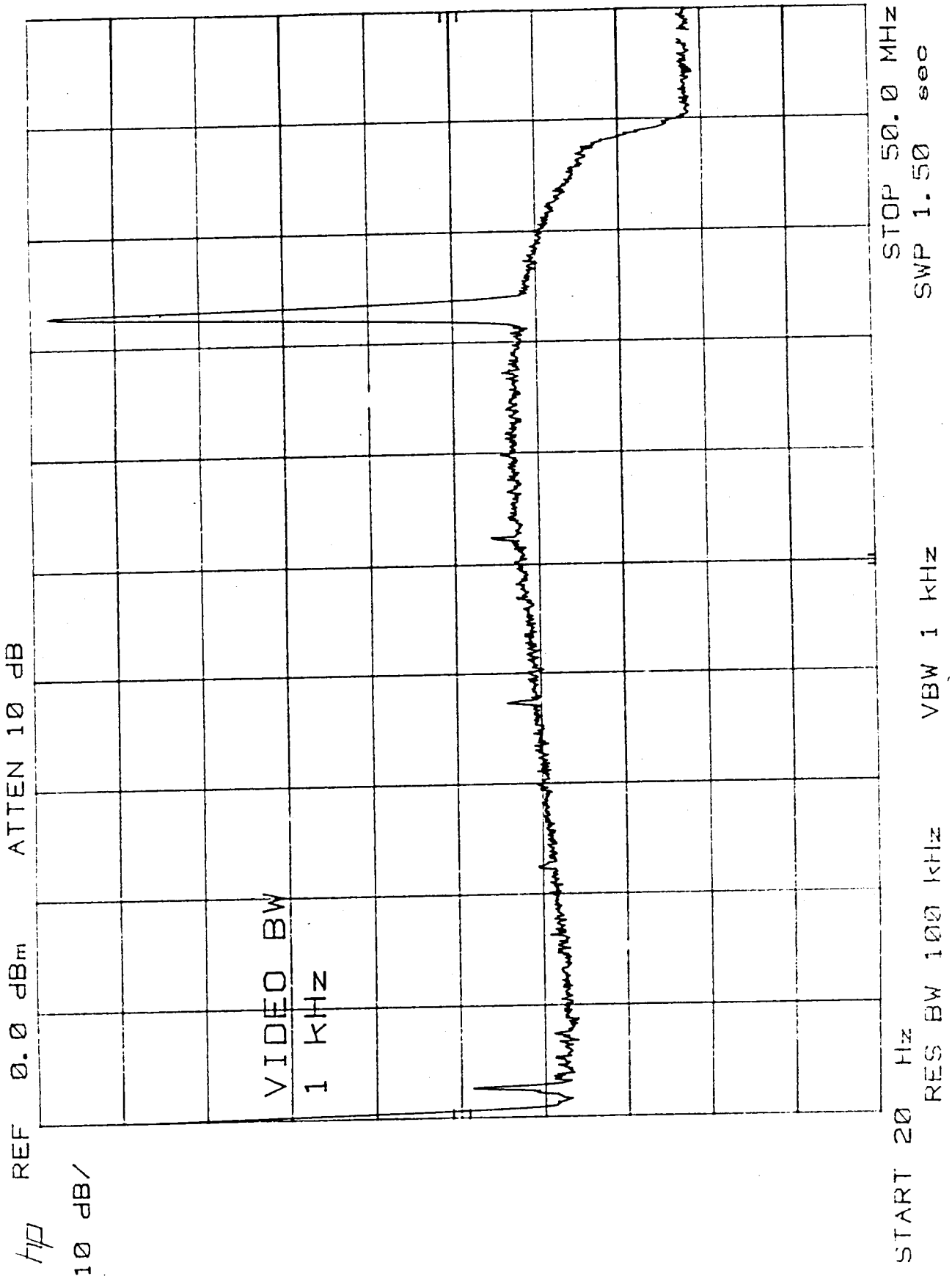

Figure 2.1.1 Spectrum Analyzer Plot at Demod Discriminator

The noise floor in figure 2.1.1 is at -60 dBm and was measured within a resolution bandwidth of 100 kHz. If we assume the noise power is flat out to 40 MHz (36.36 MHz is the ideal Nyquist baseband filter corner frequency), the noise power in a 40 MHz bandwidth is:

$$-60 \text{ dBm} + 10\log(40\text{MHz}/100\text{kHz})$$
$$-60 \text{ dBm} + 26 \text{ dB} = -34 \text{ dBm}$$

The signal to noise ratio at the discriminator output is then:

$$S/N = -2 \text{ dBm} - (-34 \text{ dBm}) = 32 \text{ dB}$$

Given that we know the RMS value of the signal at -2 dBm corresponds to 42.43 LSBs (RMS), we can compute the RMS value of the noise in the system from the following:

$$S/N = 10\log(42.43/n)^2 = 32 \text{ dB}$$

Solving for n:

$$(42.43/n)^2 = 1585$$
$$n^2 = 42.43^2/1585$$
$$n = 1.06 \text{ LSBs (RMS)}$$

From figure 2.1.2 we know the noise variance at the output of the tracking loop due to the A/D converter quantizing noise. At the 1 MHz loop natural frequency the RMS jitter is 0.6 LSBs. At the input to the loop, i.e. the A/D converter output, the quantizing noise is uniformally distributed over $\pm$ 0.5 LSB. The RMS value of the quantizing noise in a quantizing interval of width q is $q/\sqrt{12}$, or 0.29 LSBs. Thus the ratio of the RMS noise at the output of the loop to the RMS noise at the input to the loop is (0.6)/(0.29). Since we computed the amount of RMS noise at the discriminator output to be equal to 1.06 LSBs, the amount of noise at the output of the loop is 1.06*(0.6)/(0.29) = 2.2 LSBs (RMS).

Figure 2.1.2 shows the amount of RMS noise at the output of the loop due only to additive white gaussian noise at an IF signal to noise ratio of 17 dB. This noise is represented by the horizontal line labeled sigma_{disc} and is equal to 1.75 LSBs of RMS jitter. An IF signal to noise ratio of 17 dB corresponds to an E_b/N_0 of 14 dB and is computed from the following equation:

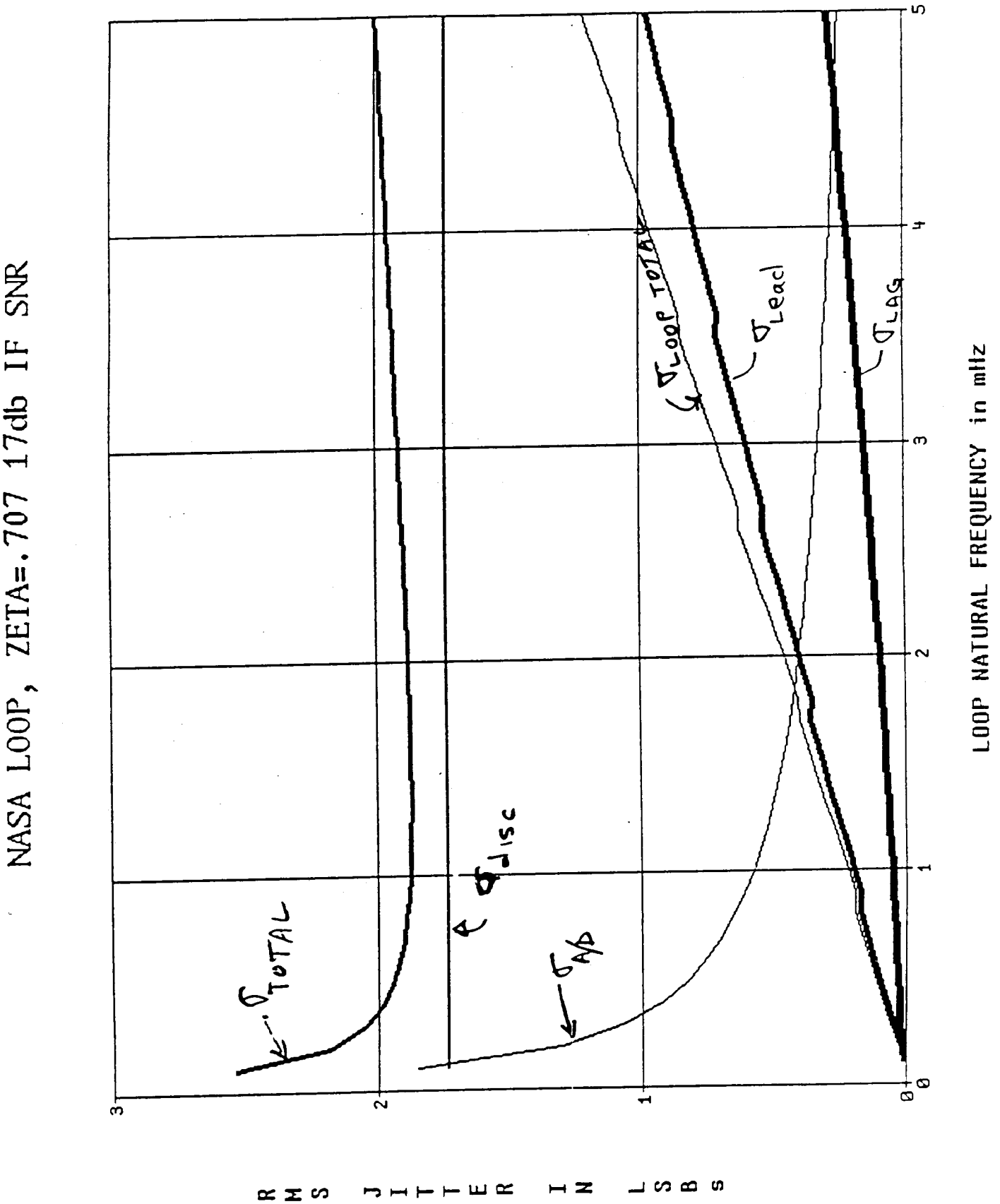

Figure 2.1.2 Loop Jitter VS Natural Frequency at 17 dB IF SNR

$$E_b/N_0 = (S/N)(BW/BR)$$
$$E_b/N_0 = 17\ dB + 10\log(100\ MHz/200\ MHz)$$
$$E_b/N_0 = 17\ dB - 3\ dB = 14\ dB$$

From this we know that 1.75 LSBs of RMS jitter at the output of the loop corresponds to an E_b/N_0 of 14 dB. Earlier we calculated the amount of noise at the output of the loop from the spectrum analyzer plot of the discriminator output to be 2.2 LSBs of RMS jitter. This means that the E_b/N_0 at IF that would correspond to the amount of noise we observe in our system with a signal only input is poorer than 14 dB and can be calculated from the following:

$$E_b/N_0|_{@\ 2.2\ LSBs} = E_b/N_0|_{@\ 1.75\ LSBs} + 10\log(1.75/2.2)^2$$
$$E_b/N_0|_{@\ 2.2\ LSBs} = 14\ db - 2\ dB = 12\ dB$$

From figure 2.1.3, an E_b/N_0 = 12 dB corresponds to a predicted error rate of approximately $2*10^{-5}$. This means that unless the amount of unwanted noise is reduced, an error rate of no better than $2*10^{-5}$ is possible.

2.2 Nonlinear Distortion

The nonlinearities from VCO baseband input to discriminator baseband output needs to be 1 % or less. For a cubic nonlinearity, this translates to a requirement that third order intermod distortion, as measure by a two tone test, be at least 45 dB down relative to the desired tones. This requirement has been difficult to achieve and maintain. We currently believe that the hardware meets this requirement, however past problems with error rate performance have often been traced to this difficult requirement. The D/A converter in the modulator was changed from a Brooktree to a Honeywell unit specifically to improve the system end to end linearity. A substantial improvement in error rate performance was obtained by making this transition.

2.3 Inter Symbol Interference

Inter Symbol Interference (ISI) has presented problems since the √Nyquist filters are specified in the frequency domain yet the performance requirements exist in the time domain. The conversion from time domain to frequency domain was made to allow the filter vendors to work within a medium they are familiar with. We have had to make manual adjustments to the tunable slug coils within the filters, once they were

MODEM ERROR RATE PERFORMANCE

The figure shows the Bit Error Rate Performance predicted for the Harris TDMA Modem compared to QPSK performance.

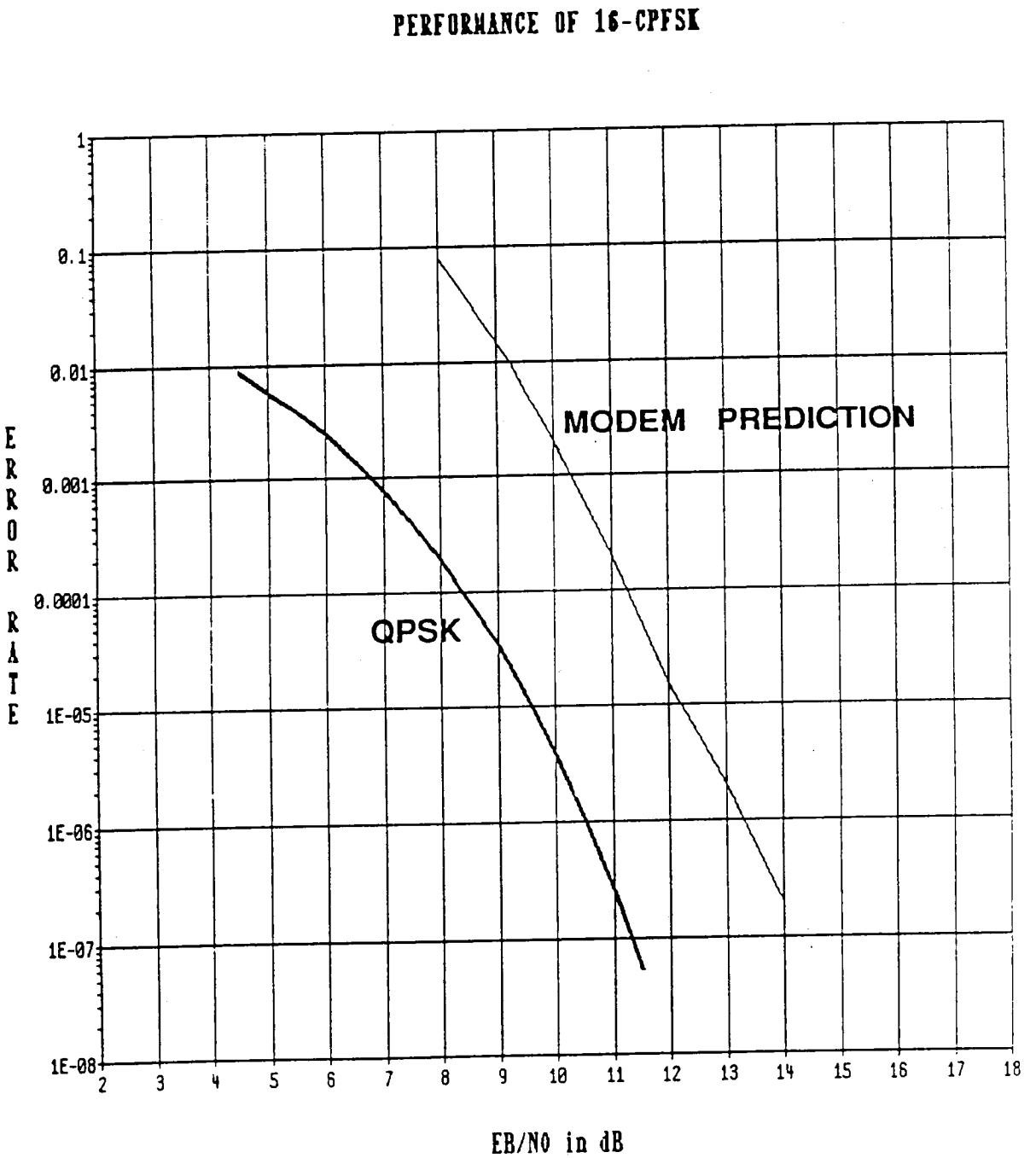

Figure 2.1.3 16-CPFSK BER Performance

C-3

installed in the system, in order to optimize BER performance.

3.0 PROOF-OF-CONCEPT MODEL TEST ANALYSES, ASSESSMENT, AND RECOMMENDATIONS

We believe that conceptually the modulation approach we selected is sound and that the problems with the POC model hardware implementation can be resolved. There are many inherently desirable aspects of our design that lend themselves to the long term goal of a low cost, highly reliable, TDMA earth station modem for commercial applications. The following sections address the benefits of the existing POC model hardware technology and potential improvements for future engineering model and production units.

3.1 Assessment of Technology Readiness to Proceed with Engineering Model Development

There are various hardware techniques incorporated into our modem which represent an advancement of the state-of-the-art in modem technology. Examples are: a high speed Op Amp, high speed A/D converter, high speed D/A converter, SAW IF filter, and 1/2 Nyquist baseband lowpass filters. The Op Amp represents advanced technology in that a true differential amplifier is required that has a very large bandwidth and a very short settling time. The A/D and D/A converters represent the state of the art in conversion technology, again because of the high speed, large bandwidth, and low distortion requirements of our system. The IF filter represents an advance in technology in that conflicting specifications, such as steep skirt selectivity coupled with almost linear phase, must be met in one filter. The 1/2 Nyquist baseband filter advances modulation technology in that it reduces the sidelobe levels of the non-filtered CPFSK spectrum at the output of the TWT, while minimizing Inter Symbol Interference (ISI) at the demodulator.

Much of the existing technology utilized in the POC Model hardware lends itself to lower recurring cost in production quantities. Examples are: the extensive use of digital circuits in the baseband processing, the use of surface acoustic wave (SAW) technology for the IF filter, and the use of monolithic microwave integrated circuits (MMIC) for the IF signal processing.

Digital technology has and still is evolving at an incredible pace. Because of shrinking geometries, integration at the chip level is increasing while the gate capacitance is decreasing, leading to lower propagation delays. Also, the cost of producing complex parts keeps

falling due to greater percentage yields over time and an ever increasingly competitive market. For these reasons, we have strived to construct a major portion of our modem using digital technology. IN the POC model we used standard ECL parts to implement a majority of the baseband signal processing functions. We envision the use of ECL gate array circuits in the engineering and production models, which have great potential for low cost when quantity purchases are made. Finally, the use of digital technology in our modem eliminates many adjustments that would have to be performed during the production and test cycles which are labor intensive and costly.

The IF filter is implemented using SAW technology. Because SAW devices are fabricated from a mask (in much the same way as digital devices), filters built using SAW technology are very repeatable from device to device. That is, the characteristics of a filter remain very consistent between various production runs. In addition to repeatability, once the mask for a SAW device has been designed, the fabrication process is automated (non labor intensive) which leads to low cost per unit if the NRE is spread over a large quantity of units. This NRE investment for the IF filter has already been made during the POC model development.

Monolithic microwave integrated circuits (MMIC) is a young technology that is maturing quickly. Many types of circuits are available now in quantities for costs as low as $20 per unit. Available functions include: AGC amplifiers, limiting amplifiers, phase shifters, phase modulators, etc., all of which operate in the GHz region. Since such powerful devices are currently available, it is not difficult to predict further integration levels, thus enabling even more complex MMICs to be fabricated. We anticipate that by the 1990's, the entire front-end chain of our modem might consist of one MMIC chip and one SAW filter on the corner of a printed circuit card.

3.2 Design Modification Recommendations for Engineering Model Development

We are currently using an analog VCO to switch frequencies with no abrupt change in phase at the symbol boundaries. In the future it will be possible and advantageous to perform the frequency modulation using a direct digital synthesis technique via a Numerically Controlled Oscillator (NCO). In addition, baseband processing circuits that are now accomlished with SSI and/or MSI ECL devices can be implemented in ECL gate arrays with a high degree of integration at the chip level, enabling many functions to be performed by one device. The improvements that are

realized by the future technologies may be in performance (as is the case of the NCO implementation of the VCO), in reliability (as is the case of the SSI to VLSI transition), and/or cost. The key technologies used in the modem and their current or future implementation strategies are summarized in Table 3.2.

Table 3.2 Current VS Future Implementation of Key Technology Items

TECHNOLOGY ITEM	CURRENT IMPLEMENTATION	FUTURE IMPLEMENTATION
Frequency Modulator	Analog VCO	Digital NCO
Frequency Detector	Bulk Analog	MMIC/SAW
IF Filter	SAW	SAW
Baseband Processing	SSI & MSI ECL	ECL Gate Array
Viterbi Decoder	Low Rate - SSI/MSI	High Rate - VHSIC

3.2.1 Frequency Measuring Circuits

The advantage of using a frequency measuring circuit in the implementation of the demodulator is that it reduces the overall hardware design complexity of the demodulator. Thus, by reducing circuit complexity, a cost savings is realized both in the POC model design effort and in future production quantities. The only disadvantage to the frequency measuring approach is the tight linearity requirements, necessary to achieve near QPSK BER performance.

The linearity of the frequency detector and VCO impacts the BER versus E_b/N_0 performance of our modem. Our design goal for the frequency linearity was 1 % which was difficult to achieve using existing technology. As technology progresses, linearities of less than 1 % will be more easily realizable. As technology allows an NCO to be implemented at the frequencies of interest, linearity will be of no concern in that an NCO is inherently linear. The VCO output power variation with frequency also impacts BER performance. Our design goal for this parameter was 0.25 dB, but again, an NCO would alleviate this problem.

The reason a VCO was used as the continuous phase frequency modulator is that VCOs were available that had suitable dynamic characteristics. The disadvantage of the VCO technology is the nonlinearity of the voltage to frequency conversion and the long term frequency drift of the VCO. An NCO, as previously touted, is inherently linear and its frequency stability is as good as its reference.

3.2.2 Baseband Circuits

The baseband signal processing functions are implemented using digital technology and therefore realize all the advantages that are inherent to threshold logic. These advantages include: stability over time and temperature, a high degree of integration at the chip level, immunity to small cross-talk and noise signals, and finally, digital circuits lend themselves to all kind of automated processes which reduce production, test, and maintenance costs. The only disadvantage of using digital circuits to implement the baseband processing functions of our demodulator are the large number of interconnections required in the baseband processing section with the use of SSI and MSI technology. This design is inherently less reliable than an implementation with fewer LSI components. As the implementation transitions from SSI/MSI to gate arrays, the number of interconnections between parts as well as the total parts count will decrease, which will increase the reliability of the modem. The high processing speeds at which we must operate (the sample rate = the symbol rate = 72.73 MHz) led to ECL technology to accomplish the required processing under worst case conditions with margin. ECL gate arrays have lagged behind CMOS and bipolar technologies but are now emerging in the marketplace with impressive equivalent gate counts and speeds. A recently completed vendor survey is included in Appendix B which highlights the capabilities of several vendors to manufacture devices that lend themselves to this modulation technology.

We estimate that the bulk of the baseband processing circuitry in the POC model demodulator could be replaced by five ECL gate array devices. Each large wire wrap card could be relaced with one gate array device. Figure 3.2.2 shows the 4 printed circuit card Viterbi decoder implementation currently used in the POC model demodulator (on the right) next to its functional LSI equivalent (on the left). Although the LSI version was developed for another application, this photograph is a dramatic example of the reduction possibilities inherent in this design implementation.

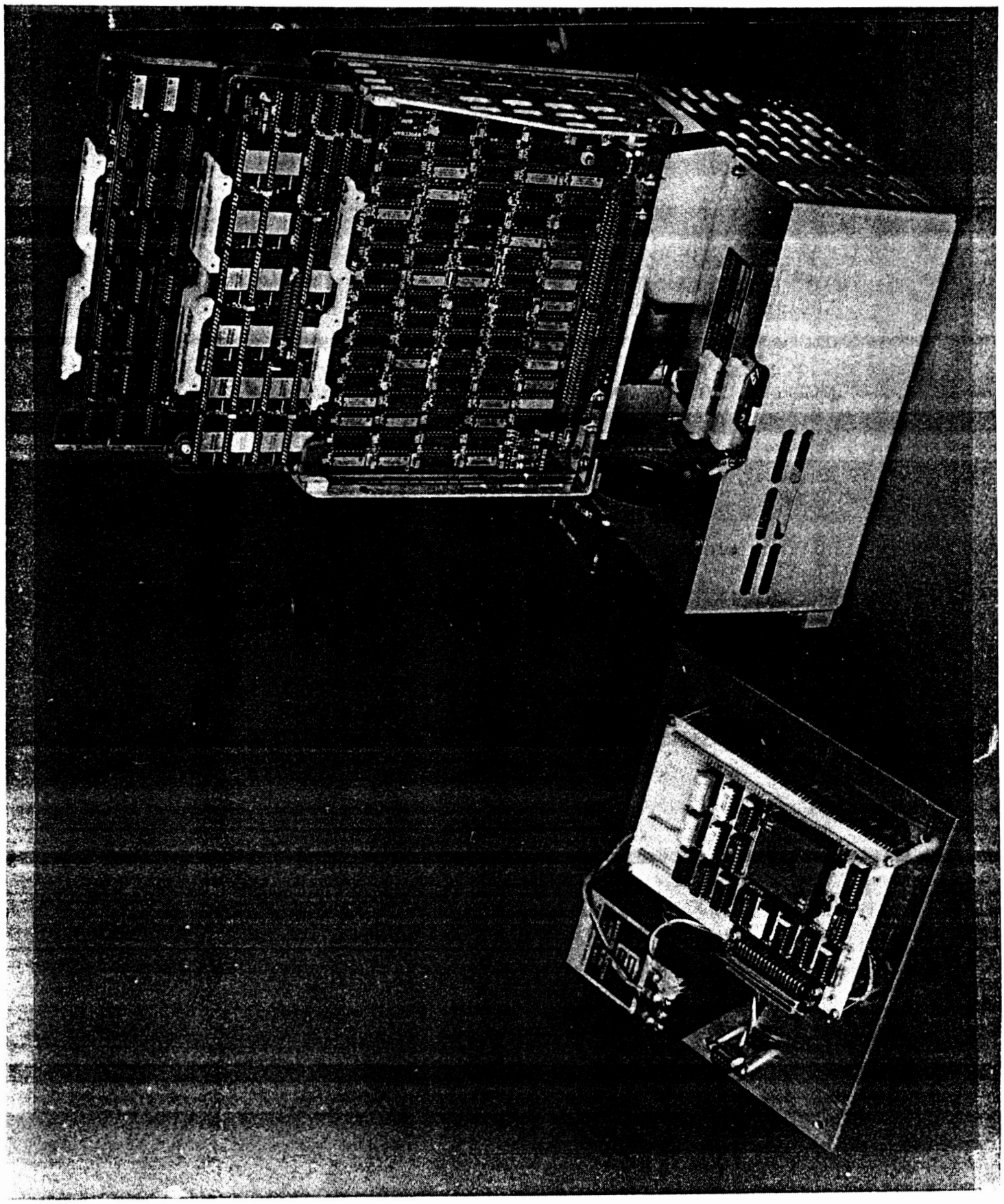

Figure 3.2.2 Four Card Viterbi Decoder and LSI Equivalent

APPENDIX A
POC MODEL TEST PLAN
POC MODEL TEST PROCEDURE
POC MODEL TEST DATA SHEETS

POC MODEL TEST PLAN AND PROCEDURE

FOR THE

NASA AMTD POC MODEL DEMODULATOR

PART OF TASK V SOW REQUIREMENT

prepared for

NASA Lewis Research Center

Contract number NAS3-24681

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1.0 INTRODUCTION

1.1 Scope

This document establishes the test requirements and describes the Proof-of-Concept (POC) Model Test Procedure used to test the POC Model demodulator developed for NASA Lewis Research Center on the Harris Study entitled *Advanced Modulation Technology Development for Earth Station Demodulator Applications.*

1.2 Description of Unit Under Test (UUT)

The UUT is the POC model demodulator which is comprised of the Demodulator chassis and the Demodulator Power Supply chassis. The Demodulator chassis contains the RF and digital circuits that transform the 3.373 GHz 16-ary CPFSK RF waveform to digital burst data. The Demodulator Power Supply chassis houses the DC power supplies that provide power to the Demodulator chassis. The chassis are standard Zero enclosures.

1.3 Applicable Documents

- POC Model Top Level Test Plan
- Contract NAS3-24681 Statement of Work (SOW)
- POC Model Performance Specification, Rev. A, November 1986

1.4 Test Equipment Required*

1.4.1 Special Test Equipment (STE)

The following Special Test Equipment has been developed on this contract for the purpose of providing the necessary and sufficient test and simulation capability for verification of POC model demodulator performance. This equipment was designed for operation in a laboratory environment. This POC model test procedure contains the Acceptance Test Procedures (ATPs) for the STE which are required to validate their performance prior to initiating the POC model test on the demodulator.

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* Equivalent equipment may be used.

Name

Continuous Phase Frequency Shift Keying Modulator No. 1
Continuous Phase Frequency Shift Keying Modulator No. 2
Signal Combiner Chassis

1.4.2 Commercially Available Standard Test Equipment

Name	Manufacturer	Model
Data Generator	Hewlett Packard	3760A
Error Detector	Hewlett Packard	3761A
Data Error Analyzer	Hewlett Packard	1645A
Synthesized Signal Generator	Hewlett Packard	8660C
Synthesized Signal Generator	Hewlett Packard	8662A
Synthesized Signal Generator	Hewlett Packard	8672A
Spectrum Analyzer	Hewlett Packard	8566
Oscilloscope	Tektronix	485

1.4.3 Cables

Test cables include those required to connect the UUT to the STE plus additional support cables for interconnections between the commercially available standard test equipment and the STE. An interconnect diagram which shows the cables required for testing is shown in figure 1.4.3.

1.5 Failure Recovery

In all cases, it is important for the test operator to record the observed anomaly and all events and conditions pertinent to the failure.

It is extremely important that the test operator carefully document the existing conditions, the state of the STE, and UUT BEFORE taking steps to determine the cause of the test failure.

If the cause of the failure of a given test or subtest is not immediately obvious, the test operator will repeat the test or subtest to determine if a recurring fault is present. If such a recurring fault is present, the test operator will initiate procedures to isolate the cause of the fault, especially to distinguish between faults attributed to the UUT versus other causes. If the UUT passes the retest, the test operator may (with concurrance from QC) elect to continue the test.

When recurring test failures are observed, the test will be halted, the UUT repaired (or adjusted), and the test will be restarted. At the time the test is restarted, the test operator, with the concurrence of the cognizant QC representative, will determine which of the tests or subtests previously completed must be scrapped and reaccomplished with the repaired UUT. This determination will be made based on the nature of the fault and the circuitry repaired or adjusted in the UUT.

In all cases where the UUT is repaired or readjusted, the activities will be documented per applicable QC standard procedures.

2.0 POC MODEL TEST PLAN

The purpose of the POC Model Test is to characterize the performance of the POC model demodulator with respect to design requirements outlined in the contractual SOW and various design goals established during the early phases of the program and defined in the POC Model Performance Specification, Rev. A, November 1986. Table 2.0 is a test requirements matrix which lists the various requirements and provides a cross reference from the SOW to other documents. The purpose of the POC Model Test is to validate those requirements listed in table 2.0 which are verifiable by testing. Analysis is provided for those requirements which are not practical to test.

The test plan is organized in the same order that testing will occur. First an acceptance test is performed on the Signal Combiner Chassis and the CPFSK Modulators. The STE must pass acceptance test criteria in order to provide the proper test environment for formal POC model demodulator testing.

2.1 Signal Combiner Chassis Test Plan

The Signal Combiner Chassis receives continuous low rate data from an external data generator, buffers it, and outputs a burst of data at the required 200 Mbps data rate for as many as three CPFSK demodulators. Along with the 200 Mbps bursted data, it provides a 200 MHz clock and a burst command which goes high while data is valid. It provides a test profile switch which is used to select test options for combinations of the modulator outputs. It also contains an internal noise source which is summed with the modulator outputs to produce the composite IF test signal for the demodulator. It receives demodulated 200 Mbps bursted data from the demodulator, buffers it, and outputs continuous low rate

REQUIREMENT	SOW PAR NO	SPEC PAR NO	TEST PLAN NO	METHOD
Min bandwidth efficiency = 2/b/s/Hz	3.2.2(a)	2.1.1(b)	2.2.3	Test/Modulator
Eb/No < 2 dB from theory at BER = 5*10E-7	3.2.2(b)	2.1.1(f)	2.3.6	Test/Demodulator
BER met over 10 dB dynamic range	3.2.2(c)	2.1.1(g)	2.3.7	Test/Demodulator
Max time to acquire sync < 200 bit times	3.2.2(d)	2.1.1(h)	2.3.8	Test/Demodulator
Max prob of acquisition failure < 10E-8	3.2.2(d)	2.1.1(h)	2.3.4, 2.3.5	Analysis
Unique word length < 20 bit times	3.2.2(e)	2.1.1(i)	2.2.1.3	Test/Modulator
Adjacent channel interference < 1 dB, eq pwr	3.2.2(f)	2.1.1(d)	2.3.11	Test/Demodulator
Co-channel interference < 1 dB, S/I = 20 dB	3.2.2(g)	2.1.1(d)	2.3.10	Test/Demodulator
10 nsec min guard time between bursts	3.2.2(h)	2.1.1(j)	2.1.3.2	Test/Signal Combiner
Min burst duty cycle = 1 burst/msec	3.2.2(i)	2.1.1(j)	2.1.2, 2.2.1.2	Test/Sig Comb, Mod
Max burst rate instability = +/-5*10E-7	3.2.2(j)	2.1.1(k)		Analysis
Min mean time to cycle slip	3.2.2(k)	2.1.1(l)		Analysis
Min data portion of burst = preamble	3.2.2(l)	Ap 4,2.4.3(f)	2.2.1.1	Test/Modulator
Ability to demodulate successive bursts	3.2.1(d)	2.1.1(e)	2.3.9	Test/Demodulator
Real time indication of start of valid data	3.2.1(e)	Ap 4,2.4.3(e)	2.3.3	Test/Demodulator
Demodulator interfaces at ECL levels	3.2.1(g)	Ap 4,2.4.3(e)		Test/Demodulator

Table 2.0 POC Model Test Requirements Matrix

data to an external bit error rate counter.

2.1.1 200 Mpbs Data Wrap Around Test

Much of the Signal Combiner circuitry can be verified by this straightforward test. Normally the 200 Mbps data produced by the Signal Combiner is routed to the Modulator, modulated onto the 3.373 GHz IF carrier, routed to the POC Model Demodulator, CPFSK demodulated, and routed back to the Signal Combiner. This normal configuration is shown in figure 2.1.1. This is the standard test configuration for BER testing.

Each of the three modulator data outputs can be individually connected directly to the receive data inputs. The data compared at the bit error rate counter to the PN sequence generated by the data generator will be verified to contain no errors. This one test verifies much of the buffering and data handling operations performed internally by the Signal Combiner. Figure 2.1.1 also shows this test configuration which wraps the modulator data, clock, and, burst command outputs back into the receive data, receive clock, and unique word detect inputs.

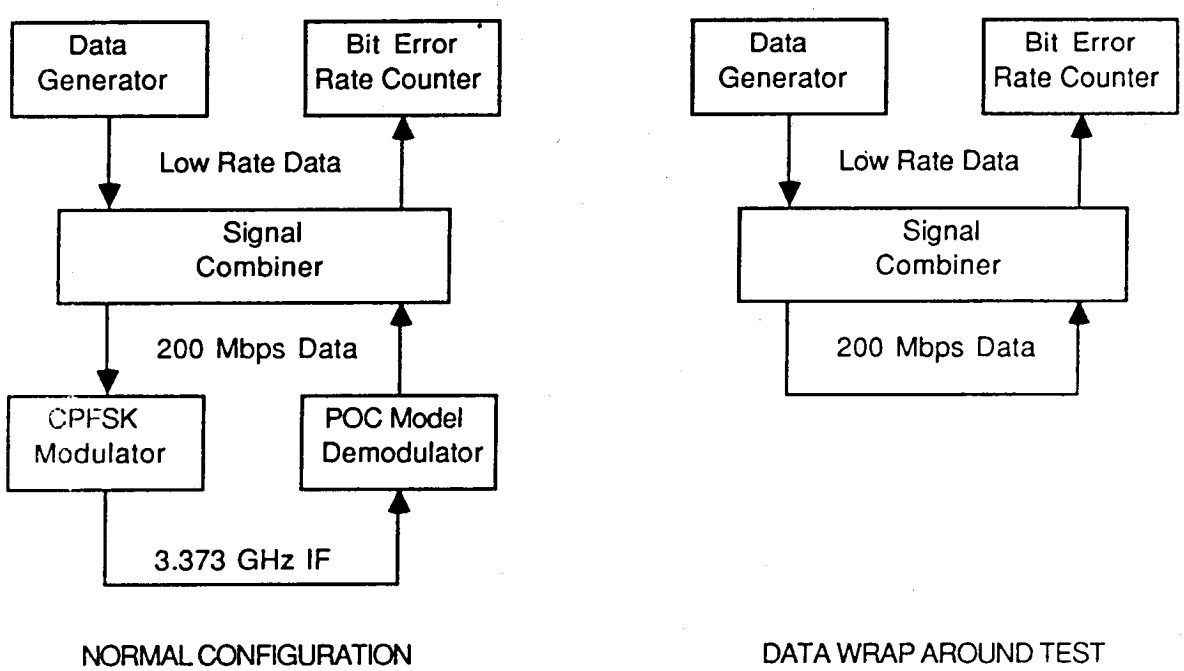


Figure 2.1.1 200 Mbps Data Wrap Around Test Configuraton

During the 200 Mbps Data Wrap Around Test, the ACQ FAILURE lamp will be observed to remain extinguished. The acquisition failure circuits that drive this lamp look for a unique word detect (UWDET) pulse back from the demodulator for every burst command (BURST) generated by

the Signal Combiner. If it misses one, the ACQ FAILURE lamp is illuminated. In the test configuration shown if Figure 2.1.1, these signals are directly connected to prevent the acquisition failure circuits from illuminating the lamp. This function will be tested by disconnecting the wrap around cable while still in the wrap around test configuration. Illumination of the lamp will be verified. The cable will then be reconnected and the action of pressing the START button will be observed to extinguish the lamp.

2.1.2 Signal Combiner Data Length Test

The Signal Combiner provides a selection of three different length data messages per burst: 170 bits, 3,734 bits, and 11,258 bits. Each of the modulator data outputs will be verified to produce the three message lengths by measuring the time interval of the burst command signal and observing the data and clock signals for each modulator output. The burst duty cyle will also be measured to verify compliance with SOW requirement 3.2.2(i) for a 1 burst per msec minimum burst duty cycle.

2.1.3 Test Profile Switch Function Test

The Test Profile Switch has two positions and controls how many bursts per frame are used and whether the incoming PN data is separated into unique data streams or all PN bits sent to all modulators. When the Test Profile Switch is in the 1 position, the desired signal at the demodulator has one burst per frame. Interfering baseband data messages are produced in this mode with overlapping burst commands for co-channel and adjacent channel testing. When the Test Profile Switch is in the MULT position, the demodulator sees the desired signal as two staggered bursts per frame.

2.1.3.1 Overlapping Burst Command Test

The purpose of the Co-channel Interferer Test is to measure the BER performance degradation with an interferer which occupies the same time slot and frequency band but is 20 dB below the desired signal. Therefore the burst commands produced by the Signal Combiner should overlap as shown in figure 2.1.3. The burst command signals from each of the modulator data outputs will be simultaneously compared to verify the overlap.

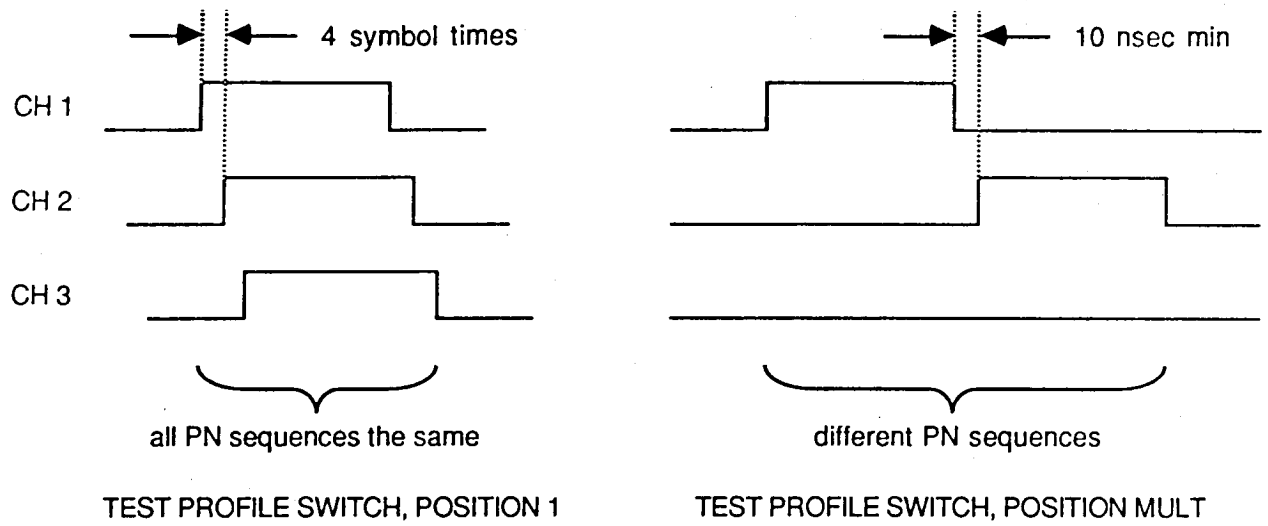


Figure 2.1.3 Burst Commands VS Test Profile Switch Position

The purpose of the Adjacent Channel Interferer Test is to measure the BER performance degradation with an interferer which occupies the same time slot and an adjacent band one half bit rate away in frequency. This is done with the interferer power equal to the desired signal power. In the Adjacent Channel Interferer Test, the burst commands produced by the Signal Combiner should have the same relationship as in the Co-channel Interferer Test. In both cases the PN sequences are the same for each of the modulator data outputs, but offset in time by four symbol periods, or 13.75 nsec. This data relationship will also be visually verified.

2.1.3.2 Staggered Burst Command Test

In the Independent User Test, consecutive messages per TDM frame are transmitted from independent sources, separated by a minimum guard time of 10 nsec. The Independent User Test demonstrates the ability of the demodulator to fully acquire consecutive independent users in one TDM frame. It is also indicates the sensitivity of the demodulator bit synchronizer to asynchronous symbol clock relationships. In the Staggered Burst Command Test, the burst commands produced by the Signal Combiner should be separated by a minimum guard time of 10 nsec as shown in figure 2.1.3. Different PN sequences for each message should also be produced. The Signal Combiner generates the different PN sequences by doubling the data generator data rate and demultiplexing the incoming PN sequence into unique sequences for each modulator. The burst command signals from each of the modulator data outputs will be simultaneously compared to verify the staggered relationship. The guard time between

successive bursts will be measured to verify compliance with the 10 nsec minimum guard time requirement of SOW 3.2.2(h). The data outputs will also be compared to verify that the messages are not the same.

2.1.4 RF Output Test

The Signal Combiner contains an internal noise source which is summed with the modulator outputs to produce the composite IF test signal for the demodulator. The maximum noise spectral density at IF will be measured and the noise output flatness will be determined. The gain through each of the modulator channels will also be measured for a 3.373 GHz CW input at -30 dBm.

2.1.4.1 Noise Spectral Density Determination

The objective of this test is to assess the noise spectral density, No, about the 3.373 GHz IF, at the output of the Signal Combiner. This test is performed with the noise source on at its highest power level and all modulators off. The first measurement is in the form of an observation. The signal combiner output will be observed on an oscilloscope. The oscilloscope should reveal a bandlimited waveform with no DC component and no noticeable clipping of the waveform. Noise flatness will be determined by observing the Signal Combiner output on a spectrum analyzer at a low video bandwidth. The noise power should be flat within $\pm$ 1 dB over a 400 MHz bandwidth centered at 3.373 GHz. N_0, or the noise spectral density measured about the IF will be determined by utilizing a feature of the spectrum analyzer which allows the rms noise level to be read out normalized to a 1 Hz noise power bandwidth. The spectrum analyzer accurately correctes the noise level measurement readout for its log amplifier and detector response and normalizes the value to a 1 Hz bandwidth. The measurement is made by centering the spectrum analyzer marker at the average noise power level within the 400 MHz bandwidth and invoking the noise level measurement feature.

2.1.4.2 RF Output Power

With the noise source disconnected, a CW 3.373 GHz signal from an external frequency synthesizer will be connected to each of the modulator IF inputs and the power level at the summed output measured. With a -30 dBm power level at each of the modulator inputs, the output power level at the SUMOUT connector should be 0 dBm.

2.2 Modulator Test Plan

A fully functional Signal Combiner Chassis, which has passed its ATP, is required to perform the ATP on the Modulator. Several SOW design requirements are verified indirectly by observing that the waveforms produced by the STE are within specified limits.

2.2.1 Baseband Data Test

The Modulator receives 200 Mbps bursted serial NRZ data from the Signal Combiner Chassis and demultiplexes it into three parallel bit streams. Every third bit in is rate one half convolutionally encoded, resulting in a 4 parallel bit symbol. Normally every three serial data bits in are used to produce a 4 parallel bit symbol. Every fourth symbol, however, is used for tracking and is derived by taking two data bits in and assigning them as the MSB and NSB of the symbol as usual. The difference is that the third data bit in is not clocked into the encoder, which is frozen. Instead, two zeros are appended as LSBs to the MSB and NSB to form the tracking symbol. Therefore, for three consecutive trios of incoming bits a symbol is formed. Every fourth symbol is formed from two incoming bits. The ratio of incoming bits to symbols is therefore 11/4. This relationship holds true for all of the data bits except for the last 16 bits in the message.

Eight consecutive zeros are clocked into the encoder for the last eight symbols in the message in order to flush the encoder or force it to terminate in an all zeros state. Two incoming serial data bits are assigned as the MSB and NSB of the symbol as usual. Instead of clocking the third data bit in the sequence into the encoder, a zero is substituted for it and clocked in instead. This process continues for the last 16 bits in, or the last eight symbols out. The ratio of incoming bits to symbols for the last 8 symbols is therefore 16/8 or 2/1.

The Modulator also generates and affixes the preamble and unique word symbols in front of the data message.

2.2.1.1 Minimum Length Message Test

The Modulator provides a data length message selector which has to match the data length selected at the Signal Combiner for one of three different length data messages per burst. The minimum length message is 170 bits long or (170-16)*4/11 + 16*1/2 (Termination Sequence) = 64 symbols. The requirement that the data portion of the minimum length message in a burst be equal in length to the preamble

portion of the burst will be verified by observing the output of an amplifier past the D/A converter and Nyquist filter, but before the VCO. The preamble, which consists of a 32 symbol long alternating f_0, f_{15} pattern followed by 32 consecutive f_0 symbols, can be clearly observed, followed by the 6 symbol long unique word. The termination sequence is derived from the last 16 message bits in and is therefore part of the data message. The relationships of the preamble, unique word, and data message are depicted in Figure 2.2.1. The number of preamble symbols will be counted and compared to the data message symbols. This test, in conjunction with the POC demodulator test verifies SOW requirement 3.2.2(l).

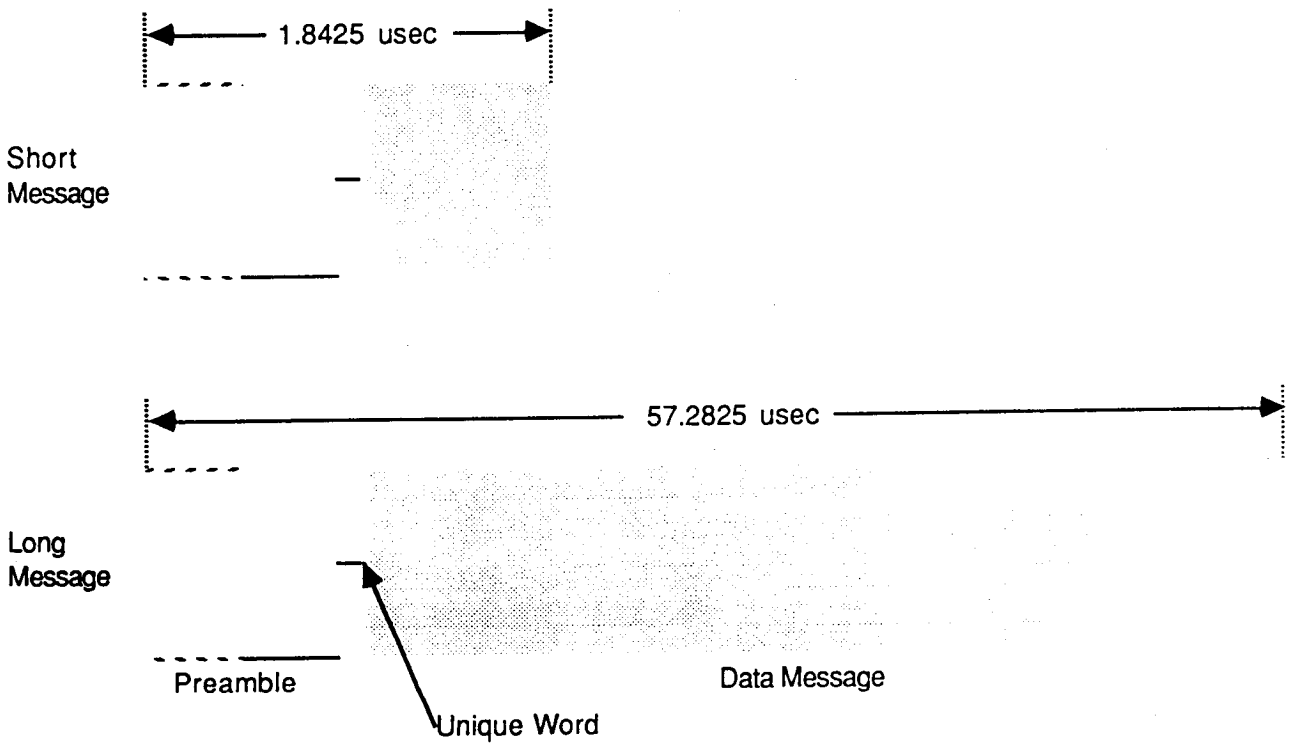


Figure 2.2.1 Burst Structure at Modulator D/A Output

2.2.1.2 <u>Modulator Data Length Test</u>

There are three possible message lengths which are selectable by the burst data length switch on the front panel: 170 bits, 3,734 bits, and 11,258 bits. Although this test was previously performed on the Signal Combiner, it is necessary to reverify the data lengths and burst duty cycle. The Modulator reclocks the incoming bit stream with an asynchronous symbol clock and creates a symbol stream complete with preamble and unique word. The burst duty cycle will also be measured to verify compliance with SOW requirement 3.2.2(i) for a 1 burst per msec

minimum burst duty cycle.

2.2.1.3 Unique Word Length Test

Using the same test configuration, the requirement that the unique word length be less than 20 bit times will also be verified. With random data furnished from the data generator, the unique word is easily distinguished from the preamble and the data message by observing multiple bursts of data. The number of unique word symbols will be counted, which is by design, six. Since 6s*11b/4s = 16.5 bits, it is obvious that SOW requirement 3.2.2(e) is met.

2.2.1.4 Unique Word Pattern Test

The format of the unique word generated by the Modulator must match one of four possible addresses which the POC Model Demodulator is designed to recognize. Both modulators must also have the same unique word in order to perform the successive bursts per frame test. The fixed unique word pattern generated by the modulator will be verified to be f_8 f_8 f_0 f_8 f_0 f_8.

2.2.3 Modulated Spectra Test

In this test, the spectra of the modulator output will be observed, recorded, and compared to the predicted spectra. The objective of this test is to verify that the modulator output spectral characteristics are such that SOW requirement 3.2.2(a) for a minimum bandwidth efficiency of 2 b/s/Hz is met.

The output of the Modulator will be observed on a spectrum analyzer and plotted on a sheet of paper. A mask printed on a transparent overlay will be placed over the plotter output and compared against the Modulator output spectra. The modulated spectra will be verified to fall within the mask limits, as shown in Figure 2.2.3. If the entire burst were comprised of random data, the resulting spectra would fall totally within the mask. Since each burst contains a non-random preamble containing an alternating f_0 f_{15} pattern, associated spectral components occur every 36.36 MHz (the fundamental frequency of the f_0 f_{15} pattern), or 1/2 symbol rate away from the center frequency. Due to the dominance of the f_0 tone in the preamble, its associated spectral component is also visible in the modulator output spectra. It is located 34.09 MHz or 1/2*15/16 symbol rate to the right of the 3.373 GHz center frequency. Due to the non-random nature of the preamble it is permissible for the preamble spectral

components to break the mask limits, as illustrated in Figure 2.2.3.

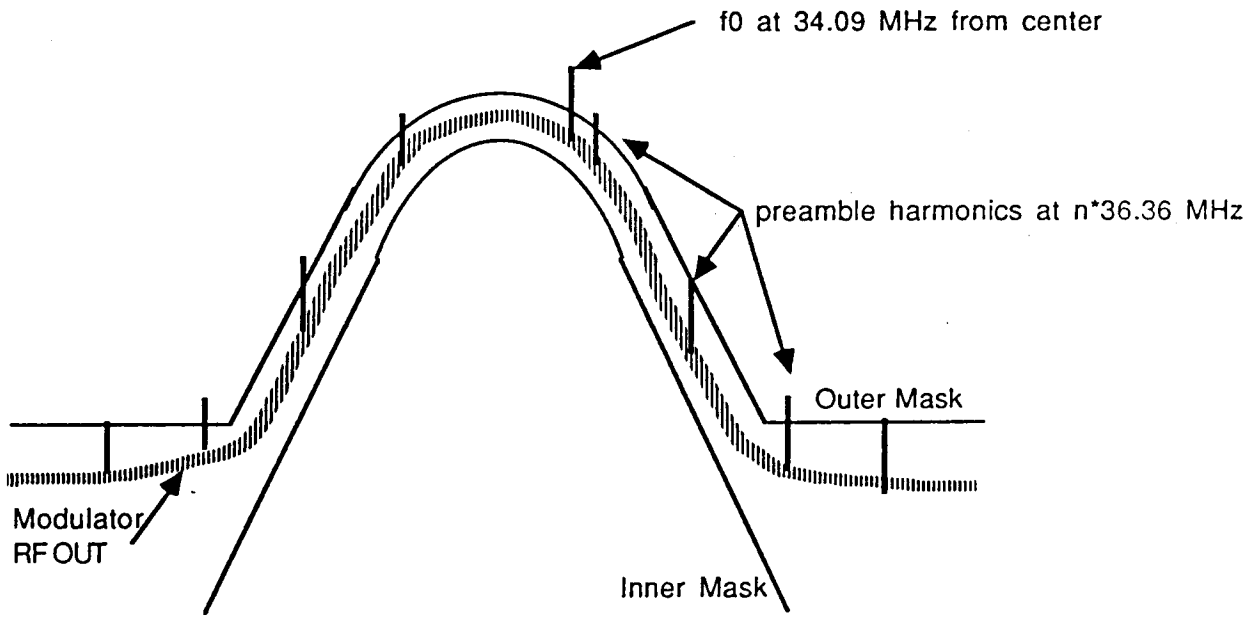


Figure 2.2.3 16-ary CPFSK Modulator Output Spectra

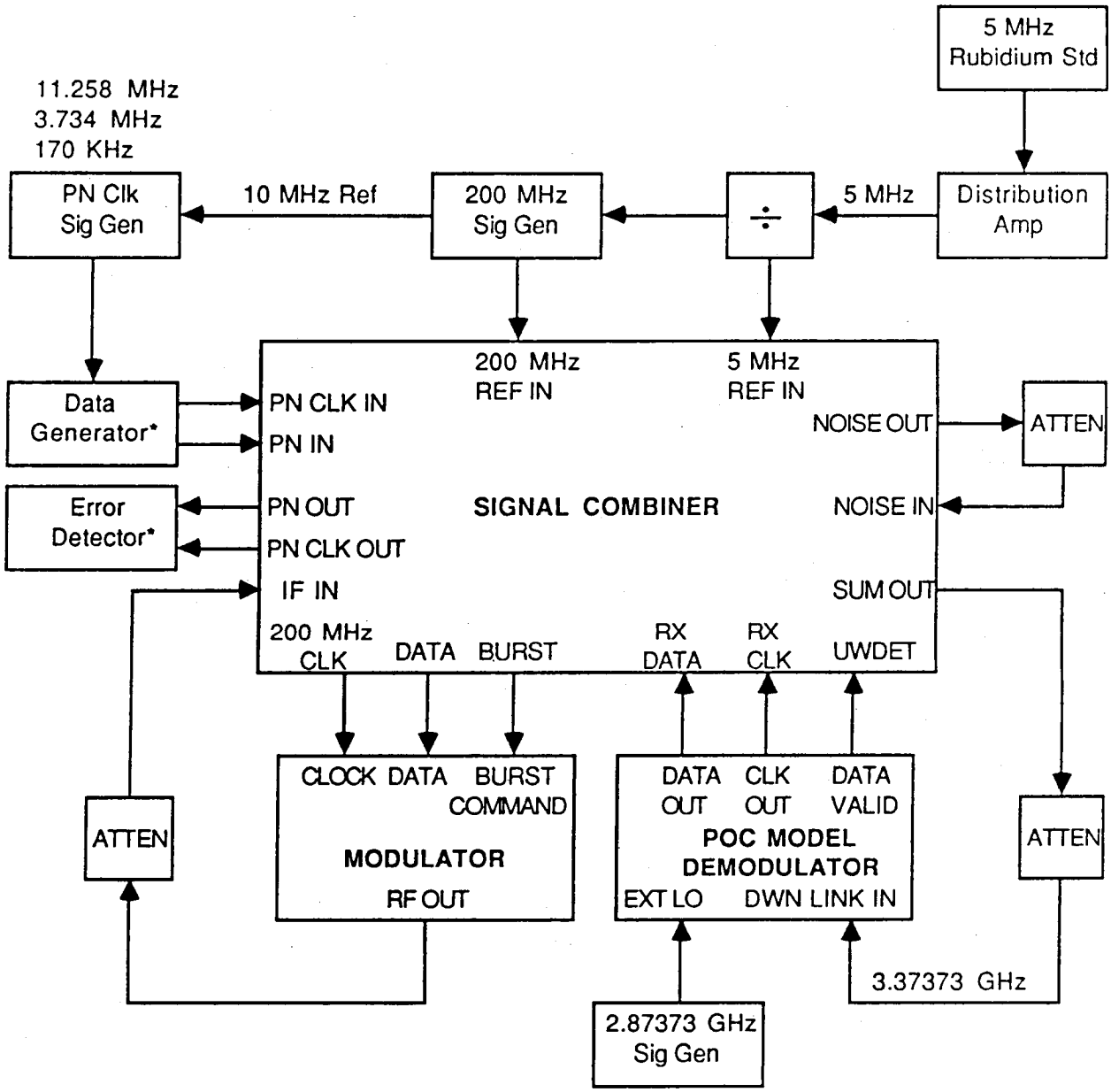
2.3 POC Model Demodulator Test Plan

This section describes the plan for testing the POC Model Demodulator. The results of this testing will be published and analyzed in the Task VII POC Model Test Report. The POC Model Test configuration is shown in Figure 2.3.

2.3.1 Eb/No Calibration

This section describes the calibration of E_b/N_o and as such is not, by strict definition, a test. The maximum noise spectral density of the Signal Combiner was determined and recorded as part of its ATP. The Modulator has been designed such that when no baseband data is supplied to the input, a single tone (carrier) output will result, if it is active. The carrier power will be measured using a spectrum analyzer at the output of the Signal Combiner, with the noise source off and only one modulator active. Using an external attenuator, the carrier power will be adjusted to the nominal value of 0 dBm. Once the nominal carrier power has been set to 0 dBm, the noise power will be attenuated to achieve a given E_b/N_o. From equation (2), the N_o required for a given E_b/N_o may be determined. Equation (3) gives the amount of noise attenuation necessary to achieve the E_b/N_o, given the maximum noise spectral density previously recorded.

$$N_o, \text{ dBm/Hz} = C, \text{ dBm} - E_b/N_o, \text{ dB} - 10\log(R_b) \quad (2)$$



* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 2.3 POC Model Test Configuration

$$\text{Noise attenuation} = N_o, \text{ maximum} - N_o, \text{ desired} \quad (3)$$

In our system the data rate, R_b is 200 Mbps. For example, to achieve an E_b/N_o of 12 dB, with a carrier power of 0 dBm, a noise spectral density of

$N_o = 0 - 12 - 10\log(200*10^6) = -95$ dBm/Hz is necessary. Thus, if the maximum noise spectral density is -78 dBm/Hz, the noise source should be attenuated by:

Noise attenuation = -78 - (-95) = 17 dB

2.3.2 Connectivity Test

In this test the demodulator is tested in the absence of external noise. This characterizes the performance of the demodulator and verifies the integrity of the test setup. This test is performed with the IF power set and held at a nominal level and with only one modulator active. The long message (12,408 bits) will be selected. The error rate achieved in this configuration will be recorded.

2.3.3 Valid Data Test

SOW subparagraph 3.2.1(e) requires the POC Model Demodulator to produce a real time indication of start of valid data. In this test the DATA VALID output is connected to one channel of a dual channel oscilloscope and the timing compared against DATA OUT and CLK OUT. The data bits and clocks are then verified to fall within the DATA VALID pulse. The test configuration is the same as used in the Connectivity Test and the long message (12,408 bits) will be selected. The duration of DATA VALID, DATA OUT, and CLK OUT will be recorded.

2.3.4 Acquisition Test

During POC Model Demodulator testing the ACQ FAILURE lamp on the Signal Combiner will be monitored. Any acquisition failures that occur during POC model testing will be recorded along with the relevant test equipment settings such as carrier power level and noise attenuation. Since it is statistically unlikely that meaningful acquistion performance data can be obtained during testing, the following acquistion failure rate analysis is provided.

2.3.5 Acquisition Analysis

SOW subparagraph 3.2.2(d) requires a probability of acquistion failure of less than 10^{-8}.

2.3.6 BER Baseline Test

In this test the demodulator is tested in the presence of

external noise. The relationship of carrier power to noise attenuation will be varied to produce a set of data points for E_b/N_o versus error rate. The resulting information will be plotted on a BER curve which shows the relationship of the measured data to the theoretical QPSK performance curve. Figure 2.3.5 shows an error rate curve for theoretical QPSK versus the predicted performance curve for our system which was published in the Task I Report. The performance requirements from SOW subparagraph 3.2.2(b) and POC Model Performance Specification, Rev. A, paragraph 2.1.1(f) are such that the P_e should be less than $5*10^{-7}$ at an E_b/N_o of 13.5 dB. This test will be performed with only one modulator active and the long message (12,408 bits) selected. The error rate achieved in this configuration will be recorded.

2.3.7 IF Power Level Variation Test

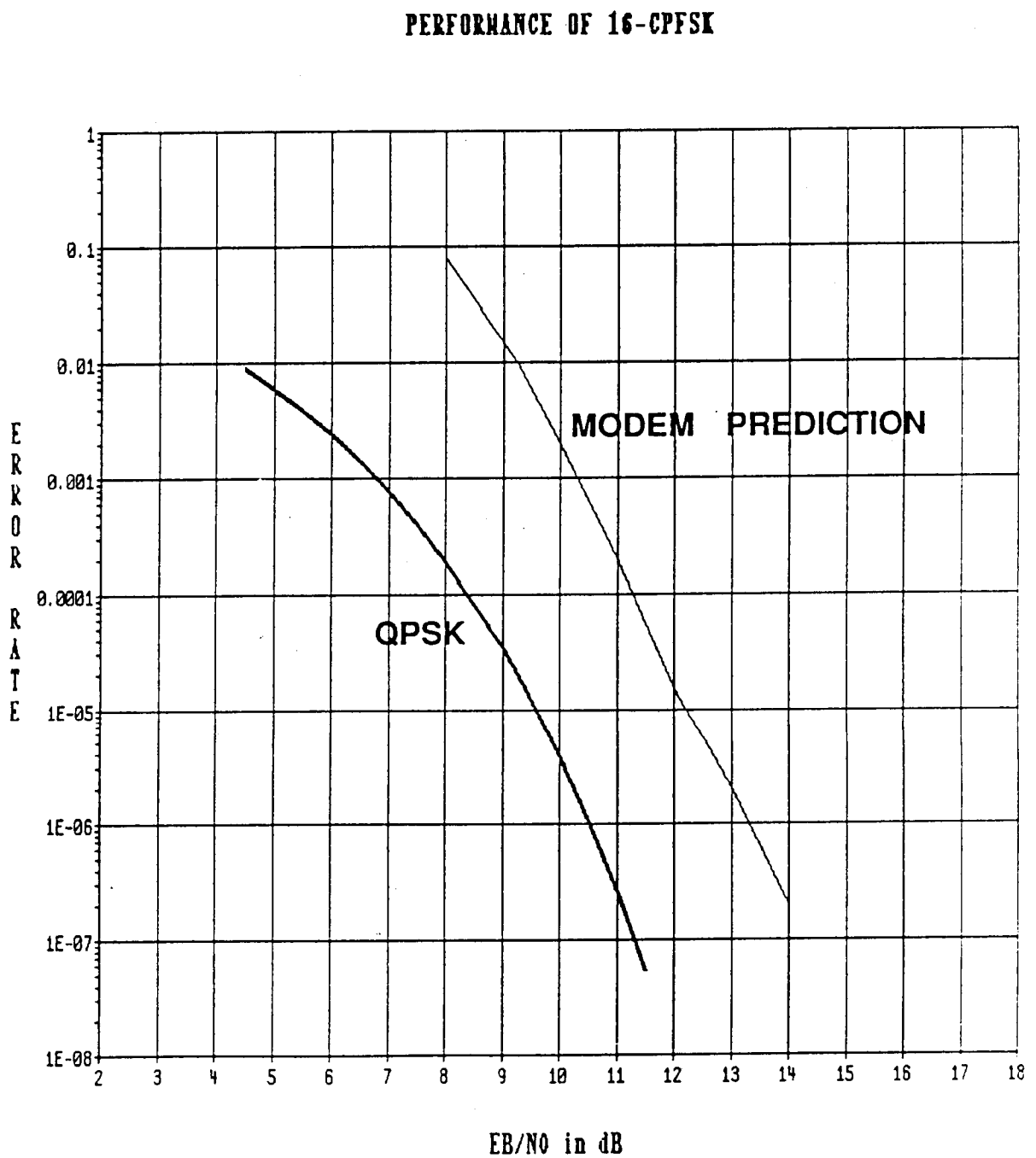
This test is similar to the BER Baseline Test except that demodulator BER performance is measured at both higher and lower than nominal IF power levels. This test statically exercises the IF limiting stage, which is required by SOW subparaph 3.2.2(c) to operate over a 10 dB dynamic range, or $\pm$ 5 dB from nominal. The actual operational effects of dynamic range on BER performance will be determined by varying the total IF power and plotting demodulator BER performance at an error rate of $5*10^{-7}$. This test will be performed with only one modulator active and the long message (12,408 bits) selected.

2.3.8 POC Model Demodulator Data Length Test

In this test, the length of the data message is varied to assess the demodulator's sensitivity to message length. Demodulator BER performance at an error rate of $5*10^{-7}$ is measured as a function of data message length while holding E_b/N_o constant. This test will determine the extent to which the demodulator has fully acquired initial phase and AGC setting by the end of the preamble. SOW subparagraph 3.2.2(d) requires a maximum time to acquire synchronization of less than 100 information bit times, or 36.36 symbol times. Harris requested and received permission to increase the maximum time to acquire synchronization from 36.36 symbol times to 64 symbol times (880 nsec). This change is reflected in the POC Model Performance Specification, Rev. A, paragraph 2.1.1(h). In our design the first 32 alternating f_0, f_{15} symbols of the preamble are used to achieve symbol synchronization and burst detect. This information is used to train the bit sync over the last 32 symbols. The last 32 all f_0 symbols are used for carrier acquisition during which time the DC restore and AGC loops track out any offsets so that the phase accumulator ends up

MODEM ERROR RATE PERFORMANCE

The figure shows the Bit Error Rate Performance predicted for the Harris TDMA Modem compared to QPSK performance.



with the correct value for f_0, prior to the start of unique word. If the maximum time to acquire synchronization requirement is not met, the demodulator will make errors early in the message and the error rate will go up as message length is decreased. If the error rate performance stays constant for all three possible message lengths, then the maximum time to acquire synchronization requirement has been met.

2.3.9 Independent User Test

In this test, two consecutive bursts separated by a minimum guard time of 10 nsec are transmitted per TDM frame. This test verifies compliance with the requirement to demodulate successive bursts per frame from independent users (SOW subparagraph 3.2.1(d)). It will also indicate any demodulator sensitivity to bit sync acquisition, since the modulators each have independent, asynchronous symbol clocks. IF power is allowed to vary up to ± 5 dB from nominal between independent sources. The medium length message (4,070 bits) is selected and the IF output frequency is set to 3.373 GHz for both modulators.

2.3.10 Co-channel Interference Test

The purpose of the Co-channel Interference Test is to measure the BER performance degradation with an interferer which occupies the same time slot and frequency band but is 20 dB below the desired signal. In the Co-channel Interference Test, the burst commands overlap as shown in Figure 2.1.3. In both cases the PN sequences are the same for each of the modulator data outputs, but offset in time by four symbol periods, or 13.75 nsec. This test verifies compliance with SOW requirement 3.2.2(g). The long message length (12,408 bits) is selected and the IF output frequency is set to 3.373 GHz for both modulators. The desired signal power level will be set to nominal and the interfering signal power level will be adjusted to achieve an error rate of $5*10^{-7}$. The power level of each modulator output will be recorded.

2.3.11 Adjacent Channel Interference Test

The purpose of the Adjacent Channel Interferer Test is to measure the BER performance degradation with an interferer which occupies the same time slot and an adjacent band one half bit rate away in frequency. This is done with the interferer power equal to the desired signal power. In the Adjacent Channel Interference Test, the burst commands overlap as shown in Figure 2.1.3. In both cases the PN sequences are the same for each of the modulator data outputs, but offset in time by four symbol periods, or 13.75 nsec. The IF output frequency of

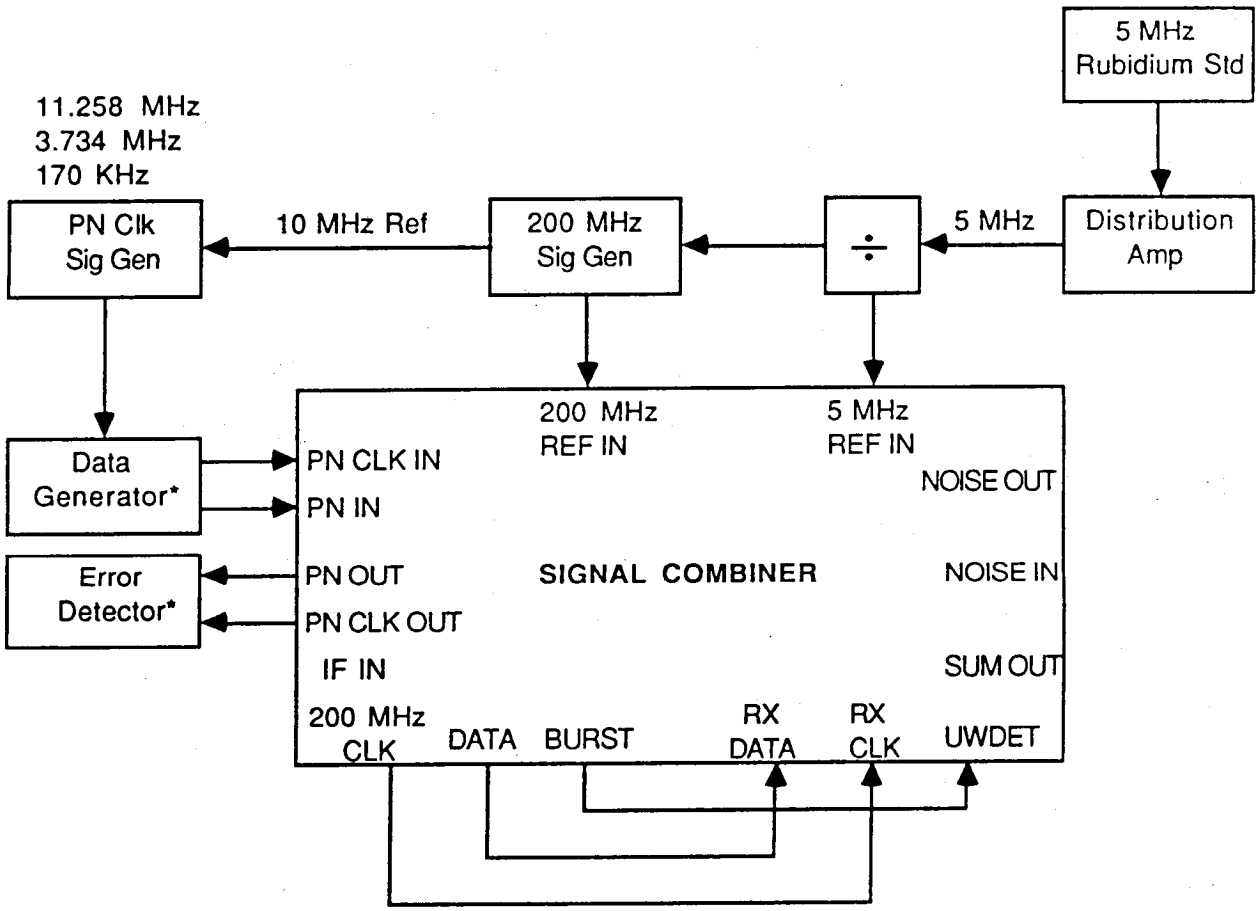
the modulator which produces the desired signal is set to 3.373 GHz and the interfering modulator is set 100 MHz away. This test verifies compliance with SOW requirement 3.2.2(f). IF power is set to the nominal level for each modulator and the long message length (12,408 bits) is used. The desired signal E_b/N_o required to achieve an error rate of $5*10^{-7}$ will be recorded.

3.0 POC MODEL TEST PROCEDURE

The POC Model Test Procedure provides an Acceptance Test Procedure (ATP) for each of the STE chassis and provides a POC Model Demodulator Test Procedure for executing the POC Model Test at the conclusion of Task VII. The purpose of these test procedures is to verify those requirements described in the POC Model Test Plan, Section 2.0, which are verifiable by testing. Analysis is provided in section 2.0 for those requirements which are not practical to test.

3.1 Signal Combiner Chassis Acceptance Test Procedure

Setup the test configuration for the Signal Combiner ATP as shown if Figure 3.1.



* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 3.1 Signal Combiner ATP Test Configuration

(a) Power the Equipment on with the cables disconnected. Allow 30 minutes for the signal generators to stabilize.
(b) Set the HP 8662A frequency to 200 MHz and the output level to 0.0 dBM.
(c) Set up the HP 3760A Data Generator and HP 3761A Error Detector as defined in Table 3.1.
(d) Set the HP 8660A frequency to 11.258 MHz and the output level to 0.9 V (+12.1 dBm, 50Ω).
(e) Connect the cables between equipment as shown.

Table 3.1 Error Detector and Data Generator Initial Settings

Error Detector

CLOCK INPUT FIELD:
- LEVEL = 0
- TRIGGER MODE = +AUTO
- RATE = 1.5 - 50 MBITS

DATA INPUT FIELD:
- PHASE = 0
- POLARITY = DATA
- PRBS LENGTH 2^N - 1 BITS = 8

DISPLAY FIELD:
- DISPLAY HOLD = MIN
- MODE = BER
- SYNC = AUTO
- INTERVAL 10^n CLOCK PERIODS = n - 5
- GATE = REP

Data Generator

CLOCK FIELD:
- TRIGGER MODE = AUTO
- RATE MBITS = EXT
- DATA DELAY ns = 0

CLOCK OUPUT FIELD:
- AMPLITUDE = 3.2 V
- VERNIER = MAX
- CLOCK/CLOCKN = CLOCKN
- DC OFFSET = +
- 0 TO 3V VERNIER = STRAIGHT UP

DATA FIELD:
- ADD ERROR
- PRBS LENGTH 2^N - 1 BITS
- WORD = 1010010100

DATA OUTPUT FIELD:
- DC OFFSET = +
- 0 TO 3 V VERNIER = 1:30
- RZ/NRZ = NRZ
- AMPLITUDE = 3.2 V
- VERNIER = MAX
- DATA/DATAN = DATA

(f) Connect the CHANNEL 1 200 MHZ CLK, DATA, and BURST outputs to the RX CLK, RX DATA, and UWDET inputs as shown.
(g) Place the DATA LENGTH switch on the Signal Combiner front panel in the L position.
(h) Place the TEST PROFILE switch on the Signal Combiner front panel in the 1 position.
(i) Record the following information in the Signal Combiner Chassis Acceptance Test Procedure Data Sheets, section 4.1:

- All test equipment serial numbers and cal due dates
- Test operator and QC initials certifying correct setup

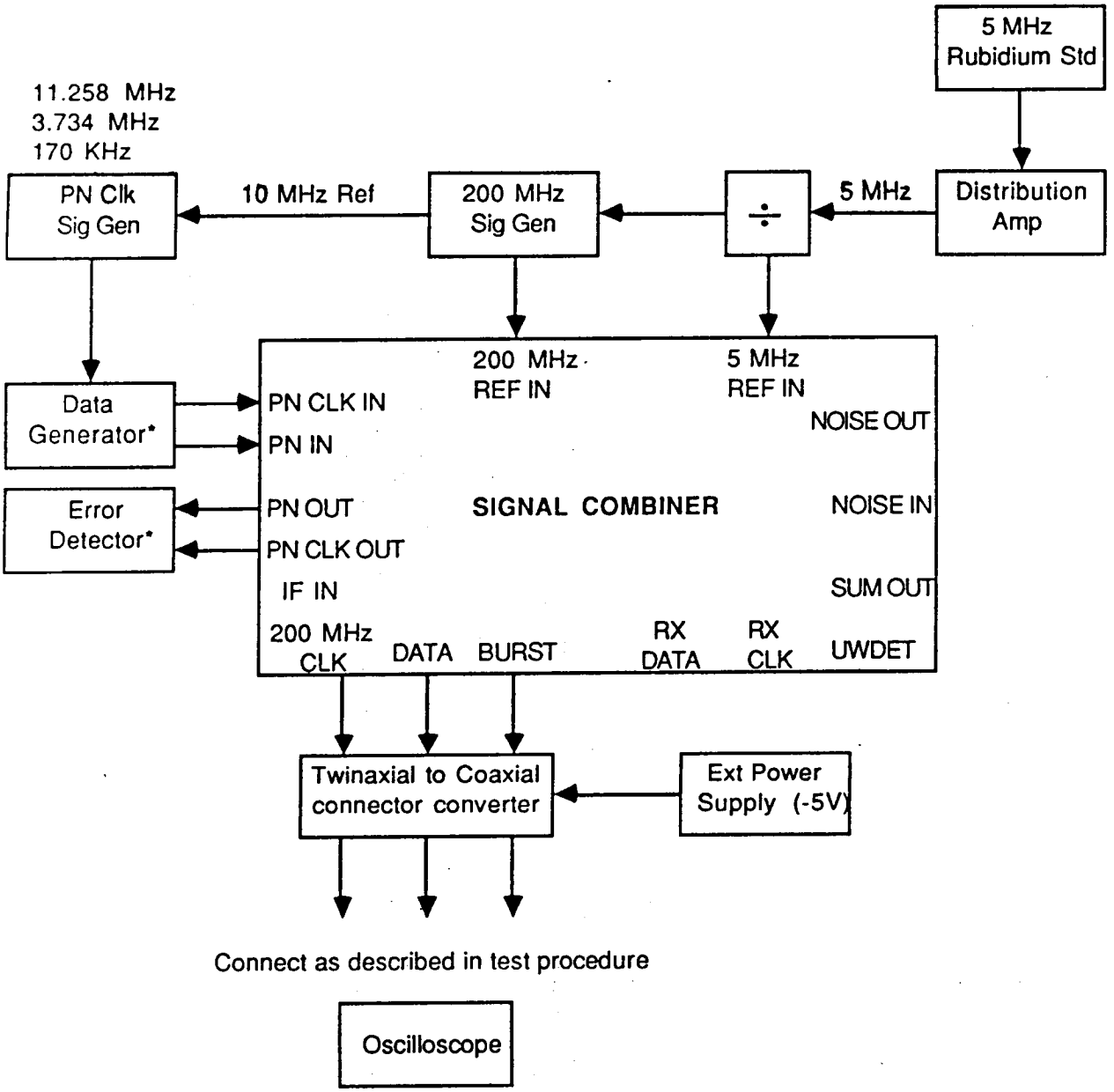
3.1.1 <u>200 Mbps Data Wrap Around Test</u>

(a) Press the RESET button on the front of the Signal Combiner.
(b) Verify that the ACQ FAILURE lamp is extinguished. The lamp should remain extinguished at all times while the wrap around cables are connected.
(c) Record the error rate displayed on the Error Detector. The error rate display should read $1.9 * 10^{-6}$.
(d) Disconnect the cable between the CHANNEL 1 BURST output and the UWDET input.
(e) Verify that the ACQ FAILURE lamp is illuminated.
(f) Reconnect the cable between the CHANNEL 1 BURST output and the UWDET input.
(g) Press the RESET button on the front of the Signal Combiner.
(h) Verify that the ACQ FAILURE lamp is extinguished.
(i) Disconnect the three cables from the CHANNEL 1 outputs and reconnect them to the CHANNEL 2 outputs.
(j) Press the RESET button on the front of the Signal Combiner.
(k) Verify that the ACQ FAILURE lamp is extinguished. The lamp should remain extinguished at all times while the wrap around cables are connected.
(l) Record the error rate displayed on the Data Error Analyzer. The error rate display should read $1.9 * 10^{-6}$.
(m) Disconnect the cable between the CHANNEL 2 BURST output and the UWDET input.
(n) Verify that the ACQ FAILURE lamp is illuminated.
(o) Reconnect the cable between the CHANNEL 2 BURST output and the UWDET input.
(p) Press the RESET button on the front of the Signal Combiner.
(q) Verify that the ACQ FAILURE lamp is extinguished.
(r) Disconnect the three cables from the CHANNEL 2 outputs and reconnect them to the CHANNEL 3 outputs.

(s) Press the RESET button on the front of the Signal Combiner.
(t) Verify that the ACQ FAILURE lamp is extinguished. The lamp should remain extinguished at all times while the wrap around cables are connected.
(u) Record the error rate displayed on the Data Error Analyzer. The error rate display should read $1.9 * 10^{-6}$.
(v) Disconnect the cable between the CHANNEL 3 BURST output and the UWDET input.
(w) Verify that the ACQ FAILURE lamp is illuminated.
(x) Reconnect the cable between the CHANNEL 3 BURST output and the UWDET input.
(y) Press the RESET button on the front of the Signal Combiner.
(z) Verify that the ACQ FAILURE lamp is extinguished.

3.1.2 Signal Combiner Data Length Test

(aa) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and trigger on the rising edge of the CH 1 input. Adjust the TIME/DIV to 10 usec/div. Adjust CH 1 VOLTS/DIV to 0.5 volts/div.
(ab) The time interval between the rising and falling edges of the BURST pulse should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(ac) Connect the CHANNEL 1 200 MHZ CLK to CH 2 of the oscilloscope and adjust CH 2 VOLTS/DIV to 0.5 volts/div.
(ad) The time duration of the 200 MHZ CLK should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(ae) Connect the CHANNEL 1 200 MHZ DATA to CH 2 of the oscilloscope.
(af) The time duration of the 200 MHZ DATA should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(ag) Connect the CHANNEL 2 BURST output to CH 1 of the oscilloscope.
(ah) The time interval between the rising and falling edges of the BURST pulse should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(ai) Connect the CHANNEL 2 200 MHZ CLK to CH 2 of the oscilloscope.



(Test Configuration for Data Length Test and Burst Command Tests)

* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 3.1.2 Test Configuration for Data Length and Burst Command Tests

(aj) The time duration of the 200 MHZ CLK should be approximately 5.6 divisions, or 56.29 ± 5 usec in duration. Record the time interval on the data sheet.

(ak) Connect the CHANNEL 2 200 MHZ DATA to CH 2 of the oscilloscope.

(al) The time duration of the 200 MHZ DATA should be approximately 5.6 divisions, or 56.29 ± 5 usec in duration. Record the time interval on the data sheet.
(am) Connect the CHANNEL 3 BURST output to CH 1 of the oscilloscope.
(an) The time interval between the rising and falling edges of the BURST pulse should be approximately 5.6 divisions, or 56.29 ± 5 usec in duration. Record the time interval on the data sheet.
(ao) Connect the CHANNEL 3 200 MHZ CLK to CH 2 of the oscilloscope.
(ap) The time duration of the 200 MHZ CLK should be approximately 5.6 divisions, or 56.29 ± 5 usec in duration. Record the time interval on the data sheet.
(aq) Connect the CHANNEL 3 200 MHZ DATA to CH 2 of the oscilloscope.
(ar) The time duration of the 200 MHZ DATA should be approximately 5.6 divisions, or 56.29 ± 5 usec in duration. Record the time interval on the data sheet.
(as) Set the HP 8660A frequency to 3.734 MHz and place the DATA LENGTH switch on the Signal Combiner front panel in the M position.
(at) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 2 usec/div.
(au) The time interval between the rising and falling edges of the BURST pulse should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(av) Connect the CHANNEL 1 200 MHZ CLK to CH 2 of the oscilloscope.
(aw) The time duration of the 200 MHZ CLK should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(ax) Connect the CHANNEL 1 200 MHZ DATA to CH 2 of the oscilloscope.
(ay) The time duration of the 200 MHZ DATA should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(az) Connect the CHANNEL 2 BURST output to CH 1 of the oscilloscope.
(ba) The time interval between the rising and falling edges of the BURST pulse should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.

(bb) Connect the CHANNEL 2 200 MHZ CLK to CH 2 of the oscilloscope.
(bc) The time duration of the 200 MHZ CLK should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(bd) Connect the CHANNEL 2 200 MHZ DATA to CH 2 of the oscilloscope.
(be) The time duration of the 200 MHZ DATA should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(bf) Connect the CHANNEL 3 BURST output to CH 1 of the oscilloscope.
(bg) The time interval between the rising and falling edges of the BURST pulse should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(bh) Connect the CHANNEL 3 200 MHZ CLK to CH 2 of the oscilloscope.
(bi) The time duration of the 200 MHZ CLK should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(bj) Connect the CHANNEL 3 200 MHZ DATA to CH 2 of the oscilloscope.
(bk) The time duration of the 200 MHZ DATA should be approximately 9.3 divisions, or 18.67 ± 1 usec in duration. Record the time interval on the data sheet.
(bl) Replace the HP 3760A and HP 3761A Data Generator and Error Detector with the HP 1645A Data Error Analyzer and set it for external clock.
(bm) Set the HP 8660A frequency to 170 KHz and place the DATA LENGTH switch on the Signal Combiner front panel in the S position.
(bn) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 0.1 usec/div.
(bo) The time interval between the rising and falling edges of the BURST pulse should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(bp) Connect the CHANNEL 1 200 MHZ CLK to CH 2 of the oscilloscope.
(bq) The time duration of the 200 MHZ CLK should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(br) Connect the CHANNEL 1 200 MHZ DATA to CH 2 of the

oscilloscope.
(bs) The time duration of the 200 MHZ DATA should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(bt) Connect the CHANNEL 2 BURST output to CH 1 of the oscilloscope.
(bu) The time interval between the rising and falling edges of the BURST pulse should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(bv) Connect the CHANNEL 2 200 MHZ CLK to CH 2 of the oscilloscope.
(bw) The time duration of the 200 MHZ CLK should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(bx) Connect the CHANNEL 2 200 MHZ DATA to CH 2 of the oscilloscope.
(by) The time duration of the 200 MHZ DATA should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(bz) Connect the CHANNEL 3 BURST output to CH 1 of the oscilloscope.
(ca) The time interval between the rising and falling edges of the BURST pulse should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(cb) Connect the CHANNEL 3 200 MHZ CLK to CH 2 of the oscilloscope.
(cc) The time duration of the 200 MHZ CLK should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(cd) Connect the CHANNEL 3 200 MHZ DATA to CH 2 of the oscilloscope.
(ce) The time duration of the 200 MHZ DATA should be approximately 8.5 divisions, or 0.85 ± 0.05 usec in duration. Record the time interval on the data sheet.
(cf) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 0.2 msec/div.
(cg) The time interval between the rising edges of consecutive BURST pulses should be approximately 5 divisions, or 1 ± 0.04 msec in duration. Record the time interval on the data sheet.
(ch) Connect the CHANNEL 2 BURST output to CH 1 of the oscilloscope.
(ci) The time interval between the rising edges of consecutive

BURST pulses should be approximately 5 divisions, or 1 ± 0.04 msec in duration. Record the time interval on the data sheet.
(cj) Connect the CHANNEL 3 BURST output to CH 1 of the oscilloscope.
(ck) The time interval between the rising edges of consecutive BURST pulses should be approximately 5 divisions, or 1 ± 0.04 msec in duration. Record the time interval on the data sheet.

3.1.3.1 Overlapping Burst Command Test

(a) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 0.1 usec/div.
(b) Connect the CHANNEL 2 BURST output to CH 2 of the oscilloscope.
(c) The two burst pulses should predominately overlap, with the rising edge of the CHANNEL 1 BURST leading the rising edge of the CHANNEL 2 BURST. Verify this overlapping relationship.
(d) The time interval between the rising edges of each of the BURST pulses should be approximately 0.55 divisions, or 0.055 ± 0.05 usec in duration. Record the time interval on the data sheet.
(e) The time interval between the falling edges of each of the BURST pulses should be approximately 0.55 divisions, or 0.055 ± 0.05 usec in duration. Record the time interval on the data sheet.
(f) Connect the CHANNEL 2 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 0.1 usec/div.
(g) Connect the CHANNEL 3 BURST output to CH 2 of the oscilloscope.
(h) The two burst pulses should predominately overlap, with the rising edge of the CHANNEL 2 BURST leading the rising edge of the CHANNEL 3 BURST. Verify this overlapping relationship.
(i) The time interval between the rising edges of each of the BURST pulses should be approximately 0.55 divisions, or 0.055 ± 0.05 usec in duration. Record the time interval on the data sheet.
(j) The time interval between the falling edges of each of the BURST pulses should be approximately 0.55 divisions, or 0.055 ± 0.05 usec in duration. Record the time interval on the data sheet.
(k) Connect the CHANNEL 2 BURST output to the external trigger input of the oscilloscope and set it to trigger on the rising edge.
(l) Connect the CHANNEL 2 200 MHZ DATA output to CH 1 of the

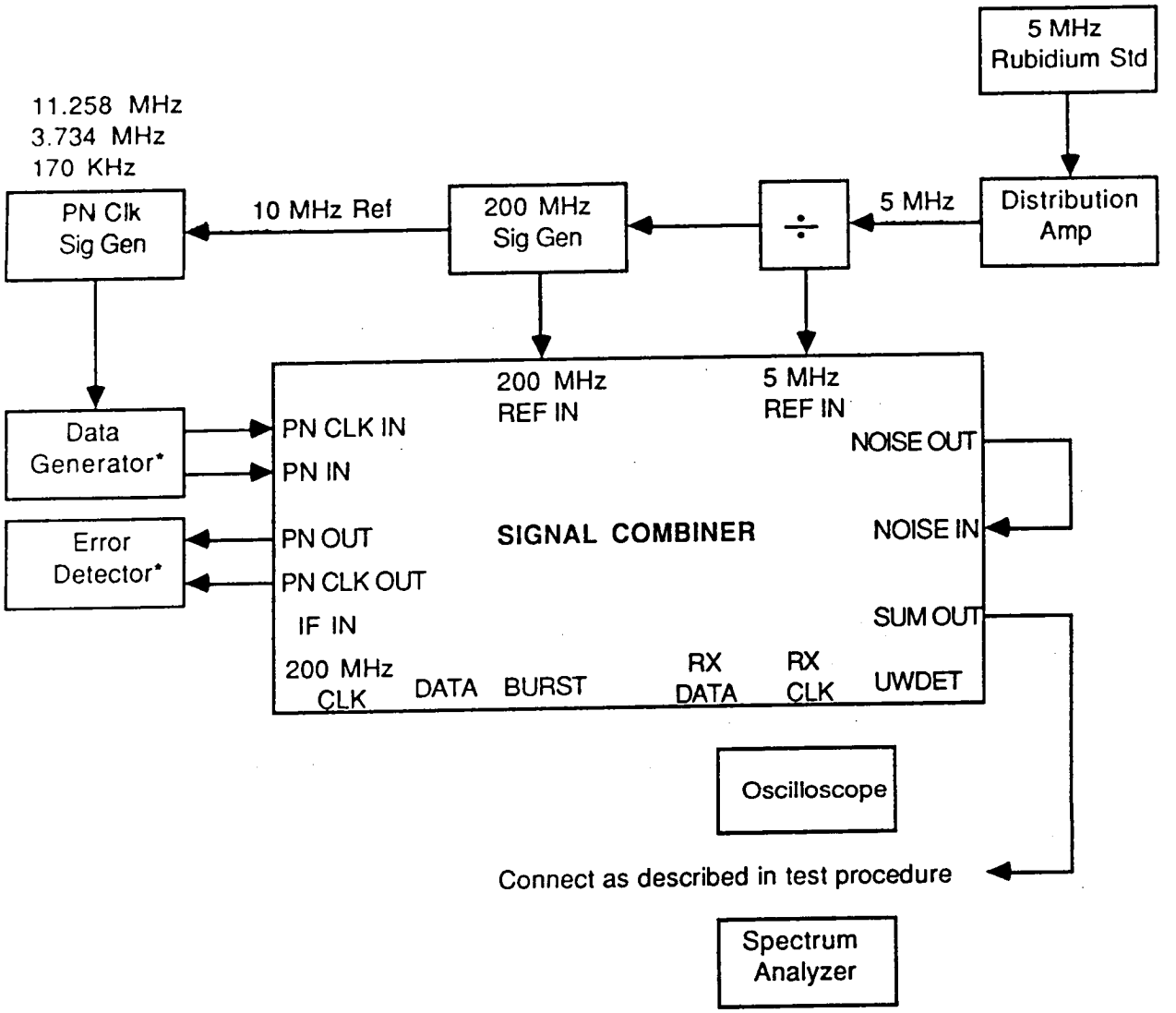
oscilloscope.
(m) Connect the CHANNEL 3 200 MHZ DATA output to CH 2 of the oscilloscope.
(n) The PN sequences for each channel should be the same, except time delayed. Verify that the sequences are the same.

3.1.3.2 Staggered Burst Command Test

(a) Set the HP 8662A frequency to 340 KHz and place the TEST PROFILE switch on the Signal Combiner front panel in the MULT position. Press Reset.
(b) Connect the CHANNEL 1 BURST output to CH 1 of the oscilloscope and adjust the TIME/DIV to 0.2 usec/div.
(c) Connect the CHANNEL 2 BURST output to CH 2 of the oscilloscope.
(d) The two burst pulses should be staggered and separated by a minimum guard time of 10 nsec. Verify this staggered relationship.
(e) Change the oscilloscope to trigger on the falling edge of CH 1 and adjust the TIME/DIV to 5 nsec/div.
(f) The time interval between the falling edge of CH 1 and the rising edge of CH 2 should be greater than 2 divisions, or 10 nsec in duration. Record the time interval on the data sheet.
(g) Connect the CHANNEL 1 BURST output to the external trigger input of the oscilloscope and set it to trigger on the rising edge. Adjust the TIME/DIV to 0.2 usec/div.
(h) Connect the CHANNEL 1 200 MHZ DATA output to CH 1 of the oscilloscope.
(i) Connect the CHANNEL 2 200 MHZ DATA output to CH 2 of the oscilloscope.
(j) The PN sequences for each channel should be different. Verify that the sequences are not the same.

3.1.4.1 Noise Spectral Density Determination

(a) Connect the Signal Combiner NOISE OUT to NOISE IN.
(b) Connect the Signal Combiner SUM OUT to CH 1 of the oscilloscope. DC couple the input.
(c) The bandlimited noise output should have no DC component. Increase the CH 1 VOLTS/DIV for maximum gain. Verify that the output has no DC component.
(d) Observe the peak noise amplitude. Verify that there is no noticeable clipping of the waveform.



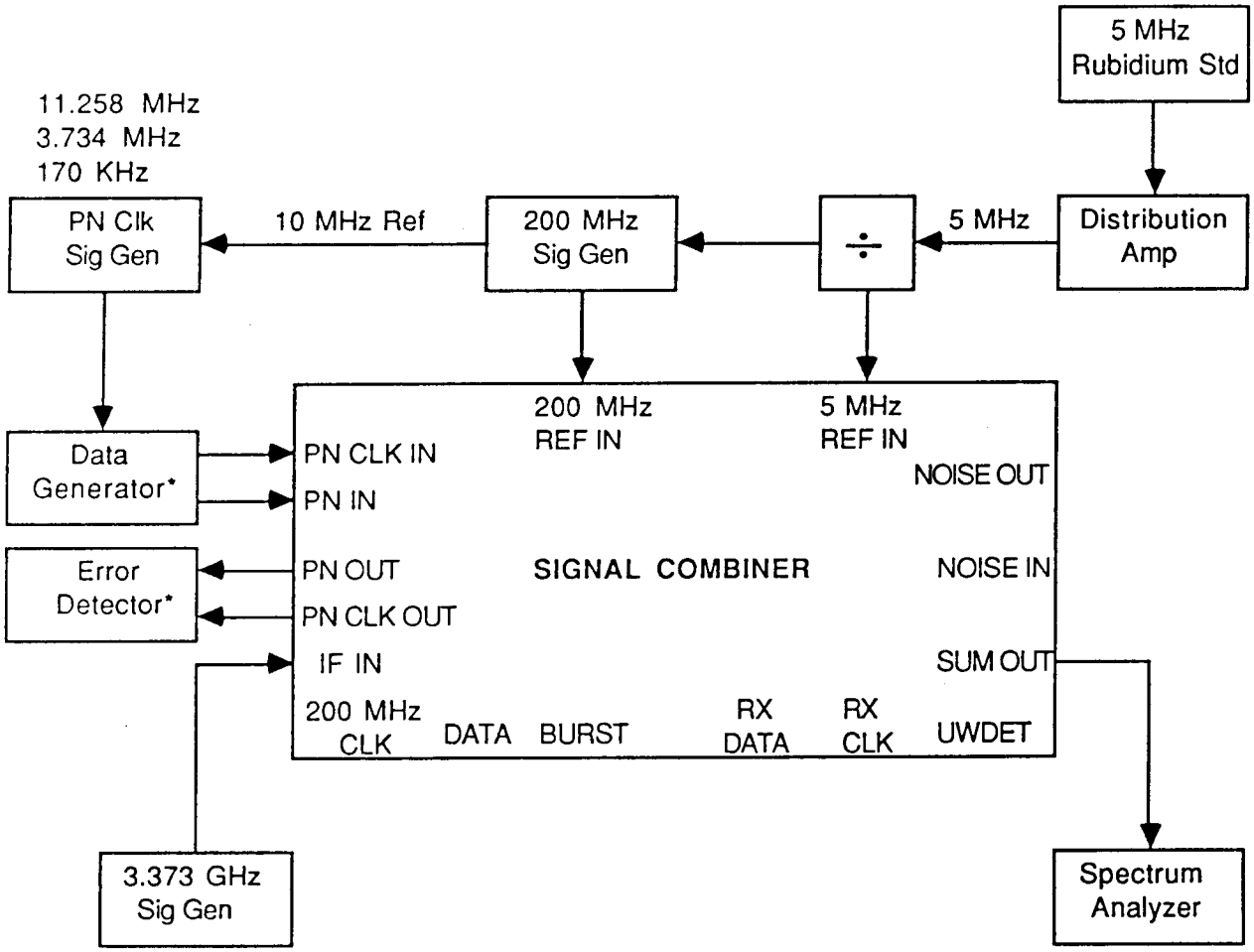
* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 3.1.4.1 Noise Spectral Density Determination Setup

(e) Connect the Signal Combiner SUM OUT to the HP 8566 Spectrum Analyzer.
(f) Set the spectrum analyzer video bandwidth to 300 Hz and the center frequency to 3.373 GHz.
(g) The noise power should be flat within ± 1 dB over a 400 MHz bandwidth centered at 3.373 GHz. Record the noise power flatness in dBs.
(h) Place the spectrum analyzer marker at a point within the 400 MHz bandwidth which is centered in amplitude with respect to the peak excursions measured in step (g).

(i) Press SHIFT, M, NORMAL to invoke the noise level measurement normalized to a 1 Hz bandwidth.
(j) Record the value for N_0 displayed in dBm/Hz.

2.1.4.2 RF Output Power



* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

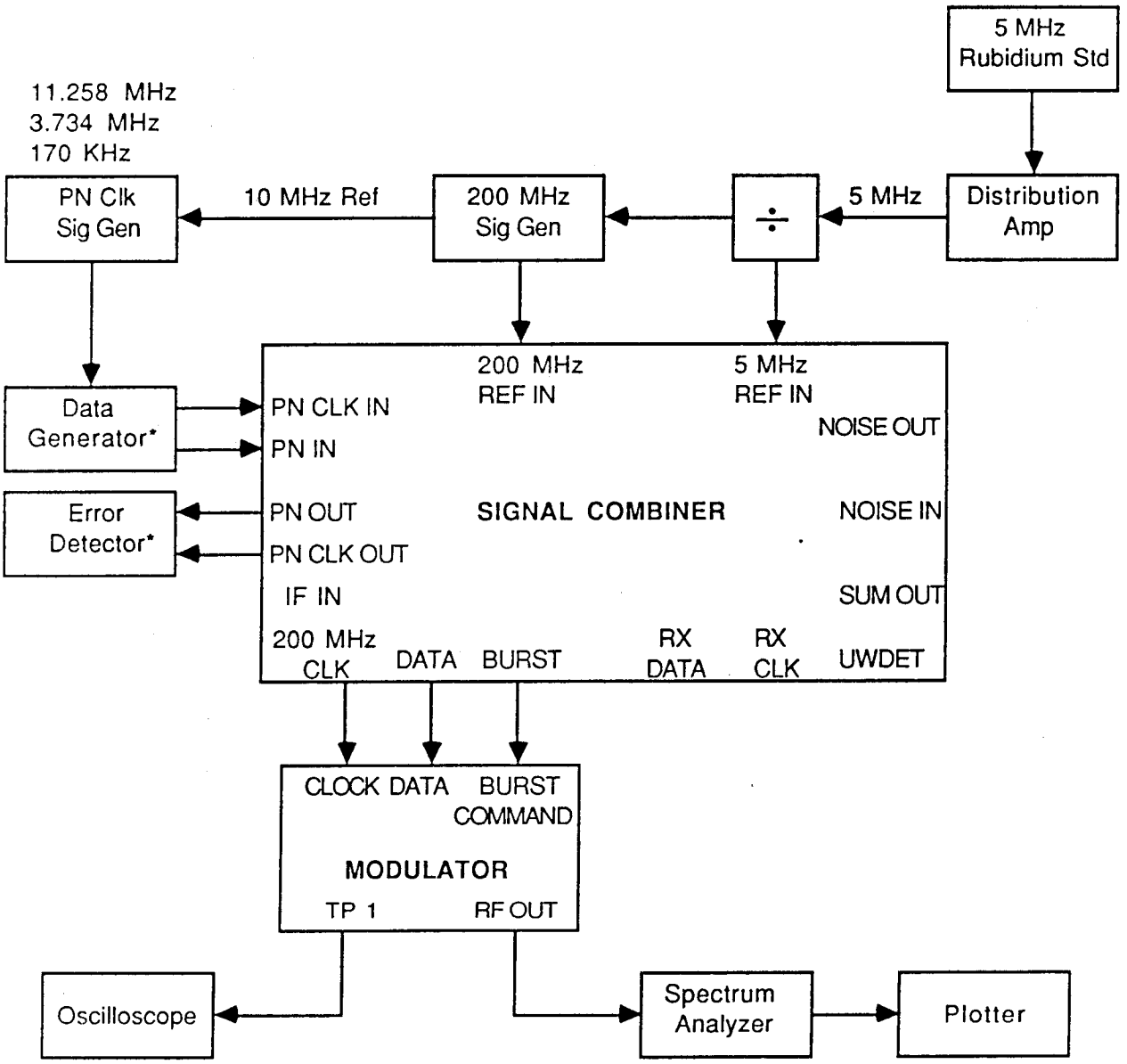
Figure 3.1.4.2 RF Output Power Test Configuration

(a) Disconnect the Signal Combiner NOISE OUT from NOISE IN.
(b) Connect a -30 dBm, 3.373 GHz signal from the HP 8672A Signal Generator to the Signal Combiner CHANNEL 1 IF IN input.
(c) Connect the spectrum analyzer to the Signal Combiner SUM OUT output.
(d) The output power level at the SUM OUT connector should be approximately 0 dBm. Record the output power level.
(e) Connect the -30 dBm, 3.373 GHz signal from the HP 8672A

Signal Generator to the Signal Combiner CHANNEL 2 IF IN input.
(f) The output power level at the SUM OUT connector should be approximately 0 dBm. Record the output power level.
(g) Connect the -30 dBm, 3.373 GHz signal from the HP 8672A Signal Generator to the Signal Combiner CHANNEL 3 IF IN input.
(h) The output power level at the SUM OUT connector should be approximately 0 dBm. Record the output power level.

3.2 Modulator Acceptance Test Procedure

Setup the test configuration for the Modulator ATP as shown in Figure 3.2.



* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 3.2 Modulator ATP Test Configuration

(a) Power the Equipment on with the cables disconnected. Allow 30 minutes for the signal generators to stabilize.

(b) Set the HP 8662A frequency to 200 MHz and the output level to 0.0 dBM.
(c) Set the HP 1645A Data Analyzer for external clock.
(d) Set the HP 8660A frequency to 170 KHz and the output level to 0.9 V (+12.1 dBm, 50Ω).
(e) Connect the cables between equipment as shown.
(f) Connect the CHANNEL 1 200 MHZ CLK, DATA, and BURST outputs to the Modulator CLOCK, DATA, and BURST COMMAND inputs as shown.
(g) Place the DATA LENGTH switch on the Signal Combiner front panel in the S position.
(h) Place the TEST PROFILE switch on the Signal Combiner front panel in the 1 position.
(i) Place the BURST LENGTH switch on the Modulator front panel in the SHORT position.
(j) Remove the top cover of the Modulator and disconnect the coaxial cable between the wideband amplifier output and the input to the VCO. Connect a test cable from the wideband amplifier output to the oscilloscope CH 1 input.
(i) Record the following information in the Modulator Acceptance Test Procedure Data Sheets, section 4.2:

- All test equipment serial numbers and cal due dates
- Test operator and QC initials certifying correct setup

3.2.1 Baseband Data Test

(a) Adjust CH 1 VOLTS/DIV to 0.5 volts/div and the TIME/DIV to 0.2 msec/div.
(b) The burst of baseband data should repeat every 1 msec or once every 5 divisions, or 1000 ± 40 usec in duration. Record the time interval of the burst duty cycle on the data sheet.
(c) Adjust the TIME/DIV to 0.2 usec/div.
(d) Measure the time interval of the preamble which consists of 32 alternating f_0, f_{15} symbols followed by 32 f_0 symbols. This time interval should be approximately 4.4 divisions, or 880 nsec in duration. Verify this approximate time interval.
(e) The next six symbols following the preamble are the unique word. From the end of the unique word, measure the remaining time interval of the burst. This message portion of the burst is obvious due to its "noisey" appearance caused by the nonrepetitive PN sequence. This time interval should be approximately 4.4 divisions, or 880 nsec in duration. Verify this approximate time interval.

(f) Change the position of switch number S2 on the Signal Combiner dip switch to change from the random external PN pattern to an internal fixed data pattern.
(g) Pull the DLY'D SWEEP knob and adjust the TIME DELAY of the oscilloscope to 10 nsec.
(h) Expand the time base and use the delay time position vernier to scan through the burst from beginning to end and count the number of preamble symbols. The number of preamble symbols should be 64. A symbol is 13.75 nsec in duration. Record the number of preamble symbols.
(i) The next 6 symbols are the unique word. The unique word pattern is $f_8\ f_8\ f_0\ f_8\ f_0\ f_8$. An f_8 is approximately halfway in amplitude between the maximum voltage excursion and the minimum voltage excursion. An f_0 corresponds to the minimum voltage excursion. The unique word pattern is shown in Figure 3.2.1. Count the number of unique word symbols and record the pattern on the data sheet.

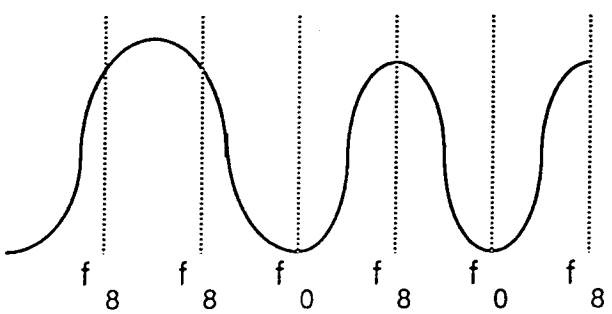


Figure 3.2.1 Unique Word Pattern at input to VCO

(j) Count the remaining number of symbols in the burst, follwing the six unique word symbols. Record the remaining number of symbols in the burst which should be 64.
(k) Take the oscilloscope out of the DELAYED SWEEP mode and adjust the TIME/DIV to 2 usec/div.
(l) The burst length should be approximately 1 division, or 2 usec (1.8425 usec to be exact) in duration. Verify this approximate time interval.
(m) Replace the HP 1645A Data Error Analyzer with the HP 3760A and HP 3761A Data Generator and Error Detector as shown in Figure 3.1.
(n) Set the HP 8660A frequency to 3.734 MHz and place the BURST LENGTH switch on the Modulator front panel in the MEDIUM position.

(o) Place the DATA LENGTH switch on the Signal Combiner front panel in the M position and press the front panel RESET switch.
(p) The burst length should be approximately 10 divisions, or 20 usec (19.6625 usec to be exact) in duration. Verify this approximate time interval.
(q) Set the HP 8660A frequency to 11.258 MHz and place the BURST LENGTH switch on the Modulator front panel in the LONG position.
(r) Place the DATA LENGTH switch on the Signal Combiner front panel in the L position and press the front panel RESET switch.
(s) Adjust the oscilloscope TIME/DIV to 10 usec/div.
(t) The burst length should be approximately 6 divisions, or 60 usec (57.2825 usec to be exact) in duration. Verify this approximate time interval.

3.2.3 Modulated Spectra Test

(a) Connect the Spectrum Analyzer to the Modulator RF OUT connector, as shown in Figure 3.2.
(b) Adjust the Spectrum Analyzer for a frequency SPAN of 364 MHz and a CENTER frequency of 3.373 GHz.
(c) Set the RES BW to 300 kHz and the VBW to 1MHz.

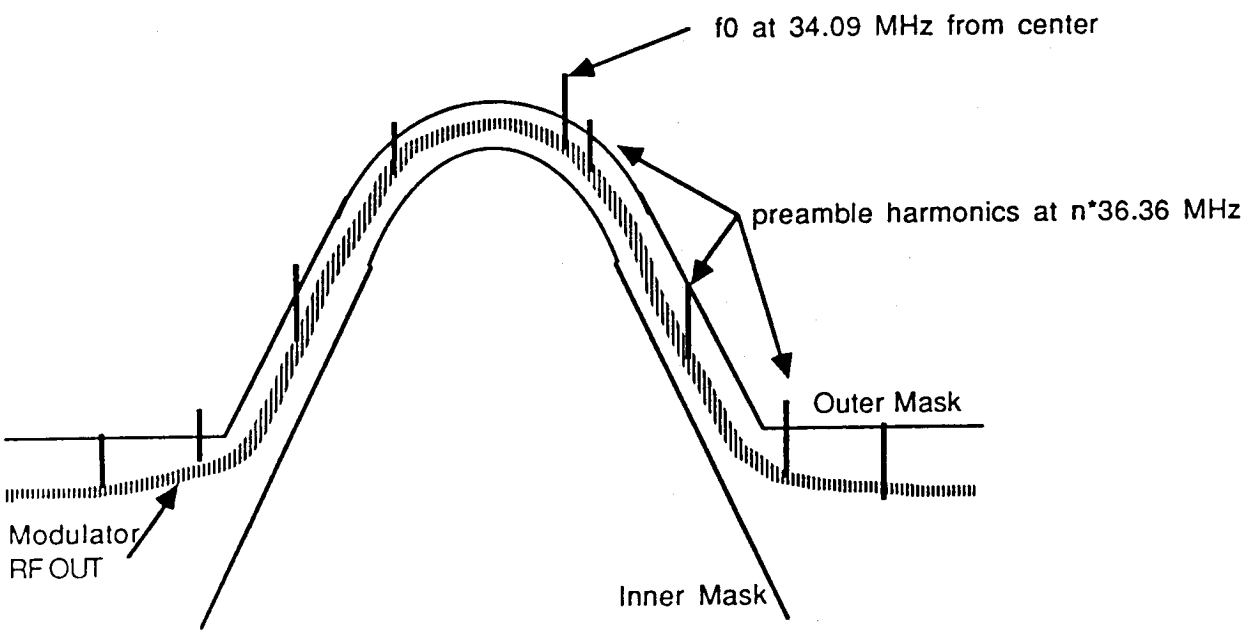


Figure 3.2.3 Modulated Spectra Waveform within Mask Limits

(d) Select LOG 10 dB/div and adjust the REFERENCE LINE and LEVEL until the center of the modulated spectra is on the first horizontal line down from the top of the display.
(e) The resulting waveform should fit within the mask provided, as illustrated in figure 3.2.3.
(f) Plot the output of the Spectrum Analyzer display and overlay the mask provided. Verify that the Modulator output falls within the mask limits.

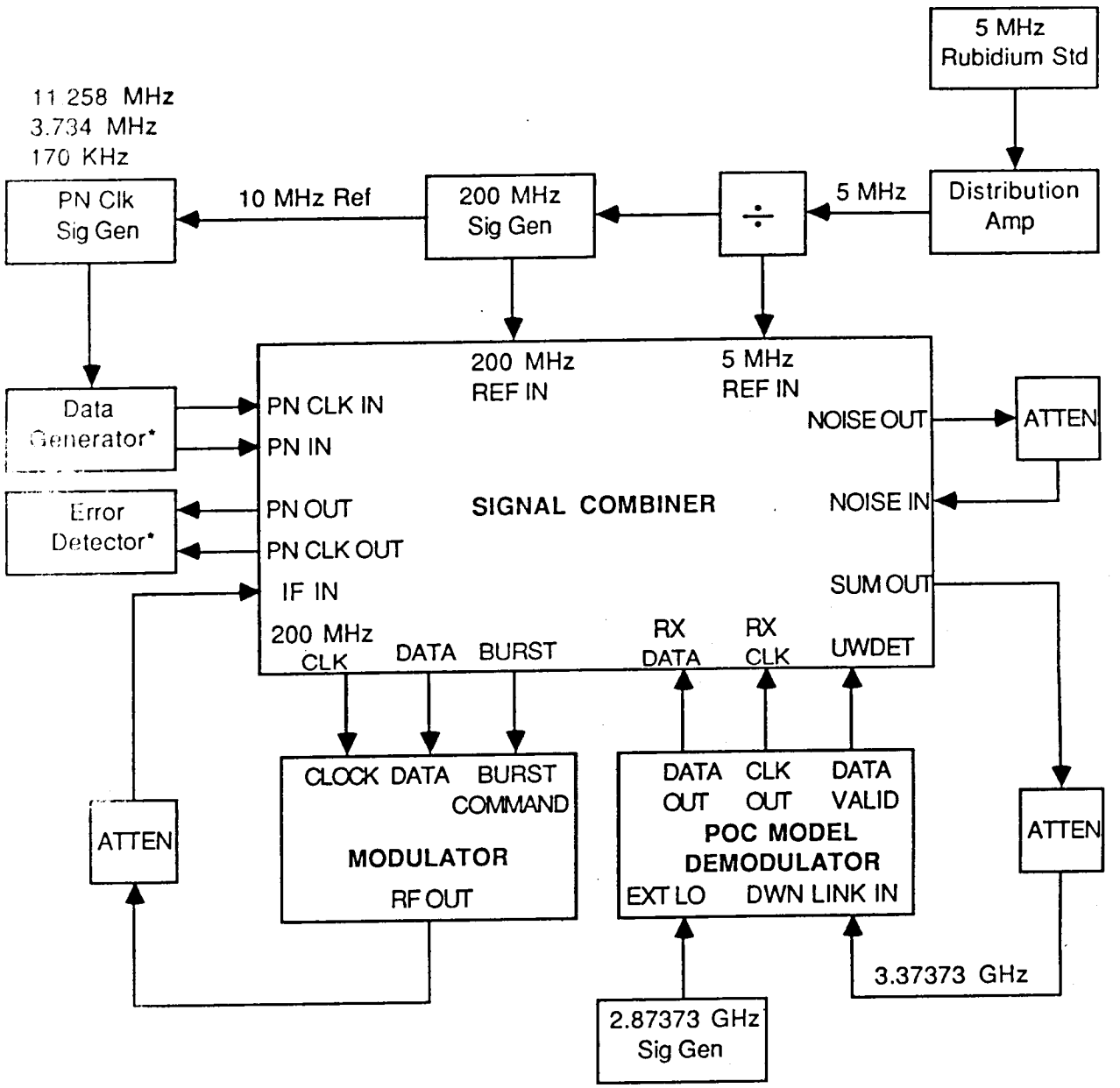
3.3 POC Model Demodulator Test Procedure

Set up the test configuration for the POC Model Test Procedure as shown in Figure 3.3.

(a) Power the Equipment on with the cables disconnected. Allow 30 minutes for the signal generators to stabilize.
(b) Set the HP 8662A frequency to 200 MHz and the output level to 0.0 dBM.
(c) Set the HP 1645A Data Analyzer for external clock.
(d) Set the HP 8660A frequency to 11.258 MHz and the output level to 0.9 V RMS (+12.1 dBm, 50Ω).
(e) Connect the cables between equipment as shown.
(f) Connect the Demodulator DATA OUT, CLK OUT, and DATA VALID outputs to the Signal Combiner RX DATA, RX CLK, and UWDET as shown.
(g) Place the DATA LENGTH switch on the Signal Combiner front panel in the L position.
(h) Place the TEST PROFILE switch on the Signal Combiner front panel in the 1 position.
(i) Place the BURST LENGTH switch on the Modulator front panel in the LONG position.
(j) Place the BURST LENGTH switch on the Demodulator front panel in the LONG position.
(k) Place the UNIQUE WORD switch on the Demodulator in the 110101 position.
(l) Set the Signal Combiner internal dip switches S1 and S2 to the open position to select an external random PN pattern as a data source. Set S4 to the closed position for coded testing. Set S8 to the closed position to select rising edge clock alignment.
(m) Record the following information in the POC Model Demodulator Test Procedure Data Sheets, section 4.3:

- All test equipment serial numbers and cal due dates

- Test operator and QC initials certifying correct setup



* The Data Generator and Error Detector are replaced by the Data Error Analyzer when the Short Burst length, i.e., 170 KHz PN clock is selected.

Figure 3.3 POC Model Test Configuration

3.3.1 <u>Eb/No Calibration</u>

(a) Disconnect the CLOCK, DATA, and BURST COMMAND inputs to the Modulator.
(b) Disconnect the NOISE OUT from the NOISE IN on the Signal Combiner.

(c) Connect the SUM OUT to the spectrum analyzer and record the measured carrier power in dBs.
(d) Add attenuation between the Modulator RF OUT connector and the Signal Combiner IF IN connector until the displayed carrier power level reads 0 dBm. Record the attenuation in dBs.
(e) Add 5 dB of attenuation at the output of the SUM OUT connector to drop the signal level to the -5 dBm nominal operating value for the Demodulator. Record the attenuation in dBs. This attenuation will be used in subsequent tests.
(f) Add an additional 5 dB of attenuation at the output of the SUM OUT connector to drop the signal level to the -10 dBm lower level operating value for the Demodulator. Record the attenuation in dBs. This attenuation will be used in subsequent tests.

3.3.2 Connectivity Test

(a) Reconnect the CLOCK, DATA, and BURST COMMAND inputs to the Modulator.
(b) Add the 5 dB of attenuation measured in 3.3.1(e) to the output of the SUM OUT connector. This drops the signal level to the -5 dBm nominal operating value for the Demodulator.
(c) Connect the output of the external attenuator at the SUM OUT output to the Demodulator DWN LINK IN as shown in Figure 3.3 and press the front panel RESET button.
(d) Record the error rate achieved in this test configuration.

3.3.3 Valid Data Test

(a) Connect the Demodulator DATA VALID output to CH 1 of the oscilloscope and trigger on the rising edge of the CH 1 input. Adjust the TIME/DIV to 10 usec/div. Adjust CH 1 VOLTS/DIV to 0.5 volts/div.
(b) The time interval between the rising and falling edges of the DATA VALID pulse should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(c) Connect the Demodulator CLK OUT to CH 2 of the oscilloscope and adjust CH 2 VOLTS/DIV to 0.5 volts/div.
(d) The time duration of CLK OUT should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.
(e) Connect the Demodulator DATA OUT to CH 2 of the oscilloscope.

(f) The time duration of DATA OUT should be approximately 5.6 divisions, or 56.29 $\pm$ 5 usec in duration. Record the time interval on the data sheet.

3.3.6 BER Baseline Test

(a) Reconnect the Demodulator DATA OUT, CLK OUT, and DATA VALID outputs to the Signal Combiner as shown in Figure 3.3.
(b) Record the value of N_0 in dBm/Hz which was determined during the ATP performed on the Signal Combiner in test 3.1.4.1, step (k).
(c) Add 83 dB to the value recorded in step (b) and record this new value. For example, if the value recorded in step (b) was -78 dBm/Hz, then 83 + (-78) = 5.
(d) In order to determine the amount of attenuation needed between the NOISE OUT and NOISE IN connectors, add the value recorded in (c) to the desired E_b/N_0. Using the same example, if an E_b/N_0 of 12 dB is desired, 12 + 5 = 17 dB of attenuation.
(e) By changing the amount of attenuation between the NOISE OUT and NOISE IN connectors, record the number of errors on the Error Detector display for each E_b/N_0 setting. The recommended range of data points would be for values of E_b/N_0 between +8 and +14 dB.
(f) Plot the number of errors versus E_b/N_0 on the BER curve graph paper provided in the data sheets.

3.3.7 IF Power Level Variation Test

(a) Remove the external attenuator at the output of the Signal Combiner SUM OUT connector and connect the SUM OUT connector directly to the Demodulator DWN LINK IN connector.
(b) By changing the amount of attenuation between the NOISE OUT and NOISE IN connectors, record the number of errors on the Error Detector display for each E_b/N_0 setting. The recommended range of data points would be for values of E_b/N_0 between +8 and +14 dB. The attenuation value for each E_b/N_0 setting is determined in the same manner as described in 3.3.6(d).
(c) Plot the number of errors versus E_b/N_0 on the BER curve graph paper provided in the data sheets for the case of 0 dBm input signal power.
(d) Add the 10 dB of attenuation measured in 3.3.1(f) to the

output of the SUM OUT connector. This drops the signal level to the -10 dBm lower operating value for the Demodulator. Connect the output of the attenuator to the Demodulator DWN LINK IN connector.

(e) By changing the amount of attenuation between the NOISE OUT and NOISE IN connectors, record the number of errors on the Error Detector display for each E_b/N_0 setting. The recommended range of data points would be for values of E_b/N_0 between +8 and +14 dB. The attenuation value for each E_b/N_0 setting is determined in the same manner as described in 3.3.6(d).

(f) Plot the number of errors versus E_b/N_0 on the BER curve graph paper provided in the data sheets for the case of -10 dBm input signal power.

3.3.8 <u>POC Model Demodulator Data Length Test</u>

(a) Add the 5 dB of attenuation measured in 3.3.1(e) to the output of the SUM OUT connector. This returns the signal level to the -5 dBm nominal operating value for the Demodulator.

(b) Connect the output of the attenuator to the Demodulator DWN LINK IN connector as shown in Figure 3.3 and press the front panel RESET button.

(c) Refer to the test results of 3.3.6. Restablish the amount of attenuation between the NOISE OUT and NOISE IN connectors which resulted in a bit error rate closest to $5*10^{-7}$. Record the number of errors on the Error Detector display and the value for E_b/N_0.

(d) Set the HP 8660A frequency to 3.734 MHz.

(e) Place the DATA LENGTH switch on the Signal Combiner front panel in the M position.

(f) Place the BURST LENGTH switch on the Modulator front panel in the MEDIUM position.

(g) Place the BURST LENGTH switch on the Demodulator front panel in the MEDIUM position.

(h) Press the Signal Combiner front panel RESET button.

(i) Record the number of errors on the Error Detector display.

(j) Replace the HP 3760A and HP 3761A Data Generator and Error Detector with the HP 1645A Data Error Analyzer and set it for external clock.

(k) Set the HP 8660A frequency to 170 KHz.

(l) Place the DATA LENGTH switch on the Signal Combiner front panel in the S position.

(m) Place the BURST LENGTH switch on the Modulator front panel in the SHORT position.
(n) Place the BURST LENGTH switch on the Demodulator front panel in the SHORT position.
(o) Press the Signal Combiner front panel RESET button.
(p) Record the number of errors on the Error Detector display.

3.3.9 Independent User Test

(a) Connect the second Modulator RF OUT to the Signal Combiner CHANNEL 2 IF IN and disconnect the first Modulator RF OUT from the Signal Combiner CHANNEL 1 IF IN.
(b) Disconnect the NOISE OUT test cable.
(c) Connect the SUM OUT to the spectrum analyzer and record the measured carrier power in dBm.
(d) Add attenuation between the second Modulator RF OUT connector and the Signal Combiner IF IN connector until the displayed power level reads 0 dBm. Record the attenuation in dBs.
(e) Reconnect the SUM OUT through the 5 dB attenuator to the Demodulator DWN LINK IN.
(f) Reconnect the NOISE OUT test cable.
(g) Reconnect the first Modulator RF OUT to the Signal Combiner CHANNEL 1 IF IN.
(h) Connect the Signal Combiner CHANNEL 2 baseband outputs to the CLOCK, DATA, and BURST COMMAND inputs of the second Modulator.
(i) Replace the HP 1645A Data Error Analyzer with the HP 3760A Data Generator and HP 3761A Error Detector.
(j) Set the HP 8660A frequency to 7.468 MHz.
(k) Place the DATA LENGTH switch on the Signal Combiner front panel in the M position.
(l) Place the BURST LENGTH switch on the Modulator front panel in the MEDIUM position.
(m) Place the BURST LENGTH switch on the Demodulator front panel in the MEDIUM position.
(n) Place the TEST PROFILE switch on the Signal Combiner front panel in the MULT position and press the RESET button.
(o) Using the same attenuation between the NOISE OUT and NOISE IN connectors as used in 3.3.8, record the number of errors on the Error Detector display.

3.3.10 Co-channel Interference Test

(a) Disconnect the first Modulator RF OUT from the Signal Combiner CHANNEL 1 IF IN and disconnect the Signal Combiner CHANNEL 2 baseband outputs from the CLOCK, DATA, and BURST COMMAND inputs of the second Modulator.
(b) Disconnect the NOISE OUT test cable.
(c) Connect the SUM OUT to the spectrum analyzer and record the measured carrier power in dBm.
(d) Add attenuation between the second Modulator RF OUT connector and the Signal Combiner IF IN connector until the displayed power level reads -20 dBm. Record the attenuation in dBs.
(e) Reconnect the SUM OUT through the 5 dB attenuator to the Demodulator DWN LINK IN.
(f) Reconnect the Signal Combiner CHANNEL 2 baseband outputs to the CLOCK, DATA, and BURST COMMAND inputs of the second Modulator.
(g) Reconnect the first Modulator RF OUT to the Signal Combiner CHANNEL 1 IF IN.
(h) Reconnect the NOISE OUT test cable.
(i) Set the HP 8660A frequency to 11.258 MHz.
(j) Place the DATA LENGTH switch on the Signal Combiner front panel in the L position.
(k) Place the BURST LENGTH switch on the Modulator front panel in the LONG position.
(l) Place the BURST LENGTH switch on the Demodulator front panel in the LONG position.
(m) Place the TEST PROFILE switch on the Signal Combiner front panel in the 1 position and press the RESET button.
(n) Using the same attenuation between the NOISE OUT and NOISE IN connectors as used in 3.3.8, record the number of errors on the Error Detector display.

3.3.11 Adjacent Channel Interference Test

(a) Disconnect the first Modulator RF OUT from the Signal Combiner CHANNEL 1 IF IN and disconnect the Signal Combiner CHANNEL 2 baseband outputs from the CLOCK, DATA, and BURST COMMAND inputs of the second Modulator.
(b) Connect the SUM OUT to the Spectrum Analyzer and adjust the center frequency of the Modulator output until the carrier frequency is 100 MHz away from the nominal 3.373 GHz.
(c) Disconnect the NOISE OUT test cable.

(d) Connect the SUM OUT to the spectrum analyzer and record the measured carrier power in dBm.
(e) Add attenuation between the second Modulator RF OUT connector and the Signal Combiner IF IN connector until the displayed power level reads 0 dBm. Record the attenuation in dBs.
(f) Reconnect the SUM OUT through the 5 dB attenuator to the Demodulator DWN LINK IN.
(g) Reconnect the Signal Combiner CHANNEL 2 baseband outputs to the CLOCK, DATA, and BURST COMMAND inputs of the second Modulator.
(h) Reconnect the first Modulator RF OUT to the Signal Combiner CHANNEL 1 IF IN.
(i) Reconnect the NOISE OUT test cable.
(j) Press the RESET button on the Signal Combiner front panel.
(k) Using the same attenuation between the NOISE OUT and NOISE IN connectors as used in 3.3.8, record the number of errors on the Error Detector display.

4.0 POC MODEL TEST DATA SHEETS

Section 4.0 contains the test data sheets for the STE ATPs and the POC Model Test of the Demodulator.

4.1 Signal Combiner Chassis Acceptance Test Data Sheets

The test operator and QC representative shall record the test data, including any pertinent comments, on the following Signal Combiner Chassis ATP data sheets.

INITIAL STARTUP DATA:

Date: _____

Test Operator (print): _____

QC Representative (print): _____

CUSTOMER WITNESS:

Name: _____

Organization: _____

UUT Serial Number: _____

TEST EQUIPMENT SERIAL NUMBERS:

EQUIPMENT	MODEL	HARRIS ID NO	CAL DUE DATE
Data Generator	HP 3760A	_____	_____
Error Detector	HP 3761A	_____	_____
Data Error Analyzer	HP 1645A	_____	_____
Signal Generator	HP 8660A	_____	_____
Signal Generator	HP 8662A	_____	_____
Spectrum Analyzer	HP 8566B	_____	_____
High Speed Oscilloscope	Tek 485	_____	_____

The remaining pages provide data sheets to be used for recording the data from the tests. Make additional copies of these data sheets as necessary for repeated tests.

4.1.1 200 Mbps Data Wrap Around Test Data Sheet

	DATA	PASS/FAIL
(b) ACQ FAILURE lamp off	_____	_____
(c) error rate display reads $1.9*10^{-6}$	_____	_____
(e) ACQ FAILURE lamp on	_____	_____
(h) ACQ FAILURE lamp off	_____	_____
(k) ACQ FAILURE lamp off	_____	_____
(l) error rate display reads $1.9*10^{-6}$	_____	_____
(n) ACQ FAILURE lamp on	_____	_____
(q) ACQ FAILURE lamp off	_____	_____
(t) ACQ FAILURE lamp off	_____	_____
(u) error rate display reads $1.9*10^{-6}$	_____	_____
(w) ACQ FAILURE lamp on	_____	_____
(z) ACQ FAILURE lamp off	_____	_____

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.1.2 Signal Combiner Data Length Test Data Sheets

	DATA	PASS/FAIL
(ab) CHANNEL 1 long BURST duration	_____	_____
(ad) CHANNEL 1 200 MHz CLK duration	_____	_____
(af) CHANNEL 1 DATA duration	_____	_____
(ah) CHANNEL 2 long BURST duration	_____	_____
(aj) CHANNEL 2 200 MHz CLK duration	_____	_____
(al) CHANNEL 2 DATA duration	_____	_____
(an) CHANNEL 3 long BURST duration	_____	_____
(ap) CHANNEL 3 200 MHz CLK duration	_____	_____
(ar) CHANNEL 3 DATA duration	_____	_____
(au) CHANNEL 1 medium BURST duration	_____	_____
(aw) CHANNEL 1 200 MHz CLK duration	_____	_____
(ay) CHANNEL 1 DATA duration	_____	_____
(ba) CHANNEL 2 medium BURST duration	_____	_____
(bc) CHANNEL 2 200 MHz CLK duration	_____	_____
(be) CHANNEL 2 DATA duration	_____	_____
(bg) CHANNEL 3 medium BURST duration	_____	_____
(bi) CHANNEL 3 200 MHz CLK duration	_____	_____
(bk) CHANNEL 3 DATA duration	_____	_____
(bo) CHANNEL 1 short BURST duration	_____	_____
(bq) CHANNEL 1 200 MHz CLK duration	_____	_____

(bs)	CHANNEL 1 DATA duration	_____	_____
(bu)	CHANNEL 2 short BURST duration	_____	_____
(bw)	CHANNEL 2 200 MHz CLK duration	_____	_____
(by)	CHANNEL 2 DATA duration	_____	_____
(ca)	CHANNEL 3 short BURST duration	_____	_____
(cc)	CHANNEL 3 200 MHz CLK duration	_____	_____
(ce)	CHANNEL 3 DATA duration	_____	_____
(cg)	CHANNEL 1 BURST duty cycle	_____	_____
(ci)	CHANNEL 2 BURST duty cycle	_____	_____
(ck)	CHANNEL 3 BURST duty cycle	_____	_____

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.1.3.1 Overlapping Burst Command Test Data Sheet

	DATA	PASS/FAIL
(c) CHANNEL 1 and 2 burst pulses overlap		_____
(d) interval between rising edges	_____	_____
(e) interval between falling edges	_____	_____
(h) CHANNEL 2 and 3 burst pulses overlap		_____
(i) interval between rising edges	_____	_____
(j) interval between falling edges	_____	_____
(n) PN sequences are the same		_____

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.1.3.2 Staggered Burst Command Test Data Sheet

	DATA	PASS/FAIL
(d) CHANNEL 1 and 2 burst pulses staggered		_____
(f) interval between burst pulses	_____	_____
(j) PN sequences are not the same		_____

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.1.4.1 Noise Spectral Density Determination Data Sheet

	DATA	PASS/FAIL
(c) no DC component in noise at SUM OUT		_____
(d) no noticeable noise waveform clipping		_____
(g) noise power flatness < ± 1 dB	_____	_____
(j) max Signal Combiner N_0 in dBm/Hz	_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.1.4.2 RF Output Power Test Data Sheet

	DATA	PASS/FAIL
(d) output power at SUM OUT for CHANNEL 1	_____	_____
(f) output power at SUM OUT for CHANNEL 2	_____	_____
(h) output power at SUM OUT for CHANNEL 3	_____	_____

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.2 Modulator Acceptance Test Data Sheets

The test operator and QC representative shall record the test data, including any pertinent comments, on the following Modulator ATP data sheets.

INITIAL STARTUP DATA:

Date: _____

Test Operator (print): _____

QC Representative (print): _____

CUSTOMER WITNESS:

Name: _____

Organization: _____

UUT Serial Number: _____

TEST EQUIPMENT SERIAL NUMBERS:

EQUIPMENT	MODEL	HARRIS ID NO	CAL DUE DATE
Data Generator	HP 3760A	_____	_____
Error Detector	HP 3761A	_____	_____
Data Error Analyzer	HP 1645A	_____	_____
Signal Generator	HP 8660A	_____	_____
Signal Generator	HP 8662A	_____	_____
Spectrum Analyzer	HP 8566B	_____	_____
High Speed Oscilloscope	Tek 485	_____	_____

The remaining pages provide data sheets to be used for recording the data from the tests. Make additional copies of these data sheets as necessary for repeated tests.

4.2.1 Baseband Data Test Data Sheet

	DATA	PASS/FAIL
(b) burst duty cycle	_____	_____
(d) preamble duration verified		_____
(e) message duration verified		_____
(h) number of symbols in preamble = 64	_____	_____
(i) number of symbols in unique word = 6	_____	_____
unique word pattern		_____
(j) number of symbols in message = 64	_____	_____
(l) short burst length duration verified		_____
(p) medium burst length duration verified		_____
(t) long burst length duration verified		_____

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.2.3 Modulated Spectra Test Data Sheet

	DATA	PASS/FAIL
(f) modulated spectra within mask		_____

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.3 POC Model Demodulator Test Data Sheets

The test operator and QC representative shall record the test data, including any pertinent comments, on the following POC Model Demodulator Test data sheets.

INITIAL STARTUP DATA:

Date: _____

Test Operator (print): _____

QC Representative (print): _____

CUSTOMER WITNESS:

Name: _____

Organization: _____

UUT Serial Number: _____

TEST EQUIPMENT SERIAL NUMBERS:

EQUIPMENT	MODEL	HARRIS ID NO	CAL DUE DATE
Data Generator	HP 3760A	_____	_____
Error Detector	HP 3761A	_____	_____
Data Error Analyzer	HP 1645A	_____	_____
Signal Generator	HP 8660A	_____	_____
Signal Generator	HP 8662A	_____	_____
Signal Generator	HP 8672A	_____	_____
Spectrum Analyzer	HP 8566B	_____	_____
High Speed Oscilloscope	Tek 485	_____	_____

The remaining pages provide data sheets to be used for recording the data from the tests. Make additional copies of these data sheets as necessary for repeated tests.

4.3.1 Eb/No Calibration Data Sheet

	DATA	PASS/FAIL
(c) SUM OUT power with no attenuation	_____	
(d) atten required for SUM OUT = 0dBm	_____	
(e) atten required at SUM OUT for -5dBm	_____	
(f) atten required at SUM OUT for -10dBm	_____	

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.3.2 Connectivity Test Data Sheet

	DATA	PASS/FAIL
(d) error rate for signal only	_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.3.3 Valid Data Test Data Sheet

	DATA	PASS/FAIL
(b) DATA VALID duration	_____	_____
(d) CLK OUT duration	_____	_____
(F) DATA OUT duration	_____	_____

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.3.6 BER Baseline Test Data Sheet

		DATA	PASS/FAIL
(b) maximum N_0 from 4.1.4.1, step (k)		_____	
(c) (b) + 83		_____	
(e) E_b/N_0 versus BER	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	

_____ _____
Test Operator Date

_____ _____
QC Representative Date

_____
Reason for Test

4.3.7 IF Power Level Variation Test Data Sheet

		DATA	PASS/FAIL
(b) E_b/N_0 versus BER for +5 dBm	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
(e) E_b/N_0 versus BER for -5 dBm	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	
	_____	_____	

Test Operator

Date

QC Representative

Date

Reason for Test

4.3.8 POC Model Demodulator Data Length Test Data Sheet

		DATA	PASS/FAIL
(c) E_b/N_0 versus BER long burst	_____	_____	
(i) medium burst BER		_____	
(p) short burst BER		_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.3.9 Independent User Test Data Sheet

	DATA	PASS/FAIL
(c) 2nd Modulator power out at SUM OUT, dBm	_____	
(d) second Modulator attenuation	_____	
(o) staggered burst BER	_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.3.10 Co-channel Interference Test Data Sheet

	DATA	PASS/FAIL
(c) 2nd Modulator power out at SUM OUT, dBm	_____	
(d) 2nd Modulator attenuation for -20 dBm	_____	
(n) BER with co-channel interferer	_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

4.3.11 Adjacent Channel Interference Test Data Sheet

	DATA	PASS/FAIL
(d) 2nd Modulator power out at SUM OUT, dBm	_____	
(e) 2nd Modulator attenuation for 0 dBm	_____	
(k) BER with adjacent channel interferer	_____	

_____ _____

Test Operator Date

_____ _____

QC Representative Date

_____

Reason for Test

APPENDIX B
GATE ARRAY INDUSTRY SURVEY

In order to properly evaluate the present gate array capability available in the industry, the circuits shown in Figures B-1 and B-2 were supplied to vendors to evaluate. Vendors were requested to calculate propagation delay, maximum thoughput rate, power dissipation, NRE costs and gate count. A variety of vendors in the CMOS, ECL and Bipolar technologies were contacted. Direct comparisons were difficult for gate count because each technology defines cell or gate in a different manner. Perhaps a better metric would be the size of the die (information that was not supplied to all vendors). Vendors were requested to quote maximum thoughput rate, or propagation delay for functional block in the diagram. This was to enable identification of the time critical circuits from each vendor and enable a functional comparison between the technologies and associated vendors. The list of vendors and their technologies are shown in Table B-1. Figure B-3 illustrates the various processing speed quotes from responsive vendors. Each speed value is identified with technology and power required to implement that speed.

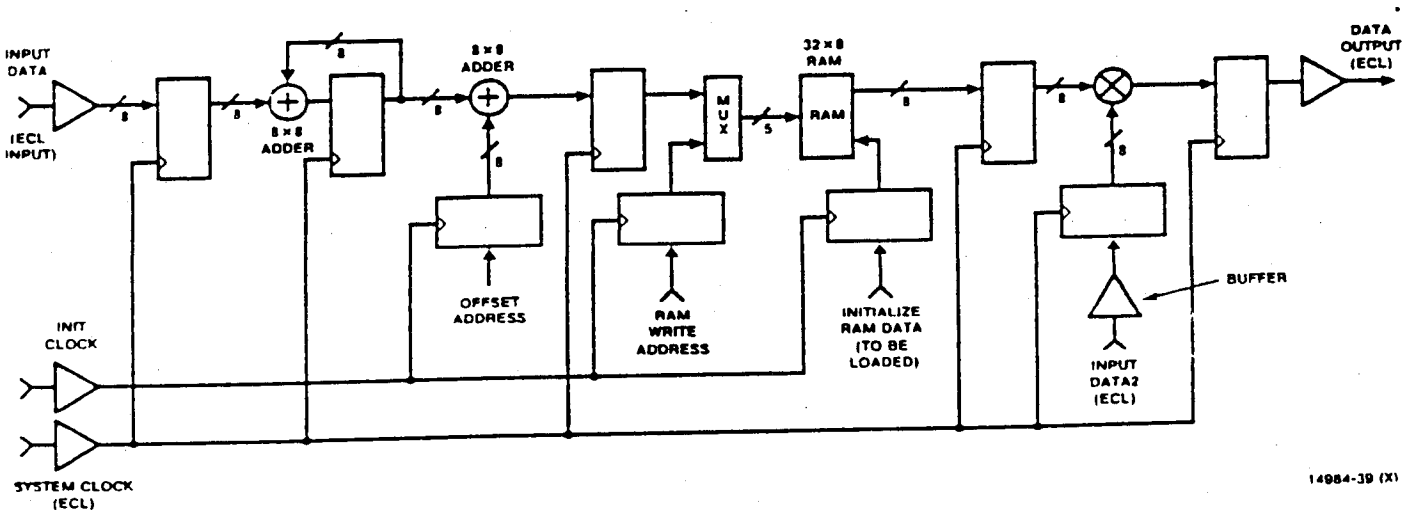
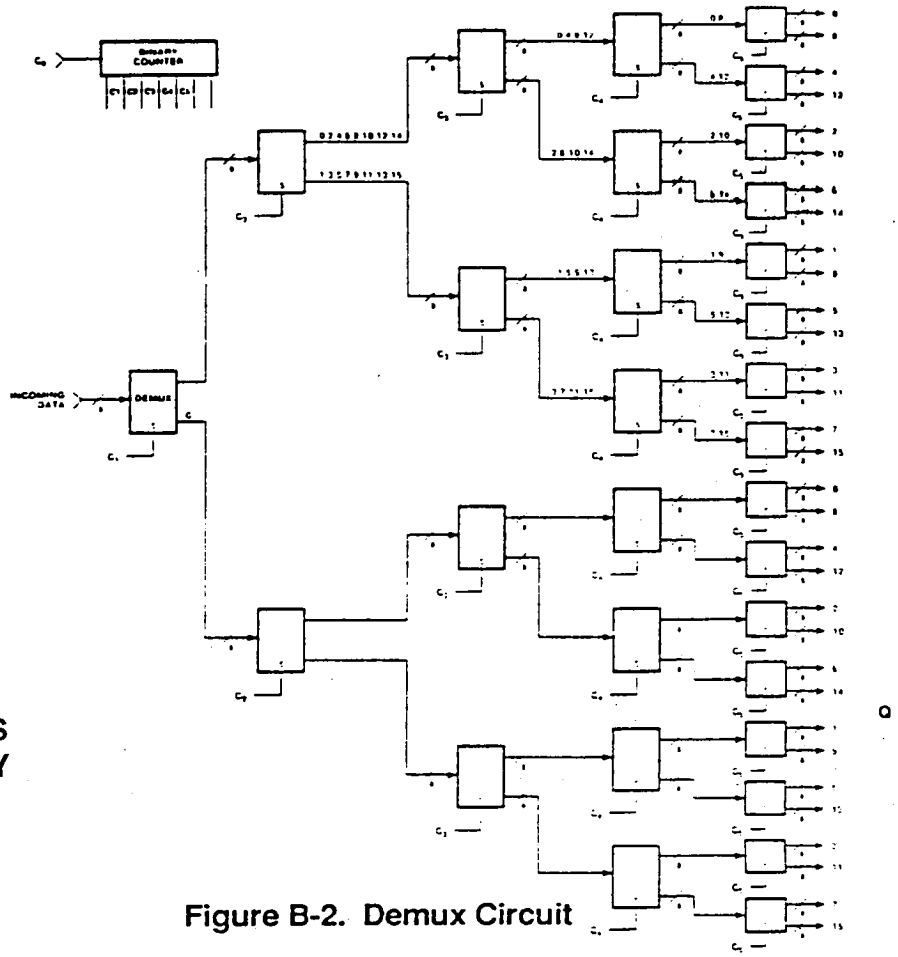


Figure B-1. Correlatation Circuit



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OF POOR QUALITY

Figure B-2. Demux Circuit

GATE ARRAY VENDOR	TECHNOLOGY
VTC Incorporated	Bipolar ASIC, CMOS ASIC
Computer Circuits Laboratories, Inc.	CCL Technology on Bipolar Process
Integrated CMOS Systems, Inc.	CMOS 1 and 1.5 Micron Process
VLSI Technology, Inc.	CMOS 1 and 1.5 Micron Process
LSI Logic Corporation	CMOS 1 and 1.5 Micron Process
Seattle Silicon	CMOS Process
GE RCA/Intersil (Harris)	CMOS 1.2 Micron Process
Sony Corporation of America	ECL Gate Arrays
Applied Micro Circuits Corporation	ECL Gate Arrays
Fujitsu Limited	ECL Gate Arrays
Plessey Semiconductor	ECL Gate Arrays

Table B-1. Gate Array Vendors Contacted for Information and Test Evaluation

Vendor reaction varied from completely compliant responses to nonresponsive. Some vendors would give generic reaction about their standard gate arrays but would not evaluate the correlator or Mux/Demux circuit for our proposal. In general, the advertised speeds of their processes greatly exceeded the speed at which data could be run into and out of the device or through a macro function such as those defined in the correlator circuit. With such a variety of responses, we felt that the best presentation for each vendor would be to summarize the responses, we felt that the best presentation for each vendor would be to summarize the responses from them and include that data in this appendix.

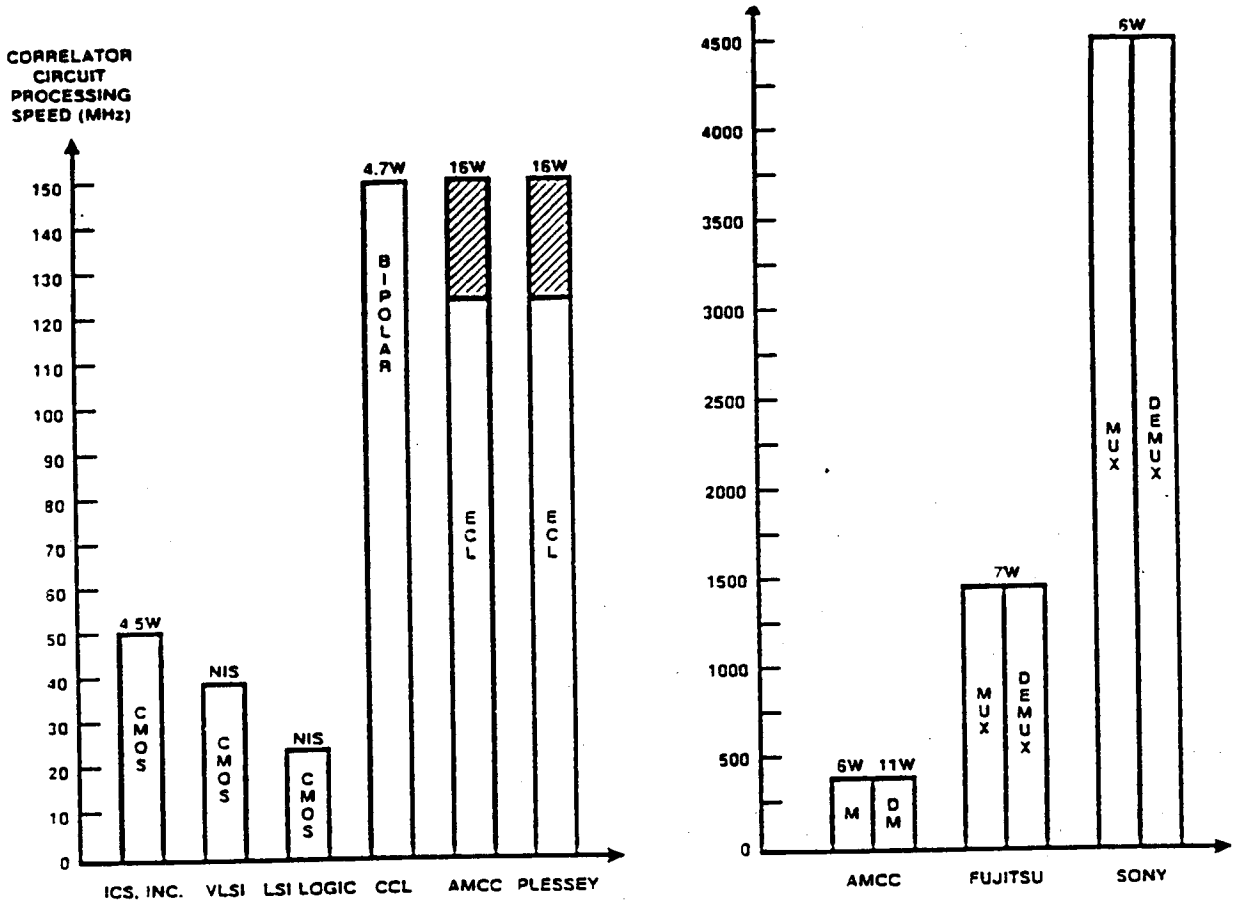

Figure B-3. Power Versus Implementation Versus Vendor

VTC INCORPORATED

Vendor was not responsive to the industry survey. Data included is from phone convcersation.

Bipolar an CMOS Gate Arrays

<u>Bipolar Process</u>

Part Number VL2000
Low Power 1000 gate gate array
Normal Power 4000 gate gate array
High density 2 micron process
Clock speeds: 500 MHz
Cell library available: digital

Part Number VL3000
30,000 gates
High density 2 micron process
Clock speeds: 1 GHz
Cell library available: linear, digital and memory

Contact: Jay Waldero CMOS
Gary Heye BIPOLAR

INTERGRATED CMOS SYSTEMS, INC.

Quote received on the correlator circuit.

CMOS Gate Arrays

8 x8 multiplier

Overall speed limiter was the 8 x 8 multiplier:	40 MHz	1.5 micron
	50 MHz	1.0 micron

1.5 micron process

a. Max clock speed	40 MHz
b. Max correlation circuits in array	4
c. I/O pins	153
d. Package requirement	256 PGA
e. Power consumption	2.5 W

1.0 micron process

a. Max clock speed	50 MHz
b. Max correlation circuits array	8
c. I/O pins	285
d. Package requirement	340 pin surface mount
e. Power consumption	4.5 W

NRE:	27,000 gates	Moderate NRE	5 weeks delivery	(1.5 micron)
	25,000 gates	High NRE	7 weeks delivery	(1.0 micron)

** The circuit evaluation did not include an accumulator.

Contact: Richard Gluck

Bruce Kligensmith

VLSI TECHNOLOGY, INC.

Quote received on the correlator cicuit.

CMOS Gate Arrays

Register/adder/register:	14.6 ns	68.5 MHz
Register/adder/mux/register:	20.5 ns	48.7 MHz
Register/RAM/register:	12 ns	83.3 MHz
Register/multiplier/register:	25.8 ns	38.7 MHz

I/O pins: 52
Package: 64 pin PGA
1.5 micron process
Die size: 140 mils
Equivalent gates: 278

No power quoted
No NRE quoted
No delivery quoted

Contact: Sunil Wadwani

SONY SEMICONDUCTOR

Quote received on the mux/demux circuit.

ECL Gate Arrays

2000 gate gate array
I/O pins: 100
Power: 6 watts
Propagation delay: 220 ps
Package: 32 pin PGA

200 gate gate array
I/O pins: 25
Power: 1.7 watts
Propagation delay: 150 ps
Package: 32 pin metal flat pack
NRE: Very low NRE
One 1:8 8 bit demux/IC
One 1.64 8 bit demux/four IC's

Contact: Masa Mizuno

APPLIED MICRO CIRCUITS CORPORATION

Fully compliant quote, i.e., quote for both correlator and mux/demux cicuit with all questions ansewered.

ECL/TTL Logic Arrays

Correlation Circuit:

Q35090T	130 MHz:	89% util;	149 pin PGA;	296 cells
QM1600T	123 MHz:	89% util;	149 pin PGA;	207 cells

2 micron oxide isolated bipolar process
NRE: Low
Speed limit: accumulator path 123 MHz
Power: Q3500T: 8.2 Watts
QM1600T: 7.8 Watts

Demultiplexer Circuit:

Q5000T	350 MHz	60% util;	226 pin PGA;	353 cells

8 bit 1:16 demux
2 micron oxide isolated bipolar process
NRE: Low
Power: 11 Watts

Mulitplexer Circuit:

Q5000T	350MHz;	33% util;	226 pin PGA;	379 cells

8 bit 16:1 mux
2 micon oxide isolated bipolar process
NRE: Low
Power: 5.8 Watts

Recommendation: Use new products currently being proven.

Q20000 series

8000 gates	NRE	Low	January 89
16000	NRE	Low	June 89

Contact: Keith Nootbar
Richard Negin

LSI LOGIC CORPORATION

Quote received for correlator circuit.

CMOS Gate Array

<u>0.7 micron process</u>

LCA 100135	60K gates
LCA 100182	80K gates
LCA 100235	100K gates

NRE: Very high

Includes: 15 prototypes
application engineer time
user's class
design capture center time
simulation
20 MHz test
verification package

Speed limit: 24 MHz due to multiplier cicuit

Power dissipation: no information supplied

Number of gates in design: verbal quote that design would fit in packages outlined above.

Contact: Bill King
Dan Deitz
Bill Casanova

Special note: LSI has a design center on the Harris facility with full time application engineers at the facility to help facilitate the design capture phase of the process.

FUJITSU LIMITED

Nonresponsive to vendor request.

Information supplied below is from vendor supplied data sheet.

ECL Gate Arrays

ET3000. 3072 gates
ET4500 4480 gates

Propagation Delay: 0.7 ns for I/O buffer

Power dissipation: 7 Watts

Package: 149 pin PGA

NRE: no information supplied

Logic Library: includes mux/demux, but no hihg level macros.

PLESSY SEMICONDUCTOR

Quote received on the correlation circuit.

ECL Gate Array

Parts available:

16000 gates
8000 gates
2000 gates

Contact: Mike Fisher

COMPUTER CIRCUITS LABORATORIES, INC.

Vebal quote received on the correlation circuit.

CCL technology on Bipolar process

Function	Prop Delay	Power
8 bit latch	0.9 ns	77 mW
5 bit mux	0.9 ns	32 mW
8 bit adder	3.2 ns	182 mW
8 x 8 multiplier	5.0 ns	1500 mW
32 x 8 SRAM	5.0 ns	800mW

Speed limited to 150 MHz by multiplier

1.5 micron bipolar process
Core power: -2.0 V
I/O power: -4.5 V
Memory power: -4.5 V
68 pins
4.7 watts maximum
0-70 temperature range
4 fin heat sink

Contact: Dennis Prestholt

SEATTLE SILICON

Vendor was not responsive to industry survey, but supplied the following information about the company:

CMOS ASIC design

Company sells technology tools to develop ASIC's
Wafers are bought from foundries: GE (Harris); VTC; AMI

Tools include: auto route and place software
design verification

Processes include 2.5, 1.5, 1.25, and 1.00 micron

Contact: John Schroeter

NASA
National Aeronautics and Space Administration

Report Documentation Page

1. Report No. NASA CR-185126	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle: Advanced Modulation Technology Development for Earth Station Demodulator Applications		5. Report Date: July 1989
		6. Performing Organization Code
7. Author(s): R.C. Davis, J.V. Wernlund, J.A. Gann, J.F. Roesch, T. Wright, and R.D. Crowley		8. Performing Organization Report No. None
		10. Work Unit No. 650-60-21
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		13. Type of Report and Period Covered: Contractor Report, Final
12. Sponsoring Agency Name and Address: National Aeronautics and Space Administration, Lewis Research Center, Cleveland, Ohio 44135-3191		14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, William D. Ivancic, Space Electronics Division, NASA Lewis Research Center.

16. Abstract

This report is the result of work performed under contract for NASA Lewis Research Center under the Advanced Modulation Technology Development program. The purpose of this contract was to develop a high rate (200 Mbps), bandwidth efficient, modulation format using low cost hardware, in 1990's technology. The modulation format chosen is 16-ary CPFSK. The implementation of the modulation format uses a unique combination of a limiter/discriminator followed by an accumulator to determine transmitted phase. An important feature of the modulation scheme is the way coding is applied to efficiently gain back the performance lost by the close spacing of the phase points.

17. Key Words (Suggested by Author(s)): 16 CPFSK, Modulation, Coding	18. Distribution Statement: Unclassified – Unlimited, Subject Category 17

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