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Bidirectional Power Converter Control Electronics

Final Report

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FINAL REPORT

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5.0 Construction and Test

1.0 Summary

This program was aimed at developing a family of control circuit designs for resonant technology, power processing hardware; which were appropriate to control the SCR driven power switching stages and series resonant networks of "Mapham" (Reference 3) derived inverter/converter configurations.

In general,the primary tasks included the following:

- Analyze the basic set of functions required to control a multi-phase bidirectional resonant power system.
- Create a set of basic designs to implement those functions.
- Build and test the basic designs
- Integrate and test the control hardware into high power breadboard/testbed systems.

Application specific power processor requirements addressed both source and load interfaces, and included regulating drivers/inverters/frequency-changers to provide high frequency (20-kHz) AC from DC or low frequency AC; and bidirectional interfaces from 20-kHz AC to DC or low frequency AC loads and users. The main functions were broken into two sections and defined as follows:

1. **General**
   - Housekeeping
   - Overload Protection

2. **Application Specific**
   - Case 1: On-board battery charging from the high frequency bus.
   - Case 2: Auxiliary ground power energizing the high frequency bus.
   - Case 3. Variable speed motor/generator starting/running/generation to and from the high frequency bus.

The original program was to be completed in approximately twelve months, and the main tasks were completed in approximately that period. However, operational testing at that time was limited to non-real-time functional tests and to low power IRAD hardware interfaces which then existed at General Dynamics. Therefore, NASA LeRC and General Dynamics agreed to extend the final completion date twice; first to verify compatibility with the 25-kW high power IRAD hardware then in construction at General Dynamics; and then to test with the subsequent LeRC contracted 25-kW testbed equipment being completed in 1987.

2.0 Introduction and Background

The high-frequency power system technology addressed by this program generates its basic AC transmission link power by exciting an underdamped, series-resonant, L-C circuit. The power bus therefore becomes an integral part of the resonant link in the more or less usual resonant converter configuration, with the load interface modules forming the output stages. Therefore the power system for a vehicle is really one large, integrated, multiple-module resonant converter.

While the basic configuration is a series resonant design, it is not the familiar "Schwarz" (Reference 4) type. Alternately, it places the load (reflected through the output transformer) in parallel with the resonant capacitor in the method proposed by Neville Mapham (Reference 3). Figures 2-1 and 2-2 show the two circuit approaches.

This gives us a system driver (inverter) that is essentially a voltage source as compared to the more usual "Schwarz" current source. This has obvious advantages for a power system. The line voltage is independent of the load (on a first order basis) and is tolerant of open circuits, obvious requirements for a utility system. In addition, the output frequency is clock-controlled, and independent of variations in the resonant circuit components, which is a significant development for this class of hardware.

The basic power output hardware configuration for a single driver is shown in figure 2-3. Two or more such drivers are arranged in series, with different phase shifts between one another, to add and provide power output closed-loop regulation. The control circuits noted (c) in the above figures are the subject of this contract.

3.0 Resonant Processor Operation and Control Requirements

3.1. "General" Functions

3.1.1. Housekeeping

Housekeeping functions are those that are associated with module operations, independent of the chosen module output character, or those that are inherently necessary to assure proper operation of the module or assembly.

The first task to be accomplished in this contract effort was to examine the operational power components of a typical driver or receiver module to find those common tasks associated with the operation of the bridge-connected power switches.

When functioning as a driver (inverter), there are four primary switch states. The component designators for the following discussion are shown in Figure 3-1a, in Chapter 8. State 1 has switches A_f and D_f turned on. The current in the output capacitor, C_O is shown in period 1 of Figure 3-1b. Since the series resonant circuit of L_O and C_O is underdamped, C_O is charged to a voltage above the power supply voltage, V_{CC}. If switches A_r and D_r are now turned on, the current shown in period 2 flows in C_O. If B_f and C_f are turned on during period 2, after a delay long enough to allow A_f and D_f to turn off, but before the current has decayed to zero, the resulting current is shown in period 3 of Figure 3-1b. It charges C_O to its maximum value (in the reverse direction) to provide the energy for period 4, when B_r and C_r are turned on. The time correlated voltage across C_O is shown in Figure 3-1c. It is obvious that if this periodic operation is continued, a continuous sinusoidal output voltage is produced at half the basic clock rate. Housekeeping functions to be performed for this operation are:

1. Alternate turn-on of the forward (S_f) switch pairs at the leading edge of the clock pulse.

2. Turn-on of the appropriate reverse switches (S_r) at the zero crossings of the C_O current.

3. Detection of the V_{CC} polarity and reversal of the switch turn-on "sense" on a real time basis for AC input power operation.

4. Disabling of all switch operation for turn-off and primary control.

3.1.2. Short Circuit Protection

When the output of this resonant converter topology is overloaded or shorted, the resonant circuit is no longer underdamped, and the forward current does not return to zero before it is time for the next clock pulse. If that pulse were applied, the power input would be shorted in the common "all switches on" bridge circuit failure mode. A requirements decision was made to incorporate a switch control logic input which checks to see if an appropriate reverse current has occurred, before an opposite polarity switch can be turned on. While equivalent protection could be accomplished through forced-commutation of the output switches, this choice would either complicate the power circuitry significantly or restrict the available choices for power switching components by eliminating the entire family of thyristor devices.

3.2. Application Specific Functions

3.2.1. Case 1, On-board Battery Charging from the High Frequency Bus

The requirement for on-board battery interface control generates the need for bidirectional operation. The basic housekeeping/short protection logic described in section 3.1 provides all the necessary control for the single-module reverse (source) mode.

When operated as a receiver (load interface), bus power is applied to the same high frequency interface (as if it were a driver) and the switches are sequenced to provide full wave rectified power at the V_{CC} terminals. Therefore, high-frequency, polarity-determining inputs must be supplied to the logic to control switch sequencing for output polarity control. Equivalent clock signals to operate the logic are generated from the high frequency bus input.

The added control function for this case is output current regulation. To avoid the complication and power losses associated with a separate, additional DC output regulator, it was decided to use the existing switches to control power output by phase delay switching. This creates a functional requirement for an analog to digital regulator circuit that delays the clock pulses to the control logic, an amount controlled by the output current feedback.

3.2.2. Case 2, Auxiliary Ground Power or AC Power Energizing the High Frequency Bus.

Requirements for the housekeeping logic already would enable the circuitry to deal with AC inputs. The only consequence of simply using the AC V_{CC} equivalent would be that the output high frequency would be amplitude modulated at the AC power input frequency. A simple solution is to use a three phase source (one phase powering each of three driver modules) and add the outputs by putting them in series. With this arrangement, the high frequency signals are all in phase, adding directly, and their modulation envelopes are in the usual three phase relationship, adding to a nearly constant high frequency AC power bus output. The conventional choice to do this function would be to put a three phase rectifier-filter on the input to provide a DC Vcc. But the conventional approach would add significant losses, not found in the chosen approach.

3.2.3. Case 3, Variable speed Motor/Generator starting/running/generation to and from the high frequency bus.

This application is the most complex of the specific requirements. The preceding two cases can be subsets of this most general case. Control circuitry designed to meet the requirements of case 2 will meet the generator/generation requirements of this case. The requirements for Bidirectional operation and output regulation (which can be used for low frequency motor output amplitude control) are developed in case 1. The remaining added functions are for frequency control of the output to the motor. They include a range of fixed frequencies, ramped frequency changes at constant rates or rates based on analog feedbacks for constant V/F control or constant torque starting.

3.3. Other Requirements

3.3.1. Regulation

While not specifically called out, proper system operation requires high frequency bus regulation. The regulation technique selected for this program operates by the "phasor" addition of the high frequency AC output voltages of two or more resonant inverter modules. This approach is completely consistent with the overall hardware requirements of the program which demand low losses and low output distortion.

3.3.2. Command Interfaces

Today's technologies require that hardware operation and test be computer controlled. To be consistent with modern laboratory techniques, and to anticipate typical operational airborne requirements for this class of equipment, all control and data interfaces for this program are designed to be computer compatible. It was agreed that these interfaces should be designed to be compatible with normal CMOS requirements and parameters. Table 3-1 (in Chapter 9) shows the typical specifications used.

4.0 Hardware Design

4.1 Requirements Specification

This first phase of the program was to develop and formalize the actual circuit and operational requirements for the hardware in a requirements specification, and submitted that specification to NASA LeRC for review and approval, prior to starting on the actual hardware design and development.

That specification is included in this report as Appendix A.

4.2 Predesign

The predesign stage of the program was to develop preliminary detailed circuit designs for the three application specific pieces of hardware in the program work statement; which also incorporated the general requirement provisions. These were then broken down into the lowest possible level building blocks having unique, identifiable functions, above the piece part level. Since the interfaces required CMOS parametric compatibility, the standard 4000-series CMOS logic family was chosen to implement the digital circuit topologies, and low-performance, non-critical operational amplifiers were chosen for the analog hardware implementation.

These low level functional blocks were successively combined into higher level ones, with the primary goal and limit aiming toward a set of large scale blocks that were common across all the Specific applications. Without repeating the details of all the subsequent iterations, the end result of that process identified five major, common building blocks. They are:

- Bridge/driver housekeeping and control (includes short circuit protection and input fault clearing)

- Analog regulation for the high frequency bus (combined with receiver AC and DC output regulation)

- AC output frequency synthesis and control
- High frequency system clock
- Digital input interfacing and storage

Appendix B shows the detailed worksheets used for this process. Section 4.4 shows how these blocks are arranged for the three Application Specific Functions.

4.3 Circuit Design and Development

4.3.1 Housekeeping Module

The housekeeping module is specifically designed to interface the logical functions with the control of the individual power switches in a single driver or receiver module. In addition, it became a "catch all" for those miscellaneous operations not clearly belonging somewhere else, but always required for operation. The housekeeping module appears in every application (driver or receiver) module, while multiples or subsets of the others are used, depending on the application. It performs the following detailed functions.

Outputs: Since the most general case of an application module has anti-parallel pairs of thyristor-family power switches in each of the four bridge driver or receiver positions, eight individual logic level command outputs are required.

Inputs: On the input side, this module processes several signals:

- Input polarity signals for low frequency AC power (V_{CC}) inputs.
- Enable signals which determine that the bridge currents have been proper to fire the next set of thyristors.
- Zero crossing indicators for "flyback" thyristor firing.
- The primary firing signals from the system clock.
- Line fault clearing command.

Functions: The module acts on those input signals to provide outputs according to the following functions:

- Logically control the 40-kHz clock to provide appropriate thyristor firing signals for 20-kHz output generation.
- Invert the sense of the firing logic in response to a negative power input polarity.
- Provide "flyback" thyristor firing signals, appropriately timed with respect to the zero crossings of the primary current.
- Inhibit the outputs if the "proper current enable" signal is not received.
- Provide a zero output for line fault clearing, if commanded.

Since the digital design process to implement these functions is straight forward and not mysterious, it will not be recounted here. The final result, is documented as the module schematic, Figure 4-1.

4.3.2 Regulation Control

Receiver Regulation: Receiver modules basically provide full wave rectification, individual 20-kHz half-sine pulse steering, and output filtering to create DC or low frequency AC; as required by user loads. Regulation is accomplished in one of two ways: Pulse population, by sending or omitting full half-sine 25µsecond pulses, or phase delay regulation of each half-sine pulse. The regulation loop is a conventional first order servo loop design which samples the output voltage and compares it to a digitally-generated reference signal. Output current is also detected and used with a similar higher-gain loop to provide an overriding limit function.

Driver Regulation: Since the receiver loop design acts on single 20-kHz half-sine pulses, its response is also appropriate for driver regulation. The driver case only requires the phase delay output mode; to delay driver clock signals to the second of two series-connected drivers, for our AC "Phasor" regulation of the high frequency (20-kHz) power bus.

Phasor Regulation puts the outputs of two or more drivers in series, and then controls the relative phase angle between them, by controlling the clock phase. That control is based on a comparison between a digitally-generated reference signal and a feedback signal from the output voltage. The output magnitude is therefore controlled by the classical addition of two (or more) AC voltages which are the same frequency, but different phase. The resultant is the vector addition of the two output phasors. (See Figure 4-2.) In this case, the power bus voltage and current are both sampled and compared with digitally-generated references with the same analog loop.

Because of the nearly identical operational requirements, it was possible for us to design a single analog module for both jobs, which then became the standard regulator "building block" module. Its schematic is shown as Figure 4-3.

Since the phase delay output control has unity gain and zero phase shift in the frequency domain of interest (as shown by R.D.Middlebrook,see Reference 5), and the analog portion is clearly single order, the control loop is unconditionally stable over a wide control range. The final design has a useful frequency response in the 3-kHz range with a DC gain approaching the open loop operational amplifier gain. High frequency characteristics, and therefore also transient response, are controlled by the characteristics of the resonant output network in the driver module.

4.3.3. AC Output Frequency Synthesis and Control

The synthesis of low frequency AC outputs to a three phase user load (typically an AC permanent magnet or induction motor) represents the most complex of the functional building blocks developed by this program. The contract requirements demand the ability to provide a wide range of output frequencies, and to change frequencies in an orderly, controlled way for motor starting and speed control. While a single module was designed, its major functions are discussed separately below for the sake of clarity.

Output Level Control: The method used to create the various output levels without resorting to analog control uses the different impedances seen at the various inputs of the typical "Y" connected motor. Referring to Figure 4-4a, if we connect the "+" output to phase B, and the "return" to phase C, there is no current in phase A, +V/2Z in phase B, and -V/2Z in phase C, as plotted in figure 4-4b. In the next 30° period, we connect "+" to phase A and B, and "return" to phase C, the currents are as shown in the second segment of 4-4b.

Next, we connect "+" to A, open B, and "return" to C, and get +V/2Z in A and -V/2Z in C. As we alternately connect and not connect a phase, and rotate those states around the three phase positions, the complete waveform shown in Figure 4-4b is constructed. You can see that the levels approximate a sine wave and the phase relationships of the currents in the three phases of the load are appropriate to normal three phase operation. Thus, a very reasonable three phase sine construction is accomplished, with only switching, with the additional systematic advantage that the low frequency current modulation in the line is only 25% peak.

The logic to steer thyristor firing signals to the appropriate outputs is again straight forward, and shown in Figure 4-5. It simply counts through the twelve sequential output states in response to a "change output step" signal from the countdown logic.

Frequency Control: Steady state frequency control is accomplished by "counting down" the half-sine pulses of the 20-kHz AC power bus input and steering them to the appropriate outputs to synthesize a full cycle of the low frequency output with twelve steps or voltage levels. Therefore, the highest frequency available, while still keeping the twelve steps is:

$$f_H = 1/(25\mu\text{sec} \times 12) = 3.3\text{-kHz}$$

The next lower frequency would use two pulses per step and:

$$f_H = 1/(25\mu\text{sec} \times 24) = 1.167\text{-kHz}$$

Since the frequency granularity is poor at or near the high frequency limits, a different method of division (using the same basic principle) was later developed, but this program and the subsequent Testbed programs with which it interfaced were not changed, since the basic technique proved the principle satisfactorily.

The actual circuitry had to be designed to count down any number of pulses, depending on the receiver output frequency required. A "comparison counter" is used as shown in Figure 4-6. The number of pulses per output level is inputed to a digital comparator, and each 20-kHz half-sine pulse incremented a counter. When the comparator senses an equality, the counter is reset and a "change output step" signal is sent to the "amplitude control logic".

Frequency Change Control: The last function to be performed by this module is the controlled, orderly change of output frequency in response to a digital input command or analog feedback signal. In this way, motor speed changes or start up characteristics (constant torque or V/F) can be controlled. To that end, a comparison counter was also used. See Figure 4-7. The initial frequency value is loaded into an up-down counter as a preset value. The final frequency is set into the comparator. Count direction is controlled by whether the final value is higher or lower than the initial preset. The instantaneous counter value is the input to the "frequency control comparator". The "frequency change counter" is incremented by a clock whose rate is dependent on either a digitally-commanded input or an analog feedback, depending on the mode desired.

4.3.4. High Frequency System Clock

To operate a single inverter/driver with a 20-kHz AC output, a train of 40-kHz clock pulses are required. One clock pulse is required for each independent output switch state change, to generate a (+) or (-) half-sine output pulse.

The system requirements are for single-phase or three-phase 20-kHz outputs. Therefore, three independent clock pulse trains must be synthesized, which are synchronized and phase shifted from one another to produce the required 120 electrical degree shift in the 20-kHz power outputs. We elected to provide the required set of signals totally with digital processing, to guarantee the constancy and accuracy the three related output signals.

Therefore, the basic required clock signal is 120-kHz, the lowest frequency that can be counted down to three 40-kHz pulse trains with the necessary 120° output relationship. A fully-developed flight type system would derive this higher frequency signal from a crystal controlled oscillator or use a related computer clock. Even though this program is primarily a demonstration of the overall control functions, and that level of accuracy was not required, we used a crystal controlled 120-kHz oscillator module to make sure that frequency variations are eliminated as variables which could effect the other data taken during testing. (See Figure 4-8.)

The count-down logic for the related 40-kHz outputs is of the classical type, and it is shown in Figure 4-9.

Switch S-1 is used to switch the three outputs so that they are in-phase, making the power outputs that they control into three independent single phase units, in phase with one another. In this mode the controlled modules could be connected in series or parallel for use in single phase power systems.

4.3.5. Digital input interfacing and storage

Since the overall supervisory control of all modern systems of this type will be via computers, it is necessary to design this equipment to be compatible with digital command inputs and outputs, from a data bus.

This development is far in advance of the selection of a serial data bus technology and type for any of its anticipated missions. For control of this type of hardware, all serial data is ultimately reduced to a parallel input word, with a number of bits appropriate to the resolution and accuracy required by the application. Therefore, we elected to use a simple parallel data input to demonstrate compatibility with digital control, assuming that standard data bus to parallel output converters would be used, from the communication technology finally chosen for the individual applications.

One additional arbitrary choice was made. Since computer data is routinely stored in eight bit "bytes", and the related logic hardware is generally partitioned in "fours" and "eights", we elected to use eight bit resolution for this demonstration hardware, while making sure that the basic technology would easily expand to support higher resolutions, where they were identified and required. This decision made the granularity of some controlled functions (such as receiver output frequency) somewhat coarse, but provided the necessary demonstration of the techniques to validate the principles, and also would allow for easy later expansion to higher resolutions.

There are four basic types of input command functions:

Eight-bit digital word storage. This was implemented with a simple eight-bit, clocked latch, from 4000-series CMOS series logic, as shown in Figure 4-10.

Analog loop reference signals. An eight-bit, clocked latch, with outputs connected to an R-2R ladder network, in the usual digital to analog converter manner, provides for the analog value to be summed with a feedback signal to derive the required control loop error signal. See Figure 4-11 and Section 4.3.2 for additional details.

Direct digital word storage interfaces. Some functions already have digital input storage capability, and no additional latched storage is required. The comparison counter used in receiver frequency synthesis can be accessed directly with parallel digital inputs, which are loaded when the counters and comparator are strobed. See Figure 4-12 and Section 4.3.3 for details.

Analog data. Since some functions (ie. frequency synthesis) are digitally implemented and have inputs from analog sources, those interfaces require analog to digital conversions. The ultimate goal of the building blocks developed in this program is large scale custom or semi-custom integrated circuits. Therefore, a simple A-to-D converter function was implemented with the same series hardware selected for the other building blocks, rather than use an already developed separate A-to-D device. See Figure 4-13.

4.4. Construction of Application Specific Functions

4.4.1. Case 1, On-board Battery Charging from the High Frequency Bus

The requirement for on-board battery interface control generates the need for bidirectional operation. The basic housekeeping/short protection logic described in Section 3.1 provides all the necessary control function for the single-module reverse (source) mode.

When operated as a receiver (load interface), bus power is applied to the same high frequency interface (as if it were a driver) and the switches are sequenced to provide full wave rectified power at the V_{CC} terminals. Therefore, high frequency polarity inputs must be supplied to the logic to control switch sequencing for output polarity control. Equivalent clock signals to operate the logic are generated from the high frequency bus input.

The added control function for this case is output current regulation. To avoid the complication and power losses associated with a separate, additional DC output regulator, it was decided to use the existing switches to control power output by phase delay switching. This creates a functional requirement for an analog to digital regulator circuit that either delays the clock pulses to the control logic, an amount controlled by the output current feedback.

Functional Implementation

The reverse (source) mode requires two power modules for high frequency power bus regulation, using the Phasor technique. Therefore, two housekeeping blocks are required, one for each set of power outputs. Since the clock signals for one power module need to be shifted and controlled, one regulator block is required. Digital commands for output voltage magnitude and output current limiting are supplied to the analog loop references by two latch/digital-to-analog input blocks. Finally, a 40-kHz clock input is required. Figure 4-14 shows the entire configuration.

The forward (receiver) mode would only require a single power output module. However, since two are required for the source mode, their DC outputs are simply paralleled for this mode. In this case, output regulation is provided by phase of pulse population control of the rectified output, and a regulator block is required for each module, adding one to the total configuration. The same input latches provide the voltage and current references, now shared by the two regulator blocks. See Figure 4-15. This now represents the total bidirectional DC configuration.

4.4.2. Case 2, Auxiliary Ground Power or AC Power Energizing the High Frequency Bus.

Requirements for the housekeeping logic already would enable the circuitry to deal with AC inputs. The only consequence of simply using the AC V_{CC} equivalent would be that the output high frequency would be amplitude modulated at the AC power input frequency. A simple solution is to use a three phase source (one phase powering each of three driver modules) and add the outputs by putting them in series. With this arrangement, the high frequency signals are all in phase, adding directly, and their modulation envelopes are in the usual three phase relationship, adding to a nearly constant high frequency AC power bus output.

Functional Implementation

To provide the three phase output addition, three power modules are required, with their output transformers connected in series. Therefore, three housekeeping blocks are used. For regulation, the phases of the power modules are controlled; one is held fixed, the second is shifted the normal amount, and the third is shifted twice that amount, for a three-phasor regulator addition. Two regulator blocks are required, one for each shifted module. Digital commands for output voltage magnitude and output current limiting are supplied to the analog loop references by two latch/digital-to-analog input blocks. Finally, a 40-kHz clock input is required. Figure 4-16 shows thee configuration for the forward mode. Figure 4-17 shows the reverse mode.

4.4.3. Case 3, Variable speed Motor/Generator starting/ running/generation to and from the high frequency bus.

This application is the most complex of the specific requirements. The preceding two cases can be subsets of this most general case. Control circuitry designed to meet the requirements of case 2 will meet the generator/generation requirements of this case. The requirements for Bidirectional operation and output regulation (which can be used for low frequency motor output amplitude control) are developed in case 1. The remaining added functions are for frequency control of the output to the motor. They include a range of fixed frequencies, ramped frequency changes at constant rates or rates based on analog feedbacks for constant V/F control or constant torque starting.

Functional Implementation

Reverse (source) operation is the simpler of the two operational modes for this function. It is identical to source mode operation of the AC module of Section 4.4.2. See Figure 4-16.

Forward (load) operation is significantly more complex. See Figure 4-18a. Three output power modules and their three housekeeping blocks are still required. Phase control or pulse population control of the rectified outputs for each motor phase is now needed, adding another regulator module, for a total of three. Shared digital commands for output voltage magnitude and output current limiting can still be supplied to the analog loop references by two latch/digital-to-analog input blocks; and the 40-kHz clock input is required.

Frequency synthesis logic blocks are added to control the sequencing of the output power switches to steer 20-kHz half-sine pulses to the appropriate motor terminals. Their detailed operation is described in Section 4.3.3. Interconnections for this operational mode are shown on Figure 4-18b. Starting and ending frequencies are stored in standard clocked latch building blocks, and the analog feedback is conditioned and scaled by an operational amplifier circuit. See Figure 4-18c.

5.0 Construction and Test

5.1 Initial Testing

The first step to verify proper operation and satisfaction of the requirements was to construct and test a set of "wire wrap" circuit boards, each of which would represent one of the basic building blocks. A sufficient number was constructed to separately assemble and test the three application specific functions. They were mounted in a card cage containing the appropriate interconnections. Since the outputs provided logic level signals only, they were connected to a buffered set of LED indicators, each of which represented an SCR in an application specific power processing module. The real time clock was not used for this testing, since output LED indications would have been too fast to reliably observe and judge for proper operation. Single pulses were applied instead and output states were noted and compared to a predetermined truth table.

Only minor troubleshooting was required to achieve proper operation in all cases, and meet all the requirements of the original contract.

5.2 High Power Compatibility Testing

As described in the introduction, the contract was extended and modified to include tests to demonstrate compatibility; first, with General Dynamics' breadboard power hardware; and later, with LeRC's testbed power hardware. The contract included authorization and sufficient funds to provide for these compatibility tests, but not for any changes or redesigns as a result of them, and additional funding was not included in the contract changes.

5.2.1. Power Breadboard

During full power, real time breadboard testing, some incompatibilities were discovered. Since the testing was performed on General Dynamics' IRAD hardware, in the midst of an IRAD development program, the determination of design changes to assure full compatibility was accomplished on that program. A full set of updated schematics is included in this report as Appendix C.

5.2.2. 25 KW Testbed

Changes developed during breadboard testing were incorporated into the circuit boards designed for the LeRC 25-kW Power System Testbed. Compatibility with this higher power equipment was then demonstrated during troubleshooting and checkout of that hardware, and is verified by observation of its proper operation.

6.0 Delivery and Final Hardware Disposition

Since the basic designs developed by this contract were ultimately incorporated into hardware which demonstrates the full set of system equipment appropriate to a Space Station power channel, it was decided that there was no need to provide additional funding to rework the original set of functional blocks, and update it to the latest configuration. Therefore, they were simply delivered in that state to satisfy the hardware delivery requirement in the contract, with the real "home" for the final designs being the 25-kW testbed hardware also delivered to LeRC.

7.0 Conclusions and Recommendations

The following conclusions and recommendations are based on testing performed at the logic level outputs for this specific development, and the results of the testing using the circuit functional blocks with actual General Dynamics and NASA testbed hardware.

7.1 Conclusions

7.1.1 It is practical to develop a family of special-purpose circuit modules, that can then be used in appropriate combinations to construct the necessary functional circuits required to operate a family of direct-generation, resonant power processors.

7.1.2 This program proved the designs for the following circuit modules:

- Housekeeping
- Analog Control (Regulator)
- Digital Input Interfacing and Storage
- High-Frequency (20-kHz and 40-kHz) System Clock
- Receiver Output Control, including low-frequency AC Output Synthesis

7.1.3 These modules were used to prove the construction of the required major power processing hardware control circuits:

- Case 1: On-board battery charging from the high frequency bus (Bidirectional DC Interface)
- Case 2: Auxiliary ground power energizing the high frequency bus (Three-phase, 60-Hz, AC Source Interface)
- Variable-speed motor/generator starting/running/generation to and from the high frequency bus (Three-phase, Variable-frequency, Bidirectional AC Interface)

7.1.4 These modules can effectively partitioned to incorporate their functions into semi-custom integrated circuits, using gate array or PAL technology.

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7.2 Recommendations

7.2.1 Proceed with the development of an integrated circuit implementation to demonstrate the feasibility of that approach.

7.2.2 Develop additional module designs to accommodate the new families of power switching devices now becoming available. (MCT's and IGT's)

8.0 Figures

This Chapter is a collection of the figures from the main body of this report. They are numbered in accordance with the original chapter in which their reference first appears.

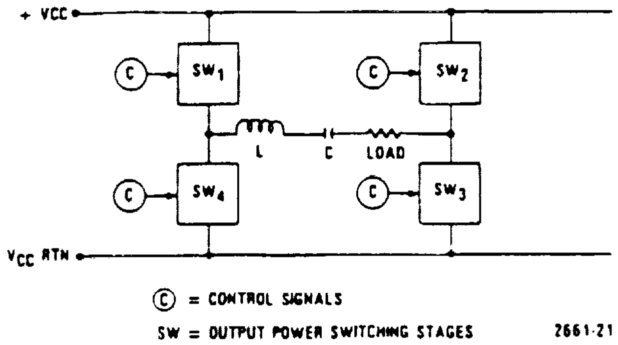

Figure 2-1, The Schwarz configuration has the load in series with the resonant circuit.

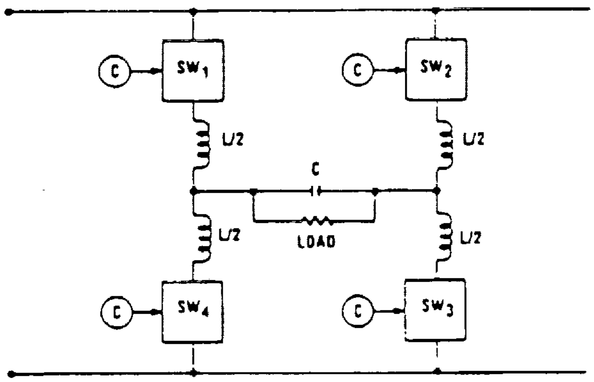

Figure 2-2, The Mapham circuit has the load in parallel with the resonant capacitor.

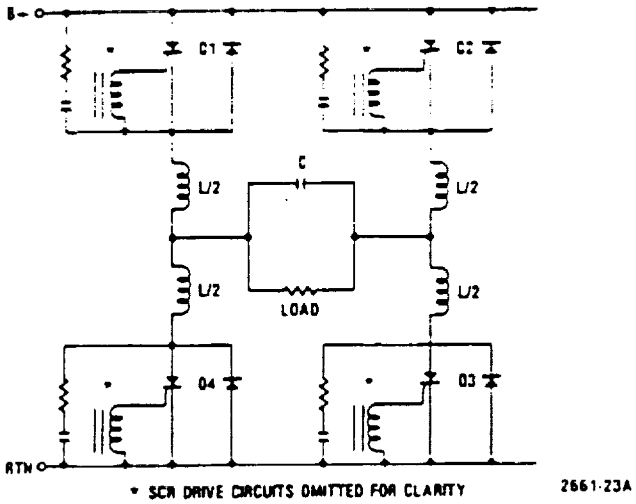

Figure 2-3, Basic Inverter Power Stage

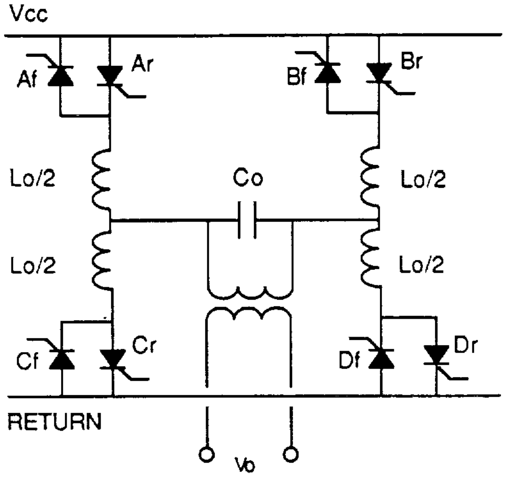

FIGURE 3.1a
TYPICAL BRIDGE DRIVER

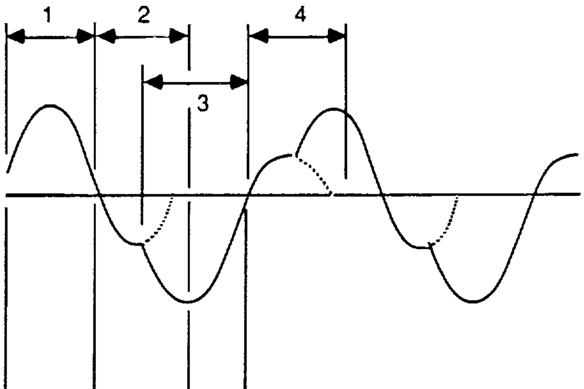

FIGURE 3.1b
(Co) CURRENT

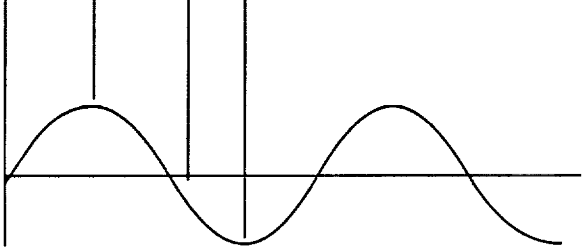

FIGURE 3.1c
(Vo) VOLTAGE

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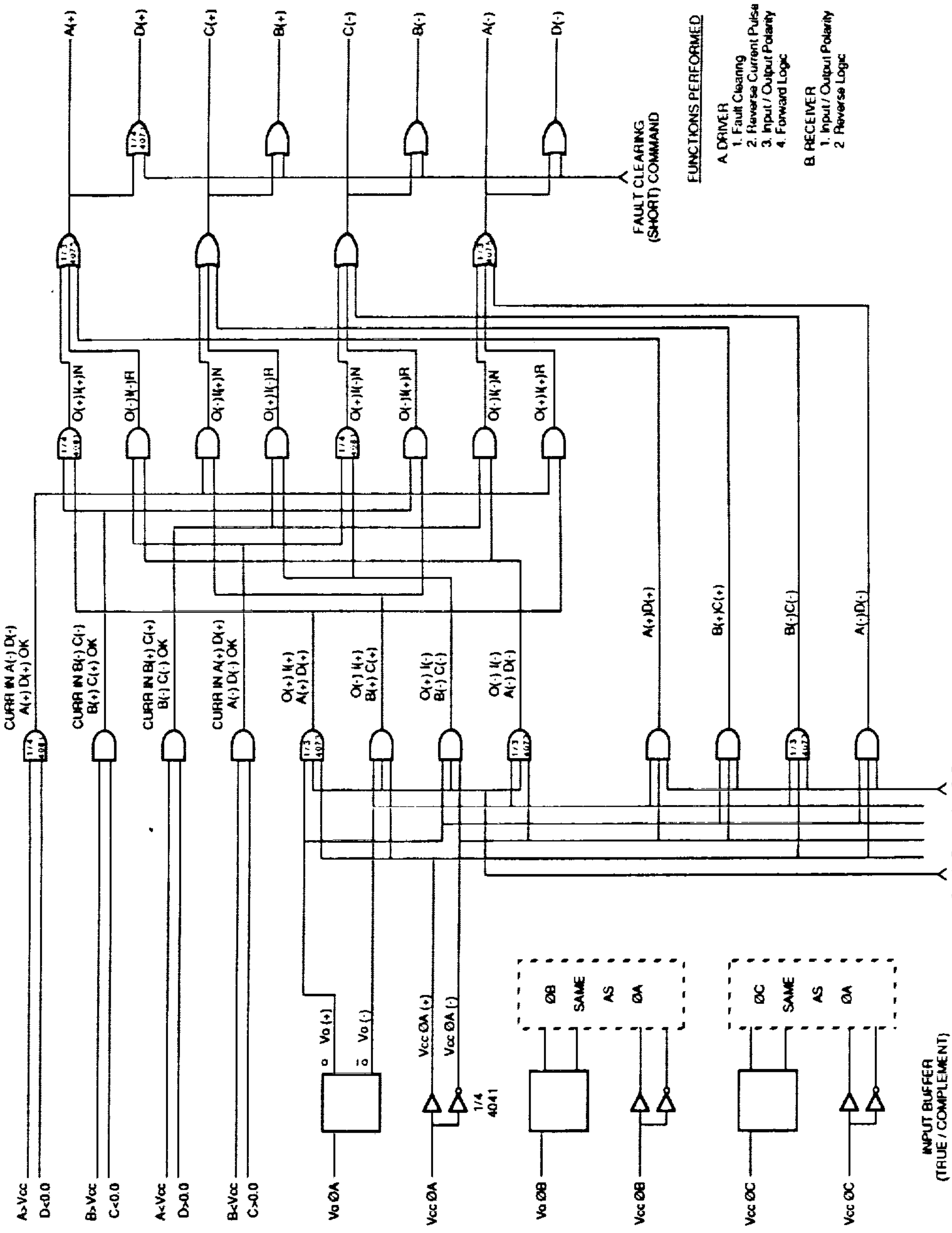
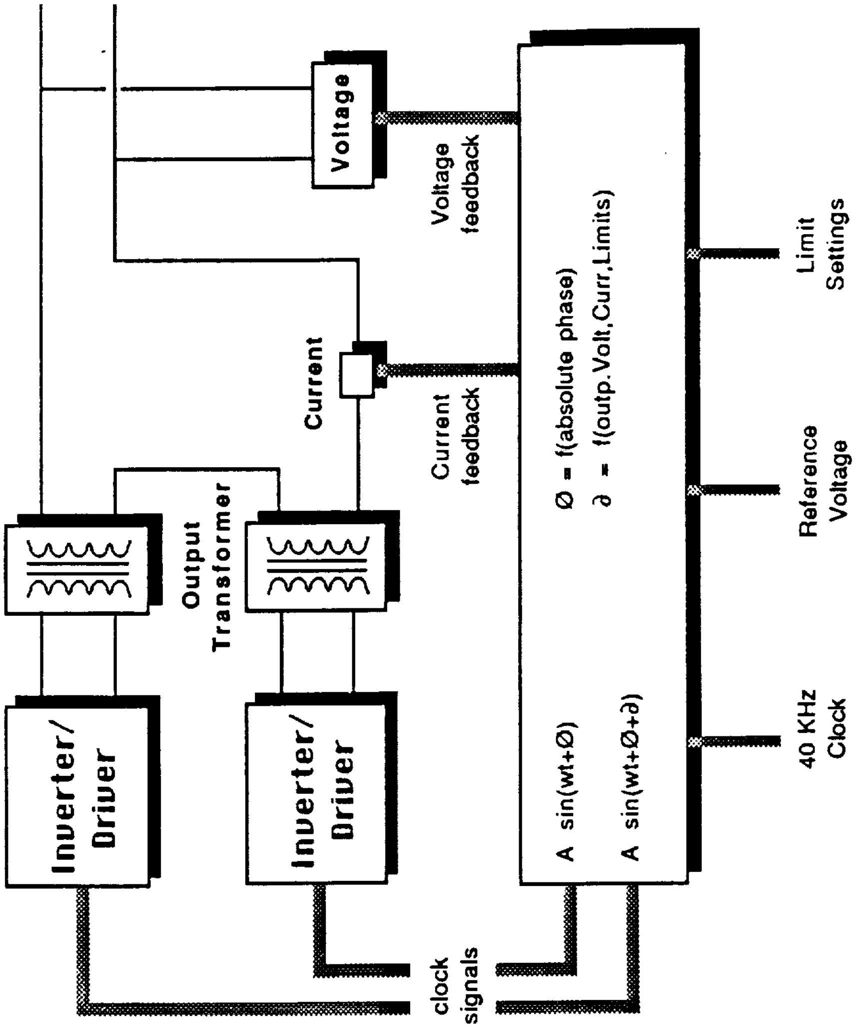
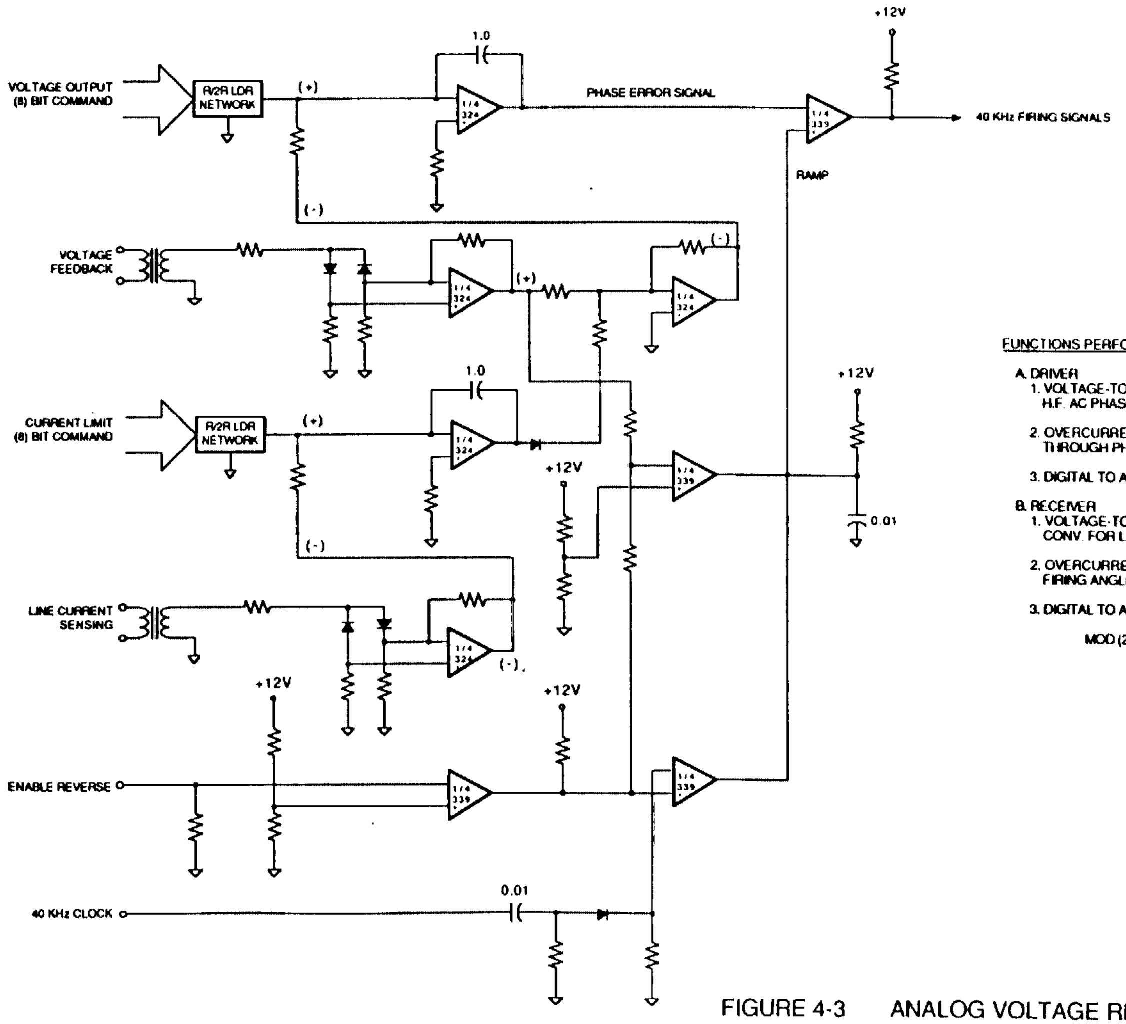


FIGURE 4.1 AC INPUT - SCR BRIDGE DRIVER HOUSEKEEPING LOGIC


Voltage
Voltage feedback
Current
Current feedback
Output Transformer
Inverter/ Driver
Inverter/ Driver
Ø = f(absolute phase)
∂ = f(outp.Volt,Curr,Limits)
A sin(wt+Ø)
A sin(wt+Ø+∂)
clock signals
Limit Settings
Reference Voltage
40 KHz Clock



FUNCTIONS PERFORMED

A. DRIVER
  1. VOLTAGE-TO-PHASE CONV. FOR H.F. AC PHASOR REGULATION
  2. OVERCURRENT LIMITING THROUGH PHASE CONTROL
  3. DIGITAL TO ANALOG REF. CONV.

B. RECEIVER
  1. VOLTAGE-TO-FIRING ANGLE CONV. FOR L.F. AMPLITUDE CONTROL
  2. OVERCURRENT LIMITING THROUGH FIRING ANGLE CONTROL
  3. DIGITAL TO ANALOG REF. CONV.

MOD (2)

FIGURE 4-3 ANALOG VOLTAGE REGULATOR LOOP - VOLTAGE AND CURRENT LIMITING

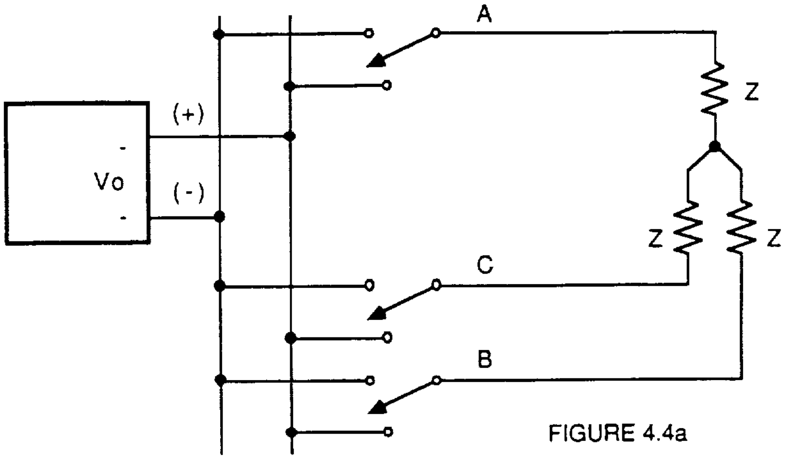


FIGURE 4.4a

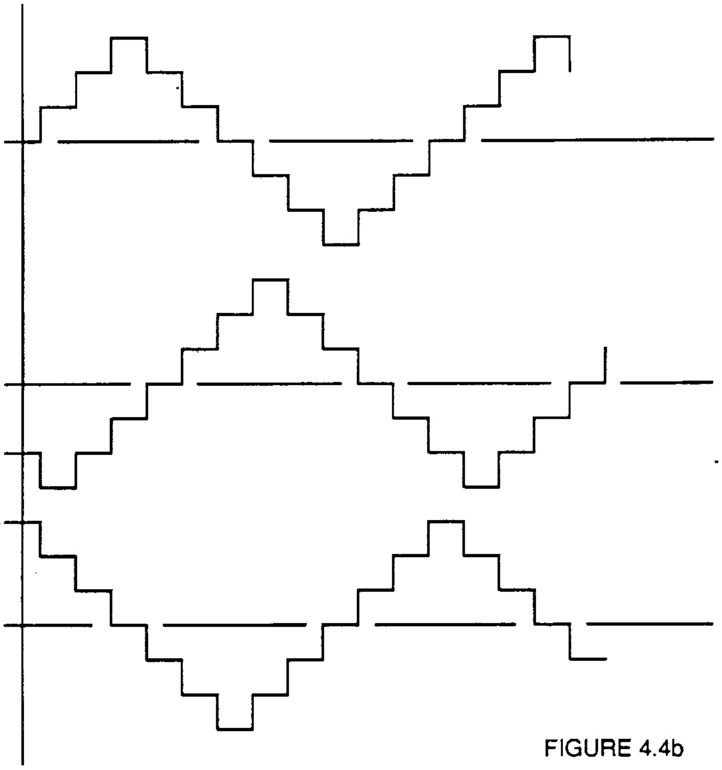


FIGURE 4.4b

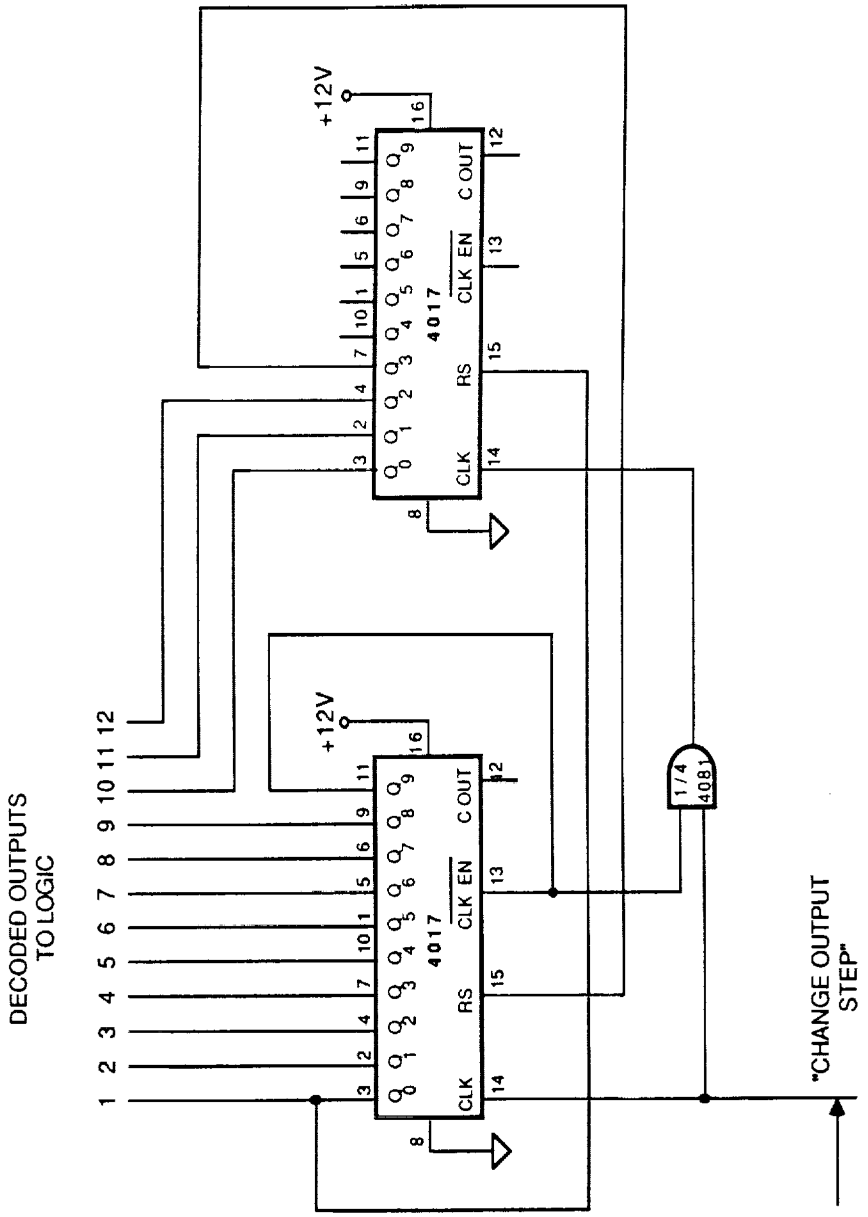

DECODED OUTPUTS TO LOGIC
1 2 3 4 5 6 7 8 9 10 11 12
+12V
+12V
4017
4017
Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9
CLK
RS
CLK EN
C OUT
3 2 4 7 10 1 5 6 9 11 16
14 15 13 12 8
1/4 4081
"CHANGE OUTPUT STEP"

FIGURE 4.5

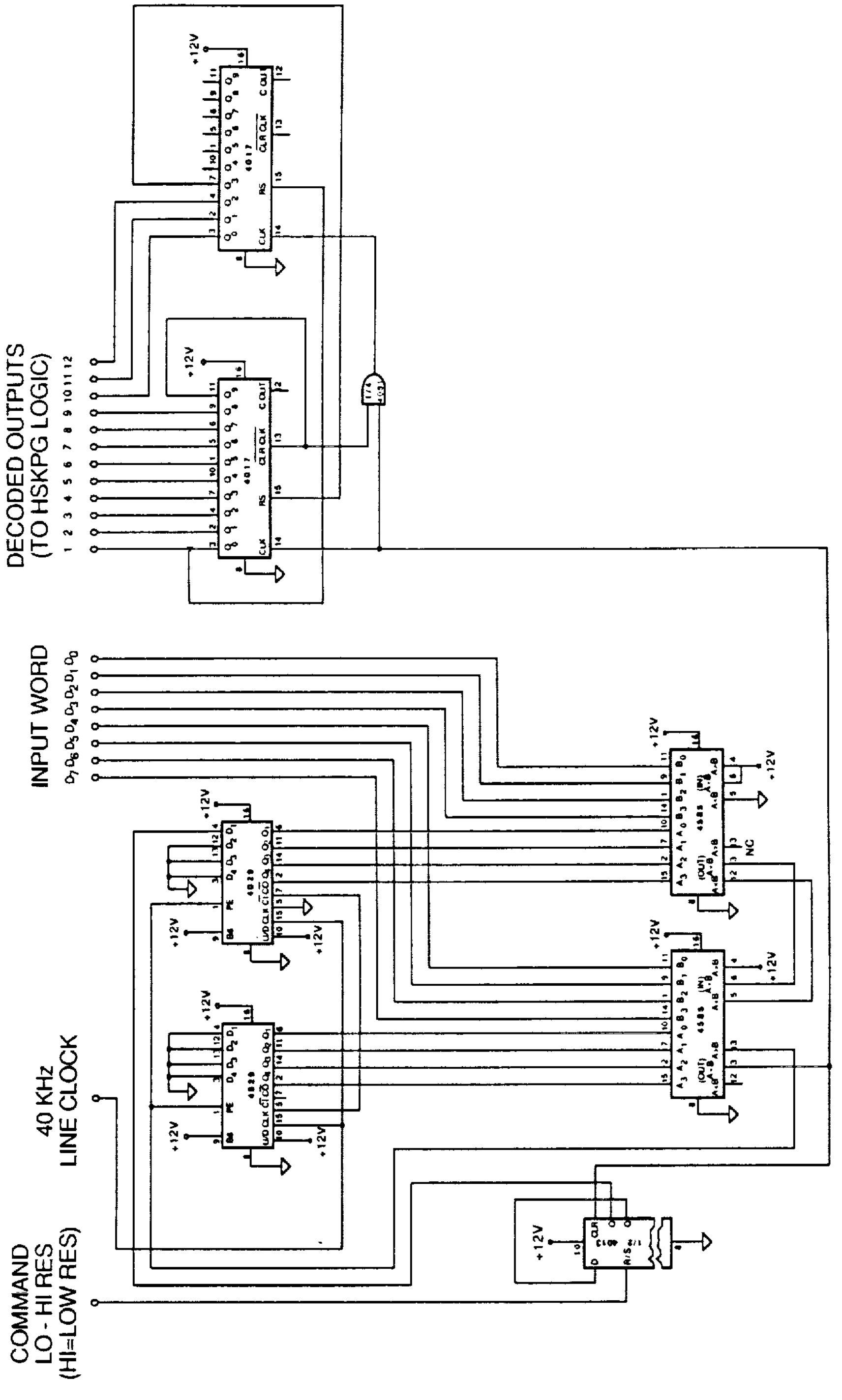


FIGURE 4.6 LOW FREQUENCY OUTPUT SYNTHESIS MODULE

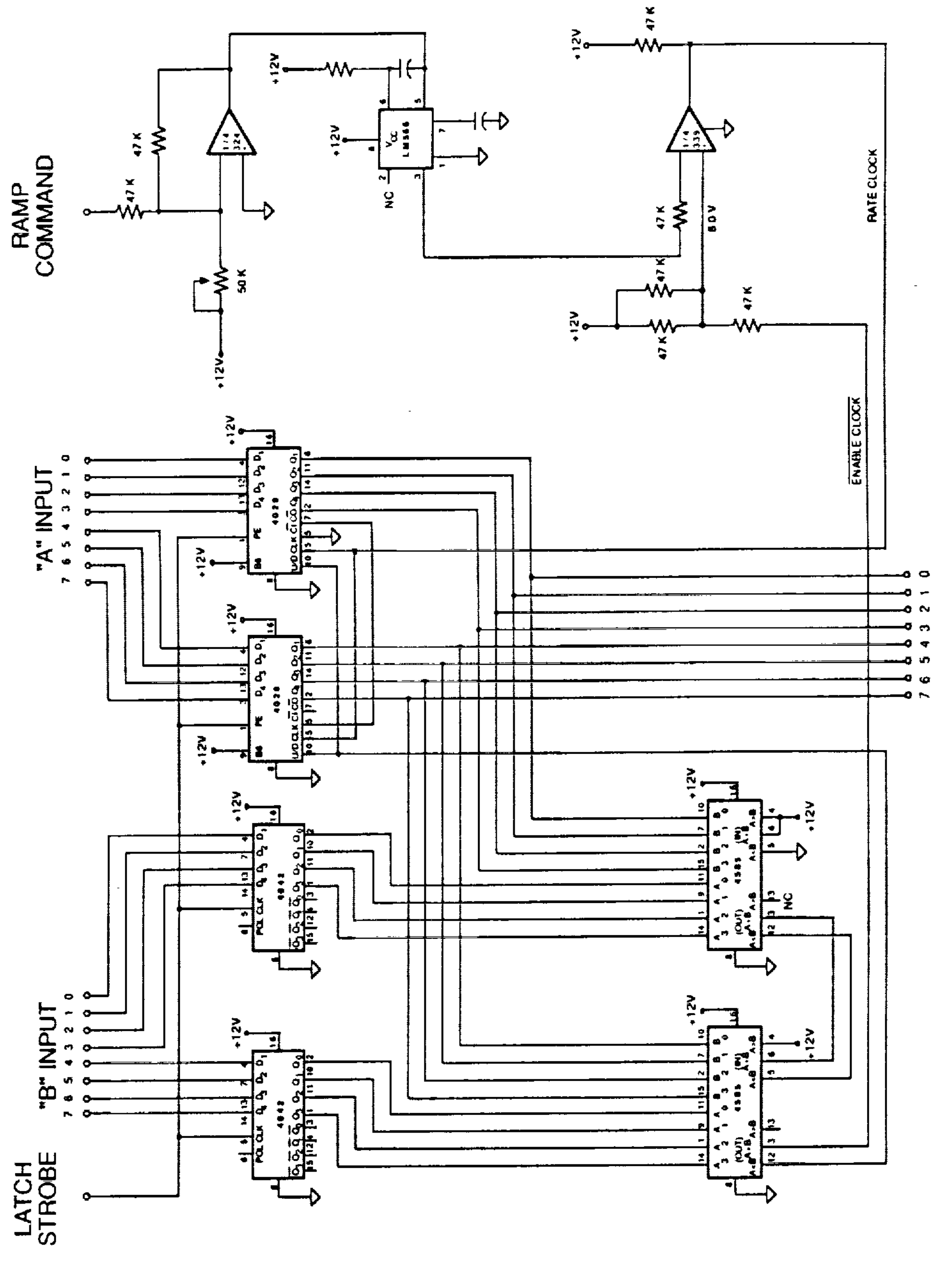


FIGURE 4.7 DIGITAL INPUT (WITH COMMAND WORD RAMP GENERATOR)

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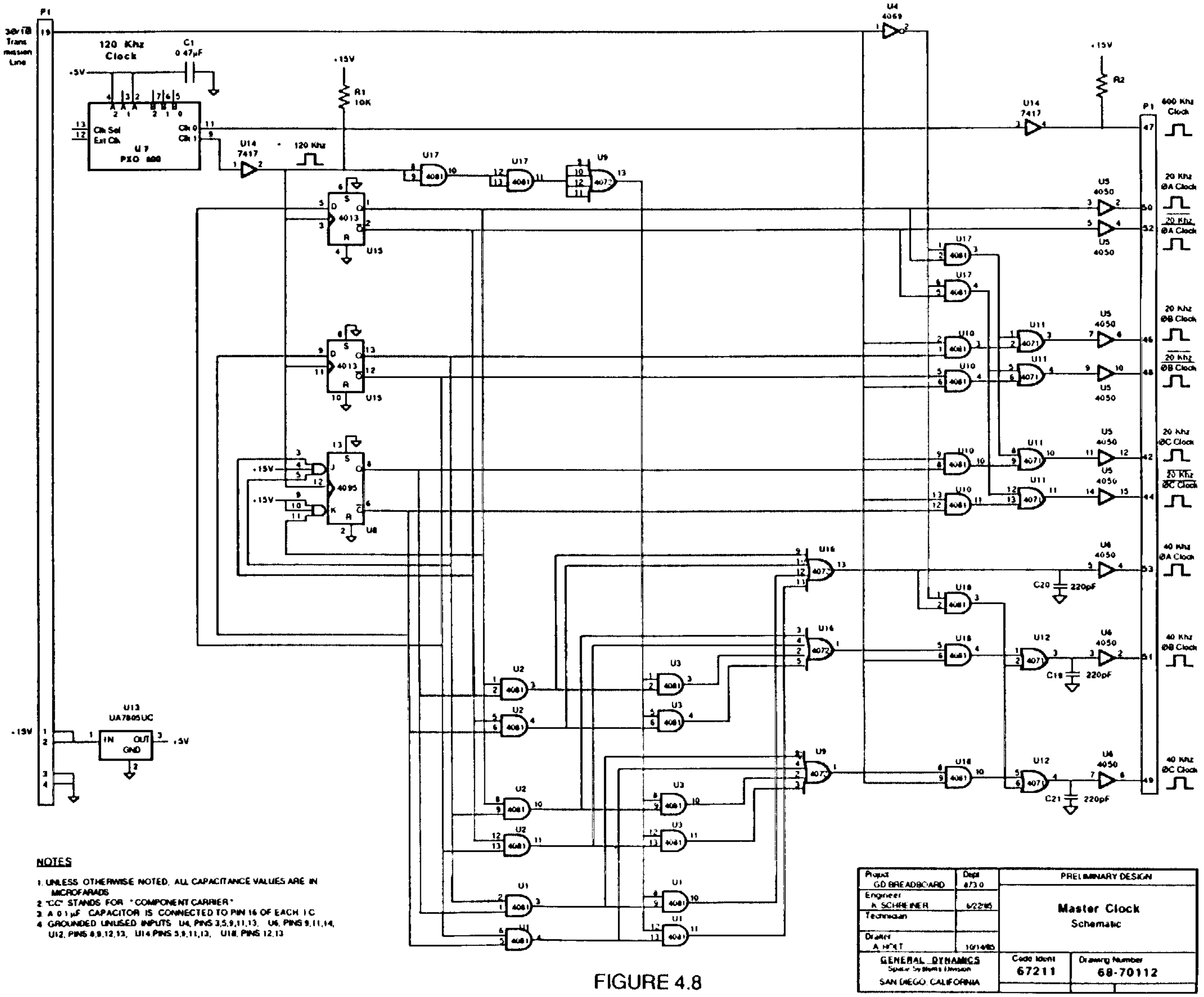
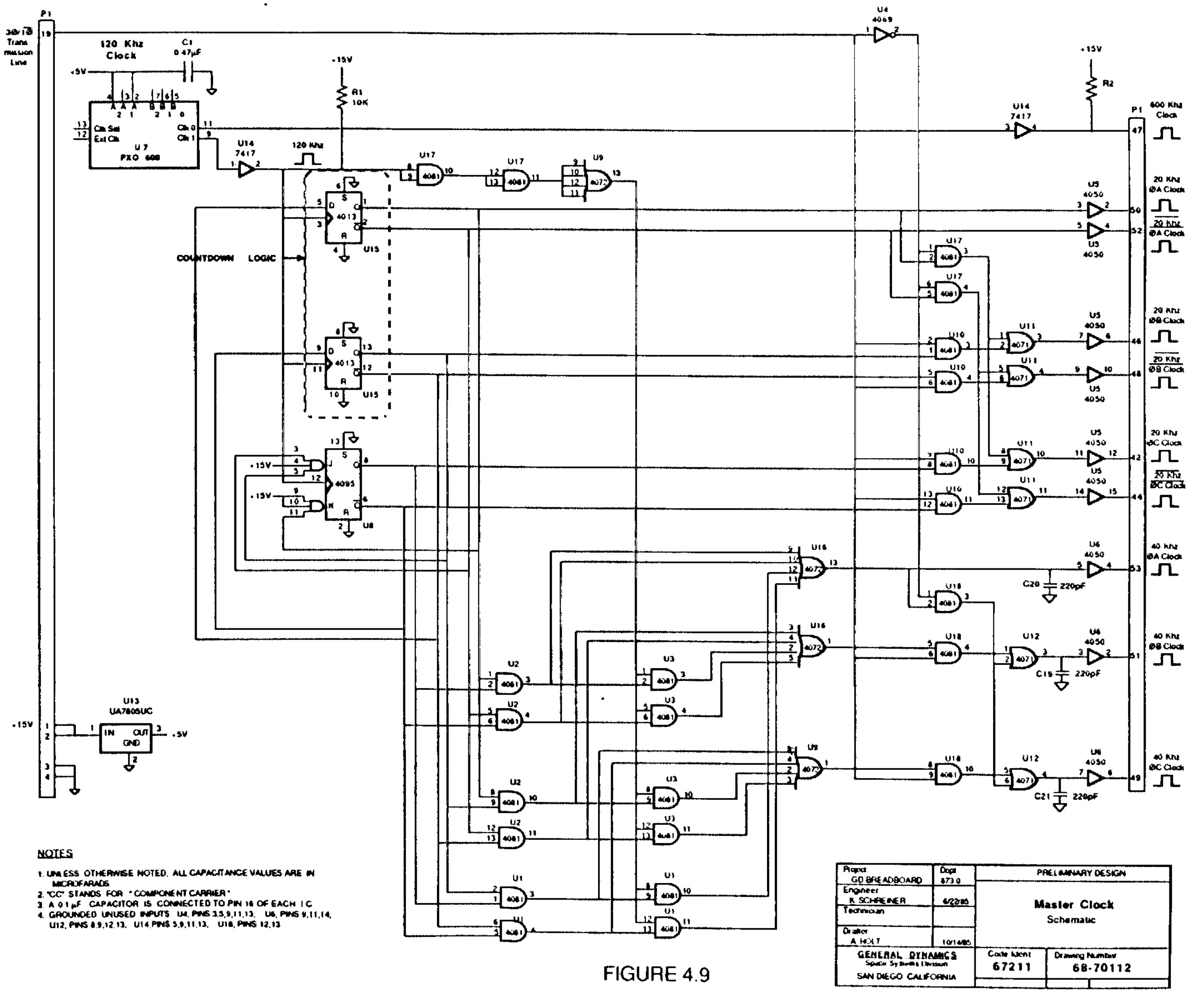


NOTES

1. UNLESS OTHERWISE NOTED, ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. "CC" STANDS FOR "COMPONENT CARRIER"
3. A 0.1 µF CAPACITOR IS CONNECTED TO PIN 16 OF EACH I.C.
4. GROUNDED UNUSED INPUTS U4, PINS 3,5,9,11,13, U6, PINS 9,11,14, U12, PINS 8,9,12,13, U14 PINS 5,9,11,13, U18, PINS 12,13

Project GD BREADBOARD
Dept 4730
Engineer K. SCHREINER 6/22/85
Technician
Drafter A. HOLT 10/14/85
GENERAL DYNAMICS
Space Systems Division
SAN DIEGO, CALIFORNIA
PRELIMINARY DESIGN
Master Clock
Schematic
Code Ident 67211
Drawing Number 68-70112

FIGURE 4.8



NOTES

1. UNLESS OTHERWISE NOTED, ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. "CC" STANDS FOR "COMPONENT CARRIER"
3. A 0.1 μF CAPACITOR IS CONNECTED TO PIN 16 OF EACH I.C.
4. GROUNDED UNUSED INPUTS U4, PINS 3,5,9,11,13, U6, PINS 9,11,14, U12, PINS 8,9,12,13, U14, PINS 5,9,11,13, U18, PINS 12,13

FIGURE 4.9

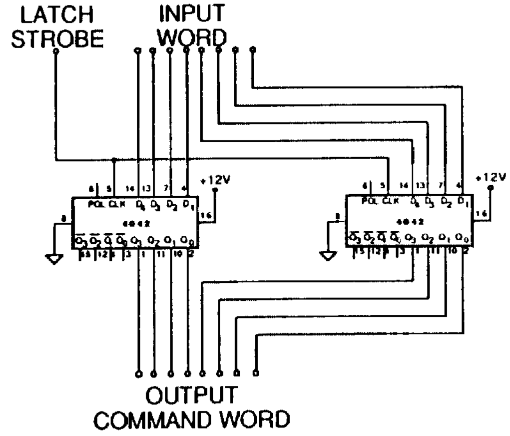


FIGURE 4.10 FIXED COMMAND INPUT LATCH

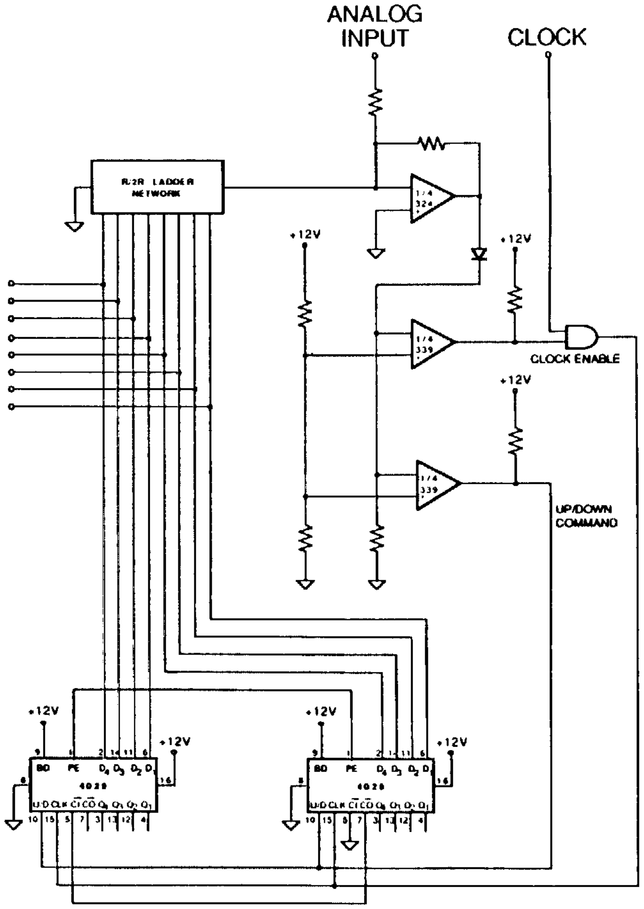


FIGURE 4.11 FIXED COMMAND INPUT LATCH

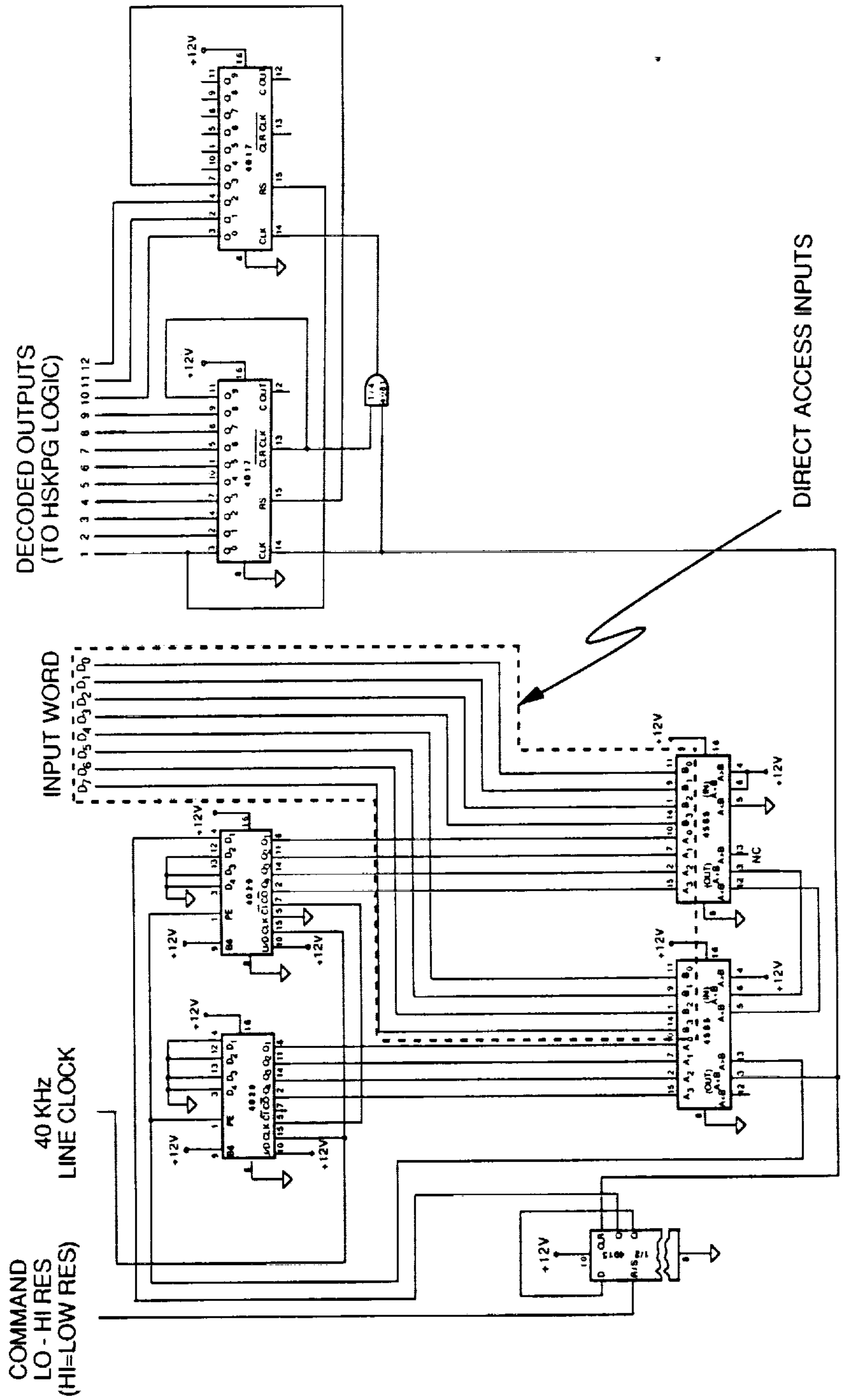


FIGURE 4.12 LOW FREQUENCY OUTPUT SYNTHESIS MODULE

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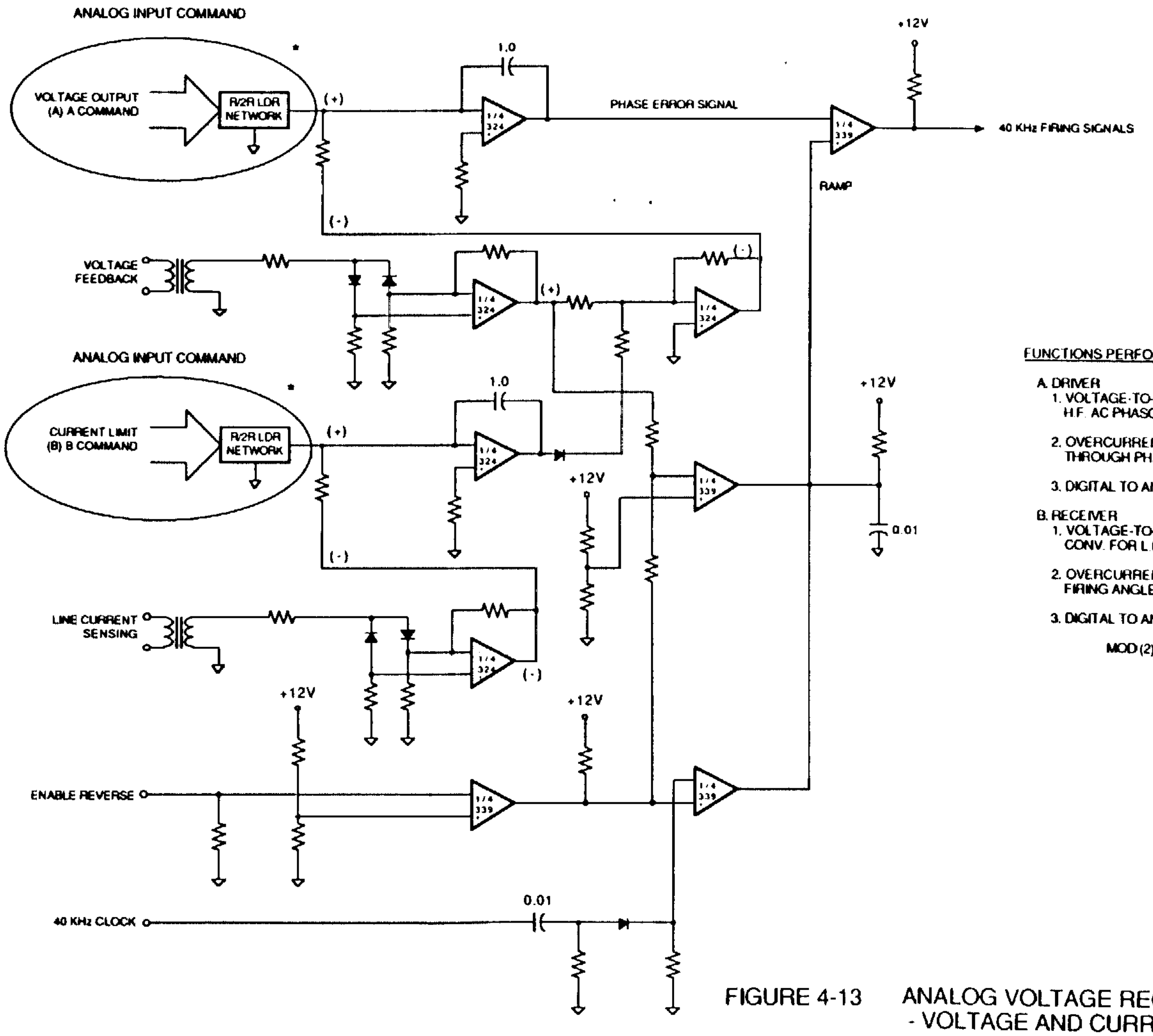

FUNCTIONS PERFORMED

A. DRIVER
  1. VOLTAGE-TO-PHASE CONV. FOR H.F. AC PHASOR REGULATION
  2. OVERCURRENT LIMITING THROUGH PHASE CONTROL
  3. DIGITAL TO ANALOG REF. CONV.

B. RECEIVER
  1. VOLTAGE-TO-FIRING ANGLE CONV. FOR L.F. AMPLITUDE CONTROL
  2. OVERCURRENT LIMITING THROUGH FIRING ANGLE CONTROL
  3. DIGITAL TO ANALOG REF. CONV.

MOD (2)

FIGURE 4-13 ANALOG VOLTAGE REGULATOR LOOP - VOLTAGE AND CURRENT LIMITING

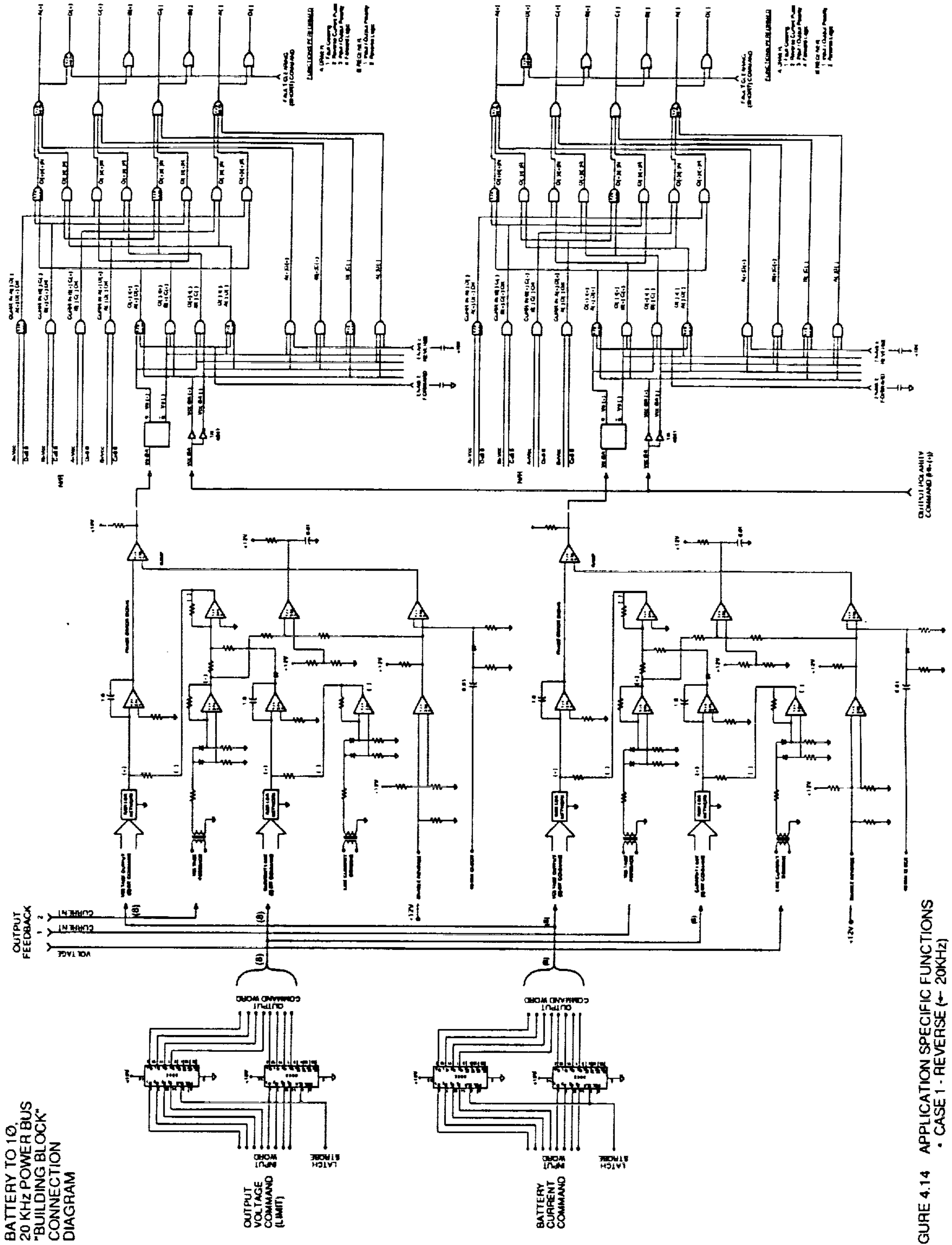

FIGURE 4.14 APPLICATION SPECIFIC FUNCTIONS
• CASE 1 - REVERSE (← 20KHz)

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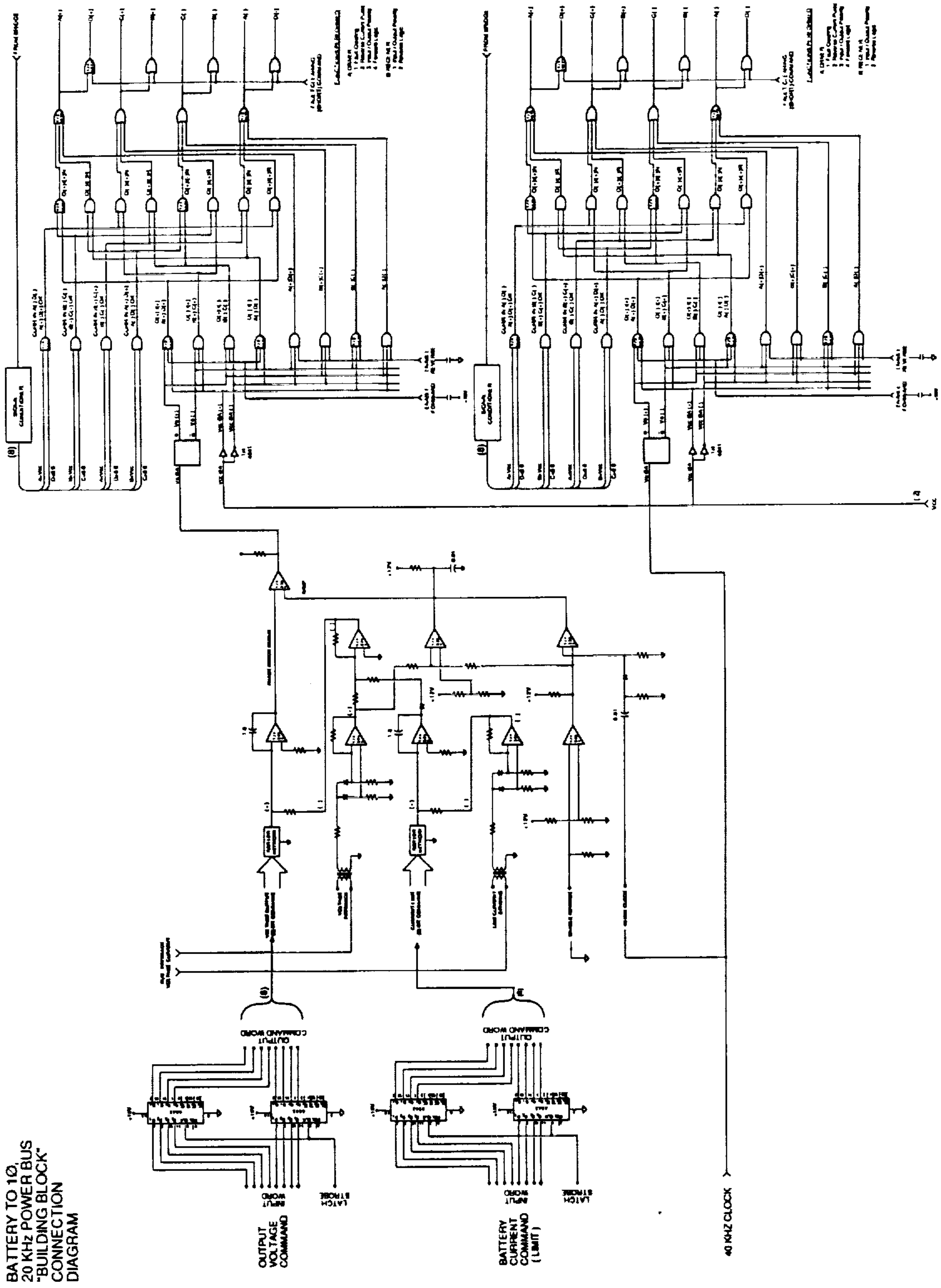

FIGURE 4.15 APPLICATION SPECIFIC FUNCTIONS
• CASE 1 - FORWARD (→ 20KHz)

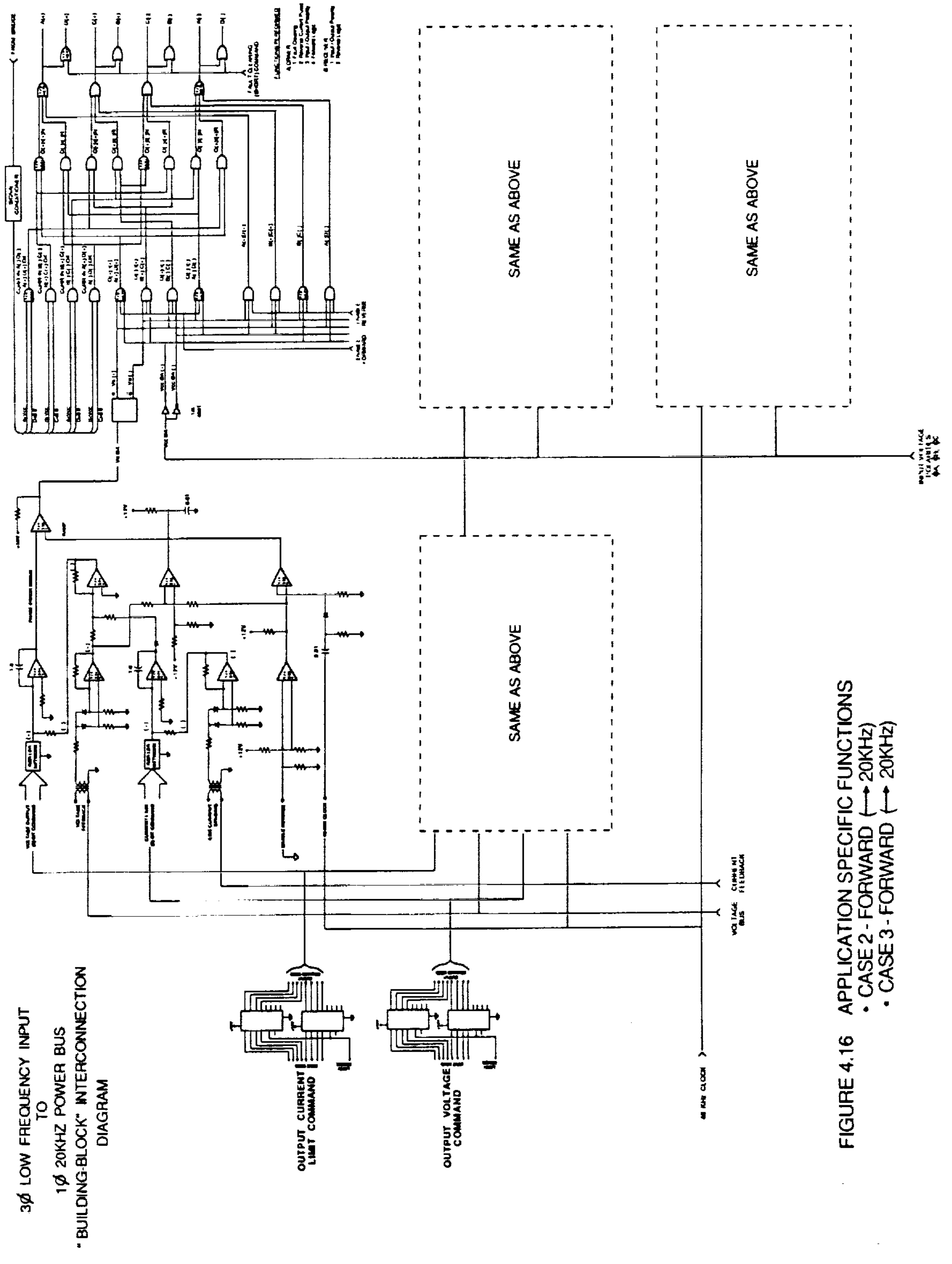

FIGURE 4.16 APPLICATION SPECIFIC FUNCTIONS
• CASE 2 - FORWARD (⟷ 20KHz)
• CASE 3 - FORWARD (⟷ 20KHz)

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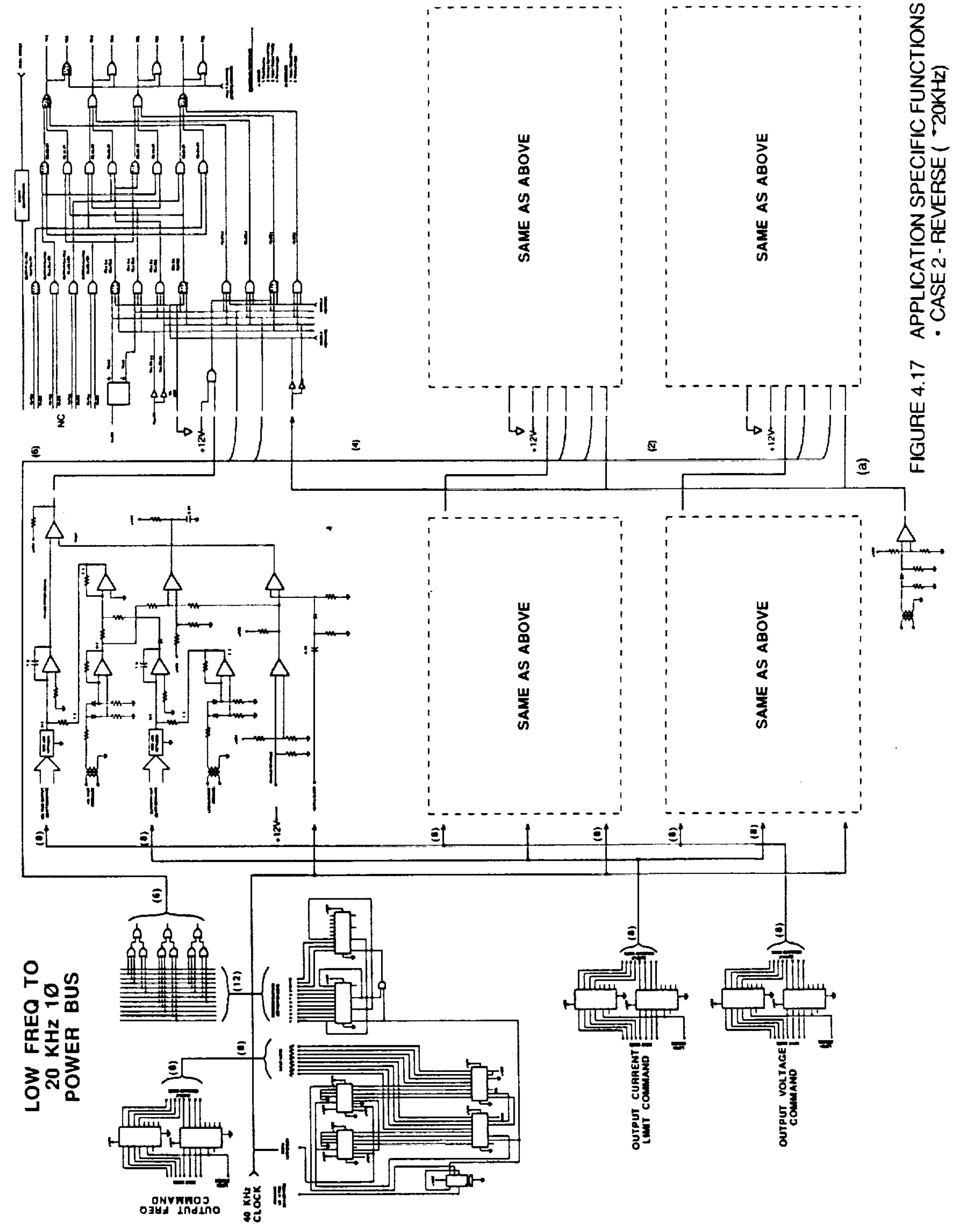


FIGURE 4.17 APPLICATION SPECIFIC FUNCTIONS
• CASE 2 - REVERSE (~20KHz)

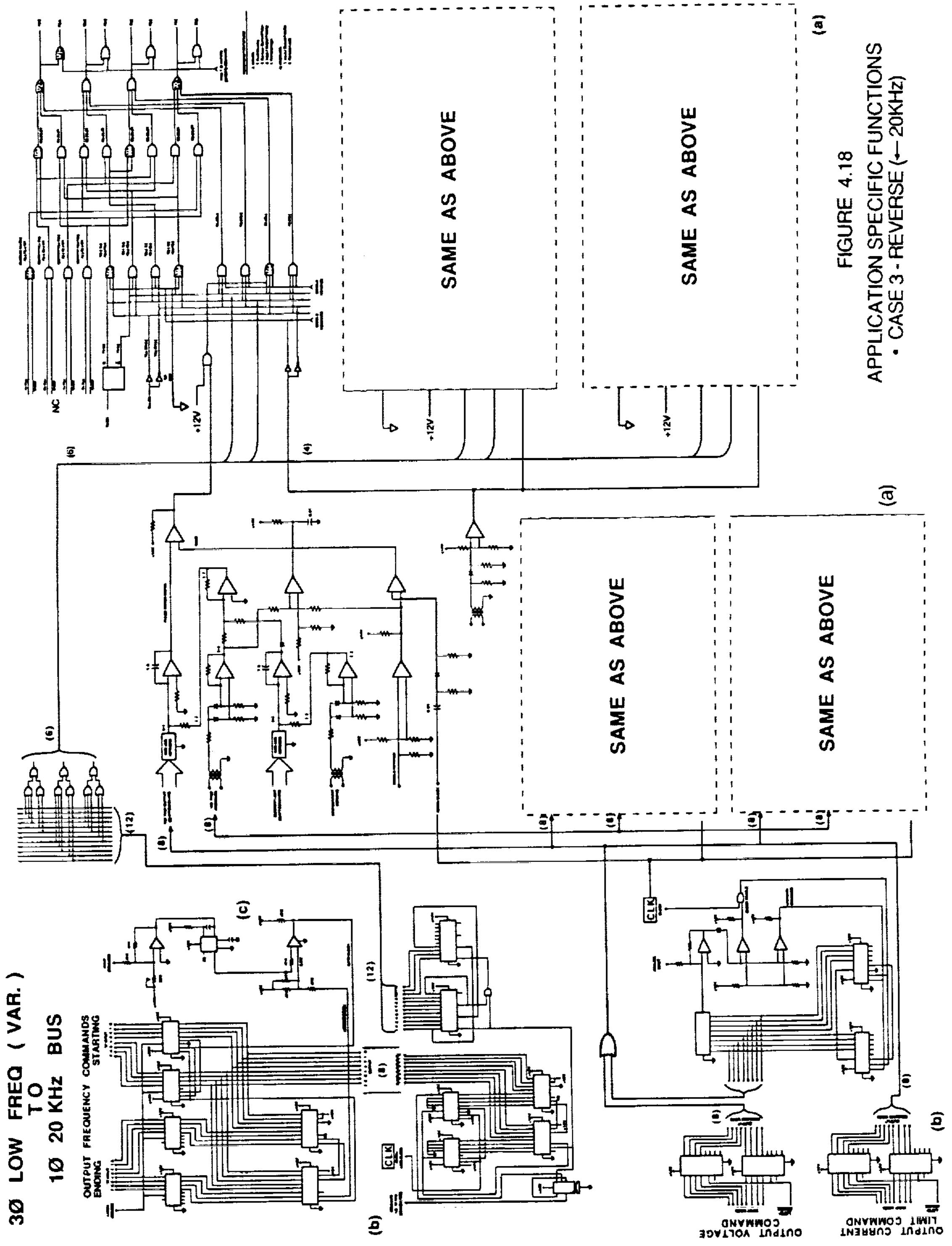
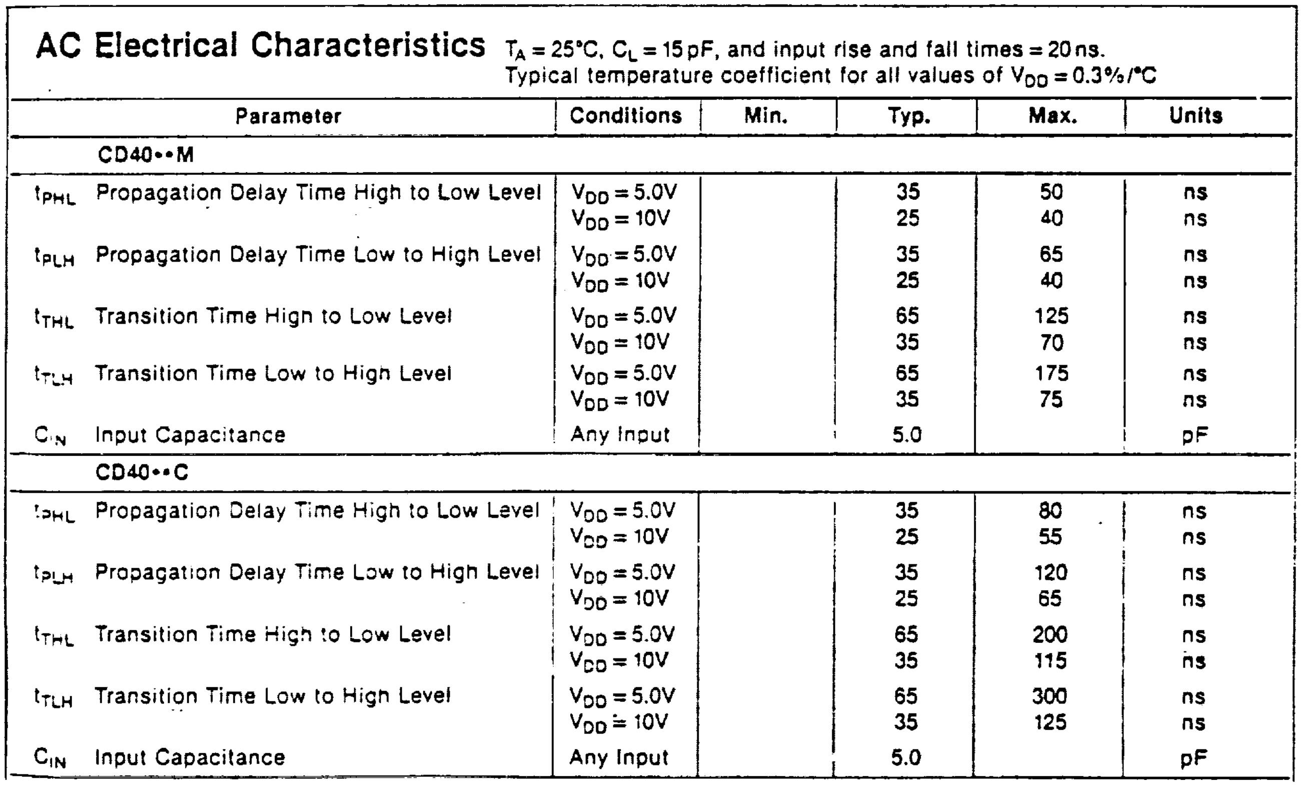


FIGURE 4.18
APPLICATION SPECIFIC FUNCTIONS
• CASE 3 - REVERSE (← 20KHz)

9.0 Tables

This Chapter is a collection of the tables from the main body of this report. They are numbered in accordance with the original chapter in which their reference first appears.

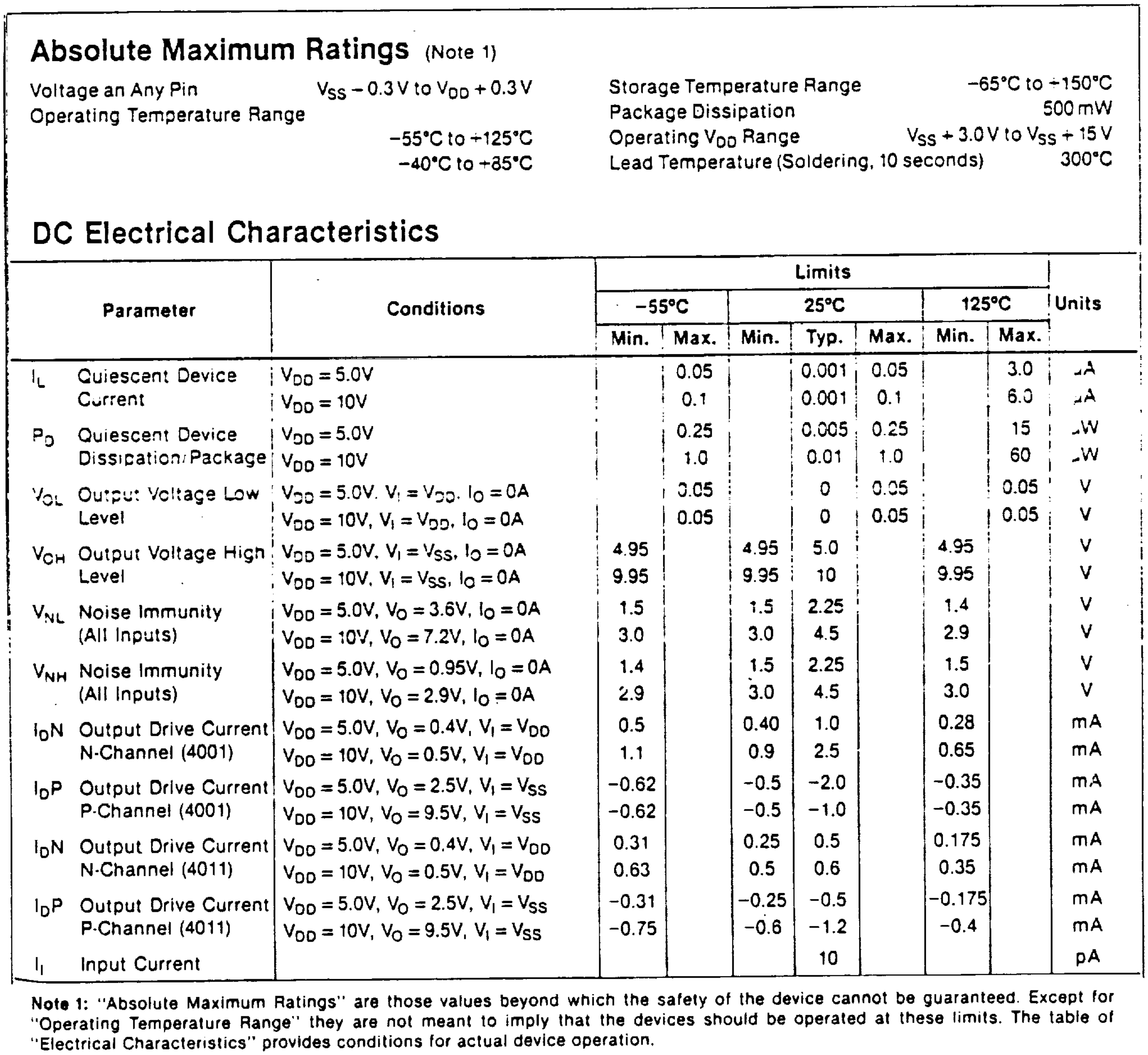
Table 3-1, Control Interface Specifications (continued)



AC Electrical Characteristics $T_A = 25°C$, $C_L = 15 pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
	CD40••M					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	50	ns
		$V_{DD} = 10V$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	65	ns
		$V_{DD} = 10V$		25	40	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$		65	125	ns
		$V_{DD} = 10V$		35	70	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$		65	175	ns
		$V_{DD} = 10V$		35	75	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
	CD40••C					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	80	ns
		$V_{DD} = 10V$		25	55	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	120	ns
		$V_{DD} = 10V$		25	65	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$		65	200	ns
		$V_{DD} = 10V$		35	115	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$		65	300	ns
		$V_{DD} = 10V$		35	125	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

Table 3-1, Control Interface Specifications



Absolute Maximum Ratings (Note 1)

Voltage an Any Pin	$V_{SS}-0.3\,V$ to $V_{DD}+0.3\,V$
Operating Temperature Range	−55°C to +125°C −40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS}+3.0\,V$ to $V_{SS}+15\,V$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Parameter		Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Device Current	$V_{DD}=5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD}=10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD}=10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V$, $V_I=V_{SS}$, $I_O=0A$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V$, $V_I=V_{SS}$, $I_O=0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=3.6V$, $I_O=0A$	1.5		1.5	2.25		1.4		V
		$V_{DD}=10V$, $V_O=7.2V$, $I_O=0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=0.95V$, $I_O=0A$	1.4		1.5	2.25		1.5		V
		$V_{DD}=10V$, $V_O=2.9V$, $I_O=0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4001)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4001)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4011)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4011)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

10.0 References

1. **"Study of Power Management Technology for Orbital Multi-100kWe Applications"**; Final Report, NASA CR 159834; J.W.Mildice, General Dynamics, Convair Division

2. **"Study of Multi-Megawatt Technology Needs for Photovoltaic Space Power Systems"**; Final Report, NAS 3-21951; D.M.Peterson, General Dynamics, Convair Division

3. **"An SCR Inverter with Good Regulation Sine-Wave Output"**; Neville Mapham, IEEE Transactions on Industry and General Applications; IGA-3, No. 2, Apr-May, 1967

4. **"Bidirectional Four Quadrant (BD4Q) Power Converter Development"**, Final Report, NASA CR 159660, F.C.Schwarz, Power Electronics Assoc. Inc.

5. **"Predicting Modulator Phase Lag in PWM Converter Feedback Loops"**, R. D. Middlebrook, Powercon 8, April 27-30, 1981

6. **"Controllable Four-Quadrant AC to DC and AC Converter Employing an Integral High Frequency Series Resonant Link"**; U.S.Patent 4,096,557, June, 1978

7. **"A Practical Resonant Converter Using High Speed Power Darlington Transistors"**; Suridar R. Babu, General Electric Co., Auburn, NY, PCI March, 1982 Proceedings, pp 122-141

8. **"Advances in Series Resonant Inverter Technology and Its Effect on Spacecraft Employing Electric Propulsion"**; R.R.Robson, Hughes Research Labs, Malibu, CA, presented at AIA/UASS/OGLR 16th International Electric Propulsion Conference, November, 1982.

Appendices

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Appendix A

Functional Requirements Specification

This appendix is a copy of the detailed Functional Requirements Specification, which was written to provide a set of requirements to which the hardware could actually be designed. It was approved by NASA LeRC prior to the hardware design phase of the program.

DESIGN REQUIREMENTS SPECIFICATION

Bi-Directional Power Control Electronics Unit

NASA Contract: NAS 3-23878

1.0 GENERAL

This controller is a device which provides the interface and control functions between the power handling devices and the supervisory system computer outputs for bi-directional power conversion between DC or low-frequency AC and the high-frequency AC power transmission bus. While the basic design is for computer control through parallel digital words, the hardware delivered on this contract shall be capable of operation from set-points commanded by manual inputs from the unit control panel.

1.1 The overall system actions performed by the integrated computer (or manual control) - controller - power switch combination are supplied by a family of modules, having the following characteristics:

1.1.1 Generator Interface - Takes variable, low frequency, engine-driven generator power and transforms it to controlled, high-fixed-frequency, AC distribution bus power.

1.1.2 Motor Interface - Provides variable frequency, variable voltage start, and run power to AC three-phase actuator and/or synchronous (PM) and induction starting motors for airborne functions, from the high-frequency AC distribution bus.

1.1.3 Battery Interface - Acts as a battery charger to interface the battery system with the high-frequency AC distribution busses. In its source mode, it converts battery power to high-frequency AC distribution bus power. The combination acts as the source for an uninterruptable power system.

1.1.4 Ground Power Interface - Provides power in either direction between the high-frequency AC distribution system and a three-phase AC ground power supply operating at 60 or 400 Hz.

2.0 APPLICABLE DOCUMENTS

The following documents, to the extent specified herein, shall apply to the design, construction, and documentation of this controller.

2.1 Contract NAS 3-23878

2.2 MIL-STD-746A, for EMI design considerations

2.3 MIL-HNDBK-217B, for reliability and failure rate considerations, to evaluate selective design component redundancy.

2.4 GDC-ACW67-006, Report Writer's Guide; for reports and documentation

2.5 Division Standard Practice - C90 Series; for hardware construction and documentation

3.0 FUNCTIONAL/OPERATIONAL DISCRIPTIONS

This unit acts as a "smart" electronic interface/controller between the electrical power system Mode Commands and the high power hardware in the system and performs the following specific functions:

3.1 Commanded Functions - in response to a digital word input simulated by a manually entered set-point from the control panel.

3.1.1 Output Amplitude Control - This is the basic steady-state output voltage or power. A D to A converter provides an analog output reference signal to be used by the output regulator. It is maintained with no further inputs until commanded to change.

3.1.2 Mode Control - Controls the basic nature of the three module types; determines whether they take power from the high-frequency AC distribution bus or supply power to it.

3.1.3 Time-varying Outputs - The motor/generator interface module shall be capable of accepting inputs to command variable motor/generator frequency or voltage and their rate of change. It can command a constant V/F ratio or current limit for motor starting.

3.1.4 Output Frequency - Setting of a steady-state output frequency for the motor interface to control motor speed.

3.1.5 Overload Limits - Output current and/or voltage, above and/or below which fault isolation action is required.

3.2 Data Functions

The following list of data measurement points shall be provided on the front panel of the unit. Values provided are nominals.

3.2.1 High frequency bus:
Frequency = 20.0 kHz
Voltage = 440/460 VRMS AC (LL)
Current = TBD
Phase Angle = TBD
Single-phase

3.2.2 Battery Charger Input/Output:
Voltage = 140/280 VDC

Current = TBD
Current or Voltage feedback mode flag

3.2.3 Auxiliary Ground Power Input/Output:
Voltage = 440/460 VRMS AC (LL)
Current = TBD
Frequency = 60 Hz
Three-phase

3.2.4 Variable-speed Motor/Generator Input:
Voltage = variable, 300-450 VAC RMS
Current = TBD
Frequency = variable, range TBD
Phase Angle = TBD
Three-phase or Six-phase

3.2.5 Variable-speed Motor/Generator Output:
Voltage = variable, range TBD
Current = variable, range TBD
Phase Angle = TBD
Frequency = variable, range 0 to 600 Hz, (current limited); range 600 to 1200 Hz, (voltage limited)
Three-phase or Six-phase

3.2.6 Starter/Generator shaft speed:
Output perameters consistant with Table 4-1
Frequency = variable, range TBD

3.2.7 Status Flags; Output perameters consistant with Table 4-1:
Current over limit
Voltage over limit
Voltage under limit
Energy flow direction
Fault status
Motor start/run

3.2.8 Current sink for reflex battery charger:
Characteristics and applicability TBD

3.3 Other Functions

3.3.1 Overload Limits - There are two levels of over current protection provided. The first raises an overload flag to the system controller advising of an out-of-spec condition that is not of immediate danger to the hardware. The second automatically turns the overloaded module off to protect itself.

3.3.2 Output Switch timing - shall be such that either/both transistors and thyristors can be used as the main power switch elements.

4.0 ELECTRONIC INTERFACE - DETAILED SPECIFICATIONS

4.1 Power Supply Inputs:

4.1.1 Operating Voltage: 10.0 VDC to 14.0 VDC

4.1.2 Maximum Supply Voltage: 5.0 VDC to 17.0 VDC (for non-spec operation)

4.1.3 Damage Limits: (-)0.5 VDC to (+)20.0 VDC

4.1.4 Current: 1.0 amp, maximum, steady-state average

4.2 Control Interfaces

4.2.1 Set Point Control - "Dip" switches, with BCD encoded outputs, to simulate computer control inputs.

4.2.2 Command Organization - Eight bit parallel data, plus strobe.

4.2.3 Electrical Characteristics - as specified in table 4-1.

4.3 Control Outputs

All power control outputs are discrete commands, used to operate switched components, and have the characteristics specified in Table 4-1

4.4 Instrumentation Interface

All signals shall be preconditioned to the following limits:

4.4.1 Analog Inputs:
Input Voltage = 0.0 to 10.0 VDC
Input Current = 0.0 to 25.0 mA DC
Other characteristics in accordance with Table 4-1.

4.4.2 Discrete Inputs:
In accordance with Table 4-1.

Table 4-1, Control Interface Specifications

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin $V_{SS} - 0.3\,V$ to $V_{DD} + 0.3\,V$

Operating Temperature Range −55°C to −125°C
−40°C to −85°C

Storage Temperature Range −65°C to −150°C

Package Dissipation 500 mW

Operating V_{DD} Range $V_{SS} - 3.0\,V$ to $V_{SS} - 15\,V$

Lead Temperature (Soldering, 10 seconds) 300°C

DC Electrical Characteristics

Parameter	Conditions	Limits							Units
		−55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent Device Current	$V_{DD} = 5.0V$		0.05		0.001	0.05		3.0	µA
	$V_{DD} = 10V$		0.1		0.001	0.1		6.0	µA
P_D Quiescent Device Dissipation Package	$V_{DD} = 5.0V$		0.25		0.005	0.25		15	µW
	$V_{DD} = 10V$		1.0		0.01	1.0		60	µW
V_{OL} Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH} Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
	$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
	$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH} Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
	$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN Output Drive Current N-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP Output Drive Current P-Channel (4001)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN Output Drive Current N-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
	$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP Output Drive Current P-Channel (4011)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
	$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Table 4-1, Control Interface Specifications (continued)

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15 pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Parameter		Conditions	Min.	Typ.	Max.	Units
	CD40••M					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	50	ns
		$V_{DD} = 10V$		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	65	ns
		$V_{DD} = 10V$		25	40	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$		65	125	ns
		$V_{DD} = 10V$		35	70	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$		65	175	ns
		$V_{DD} = 10V$		35	75	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
	CD40••C					
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$		35	80	ns
		$V_{DD} = 10V$		25	55	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$		35	120	ns
		$V_{DD} = 10V$		25	65	ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$		65	200	ns
		$V_{DD} = 10V$		35	115	ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$		65	300	ns
		$V_{DD} = 10V$		35	125	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

5.0 MECHANICAL AND ENVIRONMENTAL

5.1 Mechanical design - The controller will be housed in a standard bench-top equipment cabinet. Each circuit subelement will be assembled on a plug-un wire-wrap board. Partitioning will be functionally based and sized so that each board is translatable into a hybrid integrated circuit. The cards will be mounted in a standard card cage and all controls and instrumentation points will be provided on the front panel. Access for more detailed measurements will be provided through removable cabinet panels and extender cards.

5.2 Environmental Requirements

5.2.1 Operating temperature range:
0 degrees C. to (+)50 degrees C.

5.2.2 Storage temperature range:
(-)65 degrees C. to (+)125 degrees C.

5.2.3 Vibration and Shock:
Normal handling in a laboratory environment.

5.2.4 EMI:
Designed (but not tested) to the requirements of MIL-STD-746A.

5.3 Input/Output Connectors:
(25) Pin RS-232 type. Both halves of all connectors shall be supplied as mating pairs.

Appendix B

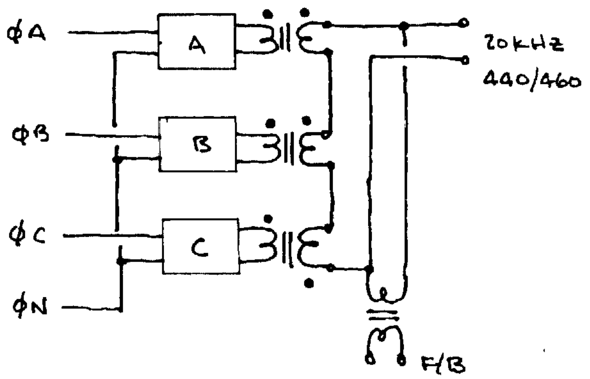
Functional Block Worksheets

These worksheets document the definition and development of the functional circuit blocks which were developed into standard functions to be used to construct the application-specific functions required by this program.

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: GROUND POWER INTERFACE
2. OPERATIONAL MODE: FORWARD OPERATION
3. INPUT POWER: 440/460 VAC RMS, THREE PHASE, 60 HZ OR 400 HZ
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: OUTPUT VOLTAGE
6. FEEDBACK QUANTITY: 20 KHZ LINE VOLTAGE
7. INTERMEDIATE CONTROL: PHASE DELAY FOR OUTPUT SWITCH SIGNALS
8. REFERENCE SOURCE: DIGITAL INPUT WORD – CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: "PHASOR" CONTROL OF SUMMED OUTPUTS FROM (3) MODULES



"FIRING" SIGNALS FOR THE SWITCHES FOR EACH OF THE THREE MODULES COME FROM THE SYSTEM CLOCK. ΦB & ΦC ARE DELAYED SO THE PHASOR-SUMMED OUTPUT VOLTAGE IS CONTROLLED. RANGE IS FROM 3X A SINGLE MODULE OUTPUT TO ZERO. CONTROL IS A CLOSED-LOOP RECTIFIER – INTEGRATOR – REFERENCE TYPE, WHICH IS AN UNCONDITIONALLY STABLE ONE-POLE CIRCUIT.

REQ'T - (3) ANALOG DELAY MODULES
(1) COMMAND INPUT MODULE

HARDWARE CODE: GPI-F-1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: GROUND POWER INTERFACE
2. OPERATIONAL MODE: FORWARD OPERATION
3. INPUT POWER: SEE GPI-F-1
4. OUTPUT POWER: SEE GPI-F-1

5. CONTROLLED PARAMETER: TRANSMISSION LINE CURRENT
6. FEEDBACK QUANTITY: LINE CURRENT - TRANSFORMER ISOLATED
7. INTERMEDIATE CONTROL: OUTPUT PHASE DELAY / FIRING SIGNAL DISABLE
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASOR CONTROL OF OUTPUT UNTIL MINIMUM OUTPUT VOLTAGE IS REACHED; THEREAFTER, BRIDGE IS DISABLED.

THRESHOLD WITH HYSTERESIS IS SET, BELOW WHICH THERE IS NO CURRENT CONTROL. LINEAR CONTROL IS SUPPLIED TO KEEP CURRENT BELOW THRESHOLD UNTIL VOLTAGE LOW LIMIT IS REACHED. FULL SHUT-OFF THEN ACTIVATED.

REQ'TS - (1) COMMAND INPUT MODULE
(1) THRESHOLD DETECTOR

HARDWARE CODE: GPI-F-2

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: GROUND POWER INTERFACE
2. OPERATIONAL MODE: REVERSE OPERATION
3. INPUT POWER: 440/460 VRMS AC, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, 60 HZ OR 400 HZ

5. CONTROLLED PARAMETER: OUTPUT "PHASE" VOLTAGE
6. FEEDBACK QUANTITY: 60 HZ OR 400 HZ (3) OUTPUT VOLTAGES
7. INTERMEDIATE CONTROL: PHASE DELAY FOR PARTIAL 20 KHZ PULSES TO OUTPUTS
8. REFERENCE SOURCE: DIGITAL INPUT WORD – CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASE DELAY "FIRING" CONTROL FOR OUTPUT SWITCHES @ 20 KHZ

"FIRING" SIGNALS FOR THE REVERSE SCR'S OR TRANSISTORS ARE GENERATED AT THE ZERO CROSSINGS OF THE 20KHZ TRANSMISSION LINE VOLTAGE. THOSE SIGNALS ARE DELAYED BETWEEN 0° AND 180° OF THE 20 KHZ SIGNAL BASED ON AN ANALOG ERROR SIGNAL, WHICH COMPARES THE MEASURED OUTPUT VOLTAGE (AC) WITH THE INPUT REFERENCE (COMMANDED VOLTAGE). SAME ONE-POLE CONTROL LOOP AS GPI-F-1.

REQ'T – (1) INPUT COMMAND MODULE
(1) D→A CONVERTER
(3) FIRING ANGLE CONTROL

HARDWARE CODE: GPI-R-1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: GROUND POWER INTERFACE
2. OPERATIONAL MODE: REVERSE OPERATION
3. INPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, 60 HZ OR 400 HZ

5. CONTROLLED PARAMETER: OUTPUT FREQUENCY
6. FEEDBACK QUANTITY: — OPEN LOOP
7. INTERMEDIATE CONTROL: OUTPUT SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: 60 HZ OR 400 HZ LINE
9. IMPLEMENTATION: CONTROL TO STEER 20 KHZ RECTIFIED OUTPUT PULSES TO PROVIDE PROPER POLARITY TO APPROPRIATE PHASES.

SIGNALS "STEERED" TO APPROPRIATE BRIDGE SWITCHES AND MODULES TO APPLY OUTPUTS TO APPROPRIATE PHASES BASED ON PATTERNS STORED IN EPROM'S AND FREQUENCY COMMANDED BY INPUT. (400 HZ OR 60 HZ)

REQ'T - (1) COMMAND INPUT MODULE
(1) FREQUENCY SYNTHESIS MODULE

HARDWARE CODE: GPI-R-2

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: GROUND POWER INTERFACE
2. OPERATIONAL MODE: REVERSE OPERATION
3. INPUT POWER: SEE GPI-R-1,
4. OUTPUT POWER: SEE GPI- R-1,

5. CONTROLLED PARAMETER: OUTPUT CURRENT LIMITING
6. FEEDBACK QUANTITY: LINE CURRENT
7. INTERMEDIATE CONTROL: OUTPUT SWITCH "FIRING" ANGLES
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASE DELAY OR TURN-OFF OF "FIRING" SIGNALS FOR OUTPUT SWITCHES BASED ON COMPARISON WITH INPUT REFERENCE.

FIRING SIGNALS CONTROLLED WITH HIGH GAIN OR DISABLED BASED ON THRESHOLD WITH HYSTERESIS.

SINGLE POLE CONTROL SAME AS GPI-F-1

REQ'TS - (1) COMMAND INPUT
(3) THRESHOLD DETECTORS

HARDWARE CODE: GPI- R-3

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: ON-BOARD BATTERY CHARGING
2. OPERATIONAL MODE: FOREWARD (CHARGING) OPERATION
3. INPUT POWER: 440/460 VACRMS, SINGLE PHASE, 20KHZ
4. OUTPUT POWER: BATTERY CHARGING CURRENT, 140/280 VDC @ TBD ADC.

5. CONTROLLED PARAMETER: OUTPUT CURRENT
6. FEEDBACK QUANTITY: DC OUTPUT CURRENT – CURRENT SHUNT VOLTAGE
7. INTERMEDIATE CONTROL: FIRING ANGLES FOR 20KHZ RECTIFIED OUTPUT PULSES
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASE DELAY "FIRING" CONTROL FOR OUTPUT SWITCHES

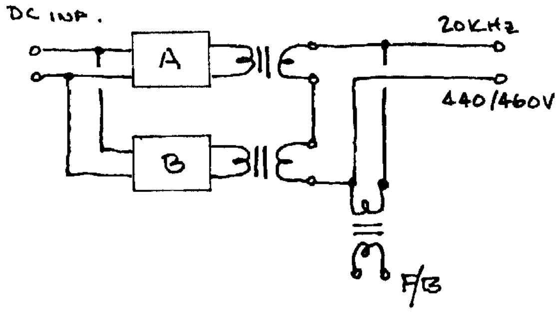
SAME AS GPI-R-1

HARDWARE CODE: OBC-F-1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: ON-BOARD BATTERY CHARGING
2. OPERATIONAL MODE: REVERSE (ENERGIZE POWER LINE) OPERATION
3. INPUT POWER: 140/280 VDC
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: OUTPUT VOLTAGE
6. FEEDBACK QUANTITY: 20 KHZ LINE VOLTAGE
7. INTERMEDIATE CONTROL: PHASE DELAY FOR OUTPUT SWITCH SIGNALS
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: "PHASOR" CONTROL OF SUMMED OUTPUTS FROM (2) MODULES



CONTROL IS THE SAME AS GPI-F-1

REQ'T - (1) COMMAND INPUT MODULE
(2) ANALOG DELAY MODULES

HARDWARE CODE: OBC - R - 1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: ON- BOARD BATTERY CHARGING
2. OPERATIONAL MODE: REVERSE (ENERGIZE POWER LINE) OPERATION
3. INPUT POWER: SEE OBC -R-1
4. OUTPUT POWER: SEE OBC - R- 1

5. CONTROLLED PARAMETER: LINE CURRENT
6. FEEDBACK QUANTITY: LINE CURRENT - TRANSFORMER ISOLATED
7. INTERMEDIATE CONTROL: SAME AS GPI- F-2
8. REFERENCE SOURCE: SAME AS GPI-F-2
9. IMPLEMENTATION: SAME AS GPI-F-2

SAME AS GPI-F-2

HARDWARE CODE: OBC - R-2

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CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: VARIABLE SPEED STARTING / GENERATION
2. OPERATIONAL MODE: REVERSE (STARTING) OPERATION
3. INPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, VARIABLE FREQUENCY; CURRENT LIMITED 0 TO 600 HZ, VOLTAGE LIMITED 600 TO 1200 HZ
5. CONTROLLED PARAMETER: OUTPUT VOLTAGE
6. FEEDBACK QUANTITY: LOW FREQUENCY, THREE PHASE OUTPUT VOLTAGE
7. INTERMEDIATE CONTROL: FIRING ANGLES FOR 20KHZ RECTIFIED OUTPUT PULSES
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASE DELAY" FIRING "CONTROL FOR OUTPUT SWITCHES.

SAME AS GPI-R-1

HARDWARE CODE: MGI - R-1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: VARIABLE SPEED STARTING / GENERATION
2. OPERATIONAL MODE: REVERSE (STARTING) OPERATION
3. INPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, VARIABLE FREQUENCY, CURRENT LIMITED 0 TO 600 HZ, VOLTAGE LIMITED 600 TO 1200 HZ
5. CONTROLLED PARAMETER: OUTPUT CURRENT
6. FEEDBACK QUANTITY: LOW FREQUENCY, THREE PHASE OUTPUT CURRENT
7. INTERMEDIATE CONTROL: FIRING ANGLES FOR 20 KHZ RECTIFIED OUTPUT PULSES
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: PHASE DELAY "FIRING" CONTROL FOR OUTPUT SWITCHES.

SAME AS GPI-R-3

HARDWARE CODE: MGI-R-2

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: VARIABLE SPEED STARTING / GENERATION
2. OPERATIONAL MODE: REVERSE (STARTING) OPERATION
3. INPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, VARIABLE FREQUENCY, 0 TO 600 HZ AND 600 TO 1200 HZ
5. CONTROLLED PARAMETER: OUTPUT FREQUENCY TO THREE PHASES
6. FEEDBACK QUANTITY: — OPEN LOOP
7. INTERMEDIATE CONTROL: OUTPUT SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: ANALOG SIGNAL - RATE OF CHANGE OF FREQUENCY (CONT)
9. IMPLEMENTATION: CONTROL TO STEER 20 KHZ RECTIFIED OUTPUT PULSES.

8. CONTINUED: DIGITAL WORD - STARTING FREQUENCY
DIGITAL WORD - FINAL FREQUENCY

SAME AS GPI-R-2, EXCEPT FOR DIFFERENT FREQUENCIES

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HARDWARE CODE: MGI-R-3

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: VARIABLE SPEED STARTING / GENERATION
2. OPERATIONAL MODE: REVERSE (STARTING) OPERATION, INDUCTION STARTER.
3. INPUT POWER: 440/460 VRMS AC, SINGLE PHASE, 20 KHZ
4. OUTPUT POWER: 440/460 VAC RMS, THREE PHASE, VARIABLE FREQUENCY 150 HZ TO 600 HZ CURRENT LIMITING
5. CONTROLLED PARAMETER: OUTPUT FREQUENCY - THREE PHASE
6. FEEDBACK QUANTITY: OUTPUT CURRENT
7. INTERMEDIATE CONTROL: OUTPUT SWITCH FIRING SIGNALS
8. REFERENCE SOURCE: DIGITAL WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: CONTROL TO STEER 20 KHZ RECTIFIED OUTPUT PULSES.

SAME AS GPI-R-3

HARDWARE CODE: MGI-R-4

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: VARIABLE SPEED STARTING / GENERATION
2. OPERATIONAL MODE: FORWARD (GENERATION) OPERATION
3. INPUT POWER: 300 VAC RMS @ 1700 HZ → 450 VAC RMS @ 2500 HZ, SIX PHASE
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: OUTPUT VOLTAGE
6. FEEDBACK QUANTITY: OUTPUT LINE VOLTAGE
7. INTERMEDIATE CONTROL: PHASE DELAY FOR OUTPUT SWITCH SIGNALS
8. REFERENCE SOURCE: DIGITAL INPUT WORD - CONVERTED TO ANALOG REFERENCE
9. IMPLEMENTATION: "PHASOR" CONTROL OF SUMMED OUTPUTS FROM (3) MODULES

TWO THREE-PHASE INTERFACES WILL BE USED FOR THIS CONTROL.

THEY ARE EACH THE SAME AS GPI-F-1

REQ'T - (6) ANALOG DELAY MODULES
(1) COMMAND INPUT MODULE

HARDWARE CODE: MGI-F-1

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: BRIDGE DRIVER FAULT PROTECTION (OL)
2. OPERATIONAL MODE: FORWARD OPERATION OF DRIVER MODULES
3. INPUT POWER: AC OR DC
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: BRIDGE DRIVER SWITCH PAIR CANNOT BE TURNED "ON" UNLESS OPPOSITE SIDE HAS TURNED "OFF"
6. FEEDBACK QUANTITY: NEGATIVE CURRENT IN OPPOSITE SIDE PAIR
7. INTERMEDIATE CONTROL: POWER SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: NONE
9. IMPLEMENTATION: DISABLE FIRING SIGNALS TO A BRIDGE SWITCH PAIR UNTIL NEGATIVE CURRENT IS FLOWING IN THE OPPOSITE PAIR.

HOUSEKEEPING LOGIC – PART OF OUTPUT INTERFACE
– NOT AN ANALOG CONTROL LOOP
(STABILITY NOT AN ISSUE)

HARDWARE CODE: DFP (OL)

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: LINE FAULT CLEARING - TEMP. BRIDGE SHORT (OL)
2. OPERATIONAL MODE: FORWARD OPERATION OF DRIVER MODULES
3. INPUT POWER: AC FROM FACILITY SUPPLY OR GENERATOR
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: SHORT DRIVER BRIDGE TO PROVIDE ZERO VDC TO OUTPUT
6. FEEDBACK QUANTITY: LOAD FAULT DETECTION SIGNAL
7. INTERMEDIATE CONTROL: POWER SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: LOAD FAULT THRESHOLD SETTING
9. IMPLEMENTATION: LOGIC TO OVER RIDE BRIDGE INPUT SHORT INHIBIT AND PROVIDE SIMULTANEOUS "FIRE" SIGNALS TO ON SIDE OF A BRIDGE DRIVER, SHORTING THE INPUT.

HOUSEKEEPING LOGIC - PART OF OUTPUT INTERFACE
- NOT AN ANALOG CONTROL LOOP (STABILITY NOT AN ISSUE)

HARDWARE CODE: LFC (OL)

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: TRANSMISSION LINE FREQUENCY CONTROL (HOUSEKEEPING)
2. OPERATIONAL MODE: FREQUENCY CONTROL FOR ALL MODULES SUPPLYING 20KHZ
3. INPUT POWER: AC AND DC
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20KHZ

5. CONTROLLED PARAMETER: LINE FREQUENCY - 20 KHZ
6. FEEDBACK QUANTITY: — OPEN LOOP
7. INTERMEDIATE CONTROL: POWER SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: SYSTEM CLOCK
9. IMPLEMENTATION: SINGLE SYSTEM CLOCK, BUFFERED TO SUPPLY 20 KHZ AND 40 KHZ PULSES TO ALL MODULES, AS REQUIRED.

OSCILLATOR / COUNTER / CLOCK FUNCTION - NO CLOSED LOOP (STABILITY NOT AN ISSUE)

HARDWARE CODE: TLFC (H)

CONTROL FUNCTION - DEFINITION/REQUIREMENT

1. MAJOR FUNCTION: TRANSFORMER FLUX CONTROL (HOUSEKEEPING)
2. OPERATIONAL MODE: FORWARD OPERATION OF DRIVER MODULES
3. INPUT POWER: AC AND DC
4. OUTPUT POWER: 440/460 VAC RMS, SINGLE PHASE, 20 KHZ

5. CONTROLLED PARAMETER: PULSE DIRECTION TO DRIVER TRANSFORMERS, BASED ON DIRECTION OF LAST PULSE.
6. FEEDBACK QUANTITY: DIRECTION OF LAST PULSE
7. INTERMEDIATE CONTROL: POWER SWITCH "FIRING" SIGNALS
8. REFERENCE SOURCE: NONE
9. IMPLEMENTATION: MEMORY / LATCH INDICATING DIRECTION OF LAST PULSE
   DYNAMIC ONLY – NOT A REQUIREMENT WHEN ALL POWER IS OFF.

HOUSEKEEPING LOGIC – PART OF OUTPUT INTERFACE
– NOT AN ANALOG CONTROL LOOP (STABILITY NOT AN ISSUE)

HARDWARE CODE: TFC (H)

Appendix C

Schematics

These schematics represent the final designs for the various functional blocks, after the changes determined by the compatibility testing with the power hardware of the General Dynamics' breadboards, and the LeRC testbed.

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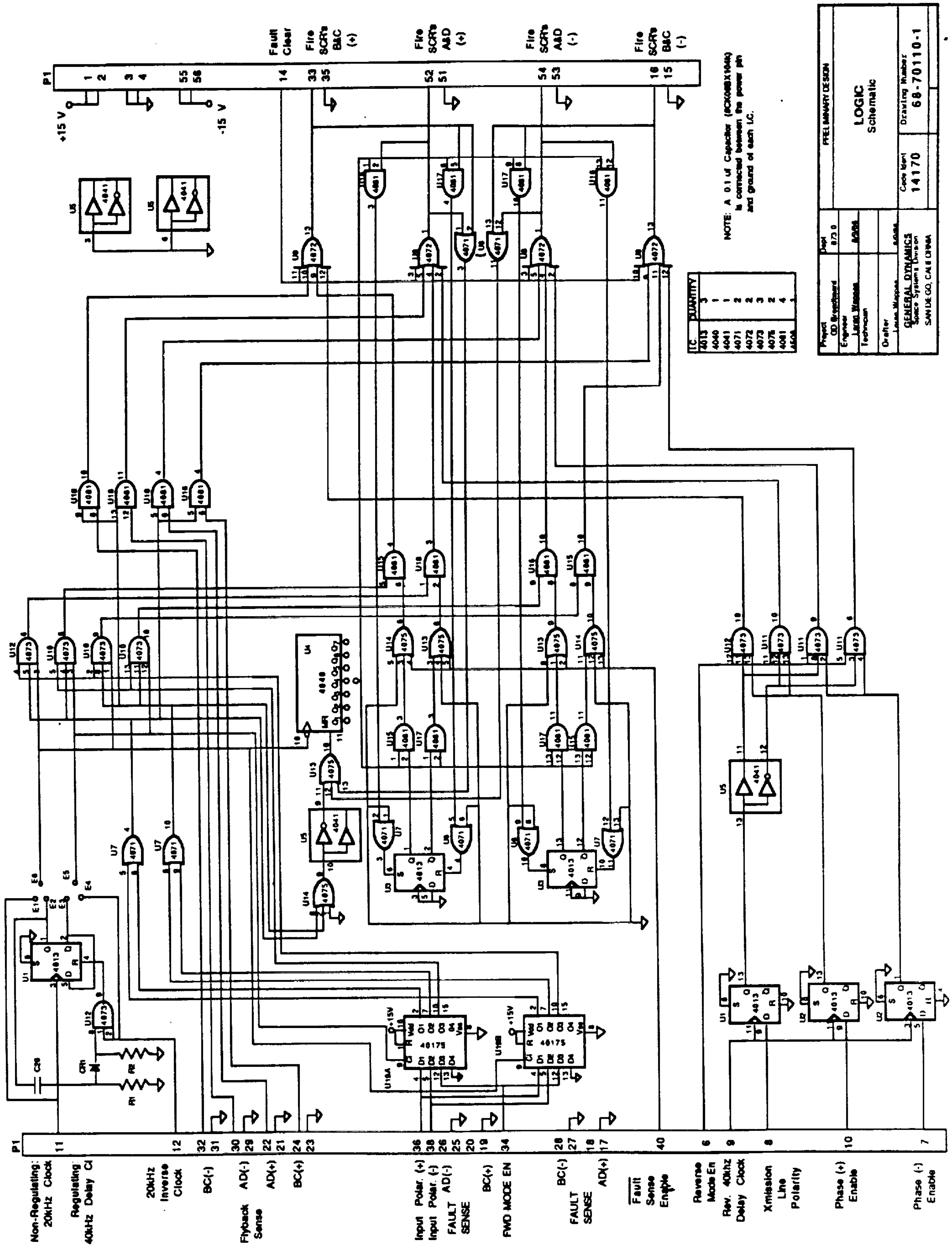

I.C.	QUANTITY
4013	3
4040	1
4041	1
4071	2
4072	2
4073	3
4075	2
4081	4
4504	1

NOTE: A 0.1 uf Capacitor (8CK068X104K) is connected between the power pin and ground of each I.C.

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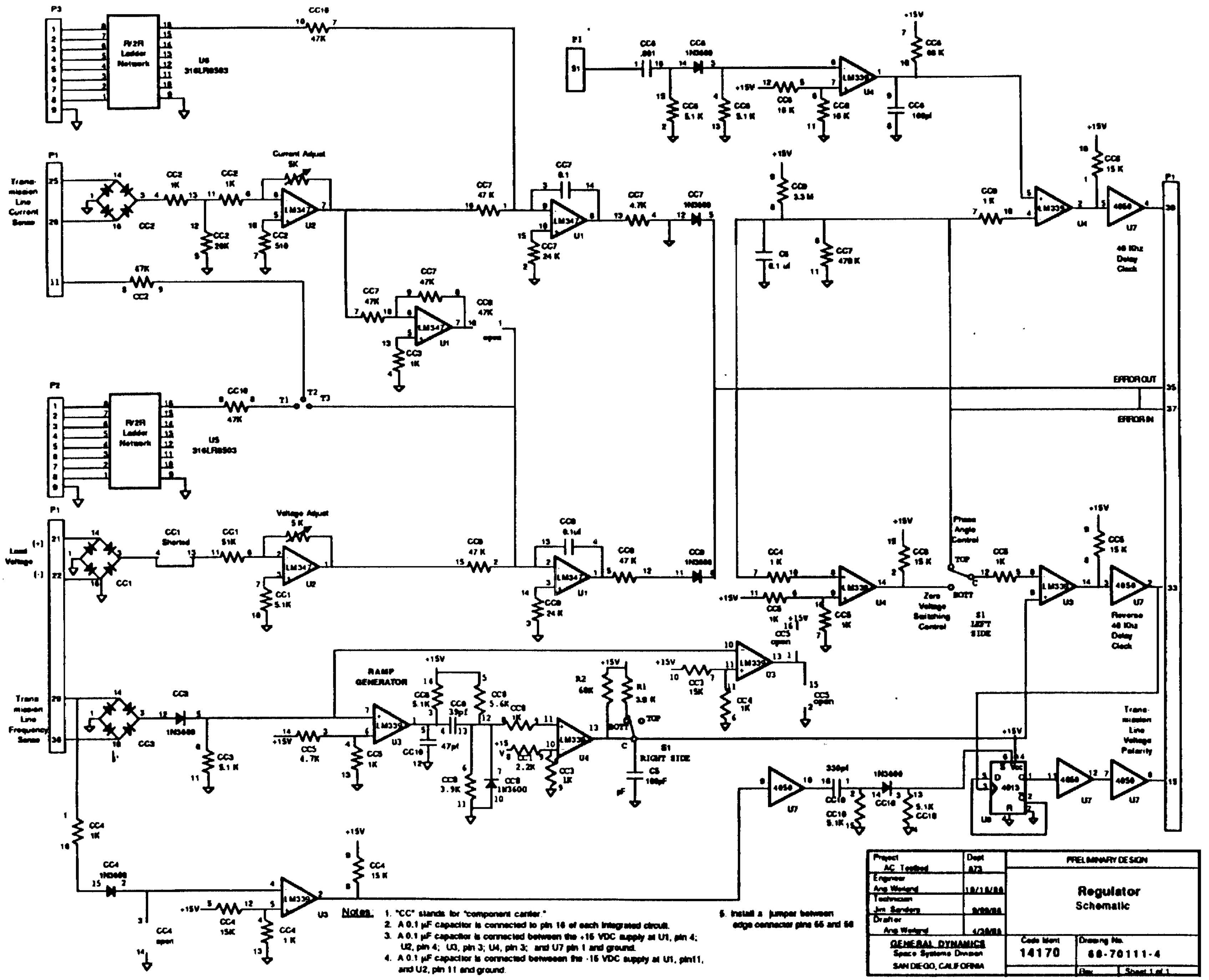

Notes:
1. "CC" stands for "component carrier."
2. A 0.1 µF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 µF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 µF capacitor is connected between the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connector pins 55 and 56

Project AC Testbed
Dept A73
Engineer Ang Weigand 10/18/88
Technician Jim Sanders 9/29/88
Drafter Ang Weigand 4/29/88
PRELIMINARY DESIGN

Regulator
Schematic

GENERAL DYNAMICS
Space Systems Division
SAN DIEGO, CALIFORNIA

Code Ident 14170
Drawing No. 68-70111-4
Rev.
Sheet 1 of 1

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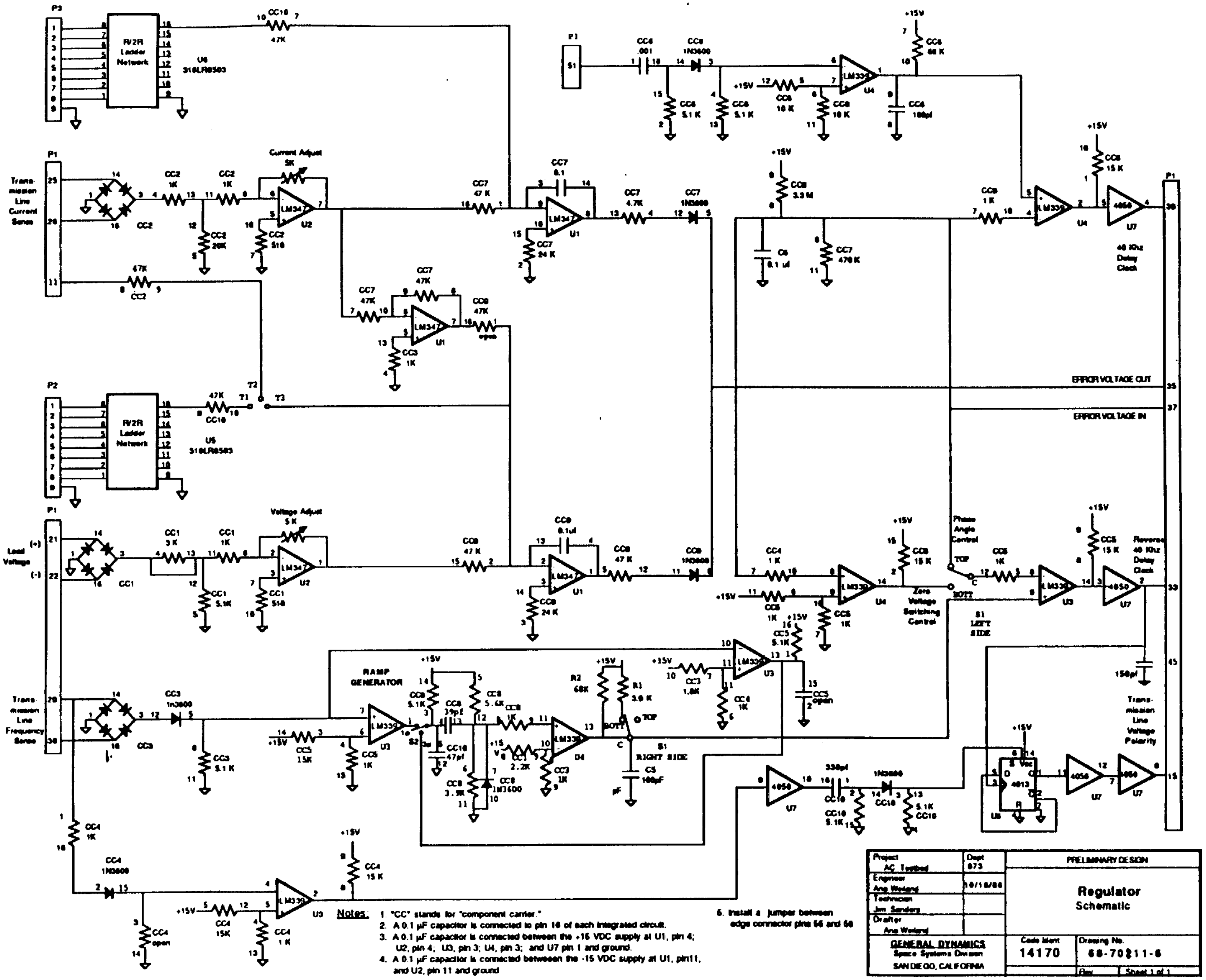

Notes:
1. "CC" stands for "component carrier."
2. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 μF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 μF capacitor is connected between the -15 VDC supply at U1, pin11, and U2, pin 11 and ground
6. Install a jumper between edge connector pins 56 and 58

Project AC Testbed	Dept 673	PRELIMINARY DESIGN
Engineer Ang Weiand	10/16/86	**Regulator** Schematic
Technician Jim Sanders		
Drafter Ana Weiand		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 14170	Drawing No. 68-70211-6
		Rev / Sheet 1 of 1

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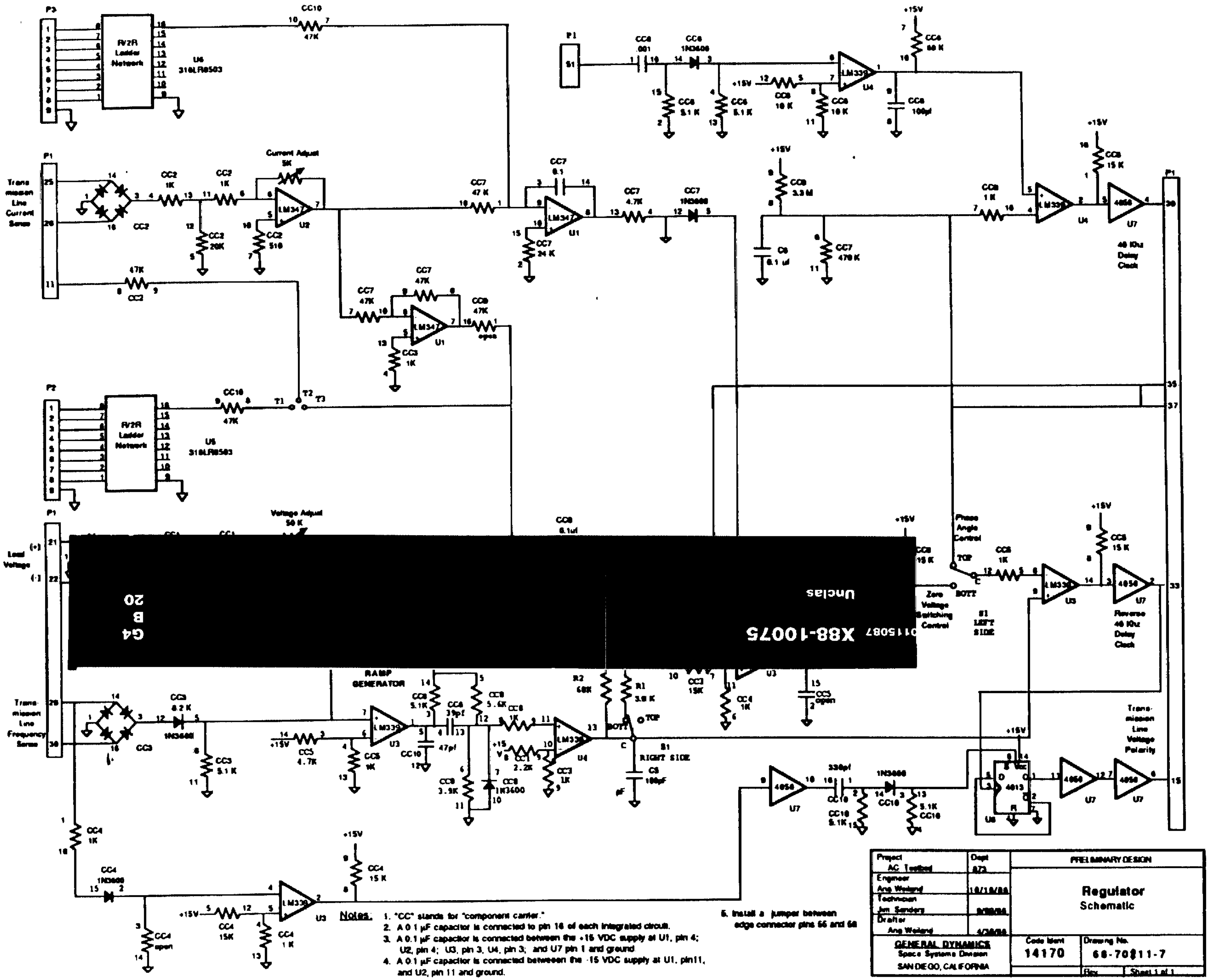

Notes:

1. "CC" stands for "component carrier."
2. A 0.1 µF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 µF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3, U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 µF capacitor is connected between the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connector pins 56 and 68

Project AC Testbed	Dept 873	PRELIMINARY DESIGN
Engineer Ang Weiland	10/18/88	**Regulator** Schematic
Technician Jim Sanders	[illegible]	
Drafter Ang Weiland	[illegible]	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 14170	Drawing No. 68-70811-7 Rev Sheet 1 of 1

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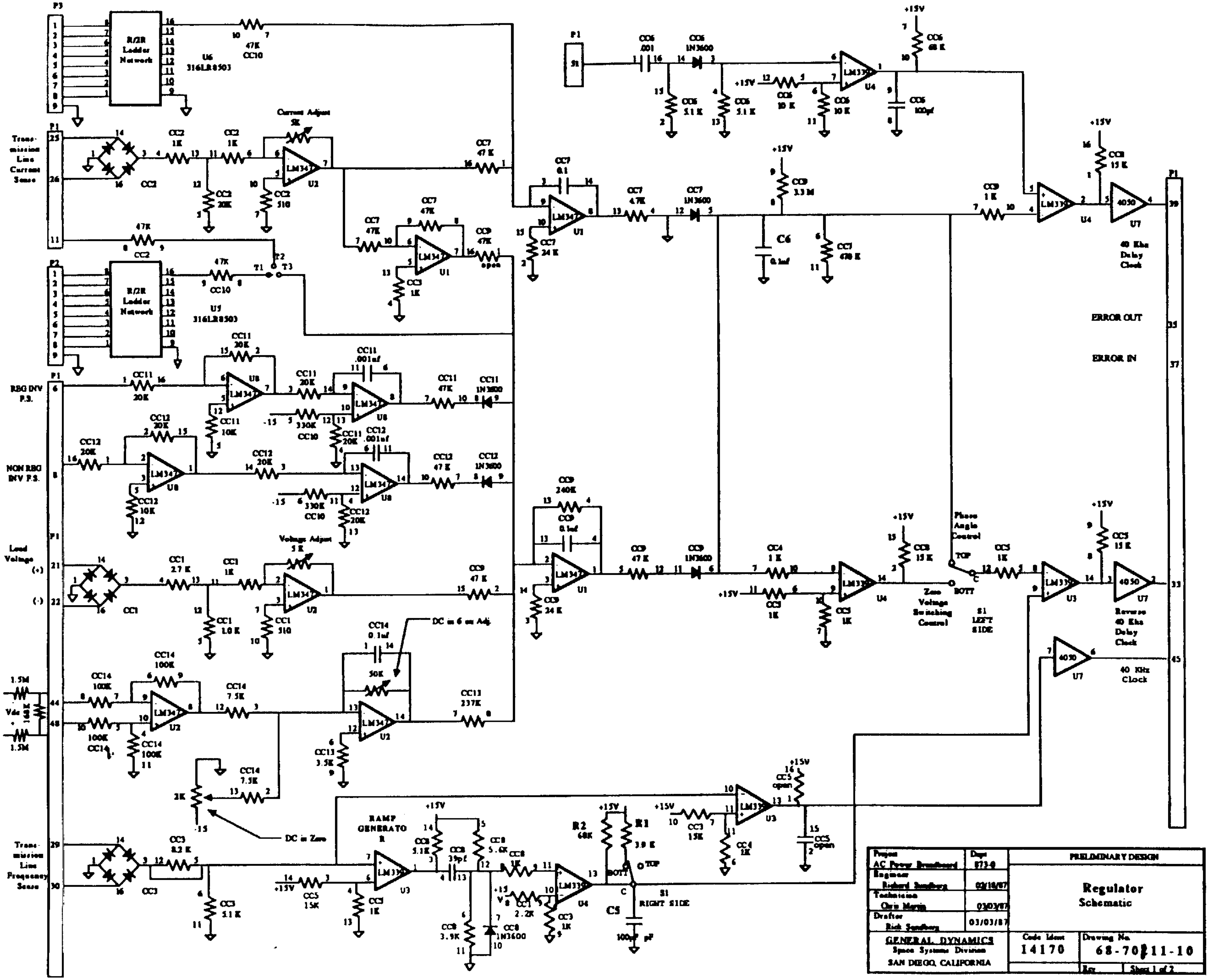

Project AC Power Breadboard	Dept 873-0	PRELIMINARY DESIGN
Engineer Richard Sandberg	02/18/87	Regulator Schematic
Technician Chris Martin	03/03/87	
Drafter Rich Sandberg	03/03/87	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 14170	Drawing No. 68-70211-10
		Rev Sheet 1 of 2

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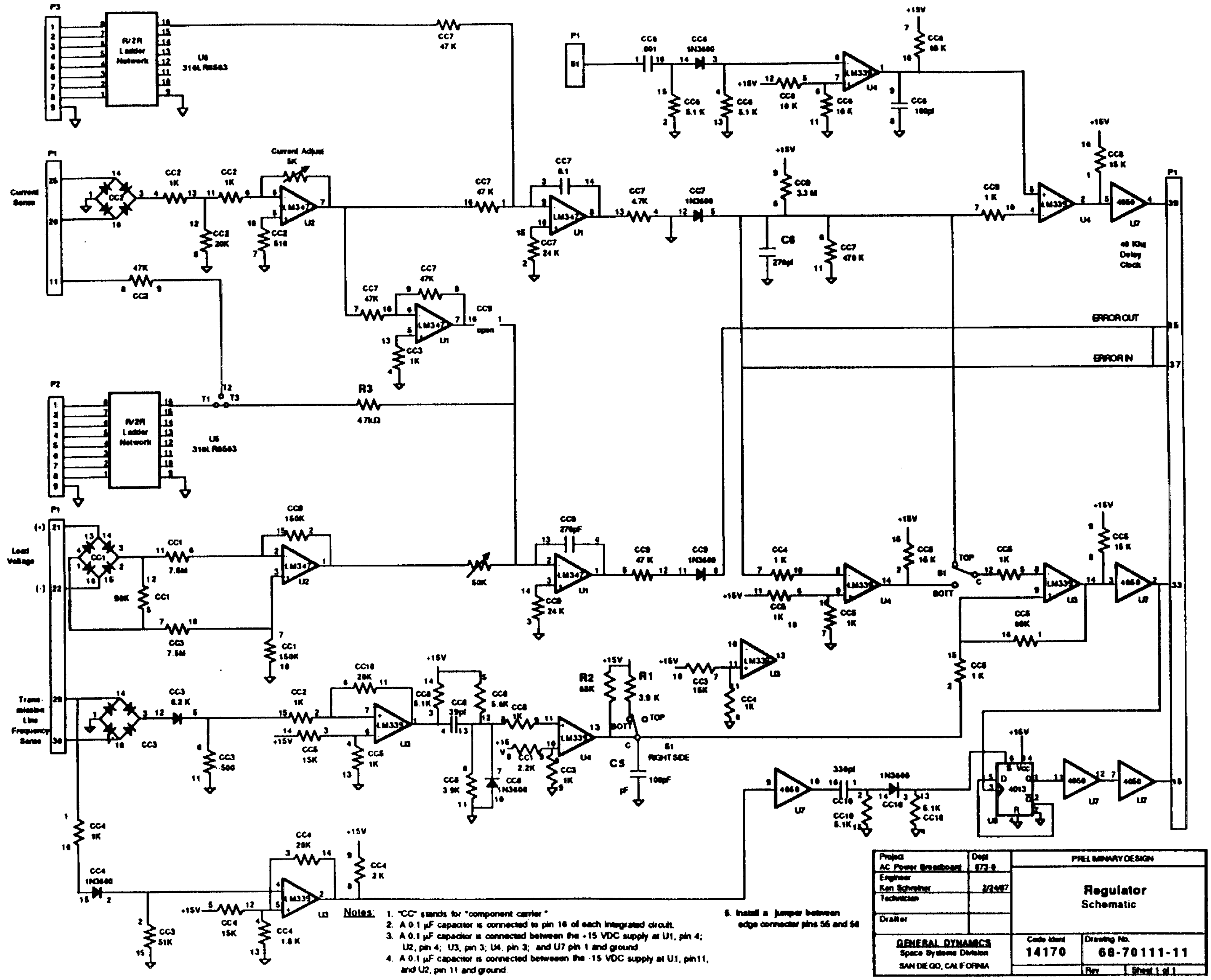

Notes:

1. "CC" stands for "component carrier."
2. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
3. A 0.1 μF capacitor is connected between the +15 VDC supply at U1, pin 4; U2, pin 4; U3, pin 3; U4, pin 3; and U7 pin 1 and ground.
4. A 0.1 μF capacitor is connected between the -15 VDC supply at U1, pin11, and U2, pin 11 and ground.
5. Install a jumper between edge connecter pins 56 and 58

Project AC Power Breadboard	Dept 873-0	PRELIMINARY DESIGN	
Engineer Ken Schreiner	2/24/87	Regulator Schematic	
Technician			
Drafter			
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA		Code Ident 14170	Drawing No. 68-70111-11
			Rev Sheet 1 of 1

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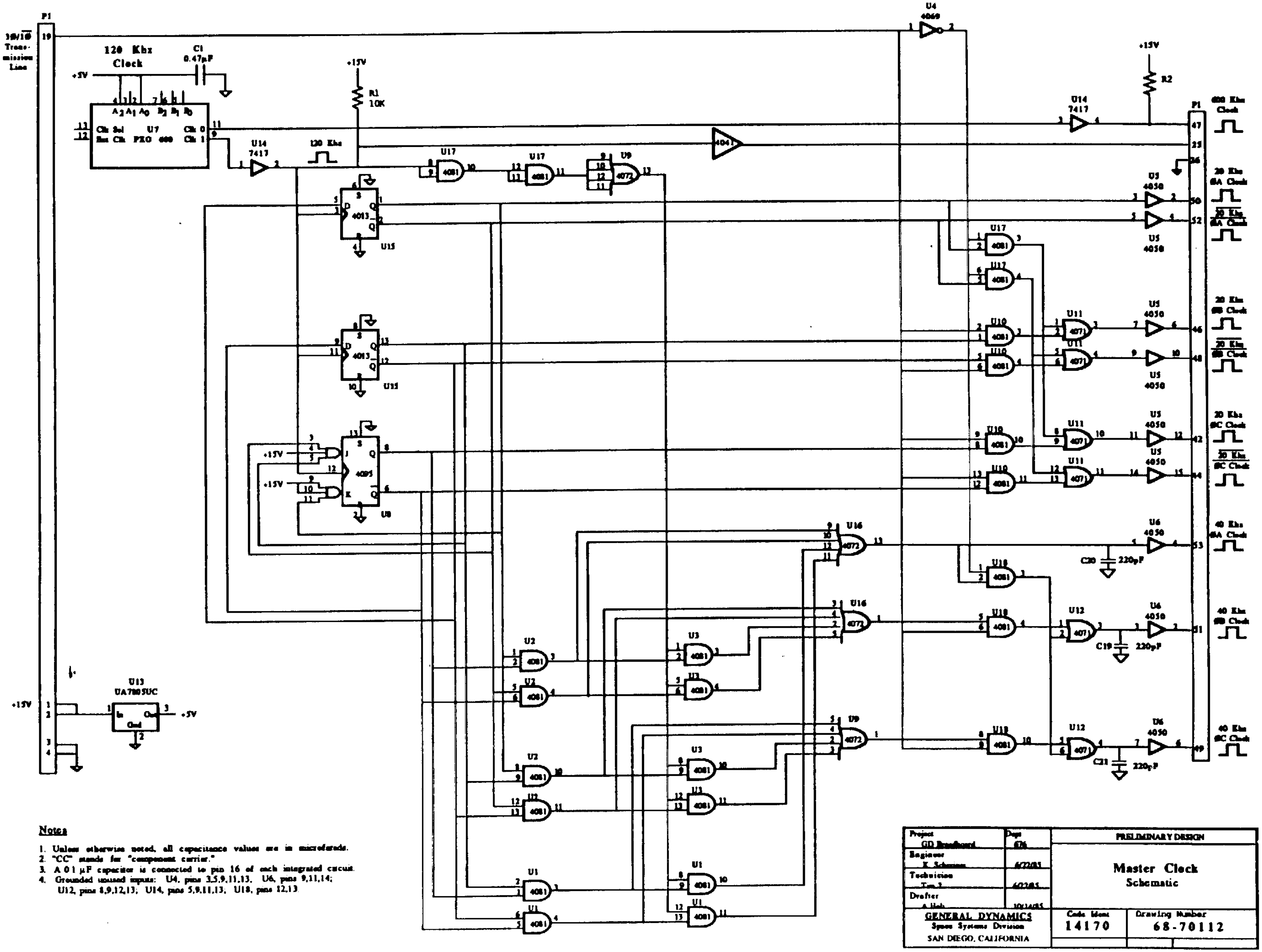
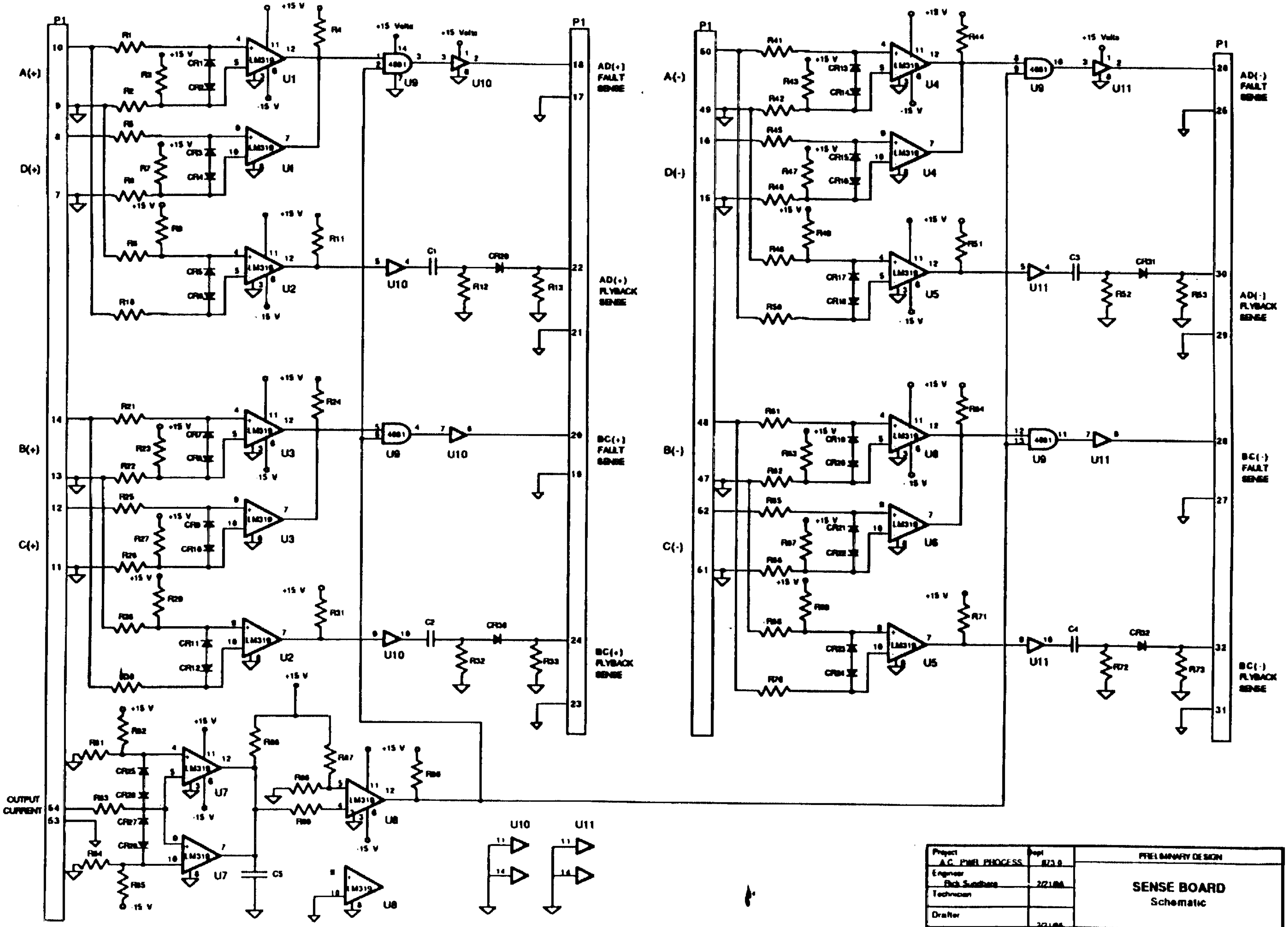


Notes

1. Unless otherwise noted, all capacitance values are in microfarads.
2. "CC" stands for "component carrier."
3. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
4. Grounded unused inputs: U4, pins 3,5,9,11,13; U6, pins 9,11,14; U12, pins 8,9,12,13; U14, pins 5,9,11,13; U18, pins 12,13.

Project GD Breadboard	Dept 676	PRELIMINARY DESIGN
Engineer K. Schemm[illegible]	6/22/85	Master Clock Schematic
Technician Tim [illegible]	6/22/85	
Drafter A. Hol[illegible]	10/14/85	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 14170	Drawing Number 68-70112



Project A.C. PWR PROCESS	Dept 873.0	PRELIMINARY DESIGN	
Engineer Bob Sundberg	2/21/84	**SENSE BOARD** Schematic	
Technician			
Drafter	2/21/84		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA		Code Ident 14170	Drawing No. 68-70113

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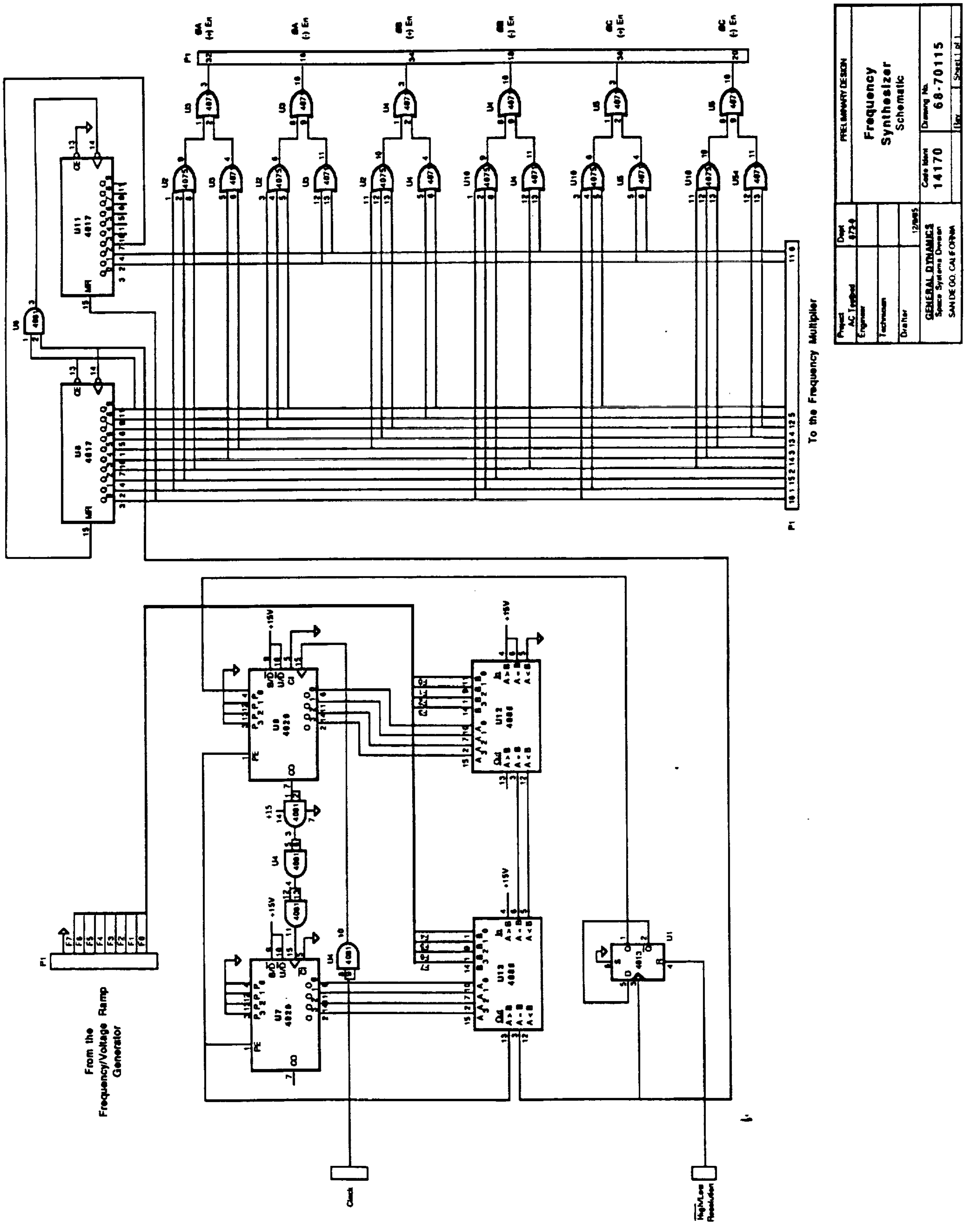

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15. Supplementary Notes

Project Manager, A. Baez, NASA Lewis Research Center, Cleveland, Ohio

16. Abstract

The object of this program was to design, build, test, and deliver a set of control electronics suitable for control of bidirectional resonant power processing equipment of the direct output type. This report describes that program, including the technical background,and discusses the results. Even though the initial program only tested the logic outputs, the hardware was subsequently tested with high-power breadboard equipment, and in the testbed of NASA contract NAS 3-24399. The completed equipment has been to LeRC with that testbed, where it is operating as a part of the Space Station Power System Test Facility.

17. Key Words (Suggested by Author(s)) Space Power Resonant Conversion Space Station Power 20-kHz Power	18. Distribution Statement

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