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Satellite Range Delay Simulator for a Matrix-Switched Time Division Multiple-Access Network Simulator

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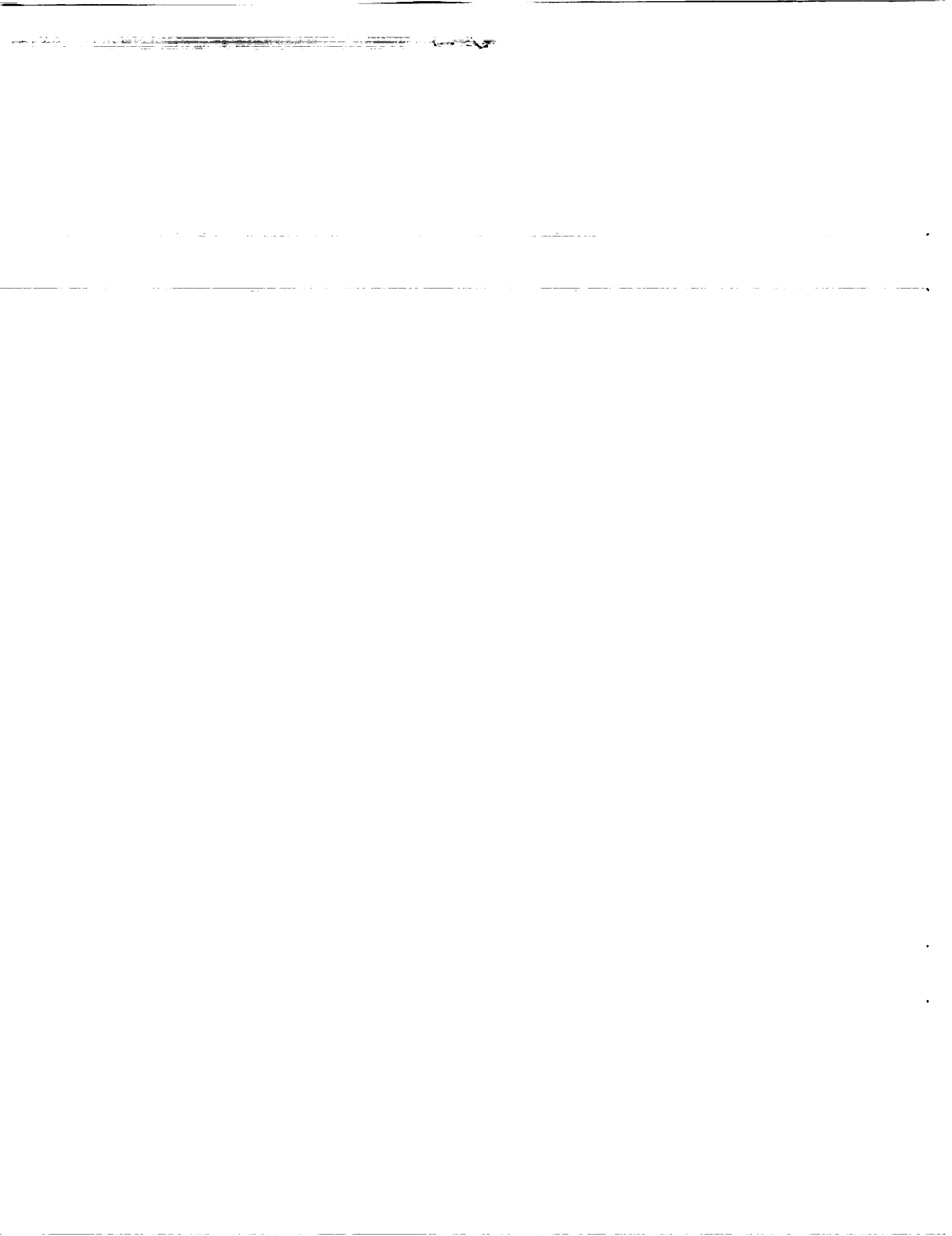*Lewis Research Center*
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NASA

SATELLITE RANGE DELAY SIMULATOR FOR A MATRIX-SWITCHED TIME DIVISION

MULTIPLE-ACCESS NETWORK SIMULATOR

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Abstract

The Systems Integration, Test, and Evaluation (SITE) facility at NASA Lewis Research Center is presently configured as a satellite-switched time division multiple access (SS-TDMA) network simulator. The purpose of SITE is to demonstrate and evaluate advanced communication satellite technologies, presently embodied by POC components developed under NASA contracts in addition to other hardware, such as ground terminals, designed and built in-house at NASA Lewis.

Each ground terminal in a satellite communications system will experience a different aspect of the satellite's motion due mainly to daily tidal effects and station keeping, hence a different duration and rate of variation in the range delay. As a result of this and other effects such as local oscillator instability, each ground terminal must constantly adjust its transmit burst timing so that data bursts from separate ground terminals arrive at the satellite in their assigned time slots, preventing overlap and keeping the system in synchronism. On the receiving end, ground terminals must synchronize their local clocks using reference transmissions received through the satellite link.

A feature of the SITE facility is its capability to simulate the varying propagation delays and associated Doppler frequency shifts that the ground terminals in the network have to cope with. Delay is achieved by means of two NASA Lewis designed and built range delay simulator (RDS) systems, each independently controlled locally with front panel switches or remotely by an experiment control and monitor (EC&M) computer.

Nomenclature

ACTS	Advanced Communications Technology Satellite
BER	bit error rate
D/A	digital to analog
DIP	dual in-line
DRAM	dynamic random access memory
ECL	emitter coupled logic
EC&M	experiment control and monitor (computer)
FIFO	first-in-first-out
GHz	gigahertz
Hz	hertz
IEEE-488	Institute of Electrical & Electronic Engineers Interface Standard
Lewis	Lewis Research Center (NASA), Cleveland, Ohio
Mbps	megabits per second
MHz	megahertz
NASA	National Aeronautics and Space Administration
P/S	parallel to serial
RAS	row address strobe
RDS	range delay simulator
RF	radio frequency
RS-232	Serial Data Communications Interface Standard
SCBERT	single channel bit error rate tester
SIP	single in-line package
SITE	Systems Integration, Test, and Evaluation
S/P	serial to parallel
SS	satellite matrix-switched
TDMA	time division multiple access
TTL	transistor-transistor logic
VCWCG	variable count word clock generator
VCXO	voltage-controlled crystal oscillator

Introduction

In 1978 NASA initiated a program to develop advanced communication satellite technologies for systems of the future. System studies performed during this period concluded that the Ku-Band frequency spectrum would reach its capacity in the 1990's and that technologies should be developed to utilize the Ka-Band (30/20 GHz) spectrum. In addition, several advanced communication satellite architectures and their associated system technologies were studied at NASA Lewis Research Center. In order to demonstrate a Ka-Band satellite communication system with advanced technologies such as multibeam antennas, onboard baseband processing, and satellite matrix switching, NASA Lewis initiated development of the Advanced Communications Technology Satellite (ACTS). To develop a laboratory test bed for verification of the advanced components and system architectures, NASA Lewis established the SITE project.[1] This facility is presently configured as a satellite-switched time division multiple access (SS-TDMA) network simulator[2] and is shown in the block diagram in Fig. 1. This paper

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describes a subsystem of this network simulator, the satellite range delay simulator.

The RDS provides a controlled variable time delay for a ground terminal's output with minimum delay capability of 151 ms (exceeding the full geosynchronous orbit delay of nominally 122 ms) and a range variation rate of up to 339 m/sec, more than two orders of magnitude greater than that of a typical satellite. Delay is achieved with a large array of dynamic random access memory (DRAM) integrated circuits in a first-in-first-out (FIFO) configuration. By reading the data out of the FIFO after a prescribed delay and at a prescribed rate (digitally controlled using a built-in oscillator) slightly different than the rate at which it was written (at the ground terminal's clock rate), a continuously changing delay is realized. A moving satellite, up to and beyond geosynchronous orbit, complete with the corresponding Doppler frequency shift, is thereby simulated.

Both data and control signals are delayed by the RDS, so that the fidelity of the ground terminal's corrections in burst timing is preserved after the delay.

The scheme of using digital semiconductor memory to achieve the delay simulation emerged as the most practical and cost effective, though it gives rise to compromises in the overall path simulation. The constraint of operating on a digital signal dictates that the uplink delay be inserted upstream of the modulator in the ground terminal. This deviates from the real world situation where the delay occurs in the modulated RF (radio frequency) path downstream of the modulator and transmitter. Also, no RDS is inserted in a downlink of the SITE network, since it would have to be located downstream of the ground terminal's demodulator, artificially complicating the ground terminal's control of the demodulator for the sake of the simulation.

However, these compromises do not alter the ground terminals' synchronization processes in the SITE environment, which is presently configured to simulate a network with a matrix switched, but non-signal-processing satellite.

The RDS units are designed specifically to work in conjunction with the present SITE ground terminals, which operate at a burst rate of 221 Mbps with a parallel data word architecture of 64 bits. The ground terminal feeds the RDS with the parallel data which is delayed, then converted to a serial stream at 221 Mbps. Other burst rates or ground terminal architectures would require modifications to the RDS.

Operation of the RDS in the SITE Laboratory has not yet begun. The first unit is in the build-up/debug stage. Some success was achieved with a first generation RDS operating in conjunction with a NASA Lewis built ground terminal. However, noise problems in the first design led to intolerable bit error rate (BER) levels. This stimulated the present design, which incorporates higher density memory packaging to reduce signal cross coupling in the wire wrap* interconnecting bundles.

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*Wire wrap is trademark of the Gardner Denver Corporation.

Approach

Regardless of what scheme is used to simulate the varying satellite range delay, it is inescapable that 122 ms worth of information being generated at the rate of 221 Mbps has to be contained at any one time in some device.

The solution found to be the most practical and cost effective is to employ semiconductor memory and the associated digital control logic in a large first-in-first-out (FIFO) memory. This implementation requires that the delay be applied at a point in the system where the signal is at digital baseband, i.e., between the ground terminal's transmit burst buffer and the modulator (see Fig. 1). Inserting the uplink delay at this point deviates from an actual satellite link where it occurs downstream of the modulator and transmitter, but this deviation does not alter the adjustments in burst timing the ground terminal must make to accommodate varying range delay.

In the present SITE configuration, the signal at the point where the RDS is to be inserted is a serial, bursted bit stream and clock running at the 221 Mbps rate, provided by a parallel-to-serial (P/S) converter in the ground terminal. To avoid immediately reconverting the serial data back to a parallel format in the RDS resulting in back-to-back P/S and serial-to-parallel (S/P) converters, the RDS accepts 64 bit parallel data from the input of the ground terminal's P/S converter. After delaying the data by an amount appropriate for the simulation, the RDS converts it to a serial, bursted stream for input to the modulator.

The parallel data words are written into a large Dynamic Random Access Memory (DRAM) bank configured to operate as a FIFO, that is, the write and read addresses are independent but sequential. The WRITE rate is controlled by an INPUT WORD CLOCK signal provided by the ground terminal. Since the word length is 64 bits, this clock rate is 221.184 MHz divided by 64, or 3.456 MHz with some deviation due to instabilities in the ground terminal's oscillator.

After a preselected delay period, the words are read from the FIFO at a controlled variable rate determined by the OUTPUT WORD CLOCK. In this manner, a changing delay period is achieved, simulating a moving satellite with the appropriate Doppler frequency shift. Thus the OUTPUT WORD CLOCK rate directly sets the simulated satellite slant range velocity (line-of-sight component of satellite's motion). An oven-controlled voltage controlled crystal oscillator (VCXO) similar to those used in the ground terminals is incorporated in the RDS. Its output (output high speed clock) is normally divided by 64 with a variable count word clock generator (VCWCG) circuit to produce the OUTPUT WORD CLOCK signal. Its input control voltage is derived from an analog-to-digital converter controlled by front panel switches when operating in the LOCAL mode, or from an experiment control and monitor (EC&M) computer when in the REMOTE mode. With this option the simulated satellite slant range velocity may be changed "on the fly" in the LOCAL mode, or a preprogrammed profile of satellite range versus time may be set and executed in the REMOTE mode. A concurrent 3240 minicomputer is used for the EC&M computer.

In practice, the RDS FIFO memory is wider than the 64 bits required for the data word length. Four additional control bits must be delayed along with each data word in order to reconstruct with fidelity the timing of the ground terminal's output after the delay: (1) Two bits carry the code for control of the VCWCG in the RDS; (2) a third bit indicates whether the accompanying word is valid (i.e. part of a data burst as opposed to meaningless bits filling in time between valid bursts); and (3) a fourth bit signals the last word in a frame. A frame consists of 864 words or 250 μs. Each valid data burst consists of an integer number of 64-bit words.

The writing and reading of the RDS memory is continuous, even though the valid data words are bursted out of the ground terminal. Valid data words as well as the dummy words in between are delayed by the RDS, which then reconstructs the ground terminal's burst pattern in its serial output.

The ground terminals constantly adjust their transmit burst timing to ensure that the bursts arrive at the satellite in their designated time slots. This is accomplished by advancing or retarding their transmit word clock during the last word of a frame by increments of one high speed clock period (1/221.184 MHz or 4.52 ns). Based on whether the satellite has moved closer, farther, or not at all, the ground terminal determines whether it has to advance, retard, or maintain the same burst timing. It then applies the proper 2 bit code of 01, 10, or 00 to its VCWCG to divide the high speed clock by 63, 65, or 64, respectively. This same code is delayed by the RDS and as the data words are read from the FIFO memory, the corresponding code is read and applied to the RDS's VCWCG circuit to divide the RDS's output high speed clock by 63, 65, or 64. Thus the INPUT WORD CLOCK and the OUTPUT WORD CLOCK which control the write and read operations of the RDS not only run at asynchronous rates, but their periods are sporadically lengthened or shortened by a bit time, due to this bit insertion/deletion process.

The actual burst timing adjustment is done by the P/S converter. Once synchronized, it outputs a continuous stream of bits at the output high speed clock rate. If during a frame the OUTPUT WORD CLOCK is advanced or retarded (a division by 63 or 65 occurs) one or more times, the P/S converter will be resynchronized at the start of the following frame. The last word in the frame, reserved for this purpose and therefore restricted from containing valid data, will be truncated or stretched by the appropriate number of bit time increments, up to a limit of 20 per frame.

In practice, a fourth binary code of 11 may be applied to the VCWCG circuit which causes it to divide by 56. This code is used only during the initial ground terminal timing acquisition and synchronization process for coarse changes in burst timing.

The modulators used by the SITE ground terminals are followed by a postmodulator switch that enables only valid data bursts to be transmitted. This switch requires a control signal from the RDS that rises one-half word time prior to the start of a valid data burst and falls a half word time after a valid data burst. The single bit code (one of the four control bits delayed along with the data)

that indicates whether the accompanying data word is valid is used to generate the POST MOD SWITCH CONTROL signal in the RDS.

System Description

Figure 2 shows a block diagram of the range delay simulator. The major elements are:

(1) FIFO memory board
(2) Timing and control board
(3) VCXO and the clock distribution board
(4) VCWCG circuit
(5) P/S converter
(6) EC&M computer interface
(7) Control panel
(8) Monitors

FIFO Memory

The heart of the system is a FIFO memory whose basic building block is a 262 144 x 1 DRAM chip with 120 ns access time. The FIFO memory word width requirement is 68 bits, 64 for the data word plus 4 control bits. The depth requirement is dictated by the maximum delay to be achieved. In order to simulate the propagation delay to a geosynchronous satellite (some 122 ms), a FIFO depth of at least 422 000 addresses is necessary, since at the word rate of 3.456 MHz, words are written at 289 ns intervals. Two banks of memory chips would provide 524 288 addresses, more than adequate delay. However, using only two banks would mean that unless the delay were fixed at exactly 262 144 addresses, part of the time the asynchronous WRITE and READ operations would be taking place within the same bank. This leads to the complication of read/write address arbitration, and approaches the limit on memory access time. By adding a third memory bank and restricting the allowable delay limits such that the RDS never would be reading and writing simultaneously from the same bank, no address arbitration is required, and the full 289 ns are available for each WRITE or READ cycle. The resulting RDS delay capability is a minimum of one bank's worth of delay (75.9 ms) and a maximum of two banks' worth (151.7 ms) with any continuously variable delay amount in between. This more than adequately covers the range delay excursions even for widely varying military satellite whose range may extend from 36 407 to 37 079 km in the course of a day, corresponding to a delay variation of 121.4 to 123.7 ms.[3] A typical domestic satellite's variation is only a fraction of this amount.

Modules consisting of five DRAM chips mounted on a single inline package (SIP) printed circuit strip are used in order to reduce the amount of interconnecting wires on the memory board. Refer to Fig. 3 for a photo of the memory board and a DRAM module. Three banks of 14 modules provide an overall FIFO memory configuration of 786 432 x 70, for a capacity of 55 Mb, as shown in Fig. 4. This depth of memory requires 20 address lines (18 per chip plus 2 to select the bank). Therefore, both the write address counter and the read address counter are sized for 20 (binary) bits.

The INPUT WORD CLOCK, which increments the write address counter, also generates a sequence of memory WRITE control signals. The two high-order bits of the write address counter select the memory bank while the low-order 18 bits select the chip address. The chips are configured with only nine

address pins, and the addressing is applied in two steps by strobing first a nine bit row address, then a nine column address. Similarly, the OUTPUT WORD CLOCK increments the Read Address Counter and generates the memory READ control signals. The multiplexing between the memory address rows and columns and enabling banks for WRITE and READ is accomplished by the control logic.

Memory Refreshing

The DRAM manufacturer's data book specifies that the memories must be refreshed by strobing each of 256 row addresses (determined by eight of the nine address pins, A0 through A7) with a row address strobe (RAS) pulse at least once every 4 ms. This condition is not met during the inactive delay period (of up to 151.5 ms) between WRITE and READ for a given address unless special refresh circuitry is incorporated into the system. A scheme to do so was designed and tested on the first generation RDS system.

This early design used pulses generated by dividing down the INPUT WORD CLOCK at such a rate that each of the required row addresses was refreshed every 2.3 ms during the delay period. The system was configured with eight banks of 65 536 bit deep memories with the same access and refresh times as those used in the present design. The refresh pulses were inhibited in two banks (i.e., those being written to and read from at the time). Refresh pulses were applied to the remaining six. A complication of this approach is that since the OUTPUT WORD CLOCK is asynchronous with respect to the INPUT WORD CLOCK (and therefore with the refresh rate), a READ cycle could have been initiated for the first address in a new bank too soon after a refresh pulse was applied to the same bank, thus violating the memory's minimum cycle time constraint. This problem was overcome in the first generation RDS by inhibiting refresh when the READ address was at the last location in each bank, ready to jump to the next bank. It was found, however, that the strobing of such a large amount of memory for refreshing added a considerable amount of noise (in synchronism with the INPUT WORD CLOCK rate) to the system. This was enough to cause occasional errors in reading the data from memory (asynchronous with the refresh pulses taking place in six other banks). By contrast, operating without refresh exhibited fewer errors. In fact, hours of error free performance were at times realized.

An independent bench test of the memories used in the present design demonstrated that they could actually operate error-free over a 12 hr test period with a refresh rate exceeding 10 sec. This was a relatively noise-free system, however. Evidently the higher the noise level, the shorter the required refresh period.

Based upon these considerations, no special memory refreshing was incorporated in the present design.

VCXO Control

The OUTPUT FREQUENCY CONTROL CODE is a 12-bit word which feeds a digital to analog (D/A) converter. This in turn controls the VCXO that generates the output high speed clock. The VCXO output is nonlinear with respect to the input control voltage, and units vary in calibration. The EC&M

computer must therefore run a calibration prior to a run to set the control algorithm's initial values. Tne VCXO type used in this design has an output frequency range variation capability of some 250 Hz above and below the nominal output value of 221.184 MHz. This is the RDS's Doppler frequency shift capability and corresponds to a simulation of a satellite's slant range velocity of ±339 m/sec, some two orders of magnitude greater than the peak of 27 m/sec exhibited by the military satellite.[3]

Clock Distribution Board

The output high speed clock coming from the VCXO in the RDS is a single-ended, emitter-coupled logic (ECL) signal that is fed into the clock distribution board. Here it is buffered and output to the P/S converter, the VCWCG circuit, and the OUTPUT FREQUENCY MONITOR. The input high speed clock from the ground terminal is also fed into the clock distribution board to be buffered and output to the INPUT FREQUENCY MONITOR. Both high speed clocks are combined in an RF mixer circuit on the clock distribution board which generates a signal for the DOPPLER FREQUENCY SHIFT MONITOR. All high speed clock signals transferred internally within the RDS are complimentary-pair ECL level and are routed via twisted pair wires.

Monitors

The following parameters are sensed and displayed by instruments mounted in the RDS rack: (1) INPUT HIGH SPEED CLOCK FREQUENCY (MHz), (2) OUTPUT HIGH SPEED CLOCK FREQUENCY (MHz), (3) DELAY (ms) or RANGE (km), and (4) DOPPLER SHIFT (Hz). All are fed to the EC&M computer over an IEEE-488 bus link.

Operation

The RDS is controlled in either one of two modes, LOCAL or REMOTE, selected by a toggle switch on the control panel (see Fig. 5). When in the LOCAL mode, the INITIAL DELAY CONTROL CODE (4 bits) and the OUTPUT FREQUENCY CONTROL CODE (12 bits) are set with thumbwheel switches, and the system is initiated by pushing the RESET button. Refer to Fig. 6 for a table of initial delay control codes. In the REMOTE mode, these functions are performed by the EC&M computer via an RS-232 data link through an interface board located in the RDS. This board converts commands from the EC&M computer to parallel binary input for the RDS using a microprocessor chip.

The initialization process must be performed prior to accepting data from the ground terminal. The RESET pulse sets three counters (write address, read address, and delay control) all to zero. The write address and the delay control counters immediately start counting at the INPUT WORD CLOCK rate. The read address counter is temporarily inhibited. When the delay control counter reaches the number of words prescribed by the INITIAL DELAY CONTROL CODE, the read address counter is enabled and it begins to count at the OUTPUT WORD CLOCK rate, asynchronous with respect to the INPUT WORD CLOCK rate. The number of words (address locations) between the WRITE and READ counters represents the FIFO level, or delay amount, and will slowly change due to the difference in the WRITE and READ clocks. By resetting the delay control counter to zero each time the write address counter rolls over and latching its value each time the read address counter does the

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same, the delay measured in number of words is captured. This parameter, called the FIFO LEVEL - WORDS is displayed on the control panel. The delay control counter is decimal rather than binary for operator convenience.

Once reset, the RDS is ready to accept data. There is no restriction on when the first valid data word should be input to the RDS after reset. It accepts whatever data appears on the input data bus, valid or not, and delays it. The 64-bit data word and 4 control bits from the ground terminal are latched into the input register at the INPUT WORD CLOCK rate. At the same rate, the write address counter is incremented and the data are written at the new address. Simultaneously, the read address counter is incremented at its rate to an address that lags the write counter address by the delay amount, and reads the word that was written at that location one range delay period earlier. Once read, the parallel data word is sent to the P/S converter which outputs a serial data stream at the high speed output clock rate. As described previously, the OUTPUT WORD CLOCK's rate is occasionally adjusted by the VCWCG circuit in response to the 2-bit VCWCG CONTROL CODE read out of the memory. This bit insertion/deletion process is then carried through the P/S converter to reproduce the ground terminal's burst timing pattern at the RDS output.

In the real world, any instability in the ground terminal oscillator used to clock transmitted data (input high speed clock to the RDS) is received by the satellite as an addition to the Doppler shift. Similarly, the RDS will control its output high speed clock rate based upon its input high speed clock rate plus or minus the desired Doppler shift.

In the LOCAL mode the system is run essentially open loop, in which the operator may change the output frequency as desired by altering the thumbwheel switch settings. In the REMOTE mode, the EC&M computer uses the monitor outputs in its algorithm to close the loop (dynamically adjust the 12-bit OUTPUT CLOCK RATE CONTROL CODE) in order to follow a preset profile of range versus time or Doppler frequency shift versus time. The profile data are contained in a file created previously by a separate program on the EC&M computer.

The RDS can simulate realistic or exaggerated satellite range variation to exercise the ground terminals' acquisition and synchronization processes beyond their normal operating range in compressed-time experiments (see characteristics).

Since the DOPPLER FREQUENCY SHIFT MONITOR is actually a counter measuring the difference frequency of the two high speed clocks (the output of an RF mixer), it senses only the frequency, not the polarity of the Doppler shift. In other words, it can sense the simulated slant range velocity, but not the direction. This limitation is not a problem when the Doppler shift is relatively large, since the polarity (simulated satellite motion direction) is uniform. The ambiguity occurs at the lower levels (less than 1 Hz) where it is not clear when the signal passes through zero. This limitation is overcome at the expense of time by having the EC&M computer compare readings of the RANGE MONITOR's output over an interval of 1 min or so to determine both the magnitude and direction of the simulated satellite motion.

It is worth noting here that the Doppler shift polarity can be determined easily and almost instantly by a human operator. This is done by observing the direction of the relative motion between the two frequencies (input and output high speed clocks) on an oscilloscope display. Unfortunately, there is no straightforward way for the EC&M computer to take advantage of this approach.

Special Test Equipment

To aid in the debugging process a single channel bit error rate test (SCBERT) board was built and is incorporated as an integral part of the RDS chassis. It tests any one of the 70 memory channels at a time by generating a bit pattern, clocking it in at the WRITE WORD CLOCK rate, passing it through the channel, clocking it out at the READ WORD CLOCK rate, and comparing the channel's output with the known pattern. The pattern length repeats every N bits, where the value of N is selectable from 2 through 16 bits using onboard switches. A count of individual bit errors is displayed on numeric displays mounted on the board. An ERROR output signal pulses whenever an error is detected, and may be used to trigger test equipment such as an oscilloscope or a logic analyzer. To provide a more realistic operating noise environment during these single channel tests, all 70 of the channels may be exercised with dynamic pseudo data from the SCBERT, each using one of eight signals offset in time from each other by 1 bit period. As a check on the test circuit itself, errors may be added intentionally at a rate of one per 65 536 times the pattern length, or about 3/sec for a 15 bit pattern running at the nominal word clock rate of 3.456 Mbps. This test feature is activated with a switch also mounted on the board. A 15 bit pattern length is usually preferred over that of 16 since the latter divides evenly into the overall FIFO memory's depth resulting in the same values being stored in the same address locations repeatedly, while the former will shift the data for each cyclic repetition of the memory address locations, rendering a realistic simulation of dynamic data and its noise producing environment.

For a more comprehensive RDS system BER test, a data generator and checker[4] is mounted in the RDS rack and can be connected with the generator's 64 bit parallel output bus feeding the RDS in place of the ground terminal, and with the checker accepting the high speed serial stream from the RDS instead of it going to the modulator. Parallel data words out of the generator are clocked into the RDS at the INPUT WORD CLOCK rate. A serial data stream is then clocked out of the RDS into the checker at the output high speed clock rate. The checker's display indicates a running count of errors received. These error detectors are limited to operating with continuous data, however, and can neither test bursted data nor data running when bit insertion/deletion is activated. Furthermore, they can only indicate that an error has occurred somewhere in the system, and cannot, for example, distinguish whether it was due to a false write or a false read.

Another piece of special test equipment is the ground terminal signal simulator. This unit consists of a separate chassis mounted in the RDS rack. As its name implies, it furnishes the required control signals to the RDS in the absence of a real SITE ground terminal. These signals are the INPUT

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HIGH SPEED CLOCK, the INPUT WORD CLOCK, the 2-bit
VCWCG CODE, the LAST WORD (of a frame) flag, and
the VALID DATA WORD flag. Also furnished is a HIGH
SPEED CLOCK divided by four required by the data
generator. A set of switches mounted on the circuit
board in the ground terminal signal simulator
allows a variety of valid data word patterns to be
simulated. The data generator, once started, out-
puts continuous data, but only the words indicated
as valid data by the VALID DATA WORD flag are
treated as such by the RDS.

Hardware

A first generation RDS design, similar in con-
cept to the present design but using individual
65 536 × 1 memory chips, required four 15 by 8 in.
(triple-width) memory boards as compared to one such
board in the present design. The first generation
design was subject to errors which occurred at seem-
ingly random times, both when tested using the BER
test set alone and when connected to a ground termi-
nal. These errors most likely stemmed from false
memory reads and writes due to noise caused by cross
coupling in the large amount of wire-wrap circuitry
operating at two asynchronous clock rates. Though
some measure of success was realized and was encour-
aging, the errors were too frequent for reliable
operation. As a result the present design, taking
advantage of denser memory packaging was initiated.

The RDS system is housed in a standard 6 ft
rack, the top portion of which is shown in Fig. 7.
At the bottom of the rack are the power supplies and
their control circuits. Mounted above them at the
rear of the rack is the RDS chassis itself, shown
in Fig. 8. Above the RDS chassis and also at the
rear are the data generator and checker, followed
by the ground terminal signal simulator. Next,
mounted at the front of the rack, is the control
panel. Finally, at the top front of the rack are
the four monitors: (1) INPUT FREQUENCY, (2) OUTPUT
FREQUENCY, (3) DELAY, and (4) DOPPLER FREQUENCY
SHIFT.

The RDS chassis is a commercial integrated cir-
cuit board enclosure that contains the following
wire-wrap boards: VCWCG, P/S converter; EC&M com-
puter interface; clock distribution and SCBERT (all
4-1/2 in. width boards); a timing and control board
(9-3/4 in.); and a memory board (15 in.).

Circuits operating at the high speed clock rate
(221.184 MHz) use 100 K ECL digital logic compo-
nents. For the majority of the circuitry, operating
at the word clock rate (3.456 MHz), both the 74F and
74LS TTL logic families were used. The 74LS compo-
nents were favored since their switching transition
times are slower, thereby reducing the amount of
induced noise in the wire wrap bundles. The faster
74F components are used only where speed is required
for critical circuit timing.

Interboard wiring is accomplished primarily
through the backplane of the chassis either with
single or twisted pair wires. Input/output signals
to and from the RDS chassis are run mainly through
connectors with flat ribbon, twisted pair, or
coaxial cables depending upon the type of signal.

The VCXO oscillator previously discussed is
mounted on the rear of the RDS chassis, in order to
keep its cable to the clock distribution board
short.

The data generator and checker chassis and the
ground terminal signal simulator chassis are also
commercial integrated circuit board enclosures.
Both contain several wire wrap circuit boards, and
the latter also contains power supplies and its own
VCXO.

The control panel (Fig. 5) has mounted on it
the thumbwheel switches for the INITIAL DELAY CON-
TROL CODE and the OUTPUT CLOCK RATE CODE, a toggle
switch to select either LOCAL or REMOTE control, a
pushbutton switch for local RESET, a six digit dis-
play for FIFO LEVEL - WORDS, and two BNC jacks for
monitoring the INPUT WORD CLOCK and OUTPUT WORD
CLOCK.

The INPUT and OUTPUT FREQUENCY MONITORS are RF
counters with a range of 50 to 600 MHz. These
instruments can operate with internal or external
standard reference signal, and the internal standard
is available as an output. Using this feature, they
are interconnected to operate on the same standard,
greatly enhancing the relative accuracy between the
two. When properly configured, these counters dis-
play the full nine digits of the high speed clock
frequencies (resolving down to 1 Hz). Both are
equipped with the IEEE-488 bus interface to communi-
cate with the EC&M computer.

The DELAY and DOPPLER FREQUENCY SHIFT MONITORS
are universal counters with an offset normalizer
option. The former displays the simulated delay
either in milliseconds, statute miles, or kilome-
ters. The latter displays the Doppler shift in
hertz, or the simulated satellite velocity in
meters per second. Again, both are equipped with
the IEEE-488 bus interface.

Characteristics

The following summarizes the overall opera-
tional characteristics of the RDS:

INPUTS:

    (1) INPUT HIGH SPEED CLOCK
    (2) INPUT WORD CLOCK (INPUT HIGH SPEED CLOCK
        divided by 64)
    (3) 64 bit parallel data words, arriving at
        INPUT WORD CLOCK rate
    (4) Control signals, arriving at INPUT WORD
        CLOCK rate (2-bit VCWCG CONTROL CODE, LAST
        WORD (of frame) flag, and VALID WORD flag)
    (5) EC&M computer signals (4-bit INITIAL DELAY
        CONTROL CODE, 12-bit OUTPUT FREQUENCY CON-
        TROL CODE, and RESET)

OUTPUTS:

    (1) OUTPUT HIGH SPEED CLOCK
    (2) Serial data stream, at OUTPUT HIGH SPEED
        CLOCK rate
    (3) POST MODULATOR SWITCH CONTROL
    (4) EC&M computer signals. (IEEE-488 bus data
        from the four monitors plus a LOCAL/REMOTE
        MODE indicator)

CAPABILITY:

    (1) Minimum delay: 75.9 ms (simulates
        22 740 km range)
    (2) Maximum delay: 151.7 ms (simulates
        45 480 km range)

(3) Input high speed clock rate: 221.184 MHz
(± drift)

(4) Output high speed clock rate: input high
speed clock rate ± Doppler frequency shift

(5) Doppler frequency shift range: ±250 Hz
(simulates satellite slant range velocity
of ±339 m/sec)

Future Plans

A second, identical RDS is planned once the first unit proves successful, to enable SITE lab network testing with independent range delay simulation on two of the system's ground terminal-to-transponder links.

Enhancements to future RDS units to make them more universal are also under consideration. These include an S/P converter at the front end, the ability to operate at clock rates other than 221 MHz, and an RDS for the downlink, applicable to link simulation for satellites with onboard processing.

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3. Silicon Solutions Inc. computer program "Silicon Ephemeris V2.0" using data provided via a "NASA Prediction Bulletin" from NASA Goddard Flight Center, Greenbelt, MD.

4. Windmiller, M.J., "Unique Bit-Error-Rate Measurement System for Satellite Communication Systems," NASA TP-2699, 1987.
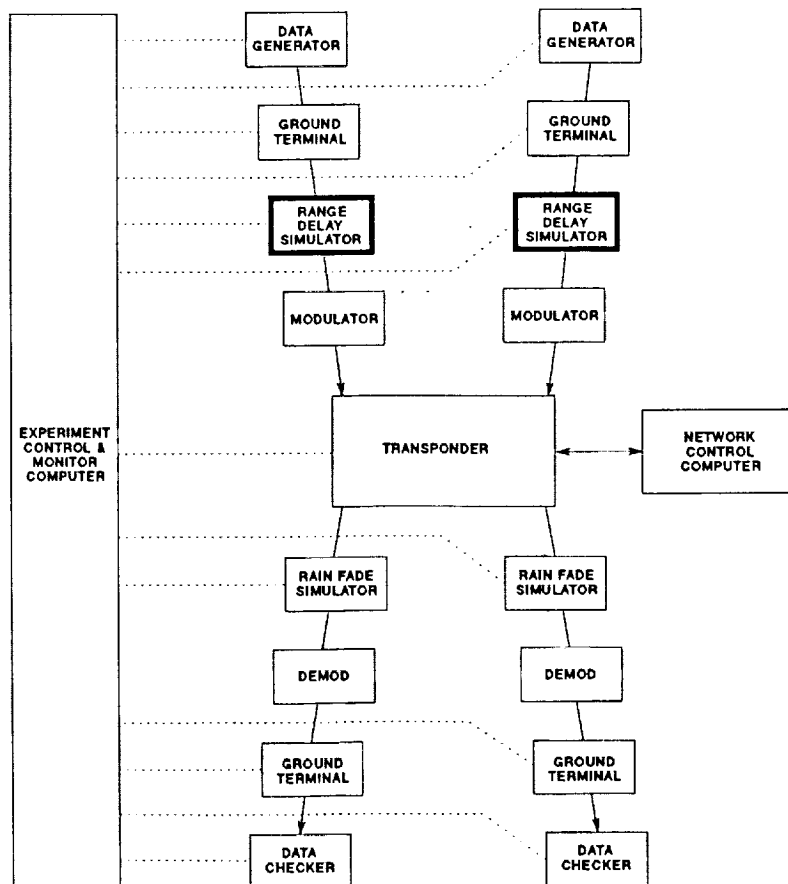
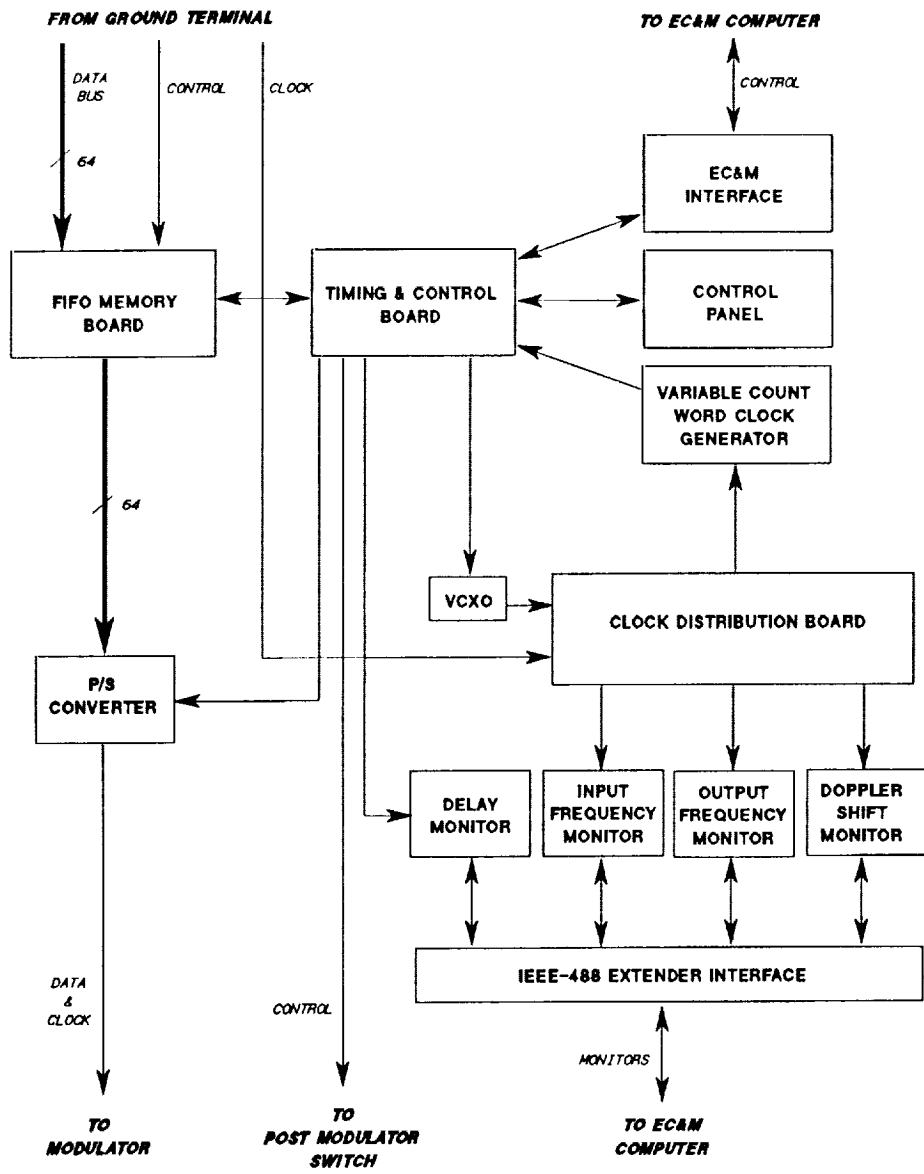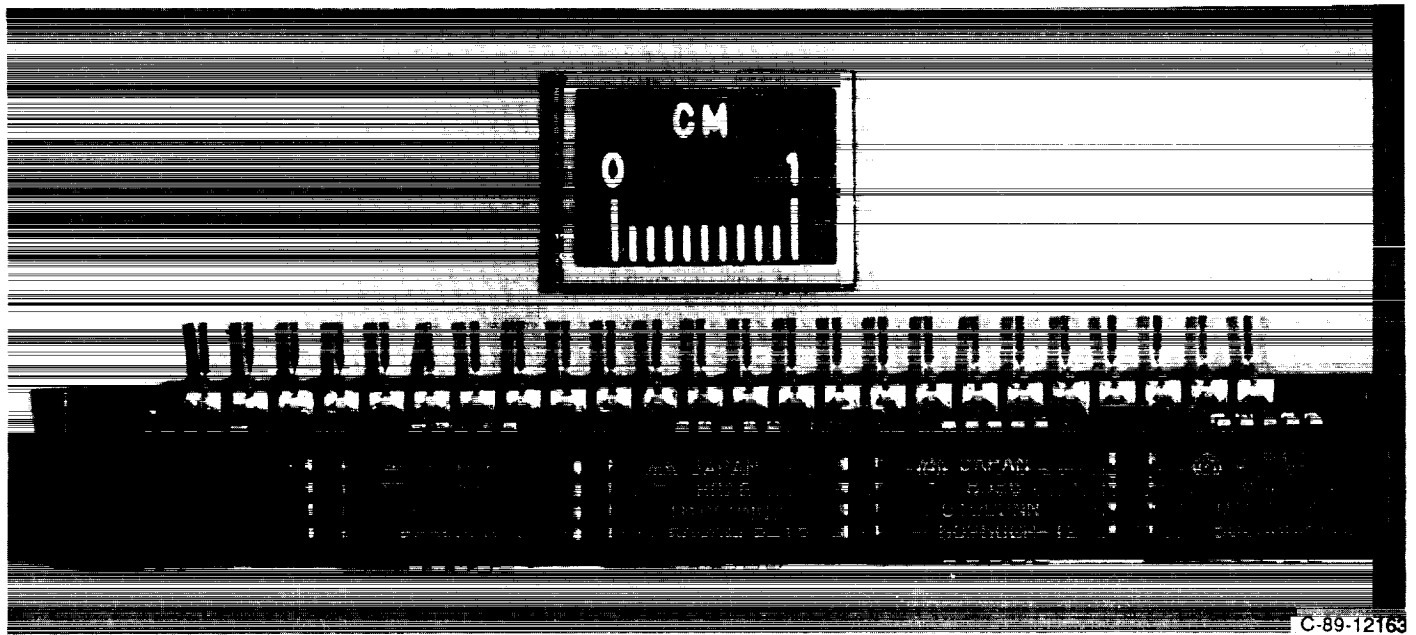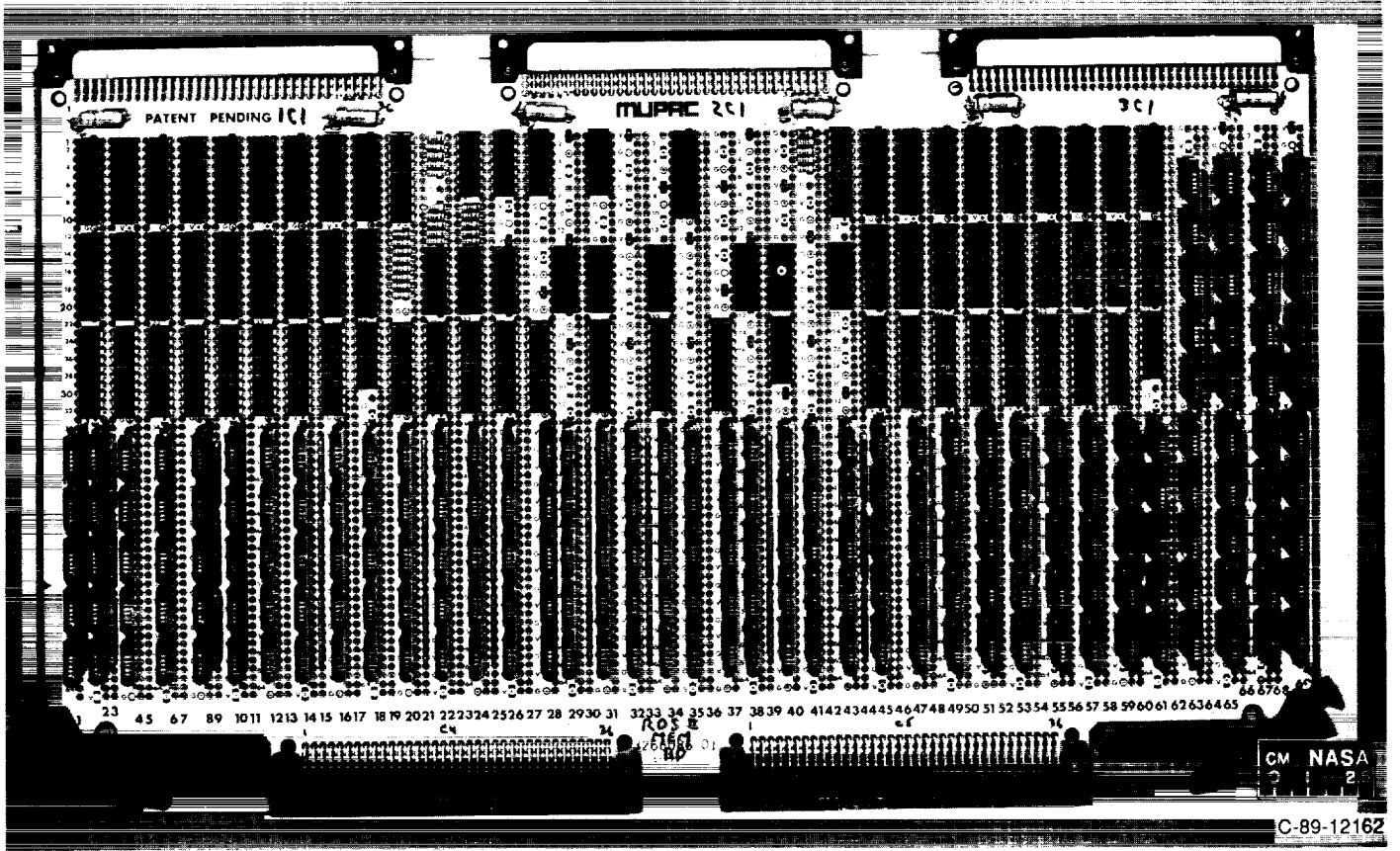Figure 1. - Site block diagram (typical configuration).

FROM GROUND TERMINAL

DATA
BUS
CONTROL
CLOCK

64

TO EC&M COMPUTER

CONTROL

```
FIFO MEMORY
BOARD
```

```
TIMING & CONTROL
BOARD
```

```
EC&M
INTERFACE
```

```
CONTROL
PANEL
```

```
VARIABLE COUNT
WORD CLOCK
GENERATOR
```

64

```
VCXO
```

```
CLOCK DISTRIBUTION BOARD
```

```
P/S
CONVERTER
```

```
DELAY
MONITOR
```

```
INPUT
FREQUENCY
MONITOR
```

```
OUTPUT
FREQUENCY
MONITOR
```

```
DOPPLER
SHIFT
MONITOR
```

```
IEEE-488 EXTENDER INTERFACE
```

DATA
&
CLOCK

CONTROL

MONITORS

TO
MODULATOR

TO
POST MODULATOR
SWITCH

TO EC&M
COMPUTER

Figure 2. - Range delay simulator block diagram.

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(a)

(b)

Figure 3. - RDS memory board (a) and DRAM module (b).

ORIGINAL PAGE
BLACK AND WHITE PHOTOGRAPH

- 3 BANKS OF 14 MODULES-EACH CONTAINING 5 MEMORY CHIPS.
- 210 MEMORY CHIPS OVERALL-55 MBIT CAPACITY.
- CHIPS ARE EACH 256K X 1 WITH ACCESS TIME OF 120 NSEC.
- FIRST-IN-FIRST-OUT (FIFO) ADDRESS CONFIGURATION.
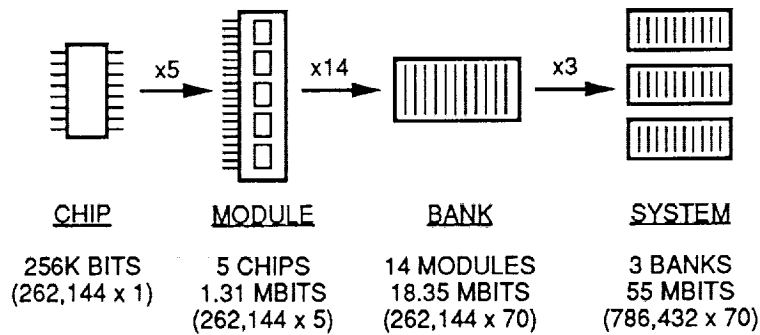- RESULTING FIFO MEMORY IS 786,432 X 70.

CHIP	MODULE	BANK	SYSTEM
256K BITS	5 CHIPS	14 MODULES	3 BANKS
(262,144 x 1)	1.31 MBITS	18.35 MBITS	55 MBITS
	(262,144 x 5)	(262,144 x 70)	(786,432 x 70)

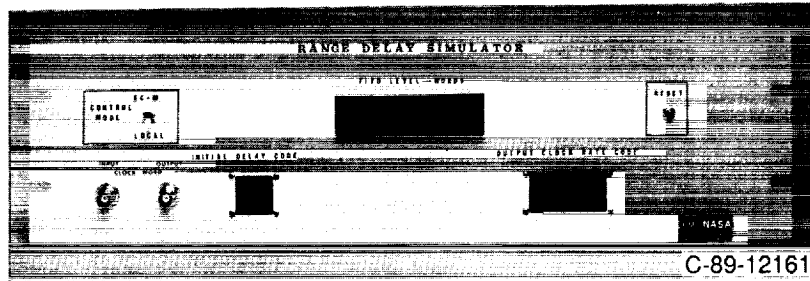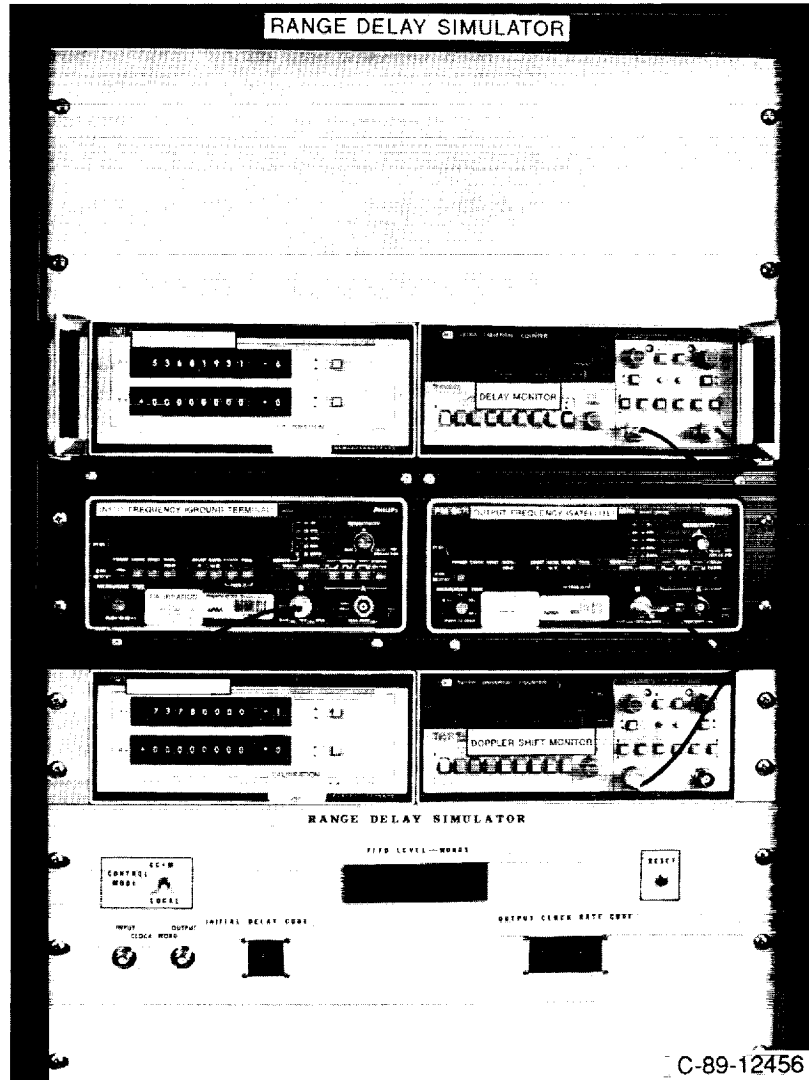Figure 4. - RDS memory organization.

Figure 5. - RDS control panel.

SWITCH SETTING	INITIAL DELAY CONTROL CODE	DELAY (WORDS)	DELAY (msec)	SIMULATED RANGE (miles)	SIMULATED RANGE (km)
0	0000	280 000	81.0	15 093	24 289
1	0001	300 000	86.8	16 171	26 024
2	0010	320 000	92.6	17 249	27 759
3	0011	340 000	98.4	18 327	29 493
4	0100	360 000	104.1	19 405	31 228
5	0101	380 000	110.0	20 483	32 963
6	0110	400 000	115.7	21 561	34 698
7	0111	408 000	118.1	21 993	35 392
8	1000	416 000	120.4	22 424	36 086
9 *	1001	424 000	122.7	22 855	36 780
10	1010	432 000	125.0	23 286	37 474
11	1011	440 000	127.3	23 718	38 168
12	1100	460 000	133.1	24 796	39 903
13	1101	480 000	138.9	25 874	41 638
14	1110	500 000	144.7	26 952	43 373
15	1111	520 000	150.5	28 030	45 108

* geosynchronous orbit

Figure 6. - RDU initial delay control codes.

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Figure 7. - Top portion of RDS rack (monitors and control panel).

Figure 8. - RDS chassis.

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16. Abstract

The Systems Integration, Test, and Evaluation (SITE) facility at NASA Lewis Research Center is presently configured as a satellite-switched time division multiple access (SS-TDMA) network simulator. The purpose of SITE is to demonstrate and evaluate advanced communication satellite technologies, presently embodied by POC components developed under NASA contracts in addition to other hardware, such as ground terminals, designed and built in-house at NASA Lewis. Each ground terminal in a satellite communications system will experience a different aspect of the satellite's motion due mainly to daily tidal effects and station keeping, hence a different duration and rate of variation in the range delay. As a result of this and other effects such as local oscillator instability, each ground terminal must constantly adjust its transmit burst timing so that data bursts from separate ground terminals arrive at the satellite in their assigned time slots, preventing overlap and keeping the system in synchronism. On the receiving end, ground terminals must synchronize their local clocks using reference transmissions received through the satellite link. A feature of the SITE facility is its capability to simulate the varying propagation delays and associated Doppler frequency shifts that the ground terminals in the network have to cope with. Delay is achieved by means of two NASA Lewis designed and built range delay simulator (RDS) systems, each independently controlled locally with front panel switches or remotely by an experiment control and monitor (EC/M) computer.

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