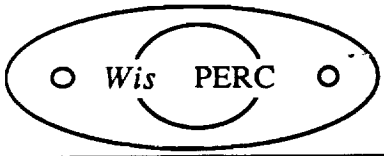

Wisconsin Power Electronics Research Center

NASA Grant Report

HIGH POWER DENSITY DC/DC CONVERTER - SELECTION OF CONVERTER TOPOLOGY

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TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Goal

The goal of this project is the development of high power, high power density dc/dc converters at power levels in the multi-kilowatt to megawatt range for the aerospace industry. The issue of high power density at these power levels has rarely been addressed. The major components in a dc/dc converter, in terms of weight, are the transformer and the filter elements. The key to reducing the weight of these components is, undeniably, in recognizing the need for higher switching frequencies. High frequency operation also allows good system response, good regulator attributes and low acoustic noise levels. However, to maintain an overall high system efficiency and low cooling requirements, the various frequency dependent losses, including semiconductor device switching losses, transformer losses and losses resulting from secondary effects such as diode reverse recovery, need a considerable attention.

Device switching losses increase proportionally with frequency. Given the state-of-the-art high speed devices, like IGBTs and MCTs, it is seen that some form of soft-switching technique, to minimize the switching losses, is mandatory. The underlying principle of soft-switching is to ensure zero voltage/zero current conditions on the switching device during its turn-on/turn-off. Such schemes are broadly classified under Zero Voltage Switching(ZVS) and Zero Current Switching(ZCS) techniques. Typically, ZVS schemes allow higher frequency operation and lower sensitivity to system parasitics, such as diode reverse recovery effects and device-parasitic-capacitor dump. Soft-switching also results in lower radiated Electromagnetic Inteference(EMI).

The transformer, a necessary element in any high power dc/dc converter for galvanic isolation, is by far the most dominant factor in the power density criteria. The two loss components associated with the transformer are core and copper losses. Since, core losses are a strong function of the frequency and the flux density, various state-of-the-art high frequency core materials, such as Ferrites, Metglas and Permalloy 80 to name a few, need to be investigated. Copper losses, arising from the skin and proximity effects, call for a better understanding of the leakage flux distribution in the winding window. This involves a study of the different winding configurations and conductor types. The losses associated with the secondary effects, mentioned earlier, arise mainly from the interaction of the leakage inductance and diode reverse recovery. The energy trapped in the leakage inductance during reverse recovery of a diode must be dissipated when the diode snaps off. This results in high voltage stresses in the circuit. Hence, minimization and control over the leakage inductance, in such applications, is also an important issue.

A significant portion of the overall power density is associated with the filter capacitors. The size of these capacitors is governed, mainly by the rms currents flowing through them. In conventional high power dc/dc converters, commutation-grade capacitors are used which tend to be bulky and lossy. The recently introduced multi-layer ceramic(MLC) capacitors offer much higher power densities and need to be investigated for our application.

This project, funded by the National Aeronautics & Space Administration(NASA), Lewis Research Center, Cleveland, Ohio, is subdivided into the following major tasks :

1) Selection of a converter topology
2) Design and fabrication of the converter
3) Extension to megawatt power levels

The focus of this report is on Task 1. The prototype converter is rated for an output power of 50 kW at an input voltage of 200 Vdc and

output voltage of 2000 Vdc. The overall power density must be 0.2 - 0.3 kg/kW. The switching frequency has been selected as 50 kHz.

1.2 Organization of Report

A brief survey of the state-of-the-art in the dc/dc converter topologies is presented in Chapter Two. In the light of the given specifications three full-bridge converter topologies, with quasi-square wave(square wave with resonant switching transition) operation, are proposed.

The detailed analysis and operating characteristics of each of the proposed topologies are presented in Chapter Three. A fundamental model for the dual active bridge topology is also shown here.

Chapter Four deals with the issue of selection of the optimum topology from amongst the proposed topologies, based on the requirements of high power density, high reliability and ease of control.

Conclusions and aspects of future work are presented in Chapter Five.

CHAPTER 2

REVIEW OF PREVIOUS WORK

2.1 Introduction

In the light of our design objectives of high power and high power density the existing literature on dc/dc converter technologies is reviewed. Various state of the art hard-switching pwm schemes are examined, and it is seen that the advantage of high power density achievable by increasing the frequency are soon offset by the high switching losses incurred. Recognizing the need for a soft-switching methodology, to eliminate the switching losses at the high frequencies of interest, the various resonant and quasi-resonant converters are investigated. The VA stresses experienced by the switching devices and the resonant elements, especially at the high power levels, become intolerably high. The full-bridge converter derived from the resonant pole, which combines the desirable characteristics of hard-switching pwm and soft-switching schemes, is seen to be the most viable option.

2.2 Hard Switching PWM Schemes

Most dc/dc converters in use today are derived from the three basic single quadrant topologies, buck, boost and buck-boost converters, shown in Figure 2.2.1 [1]. However, since power transfer is achieved through a single switching device, such circuits are not suitable at the high power levels of interest.

At the high power end, the full-bridge converter with galvanic isolation on the intermediate high frequency ac link would be the preferred topology [1] (Figure 2.2.2). The main advantages of these schemes include, constant frequency operation allowing optimum design of magnetic and filter components, minimum VA stresses, good

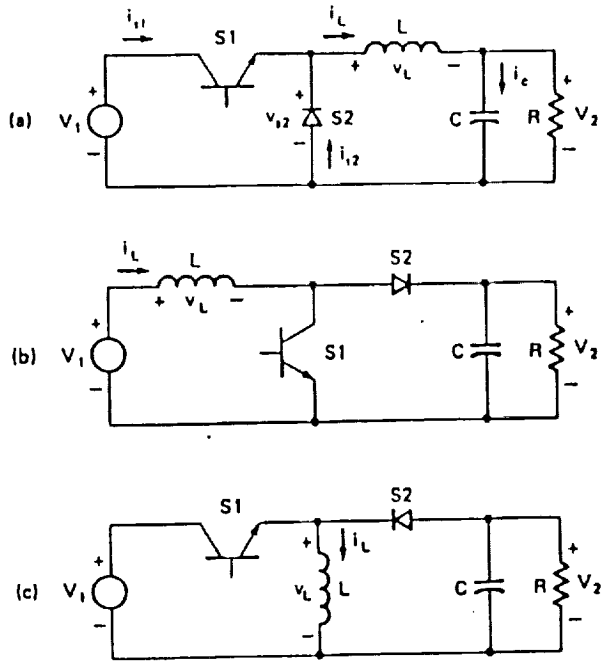


Figure 2.2.1 Low Power Hard-Switched PWM DC/DC Converters (a)Buck (b)Boost (c)Buck - Boost

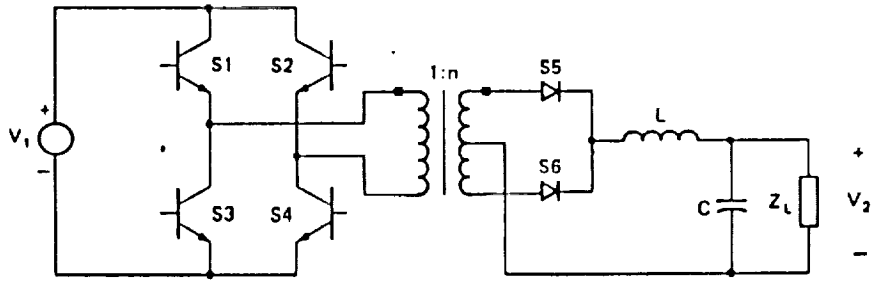


Figure 2.2.2 Full Bridge Hard-Switched PWM DC/DC Converter For High Power Application

control range and controllability. However, the major drawback of increasing device switching losses with increasing frequency, puts an upper limit on the switching frequency and hence power density. Other problems, which substantially degrade the performance of these converters at high frequencies, are the high voltage stress induced by the parasitic inductances following diode reverse recovery, the additional inductive filter required on the output(besides the capacitor) and the high amounts of radiated electromagnetic interference(EMI) generated from the hard-switching action.

2.3 Soft Switching Schemes

To limit the rate of rise of voltage/current experienced by the switching device, in hard-switching pwm strategies, often reactive snubber elements have to be used. This also provides an easy method of diverting the energy that would be dissipated in the device during the switching transition. However, the energy stored in the reactive snubber elements must typically be dissipated during a subsequent part of the switching cycle. The class of circuits which allow an automatic and lossless resetting of the snubber reactive elements through inherent circuit operation are referred to as soft switching converters, which are broadly categorized as - Zero Voltage Switching(ZVS) and Zero Current Switching(ZCS) converters.

In ZVS schemes the device is made to turn-on and off under near zero-voltage conditions. Figure 2.3.1a shows a typical implementation. The device is turned-on while the anti-parallel diode is conducting, hence by virtue of the on-state condition of the diode the device sees near zero-voltage. Turn-off is initiated when the device is carrying a certain minimum current. As the device turns off, the remaining load current charges up the purely capacitive snubber, thus limiting the rate of rise of voltage across the device. To ensure near zero-voltage condition, the device must be oversnubbed. Such a scheme inherently requires the load to be inductive, which infact interacts with the snubber capacitor during turn-off to set up a

resonant transition of the voltage. The added benefits of this scheme are prevention of voltage stresses associated with diode reverse recovery effects and elimination of the snubber capacitor dump during turn-on.

A typical implementation of ZCS scheme is shown in Figure 2.3.1b. The current through the device is now shaped in a resonant manner, with turn-off occurring naturally at the zero-crossing of the current. At turn-on the series inductance(ideally pure), limits the rate of rise of current through the device. Although, switching losses are virtually eliminated, reverse recovery effects associated with the anti-parallel diode limit the maximum frequency attainable with ZCS schemes.

Various dc/dc converters, utilizing these schemes, have been reported in the literature in the last decade(selected references are mentioned where appropriate), and will now be investigated as to their suitability for our application.

2.3.1 Resonant DC/DC Converters

The series resonant converter, shown in Figure 2.3.2 was proposed by Schwarz[2], and aimed at high power applications. Since the devices used were thyristors the circuit could only be operated under ZCS conditions, which is only effective for switching frequencies below the resonant frequency. Power densities in the 0.9-1.0 kg/kW range at a switching frequency of 10 kHz were reported. Although, these figures can be improved upon by using state-of-the-art high speed devices, high frequency magnetic material and filter capacitors(like multi-layer ceramics), the high VA stresses experienced by the LC-resonant elements and the high current stresses on the devices are a major drawback, especially at the high power levels of interest. For instance, for a 50 kW dc/dc series resonant converter, the kVA rating of the resonant capacitor is approximately 125 kVA, while that for the inductor is 80 kVA. The

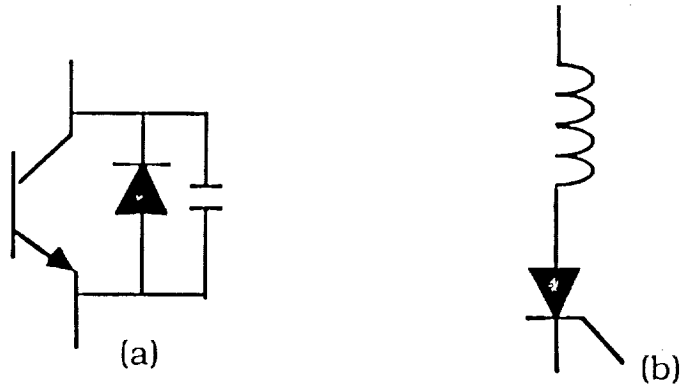


Figure 2.3.1 Typical Soft-Switching implementations
(a)Zero Voltage Switching(ZVS)
(b)Zero Current Switching(ZCS)

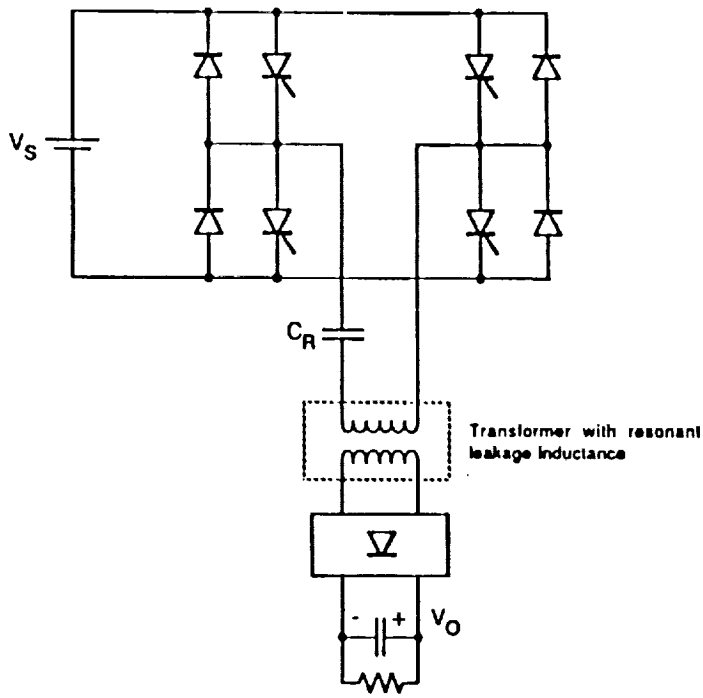


Figure 2.3.2 Full Bridge Series Resonant DC/DC Converter

peak device VA stress is 110 kVA. The component over-rating is seen to constitute a substantial penalty. Moreover, since control of power transfer is achieved by variation of frequency, design of the magnetic and filter elements and EMI-suppression over a wide frequency range become difficult issues.

The parallel output series resonant converter reported by Ranganathan, et al [3] (Figure 2.3.3a), and later extended by Steigerwald [4] to operate under ZVS conditions with gate turn-off devices(Figure 2.3.3b), also suffer from the same problems as the series resonant converter. Current-fed topologies have been discussed by Kassakian[5] and Divan[6].

As seen, in all of the above circuits, the underlying philosophy of power transfer through a resonant circuit, requires that the devices and the resonant elements be rated for a substantially higher VA product rating as compared to the output power. The higher ratings and the higher device conduction losses not only impose an upper limit on the achievable power density but also impose cost penalties which reduce the economic potential of these topologies.

2.3.2 Quasi-Resonant DC/DC Converters(QRC)

Recognizing the advantage of minimal component ratings with conventional hard-switched pwm techniques on the one hand, and the reduced switching losses with resonant converters on the other, the need for a topology with both characteristics was felt necessary. A first step in this direction was initiated by Liu and Lee[7], when they reported the ZVS - QRC derived from the basic buck, boost and buck-boost topologies, shown in Figure 2.3.4. These circuits are typically aimed at low power applications and utilize the frequency as a control variable. These converters exhibit extremely high voltage/current stresses. In particular, the ZVS schemes need to handle very high voltage stresses under light load conditions. The ZCS-QRC schemes [8] have high current stresses and are susceptible to problems related

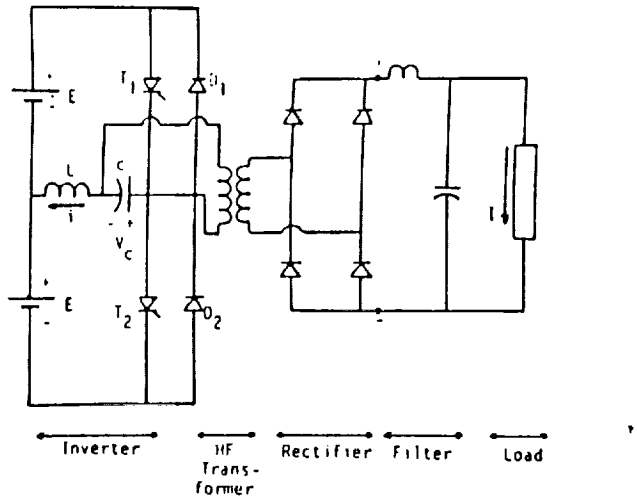


Figure 2.3.3a Half Bridge Parallel Output Series Resonant DC/DC Converter Using Thyristors

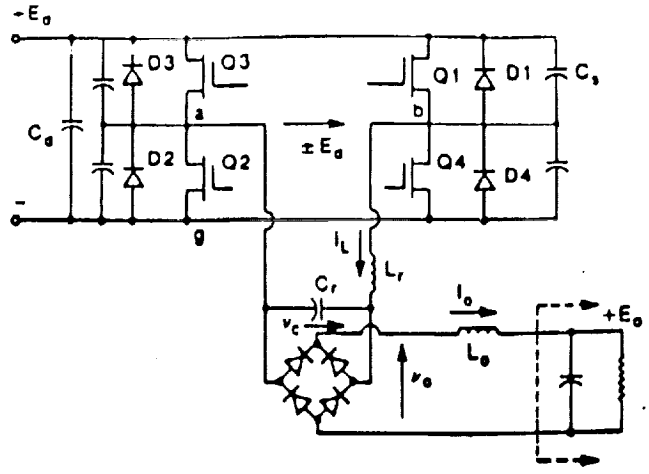


Figure 2.3.3b Full Bridge Parallel Output Series Resonant DC/DC Converter Using Gate Turn-off Devices

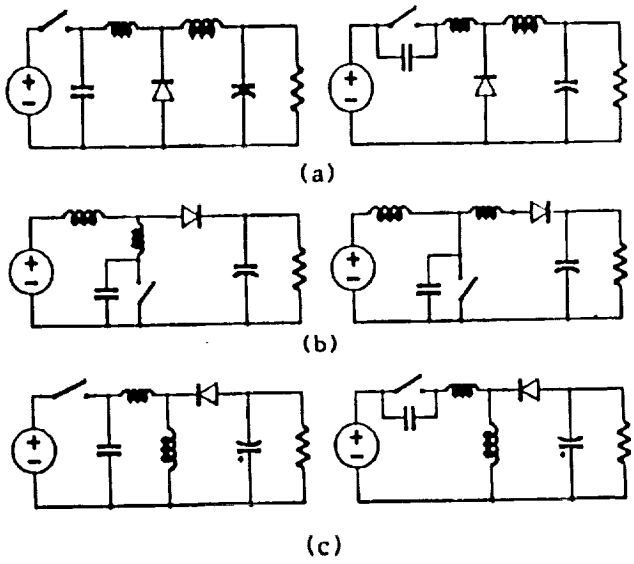


Figure 2.3.4 ZVS Quasi Resonant DC/DC Converters
(a)Buck (b)Boost (c)Buck - Boost

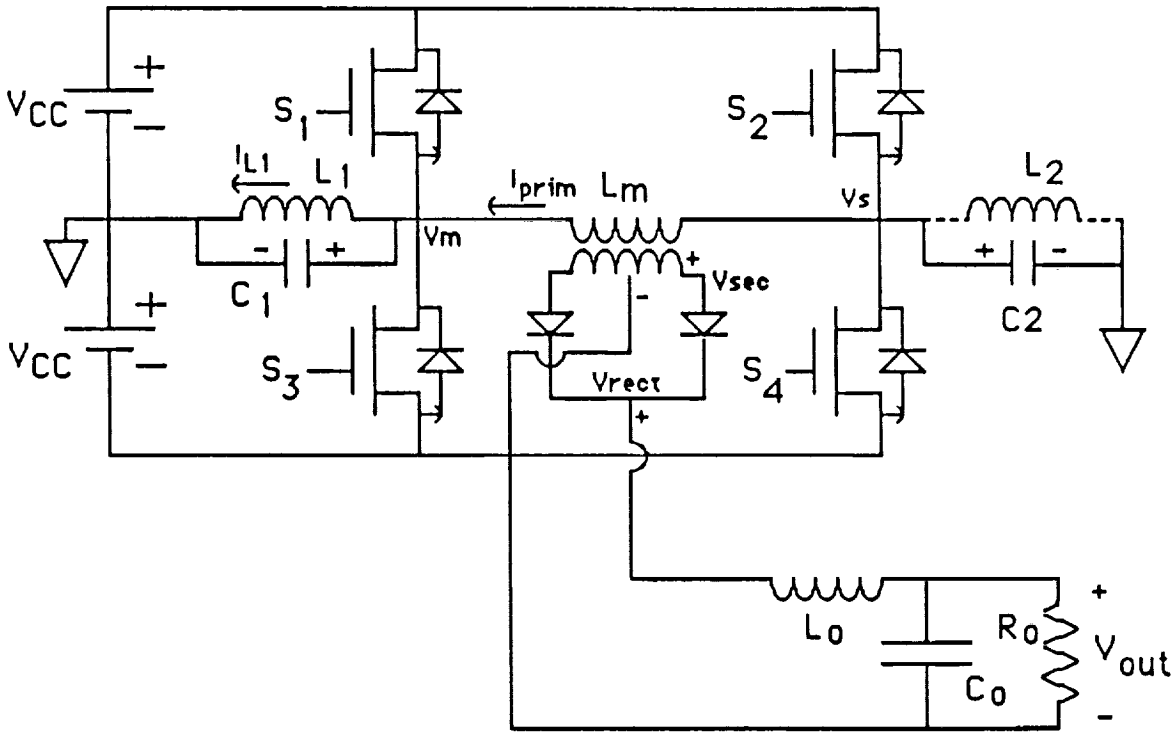


Figure 2.3.5 Pseudo-Resonant DC/DC Converter

with diode reverse recovery and device-parasitic-capacitor dump, and are hence limited in the maximum attainable switching frequency.

2.3.3 Resonant Pole Converter

The possibility of realizing quasi-square-wave voltage(square wave, resembling conventional pwm schemes, with resonant switching transitions) for soft-switching utilizing the concept of the resonant pole[9] was recently demonstrated by Patterson, et al[10]. The paper discusses a full-bridge version of the resonant pole called the pseudo-resonant dc/dc converter(see Figure 2.3.5), and is seen to be amenable for high power applications. Moreover, as mentioned earlier, very high frequency operation is easily attainable given the ZVS characteristics of the topology. This also implies that all the dominant parasitics, namely transformer leakage inductance and internal device capacitance can be efficiently utilized. With the device turn-on synchronized with its anti-parallel diode conducting, reverse recovery effects associated with the diode are virtually subdued. More importantly since the converter operates under a pwm control strategy, a wide range of operation is achievable unlike the resonant converters where frequency is the control parameter. This also simplifies the task of designing the magnetic and filter elements.

2.4 Component Technology

The power density achievable in high frequency dc/dc converters is typically limited by the state of component technology. In particular the devices, magnetic materials and capacitor technology dramatically influence the frequency, and thus the size of the converter. At higher power levels, these limitations are particularly severe. The device has been one of the major limitations in the past. The only reliable and rugged device in the past has been the thyristor. This has prompted its use in the series resonant converter, with good success. With the introduction of newer gate turn-off devices such as

Bipolar Junction Transistors (BJT's) and Insulated Gate Bipolar Transistors (IGBT's), the performance achievable has been significantly advanced. Under soft switching conditions, the BJT has been used at frequencies approaching 30 kHz in multi-kilowatt applications [11]. For the IGBT based converters, it seems possible that frequencies as high as 50 kHz may be feasible at power levels of up to 50 kHz. The possible advent of newer devices such as the MOS Controlled Thyristor (MCT) will enhance the possibilities even more.

One of the major limitations in high frequency designs has been the lack of good magnetic core materials. Ferrites have been very popular for low power applications, and are good at frequencies ranging from the tens of kilohertz to a few megahertz. However, the low flux densities and fragility of the core have limited its use in high power applications. At frequencies in the 10-20 kHz range, other core materials such as Permalloy 80/20 have shown a lot of promise in high power applications. Newer amorphous materials such as Metglas also raise the possibility of raising the frequency to the 50 kHz range. Another aspect of magnetic design which can contribute significantly to the power density is the fabrication technique. The use of co-axial winding techniques hold great promise for high power high frequency transformers.

The choice of capacitors for resonant and filter applications has been rather restricted in the past, especially for high power applications. Only the commutation grade capacitors could realize the high current ratings of interest. The size and weight associated with these capacitors was one of the major limitations in the quest for high power densities. The availability in recent years, of multi-layer ceramic (MLC) capacitors has seen gains in power densities of more than an order of magnitude. For applications where power density is the paramount concern, MLC capacitors offer a very attractive alternative.

Given advances in component technology, it is important to select the converter topology so that the components are well utilized. The use of topologies that over stress components is bound to result in

poorer power densities than topologies where the components are well utilized. The major thrust of this research effort is in the quest for dc/dc converter topologies which feature good component utilization and which offer the benefits of soft switching at the same time.

2.5 Proposed DC/DC Converter Topologies

Recognizing the potential of the resonant pole, three new dc/dc converter topologies suitable for high power applications are proposed[12]. These topologies are seen to meet basic requirements for high power dc/dc converters which could potentially realize high power densities. These features include the use of a full bridge for minimum device stresses, constant frequency operation for easier design of transformers, filter components and system controllers, the use of all major system parasitics and the use of a minimal converter topology. The concept of a minimal converter topology is important for higher power densities, because it uses only those components which are absolutely essential for a dc/dc conversion function. The three proposed topologies, which satisfy these basic criteria, are introduced below.

Proposed Topology A - Single Phase Single Active Bridge DC/DC Converter

In the pseudo-resonant dc/dc converter[10], since the transformer is coupled to the output filter inductor(which essentially behaves as a current source), large voltage spikes are induced by the leakage inductance of the transformer at every switching of the output diode bridge. This problem worsens under the diode reverse recovery effects. Hence, the leakage inductance needs to be minimized, requiring good transformer design techniques. Additional inductors L1 and L2(shown in Figure 2.3.5) are also required to achieve soft-switching of the input bridge devices over a reasonable control range.

Overall, the circuit tends to be quite complex and does not lend itself easily to high power applications.

Transferring the output filter inductor to the ac side(in effect lumping it with the leakage inductance), completely changes the operating characteristics of the converter. Energy stored in this equivalent leakage inductance can be naturally and in a lossless manner transferred to the load. Also, reasonable control range can be realized under soft-switching conditions with this sole effective leakage inductance. The above modification of the pseudo-resonant dc/dc converter suggests its suitability for high power applications, and is our new proposed Topology A, shown in Figure 3.2.1a. Power flow is governed by the phase-shift between the two resonant poles of the input bridge.

Proposed Topology B - Single Phase Dual Active Bridges DC/DC Converter

The idea behind this topology comes from an understanding of the diode recovery process as being akin to the existence of an active device in anti-parallel with it[13]. Observing that the circuit of Topology A naturally handles the diode recovery process, it is proposed that if the diodes are replaced by active devices then a much simpler control strategy can be devised. The input and active output bridges can generate fixed-frequency square waves(in reality, quasi square waves given the resonant nature of the switching transitions for soft switching) which are phase-shifted from each other. The power transfer can now be controlled by controlling this phase-shift. Also, given the symmetrical nature of the converter, bidirectional power flow can be achieved. Figure 3.3.1a shows a circuit schematic of this new proposed topology.

Proposed Topology C - Three Phase Dual Active Bridges DC/DC Converter

This topology is a three phase extension of Topology B(see Figure 3.4.1a). At the time this circuit was proposed, it was felt that this would indeed realize the highest power density considering the much lower filter capacitor requirements, and the state-of-the-art in high power density capacitors then being the commutation grade. However, with the recently available Multi-Layer Ceramic(MLC) capacitors, it is seen that Topology B can achieve comparable power densities with the added advantage of a simpler transformer. Nevertheless, for the sake of completeness this topology will also be fully analyzed and compared with the other two proposed topologies.

It must be mentioned here that the dual of topologies A and B using thyristors have been analyzed and implemented for superconducting magnetic energy storage(SMES) systems[14,15,16].

To conclude this section, all the three proposed topologies possess the following desirable features:

- virtually zero switching losses for all devices
- use of transformer leakage inductance as the main energy transfer element, potentially capable of higher power densities
- operate at constant frequency in a pwm manner
- high efficiency(no trapped energy)
- low sensitivity to system parasitics
- possibility of paralleling, as a result of the current transfer mechanism

In addition, the dual bridge topologies exhibit

- two-quadrant operation
- buck-boost operation
- smaller transformer and filter.

The focus of this report, as mentioned earlier, is the selection of a suitable converter topology to meet the desired objectives. With this in mind, the three proposed topologies are thoroughly analyzed to provide a theoretical basis for comparison and selection.

CHAPTER 3

STEADY STATE ANALYSIS OF PROPOSED TOPOLOGIES

3.1 Introduction

This chapter presents the analysis of the steady state operating characteristics of the three proposed dc/dc converter topologies[12] :

(a) Single-Phase Single Active Bridge DC/DC Converter(Topology A)
(b) Single-Phase Dual Active Bridges DC/DC Converter(Topology B)
(c) Three-Phase Dual Active Bridges DC/DC Converter(Topology C)

These topologies are "minimal" in structure in that they consist of the input and output filters, the two device bridges(active and/or passive, and single or three phase versions) and a transformer, all components essential for a dc/dc converter. They all operate at a constant switching frequency and exhibit soft switching for reduced switching losses. The circuits utilize the leakage inductance of the transformer as the main energy transfer element thus rendering the filters on both the input and output sides purely capacitive.

Since high power density is a crucial requirement, it is important to minimise the device switching losses by adopting a soft-switching methodology. In the proposed topologies all semiconductor devices can operate under conditions of zero-voltage switching. To elaborate, the turn-on of any active device such as MOSFET, BJT, IGBT, MCT is initiated while its anti-parallel diode is conducting. This ensures that the active device naturally takes over as the diode current reverses, and more importantly under almost zero-voltage conditions. Thus, turn-on losses are virtually eliminated. An added benefit of this mode of turn-on is the prevention of high voltage stresses, typical of inductive circuits in the presence of diode reverse recovery effects.

To realize zero-voltage turn-off, purely capacitive snubbers are required. Moreover, the turn-off process must be initiated when the active device is carrying a certain minimum current, the value of which is dependent on the circuit inductance and snubber capacitance. As the current through the device falls, the remaining current is diverted to the snubber capacitor causing its voltage to rise in a resonant manner. To maintain almost zero-voltage across the device during its fall time, and hence virtually eliminate the turn-off losses, the device needs to be oversnubbed.

The necessary conditions at the instant of turn-on and turn-off dictate a certain phase relationship between the voltage and current as seen from the a.c. terminals of the input and output bridges. To realize these conditions, each bridge must be operated such that an effective lagging load is seen by looking into the transformer from its a.c. terminals. These constraints, which are crucial for realizing soft-switching on all the devices of both the bridges(and will be hence referred to as the soft-switching constraints), limit the region of operation on the Vout - Iout plane, as will be seen in the following analyses.

The primary objectives behind the analysis of each topology is :

1) to study the dependence of the output power, output voltage, transformer-kVA and filter capacitor-kVA on the control parameters

2) to identify the regions of operation, under soft-switching, on the Vout-Iout plane, and finally

3) to ascertain first-pass numbers on the kVA-ratings of the transformer and filter elements and device stresses at the given specifications, under optimum operating conditions for each topology. This gives a basis for comparing the three topologies.

To simplify the analysis the following assumptions are made with regard to each component of the proposed circuits :

A) The Switching Device :

1) Forward drop across the transistor or its antiparallel diode is zero.
2) The switching speed of the transistor/diode is infinite.
3) The diode has no reverse recovery effect.

B) The Transformer :

1) Negligible winding resistance as compared to the leakage reactance at the high switching frequencies of interest.
2) Infinite magnetizing inductance.

C) The Filter Capacitors :

1) Infinite capacitance, hence can be modelled as voltage sources.
2) Zero Effective Series Resistance(ESR).
3) Zero Effective Series Inductance(ESL).

D) The Snubber Capacitors :

1) The influence of the snubber capacitors on the voltage and current at the transformer terminals is ignored. This is justifiable, for this analysis, since it only comes into play during the switching transitions, which is substantially smaller than the switching period.

The influence of finite magnetizing inductance of the transformer and the minimum current constraint at initiation of turn-off of the active devices on the limits of the desired region of operation for each topology, will be presented in a future report.

3.2 Single-Phase Single Active Bridge DC/DC Converter(Topology A)

Figure 3.2.1(a) shows the circuit schematic of Topology A. It consists of a dc voltage source followed by a capacitive filter feeding into a single-phase input active bridge, which serves as the dc to high frequency inverter. The input filter eliminates the undesirable high frequency current components generated by the switching action of the inverter. A transformer interfaces the inverter to the output diode rectifier bridge with a capacitive filter on its output side. Again, the purpose of the output filter is the same as that of the input. Conceptually, the entire circuit can be viewed as a voltage source interfaced to another voltage source through a current source, which is essentially the transformer modelled by its leakage inductance. The primary-referred equivalent circuit is shown in Figure 3.2.1(b). L is the total leakage inductance referred to the primary side.

The output dc voltage, and hence the output power, can be controlled by controlling the primary voltage of the transformer. To achieve this the two poles of the input bridge are phase shifted from each other by an angle β. Figure 3.2.2 shows the operating waveforms. v_{ag} and v_{bg} are the pole voltages, and v_p, which is the difference in the two pole voltages, is applied across the primary winding of the transformer. Moreover, since the output diode bridge is current driven the following constraints must be satisfied :

(i) When i_p is positive , v_s' must be positive(= V_o')
(ii) When i_p is negative, v_s' must be negative(= $-V_o'$)

Three modes of operation can be identified. In each mode, the inductor current, i_p as a function of $\theta = \omega t$, where ω is the switching frequency,is given by,

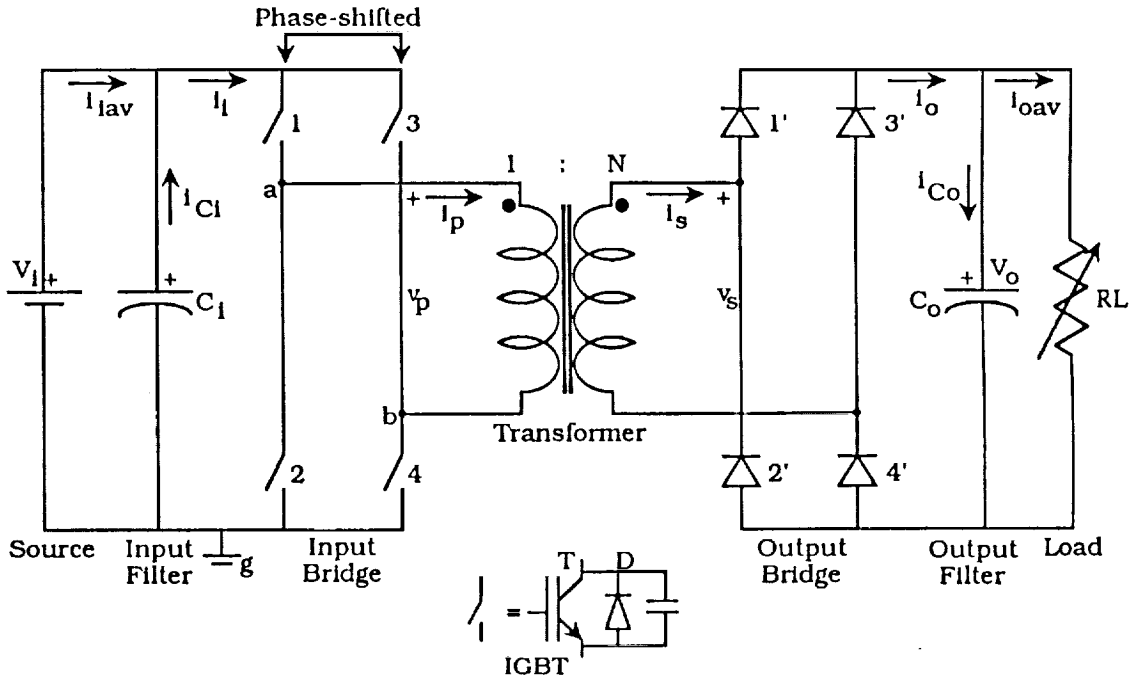


Figure 3.2.1a Schematic of Single Phase Single Active Bridge DC/DC Converter(Topology A)

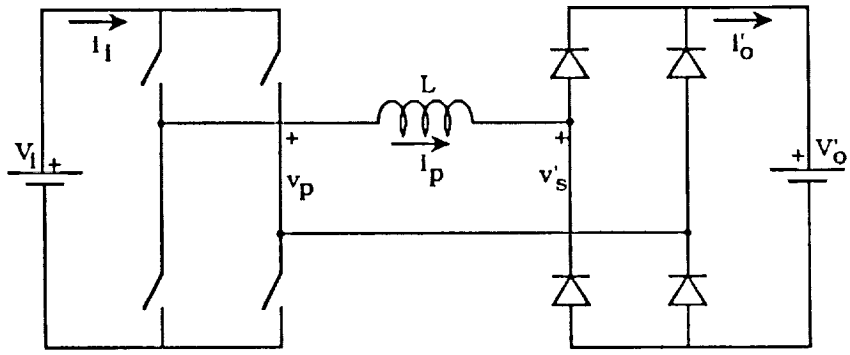
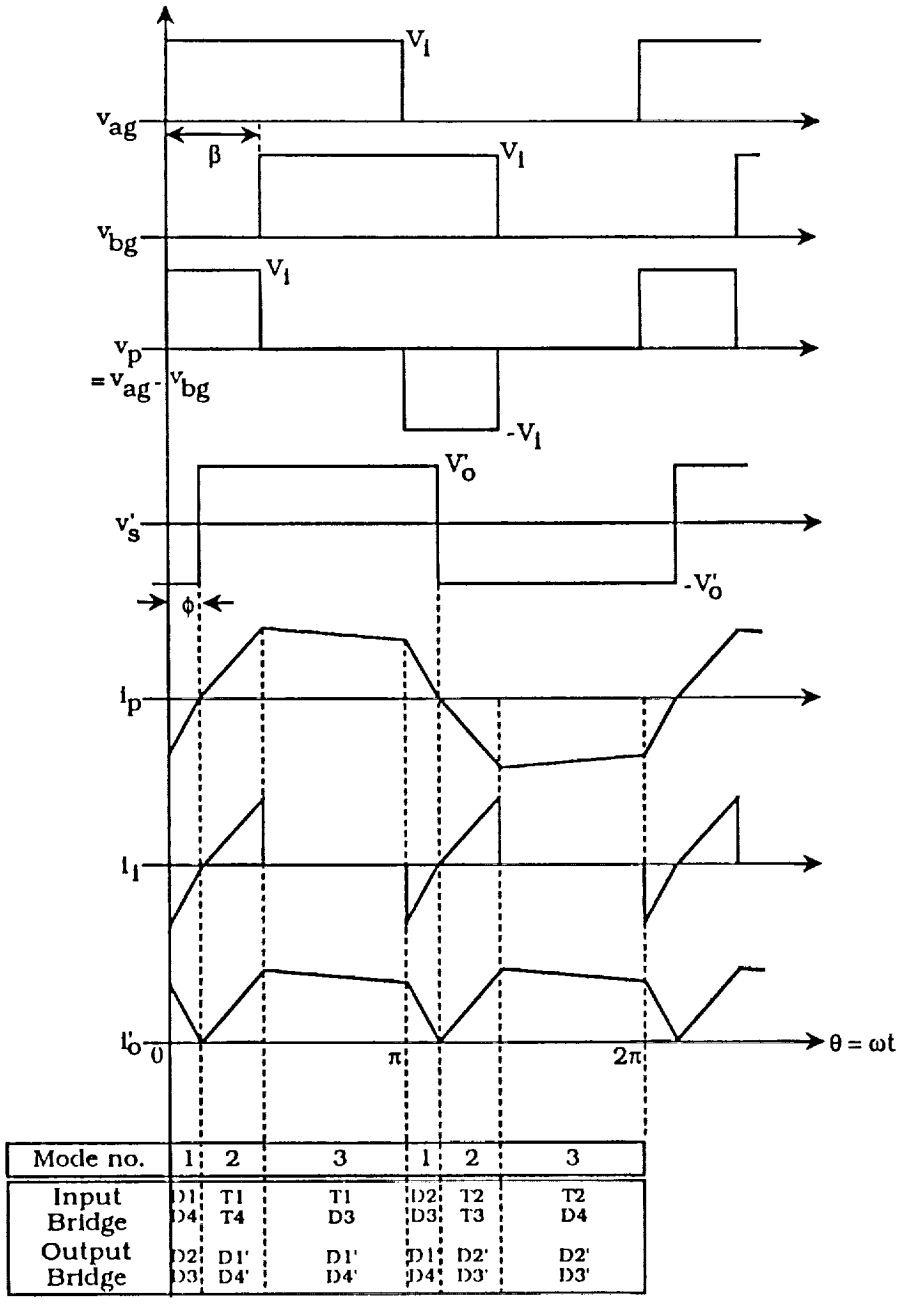


Figure 3.2.1b Primary-Referred Equivalent Circuit of Topology A



Mode no.	1	2	3	1	2	3
Input Bridge	D1 D4	T1 T4	T1 D3	D2 D3	T2 T3	T2 D4
Output Bridge	D2 D3	D1' D4'	D1' D4'	D1' D4'	D2' D3'	D2' D3'

Figure 3.2.2 Idealized Operating Waveforms for Topology A

$$i_p(\theta) = \frac{\left[v_p(\theta) - v_s'(\theta)\right]}{\omega L}(\theta - \theta_i) + i_p(\theta_i) \qquad \theta_i \le \theta < \theta_f$$

...(3.2.1)

where, θ_i and θ_f are the start and end of each mode respectively, and $i_p(\theta_i)$ is the initial current of each mode. Therefore, from Figure 3.2.2 and Equation(3.2.1),

Mode 1 : $0 \le \theta < \phi$

$$v_p(\theta) = V_i \quad ; \quad v_s'(\theta) = -V_o'$$

$$i_p(\theta) = \frac{V_i + V_o'}{\omega L}(\theta) + i_p(0) \qquad \text{...(3.2.2)}$$

Mode 2 : $\phi \le \theta < \beta$

$$v_p(\theta) = V_i \quad ; \quad v_s'(\theta) = V_o'$$

$$i_p(\theta) = \frac{V_i - V_o'}{\omega L}(\theta - \phi) + i_p(\phi) \qquad \text{...(3.2.3)}$$

Mode 3 : $\beta \le \theta < \pi$

$$v_p(\theta) = 0 \quad ; \quad v_s'(\theta) = V_o'$$

$$i_p(\theta) = \frac{-V_o'}{\omega L}(\theta - \beta) + i_p(\beta) \qquad ...(3.2.4)$$

At the end of the half cycle, from symmetry conditions,

$$i_p(\pi) = -i_p(0) \qquad ...(3.2.5)$$

Hence, solving for $i_p(0)$, the complete current waveform can be obtained. From Equations(3.2.2) - (3.2.5),

$$i_p(0) = \frac{V_o'(\pi - 2\phi) - V_i\beta}{2\omega L} \qquad ...(3.2.6)$$

From the soft-switching constraints, which require that the active device be conducting at turn-off, we get,

$$i_p(0) \leq 0$$

This, in turn, implies that,

$$\phi \geq 0 \qquad ...(3.2.7)$$

Further, from the output diode bridge constraints,

$$i_p(\phi) = 0$$

But, from Mode 1, at $\theta = \phi$,

$$i_p(\phi) = \frac{V_i + V_o'}{\omega L}(\phi) + i_p(0) = 0$$

Hence,

$$i_p(0) = -\frac{V_i + V_o'}{\omega L}(\phi) \qquad \ldots(3.2.8)$$

Therefore, equating the right-hand sides of Equations (3.2.6) and (3.2.8), we get,

$$\phi = \frac{1}{2}(\beta - d\pi) \qquad \ldots(3.2.9)$$

$$\text{where, } d = \frac{V_o'}{V_i} \qquad \ldots(3.2.10)$$

The parameter d represents the primary-referred dc voltage gain of the converter, often referred to as the dc conversion ratio. Comparing equations (3.2.7) and (3.2.9),

$$\beta - d\pi \geq 0$$

or,

$$d \leq \frac{\beta}{\pi}$$

Moreover, the diode bridge on the output restricts the minimum value of the output voltage to zero. Hence,

$$d \geq 0$$

Combining the above two constraints,

$$0 \leq d \leq \frac{\beta}{\pi} \qquad \ldots(3.2.11)$$

Bearing in mind the symmetrical manner in which the input and output bridges operate, the variation of β over the range 0 to π covers the entire operating region allowing soft-switching. Hence, theoretically, the maximum value of d obtainable is 1, as given by the above constraint relation. However, no power can be transferred under these conditions, since the resultant phase-shift between the two bridges is zero.

From a knowledge of $i_p(\theta)$ and the input and output converter switching functions, the steady state operating characteristics of the various quantities of interest, viz. output power, filter-kVA and transformer-kVA over the control parameter, β, and d are derived. Each of these quantities have been normalized to the following base:

$$\text{Voltage base, } V_b = V_i \qquad \ldots(3.2.12a)$$

$$\text{Current base, } I_b = \frac{V_i}{\omega L} \qquad \ldots(3.2.12b)$$

$$\text{Power base, } P_b = V_b * I_b = \frac{V_i^2}{\omega L} \qquad \ldots(3.2.12c)$$

Moreover, since all the voltages and currents are referred to the primary side of the transformer the turns ratio must be taken into account to get the actual output quantities. For instance, $V_o = NV_o'$, $i_o = i_o' / N$, where N is the turns ratio of the transformer.

Output Power :

$$P_o = V_i I_{iav} = V_o' I_{oav}'$$

Now,

$$I_{iav} = \frac{1}{2\pi}\left[(\phi)i_p(0) + (\beta - \phi)i_p(\beta)\right]$$

$$= \left[\frac{V_i}{\omega L}\right]\frac{d}{4}\left[2\beta - \pi d^2 - \frac{\beta^2}{\pi}\right]$$

Hence,

$$P_o = \left[\frac{V_i^2}{\omega L}\right]\frac{d}{4}\left[2\beta - \pi d^2 - \frac{\beta^2}{\pi}\right] \qquad ...(3.2.13)$$

To ascertain the absolute maximum power transfer point, the output power is first partially differentiated with respect to β, keeping d constant. Hence,

$$\frac{\partial P_o}{\partial \beta} = \left[\frac{V_i^2}{\omega L}\right]\frac{d}{4}\left[2 - \frac{2\beta}{\pi}\right] = 0$$

This gives us a very convenient result that for any d(within the permissible range), maximum power can be transferred at $\beta = \pi$. Of course, to ensure that this is the maximum power condition, one must verify that the second derivative of output power with respect to β is less than zero at $\beta = \pi$. This is seen to be true.

Now, to find the absolute maximum power transfer point for the converter, the output power can now be differentiated w.r.t. d after setting $\beta = \pi$. Hence,

$$\frac{dP_o}{dd} = \left[\frac{V_i^2}{\omega L}\right]\frac{\pi}{4}\left[1 - 3d^2\right] = 0$$

or,

$$d \approx 0.58$$

Thus, d = 0.58 and $\beta = \pi$ gives the absolute maximum power transfer point.

Figure 3.2.3 shows the variation of output power, P_o, as a function of the control variable, β, with d as a parameter. For each value of d the output power is shown over the soft-switching region. The locus of the minimum power for each d defines the soft-switching boundary, and corresponds to $d = \beta / \pi$. As d increases the range of β, over which soft-switching can be achieved, diminishes. The curve corresponding to d = 0.58 is shown. The absolute maximum power transfer point is also shown on this curve at $\beta = \pi$(see point labelled X).

Transformer kVA :

$$T\_kVA = \frac{v_{prms} * i_{prms} + v'_{srms} * i'_{srms}}{2}$$

However, since magnetizing current is assumed zero,

$$i_{prms} = i'_{srms}$$

Therefore,

$$T\_kVA = \frac{(v_{prms} + v'_{srms}) * i_{prms}}{2} \qquad \text{...(3.2.14a)}$$

where,

$$v_{prms} = V_i \sqrt{\frac{\beta}{\pi}}$$

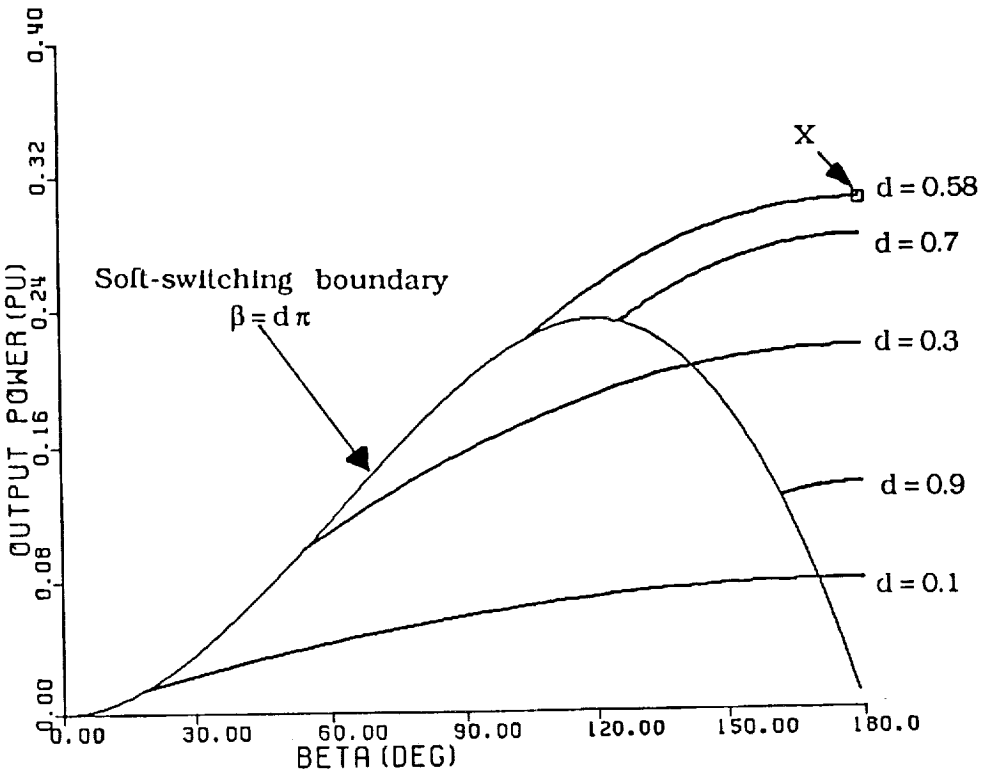


Figure 3.2.3 Output Power vs Beta with d as a parameter, under soft switching operation(Topology A)

$$v'_{srms} = V'_o = d\,V_i$$

$$i_{prms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_p^2\, d\theta}$$

Define,

$$\text{Transformer Utilization} = \frac{P_o}{T\_kVA} \qquad \ldots(3.2.14b)$$

Figure 3.2.4a shows the dependence of the transformer kVA on β and Figure 3.2.4b shows its dependence on the output power. In each case a family of curves is plotted with d as the parameter. Again, the soft-switching regions are shown. The locus of the minimum kVA for each d defines the soft-switching boundary. Various design points can be selected based on issues of maximum power transfer capability or range of controllability under soft-switching. From Figure 3.2.4b, it is seen that as one alternative, the transformer can be designed to handle the absolute maximum power of 0.302pu(which is shown on the curve corresponding to d = 0.58) for the minimum kVA. This gives a transformer kVA of 0.475pu and hence, a transformer utilization of 0.636. However, this restricts the range of control upto a point where the transformer kVA cannot exceed the above value. On the other hand, for full range of control over β, the transformer would have to be designed for the maximum kVA required, which is approximately 0.55pu. However, under these conditions the best transformer utilization turns out to be 0.549, which is poorer than the first design. Thus, it is seen that a trade-off between size(and, hence, power density) and controllability must be made.

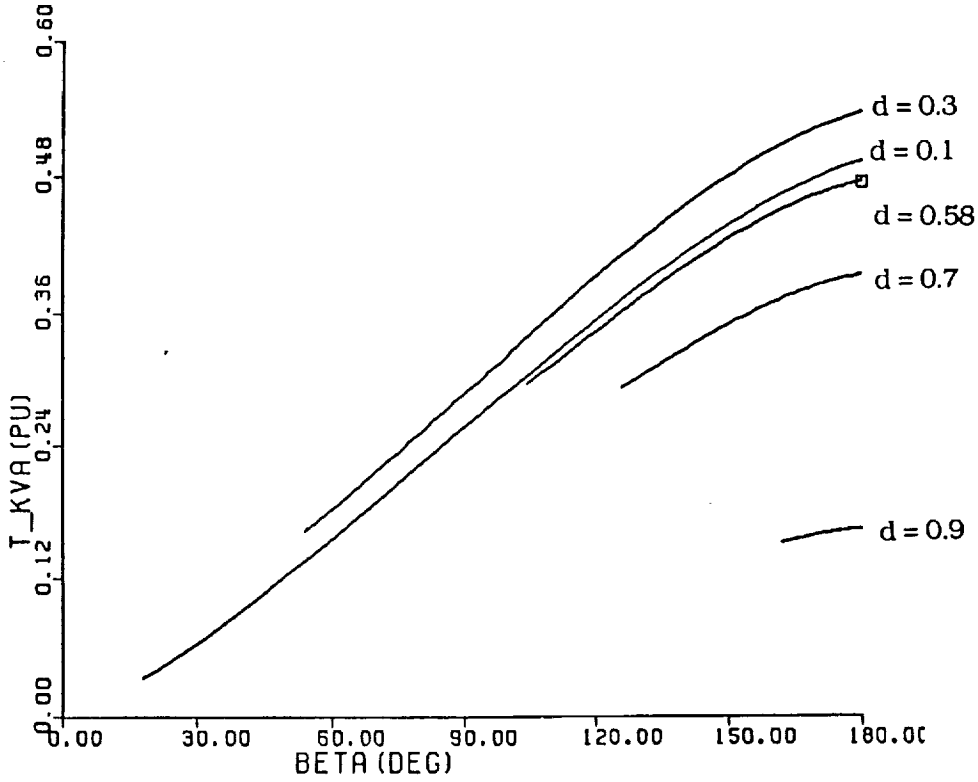


Figure 3.2.4a Transformer kVA vs Beta with d as a parameter, under soft switching operation(Topology A)

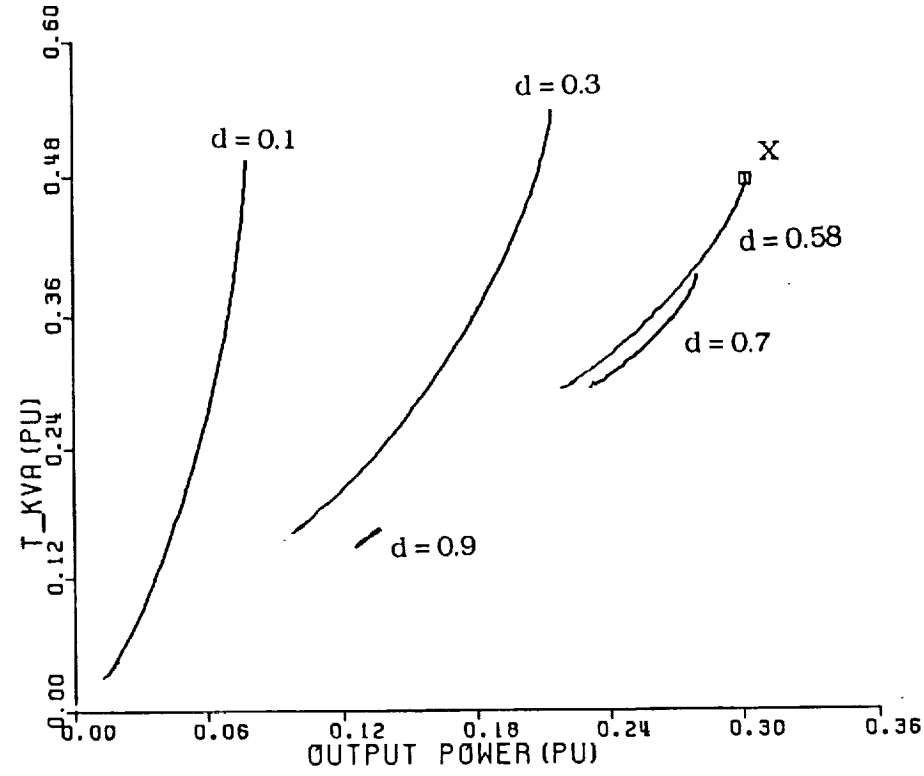


Figure 3.2.4b Transformer kVA vs Output Power with d as a parameter, under soft switching operation(Topology A)

Input Filter Capacitor kVA :

$$Ci\_kVA = V_i^* \, i_{Cirms} \qquad ...(3.2.15)$$

where,

$$i_{Cirms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_i^2 \, d\theta - i_{iav}^2}$$

Figures 3.2.5a and 3.2.5b show the variation of the input filter capacitor kVA with β and output power, respectively, with d as the parameter. Each curve extends over the soft-switching region only. For a given d, as β increases, the capacitor kVA increases. This is because the harmonic(ripple) content of the current into the input converter increases. Again, it is seen from Figure 3.2.5b that good controllability demands high kVA ratings on the input filter and, hence, bigger size. For maximum power transfer, only a certain minimum kVA is required which is a little more than half that required for full control. However, one loses on the range of control.

Output Filter Capacitor kVA :

$$Co\_kVA = V_o' \, * \, i_{Corms}' \qquad ...(3.2.16)$$

where,

$$i_{Corms}' = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_o'^2 \, d\theta - i_{oav}'^2}$$

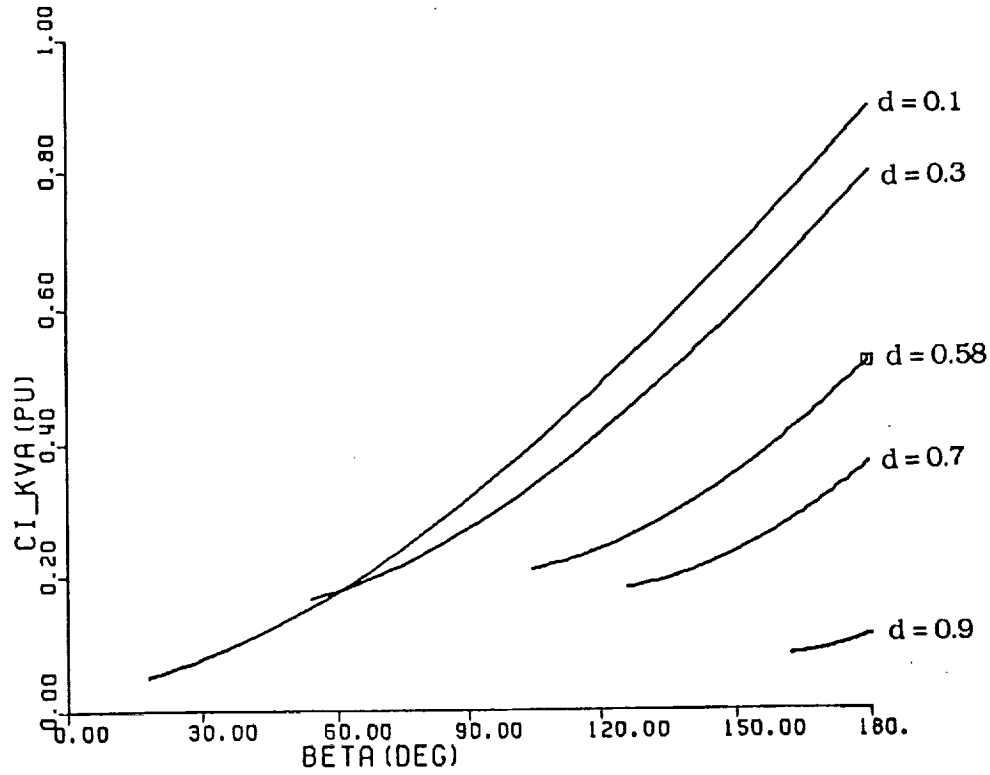


Figure 3.2.5a Input Filter Capacitor kVA vs Beta with d as a parameter, under soft switching operation(Topology A)

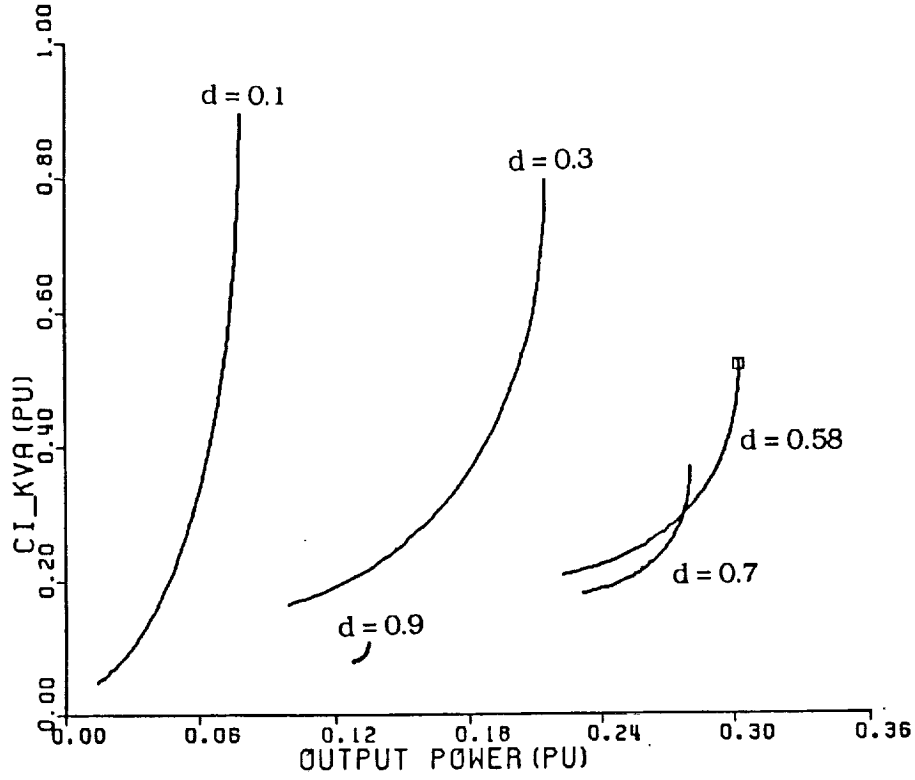


Figure 3.2.5b Input Filter Capacitor kVA vs Output Power with d as a parameter, under soft switching operation(Topology A)

Figures 3.2.6a and 3.2.6b show the variation of the output filter capacitor kVA with β and output power, respectively, with d as the parameter. Each curve extends over the soft-switching region only. The trend in the variation for a given d, as β increases, is similar to that of the input capacitor kVA. However, the worst case turns out to be for d = 0.58. Moreover, comparing the relative magnitudes of the kVAs required for the input and output capacitors, it is seen that, in general, over the entire operating region, the output capacitor kVA requirement is much lower. This is a consequence of the output bridge being a diode bridge, and hence restricting the output current to be unidirectional only. Selection of the output capacitor, based on the minimum kVA required for maximum power transfer suffices, since this also allows full control.

Figure 3.2.7 shows the entire region of soft-switching on a V_o' - i'_{oav} plane. For higher output voltages, the load range becomes smaller. A more detailed discussion on this plot will be presented in the subsequent chapter on the comparison of the proposed topologies.

Analysis of this topology has been carried out for operation under continuous conduction only. Under lightly loaded conditions, with the diode bridge at the output, the circuit can exhibit discontinuous conduction modes of operation. However, this would violate the minimum current constraint for the active devices in the input bridge, at turn-off. This in turn would lead to hard-switching of all the active devices. Discontinuous conduction will not be analyzed, but it is important to keep in mind the restriction this imposes on the minimum load for achieving soft-switching on all the active devices.

In practice, a major limitation on the operation of this converter is seen to arise from the reverse recovery effects of the output diodes. In brief, the phenomenon of diode reverse recovery is the removal of the stored charge on the junction capacitance during turn-off. The required peak reverse current is, thus, a function of the rate of fall of forward current through the diode(which is governed by the circuit

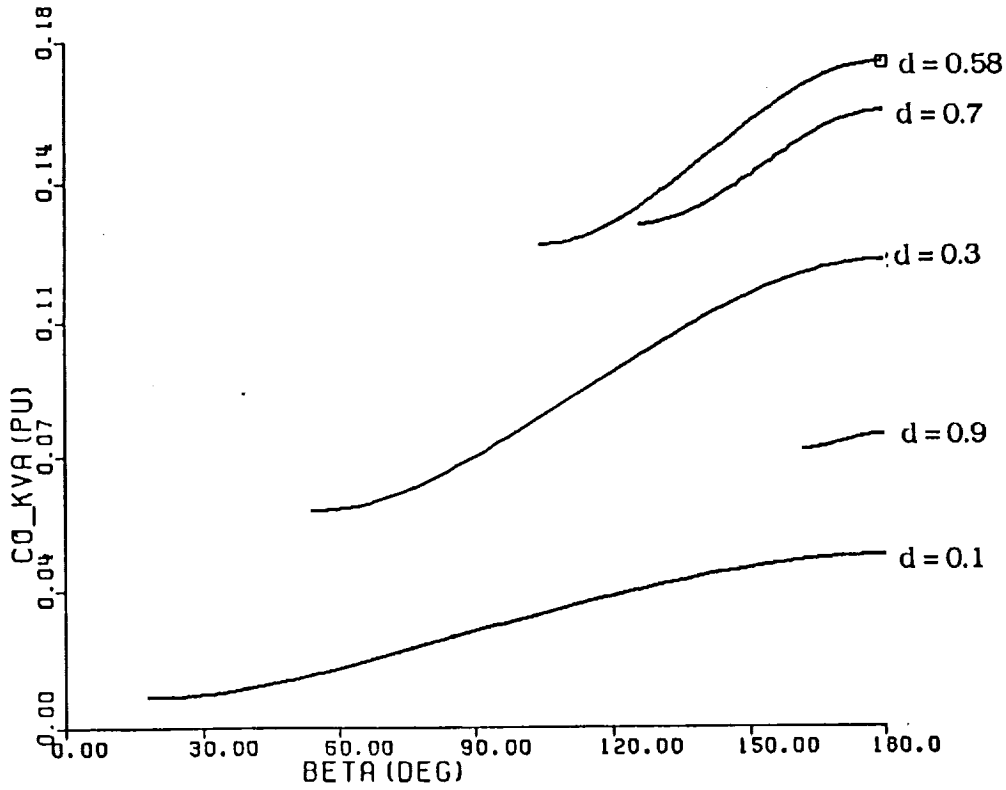


Figure 3.2.6a Output Filter Capacitor kVA vs Beta with d as a parameter, under soft switching operation(Topology A)

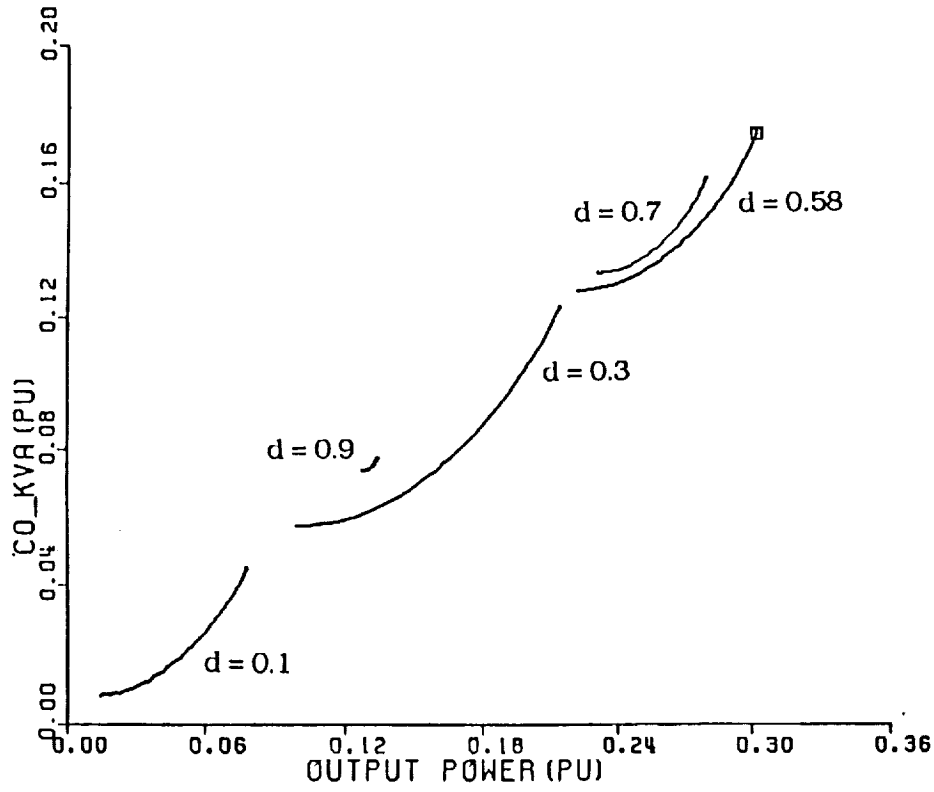


Figure 3.2.6b Output Filter Capacitor kVA vs Output Power with d as a parameter, under soft switching operation(Topology A)

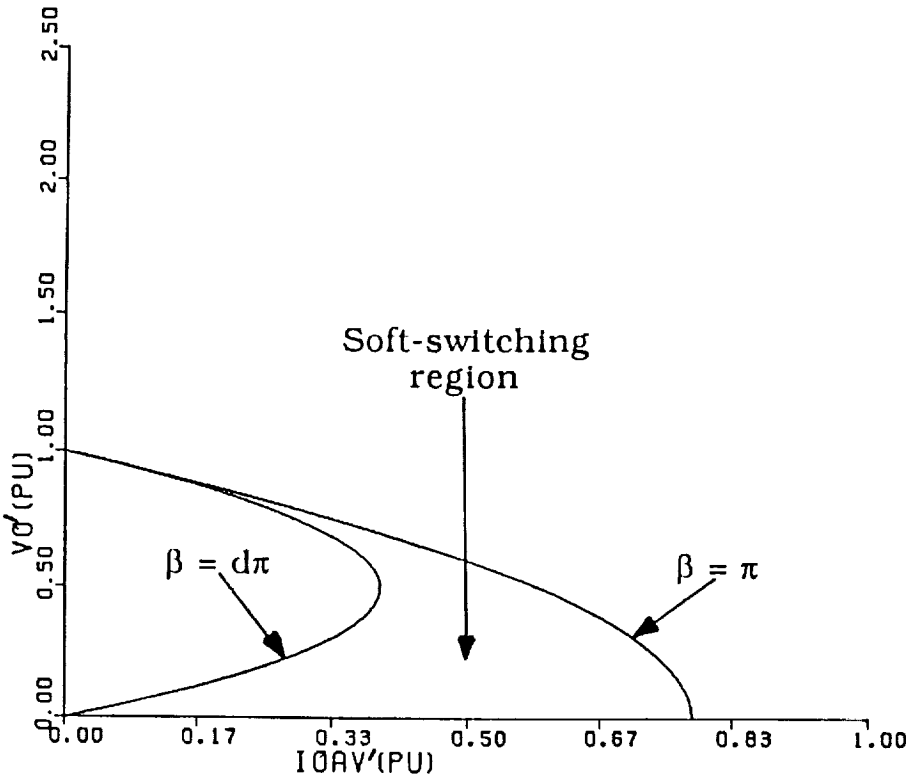


Figure 3.2.7 Output Voltage vs Output Current, showing soft switching Boundaries and Region(Topology A)

inductance and switching frequency). Given the need for high switching frequency(for high power density) and reasonably low leakage inductance, one could expect very high peak reverse currents. Now, a fast recovery diode, would lead to very high voltage stresses on the circuit elements owing to the fact that a large current(reverse diode current) flowing through the leakage inductance is 'snapped off'. On the other hand, a slow recovery diode would impose an upper limit on the switching frequency. These considerations force a designer to make certain trade-offs, which at times inhibits one from exploiting the full capabilities of a circuit.

However, as reported recently in Reference [13], the diode recovery process is conceptually akin to the existence of an active device in anti-parallel to the diode. Recalling our soft-switching constraint that the active device must take over conduction from its anti-parallel diode, it follows that if the output diodes are now replaced by switching devices(active device with anti-parallel diode) then the output bridge also naturally(and most importantly benignly) handles the diode reverse recovery process. The circuit can now be operated with a simpler control strategy in which the input and output bridges generate square waves phase-shifted from each other. Also, all the active devices of both the bridges can operate under soft-switching conditions. Two quadrant operation is also realizable. The following section analyzes this new topology.

3.3 Single-Phase Dual Active Bridges DC/DC Converter(Topology B)

Figure 3.3.1(a) shows the circuit schematic of Topology B. It is similar to Topology A except, the output diode bridge has been replaced by an active bridge, and hence the name. The leakage inductance of the transformer is, again, used as the main energy transfer element from the input to the output. The primary-referred equivalent circuit is shown in Figure 3.3.1(b). L is the total leakage inductance referred to the primary side.

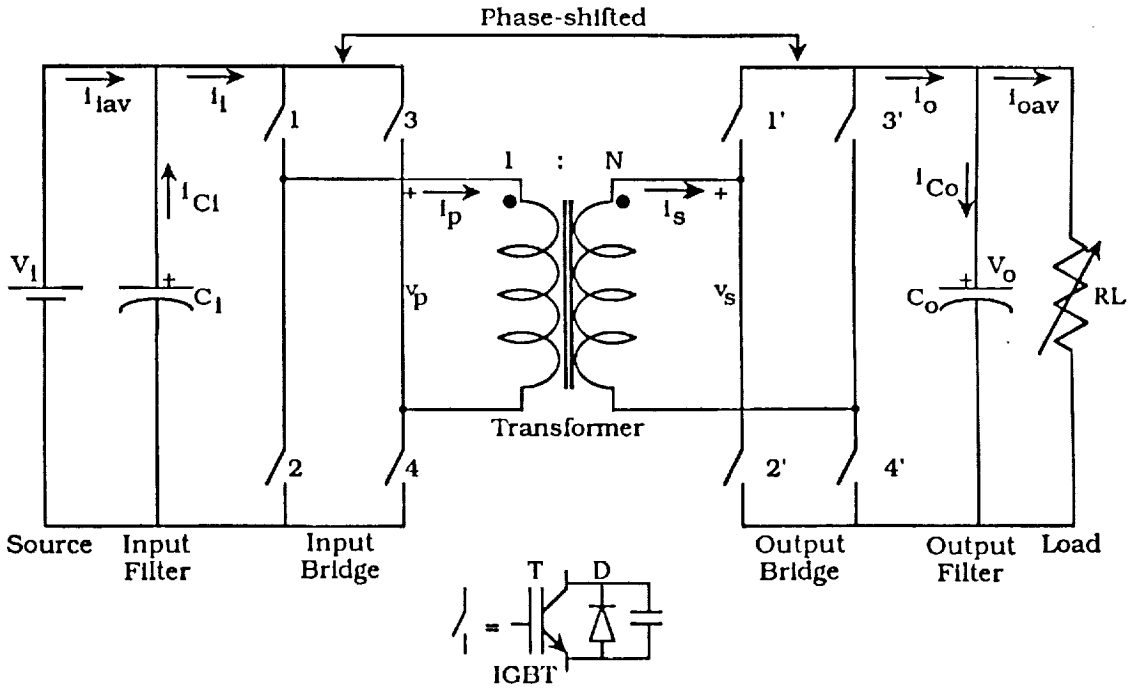


Figure 3.3.1a Schematic of Single Phase Dual Active Bridges DC/DC Converter(Topology B)

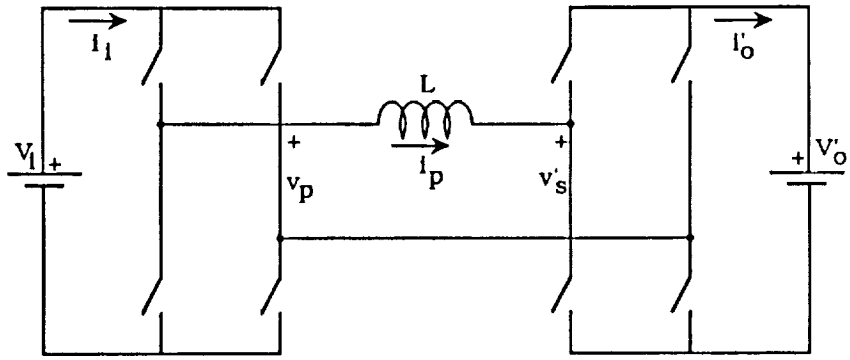


Figure 3.3.1b Primary-Referred Equivalent Circuit of Topology B

The output dc voltage, and hence the output power, can now be controlled by controlling the phase shift, ϕ, between the two active bridges. Both the bridges operate as simple square wave inverters, as viewed from their dc sides, switching at a constant frequency. However, by phase-shifting the square waves the effective voltage across the leakage inductance and hence the current can be controlled. Figure 3.3.2 shows the operating waveforms for a dc conversion ratio less than unity($V_i > V_o'$).

Two modes of operation can be identified. In each mode, the inductor current, i_p as a function of $\theta = \omega t$, where ω is the switching frequency, is given by,

$$i_p(\theta) = \frac{\left[v_p(\theta) - v_s'(\theta)\right]}{\omega L}(\theta - \theta_i) + i_p(\theta_i) \qquad \theta_i \le \theta < \theta_f$$

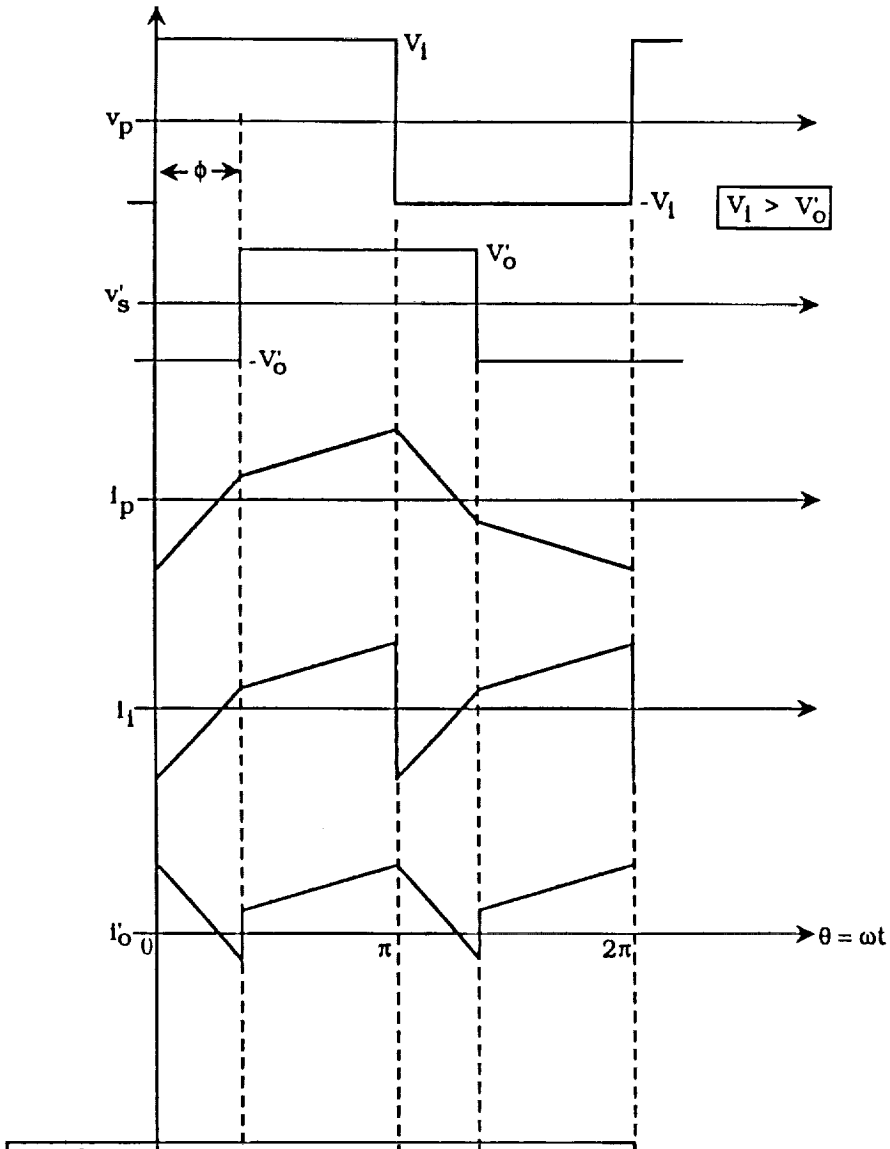
...(3.3.1)

where, θ_i and θ_f are the start and end of each mode respectively, and $i_p(\theta_i)$ is the initial current of each mode. Therefore, from Figure 3.3.2 and Equation(3.3.1),

Mode 1 : $0 \le \theta < \phi$

$$v_p(\theta) = V_i \quad ; \quad v_s'(\theta) = -V_o'$$

$$i_p(\theta) = \frac{V_i + V_o'}{\omega L}(\theta) + i_p(0) \qquad \text{...(3.3.2)}$$



Mode no.	1	2	1	2
Input Bridge	D1 to T1 D4 to T4	T1 T4	D2 to T2 D3 to T3	T2 T3
Output Bridge	D2' to T2' D3' to T3'	D1' D4'	D1' to T1' D4' to T4'	D2' D3'

Figure 3.3.2 Idealized Operating Waveforms for Topology B

Mode 2 : $\phi \le \theta < \pi$

$$v_p(\theta) = V_i \quad ; \quad v_s'(\theta) = V_o'$$

$$i_p(\theta) = \frac{V_i - V_o'}{\omega L}(\theta - \phi) + i_p(\phi) \qquad ...(3.3.3)$$

At the end of the half cycle, from symmetry conditions,

$$i_p(\pi) = -i_p(0) \qquad ...(3.3.4)$$

Hence, solving for $i_p(0)$, the complete current waveform can be obtained. From Equations(3.3.2) - (3.3.4),

$$i_p(0) = \frac{-V_i}{\omega L}\left[d\phi + \frac{\pi(1 - d)}{2}\right] \qquad ...(3.3.5)$$

Also,

$$i_p(\phi) = \frac{-V_i}{\omega L}\left[-\phi + \frac{\pi(1 - d)}{2}\right] \qquad ...(3.3.6)$$

where, $d = \frac{V_o'}{V_i}$

From the soft-switching constraints we get,

For Input Bridge $\quad i_p(0) \le 0$

therefore, substituting in Equation(3.3.5),

$$d \leq \frac{1}{1 - \frac{2\phi}{\pi}} \qquad 0 \leq \phi < \frac{\pi}{2} \qquad \ldots(3.3.7)$$

For Output Bridge $\quad i_p(\phi) \geq 0$

therefore, substituting in Equation(3.3.6),

$$d \geq \frac{\pi - 2\phi}{\pi} \qquad 0 \leq \phi < \frac{\pi}{2} \qquad \ldots(3.3.8)$$

Also, the anti-parallel diodes demand

$$d \geq 0 \qquad \ldots(3.3.9)$$

Note, constraints (3.3.7) and (3.3.8) must be used in conjunction with constraint (3.3.9).

Violating the input bridge constraint results in natural commutation of all its active devices. In other words, the device turns off when the current through it naturally reverses. This is undesirable, since the incoming active device turns on discharging its snubber capacitor and thus resulting in substantial turn-on losses. This is commonly referred to as a 'snubber dump'. Similarly, exceeding the output bridge constraint leads to natural commutation of all its active devices. The boundary represents diode bridge operation and is identical to that for Topology A, when $\beta = \pi$. The output bridge constraint will be referred to as the diode bridge constraint. The two boundaries enclose the region of soft-switching. Moreover, from Equation (3.3.7), d can be greater than unity, that is, this topology can also operate as a boost converter.

Theoretically, from Equation (3.3.7) at $\phi = \pi / 2$, d can tend to infinity. However, in practice this would lead to an unstable condition and is not realizable given real devices with finite voltage limitations. For $\phi > \pi / 2$, constraint equations (3.3.7) and (3.3.8) imply that d can

be less than zero. However, in the light of the overriding constraint (3.3.9), this is not possible. This in turn implies that the converter exhibits soft-switching for $0 \leq \phi < \pi / 2$.

Given the symmetry of the circuit, a similar analysis for $0 \geq \phi > -\pi/2$ was carried out. The square wave generated by the output bridge now leads that of the input bridge. It is seen that the directions of input and output average currents are reversed, and hence, power flow is reversed. More importantly, this reversal of power flow is also possible within soft-switching boundaries identical to those for the range $0 \leq \phi < \pi / 2$.

With a knowledge of the primary current, $i_p(\theta)$, and the converter switching functions the various quantities of interest defined in the previous section are once again calculated, and are given below.

Output Power :

$$P_o = V_i i_{iav} = V_o' i_{oav}'$$

$$= \left[\frac{V_i^2}{\omega L}\right] d\,\phi \left[1 - \frac{\phi}{\pi}\right] \qquad \ldots(3.3.10)$$

For any d, maximum power transfer is achievable at $\phi = \pi / 2$.

Transformer kVA :

$$T\_kVA = \frac{v_{prms} * i_{prms} + v_{srms}' * i_{srms}'}{2}$$

However, since magnetizing current is assumed zero,

$$i_{prms} = i'_{srms}$$

Therefore,

$$T\_kVA = \frac{(v_{prms} + v'_{srms}) * i_{prms}}{2} \qquad ...(3.3.11)$$

where,

$$v_{prms} = V_i$$

$$v'_{srms} = V'_o = d\,V_i$$

$$i_{prms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_p^2\, d\theta}$$

All other quantities are calculated as defined in the previous section. The steady state operating characteristics of each quantity of interest, normalized to the same base as defined in the last section, are plotted as a function of the control variable, ϕ, with d as a parameter. The boundaries of soft-switching are also shown on these characteristics.

Two sets of output power characteristics versus ϕ, calculated from Equation (3.3.10), are shown in Figure 3.3.3. In Figure 3.3.3a the parameter d sweeps from 0.2 to 1, with the control variable, ϕ, sweeping over the complete possible range of -90° to +90°. The direction of power flow is determined by the direction of ϕ. The soft-switching region for each value of d is identical in each quadrant. The d = 1 curve gives full control, under soft-switching. Figure 3.3.3b shows the output power characteristics for d > 1 also. The soft-switching region is now enclosed within the two boundaries given by Equations(3.3.7) and (3.3.8). For values of d > 1 or < 1, the range of ϕ

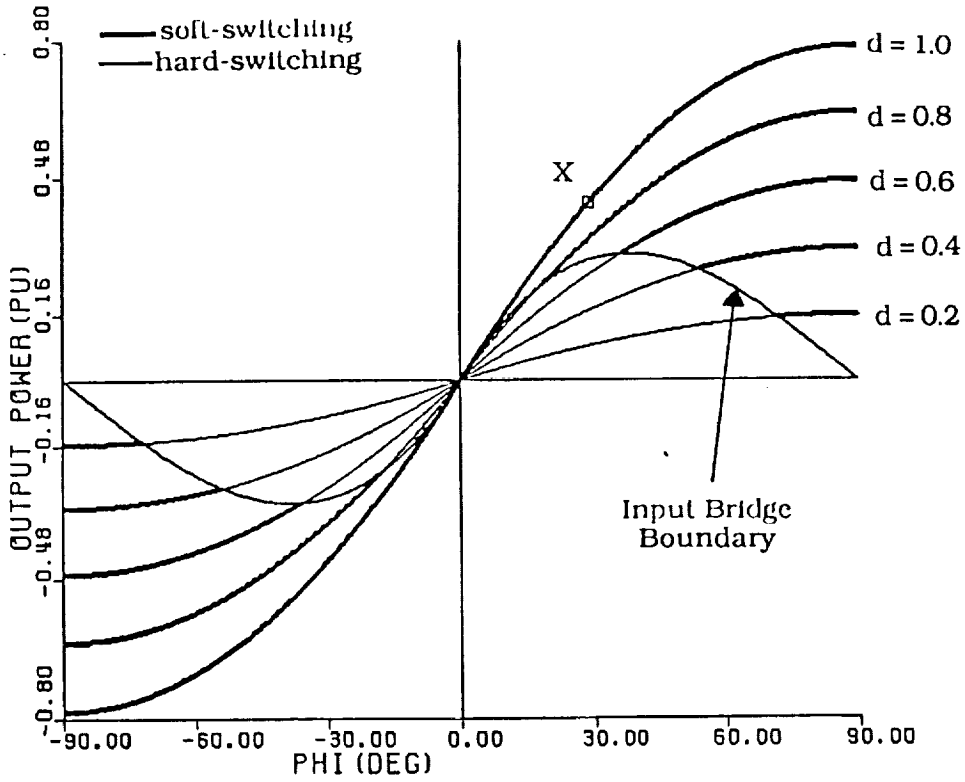


Figure 3.3.3a Output Power vs Phi with d as a parameter, showing two quadrant operation(Topology B)

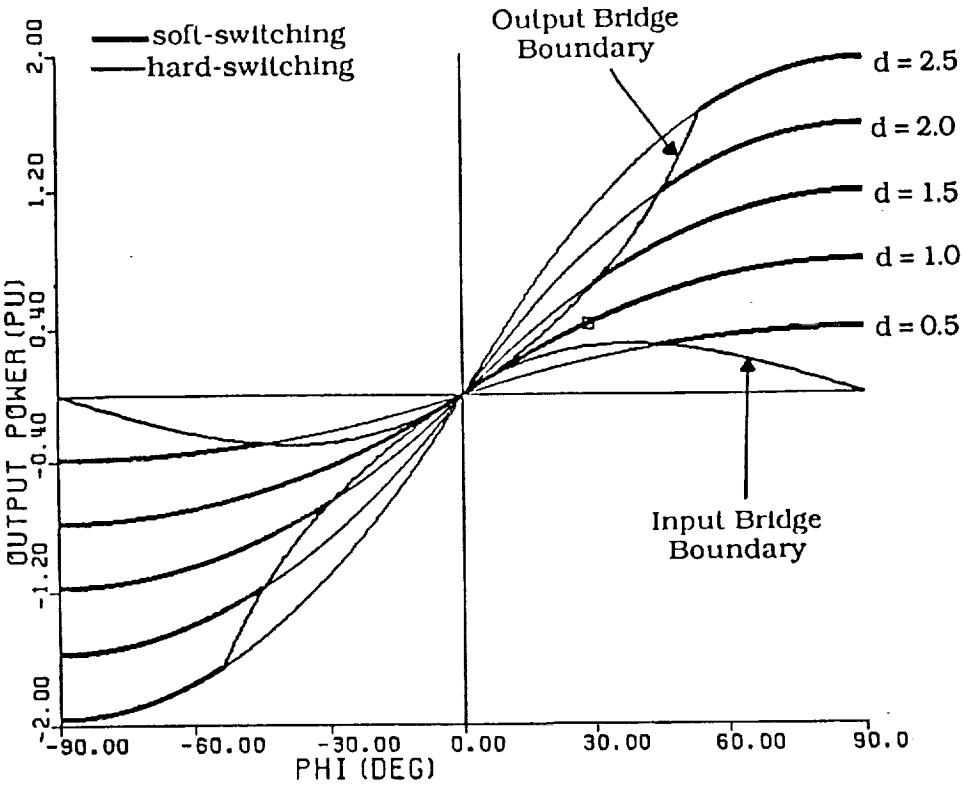


Figure 3.3.3b Output Power vs Phi with d as a parameter, showing two quadrant and buck-boost operation(Topology B)

for soft-switching is reduced. For any d maximum power transfer occurs at $\phi = \pi / 2$.

Figure 3.3.4a shows the dependence of the transformer kVA on ϕ and Figure 3.3.4b shows its dependence on the output power. In each case a family of curves is plotted with d as the parameter. Again, the soft-switching regions are shown. Various design points can be selected based on issues of maximum power transfer capability or range of controllability under soft-switching. Figure 3.3.4b shows the output bridge constraint(also, referred to as the diode bridge constraint). An interesting feature of Topology B can be brought to light, by examining the minimum transformer kVA(0.475pu) required for transferring the maximum output power(0.302pu) on the diode bridge constraint(which corresponds to the $\beta = \pi$ boundary for Topology A). For the same kVA the output power can be increased to 0.422pu at d = 1(see point labelled X), with Topology B. This gives us a transformer utilization of 0.888, an improvement of 40%. However, this restricts the range of control upto a point where the transformer kVA cannot exceed the above value. On the other hand, for full range of control over ϕ at d = 1, the transformer would have to be designed for the maximum kVA of approximately 1.3pu, resulting in a transformer utilization of 0.604. Thus, it is seen again that a trade-off between size(and, hence, power density) and controllability must be made.

One might wonder, and justifiably so, at this 40% improvement in the transformer utilization with Topology B. A possible explanation is that with the diode bridge at the output the transformer always sees a resistive load. Hence, maximum power transfer is governed by a passive impedance divider consisting of the leakage impedance and the resistive load. The output filter capacitor simply serves as a harmonic compensator. On the other hand, with an active output bridge the output capacitor can now also function as a reactive compensator, providing some of the reactive excitation necessary for the transformer. This allows more of the primary kVA of the transformer to appear as real output power.

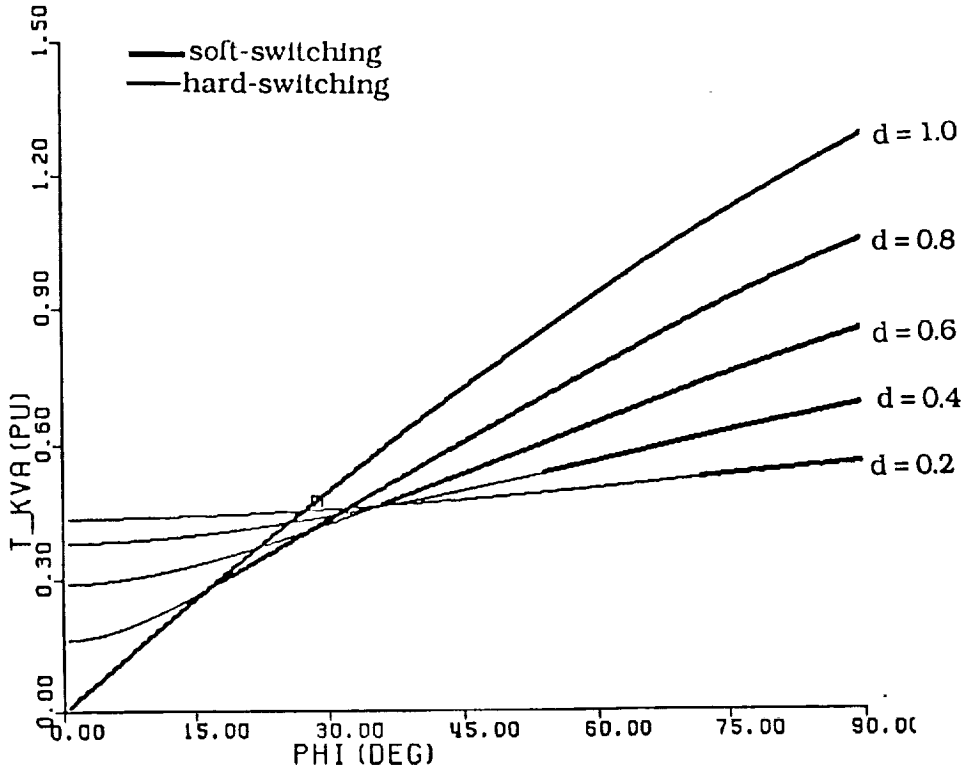


Figure 3.3.4a Transformer kVA vs Phi with d as a parameter (Topology B)

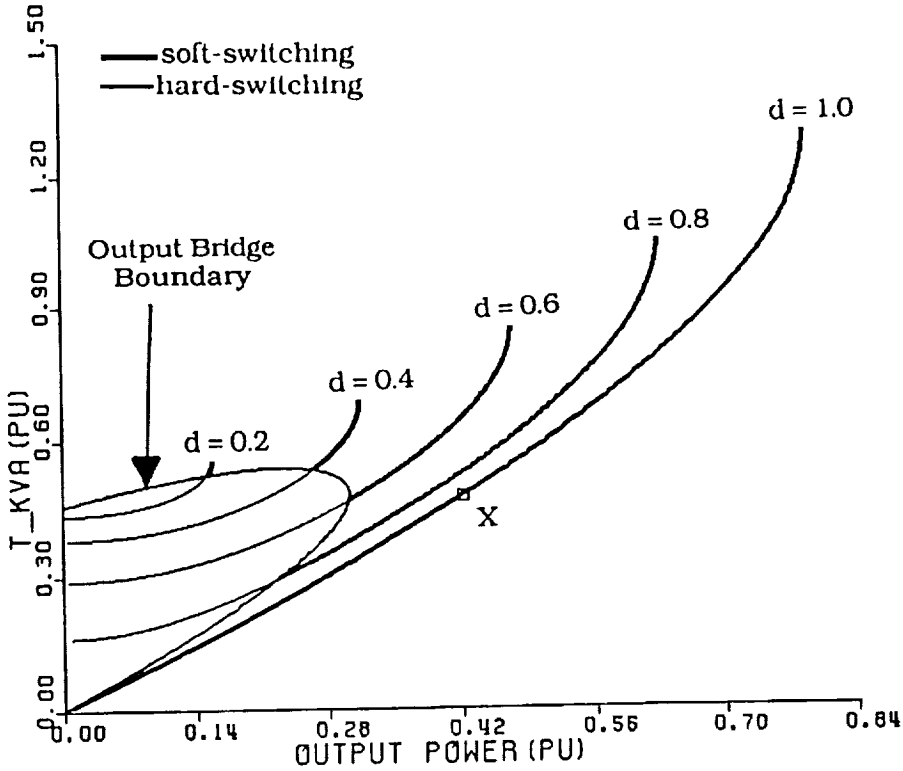


Figure 3.3.4b Transformer kVA vs Output Power with d as a parameter(Topology B)

Figures 3.3.5a and 3.3.5b show the variation of the input capacitor kVA with ϕ and output power, respectively, for various values of the parameter, d. For a wide range of ϕ the input capacitor kVA is seen to be a minimum at d = 1. Again, various design trade-offs can be made depending upon good range of controllability and high power density.

Figures 3.3.6a and 3.3.6b show the dependence of the output filter capacitor on ϕ and output power, respectively, with d as the parameter. Contrary to the input filter capacitor, for a considerable range of ϕ, the output filter capacitor kVA is highest at d = 1.

Figure 3.3.7 shows the entire region of soft-switching on a V_o' - i'_{oav} plane. At d=1(V_o' = 1pu), theoretically any load from no-load to the maximum limited by the vertical line(corresponding to $\phi = \pi/2$) can be realized. The range of load decreases on either side of d = 1.

Further comments on the merits and demerits of this topology are reserved till Chapter 4, where a detailed comparison of all the three proposed topologies is carried out.

For the sake of completeness, it is worth mentioning here that various other control strategies can be devised for Topology B. For instance, the phase-shifting operation can be performed on the two legs of the input bridge(as in Topology A) and the output bridge can then be phase staggered from the input bridge in the usual manner. Or, the phase-shifting operation can be performed on both the bridges independently, and yet have them phase-staggered from each other by a controlled angle. It can be seen that each of these control schemes have more than one degree of freedom, and hence can make the analysis relatively more complex. Moreover, they would probably lead access to different regions of operation, under soft switching, on the V_o' - i'_{oav} plane.

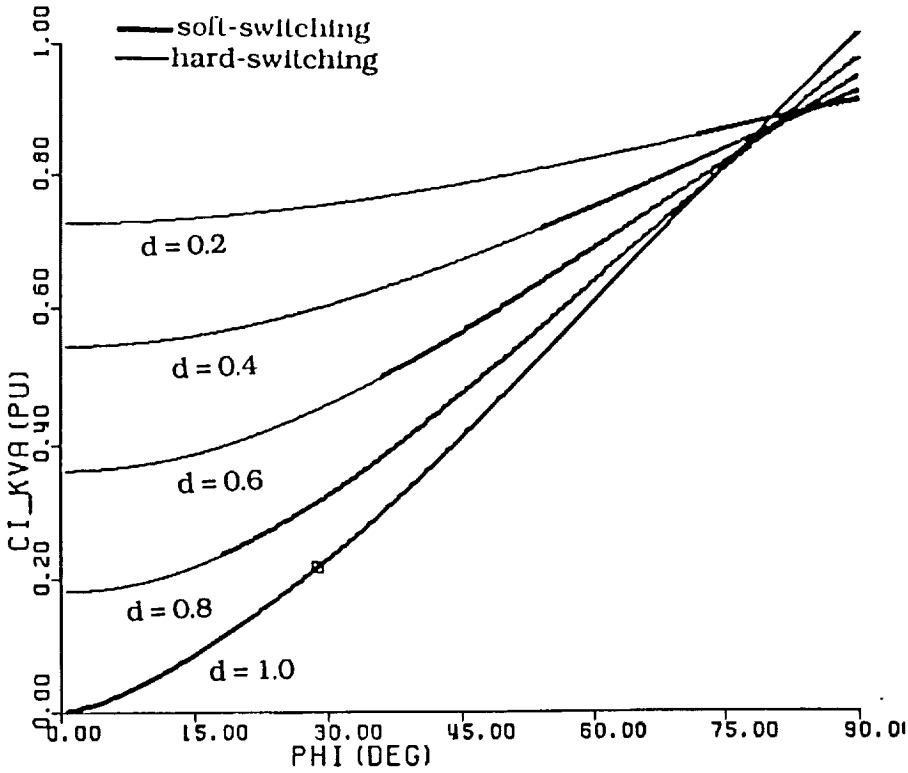


Figure 3.3.5a Input Filter Capacitor kVA vs Phi with d as a parameter (Topology B)

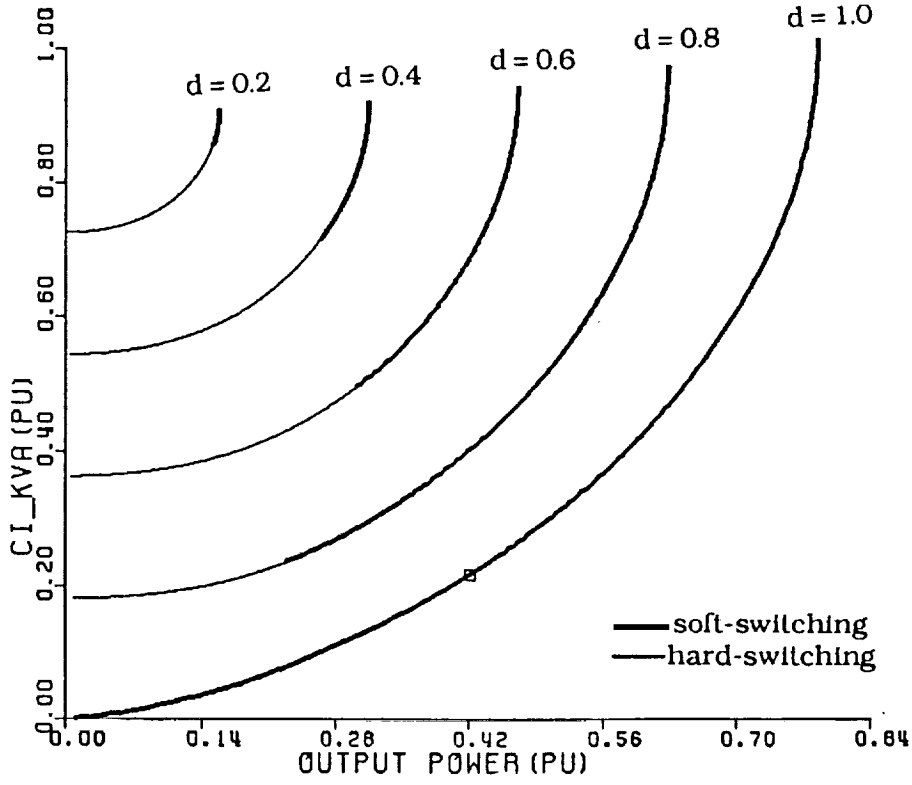


Figure 3.3.5b Input Filter Capacitor kVA vs Output Power with d as a parameter(Topology B)

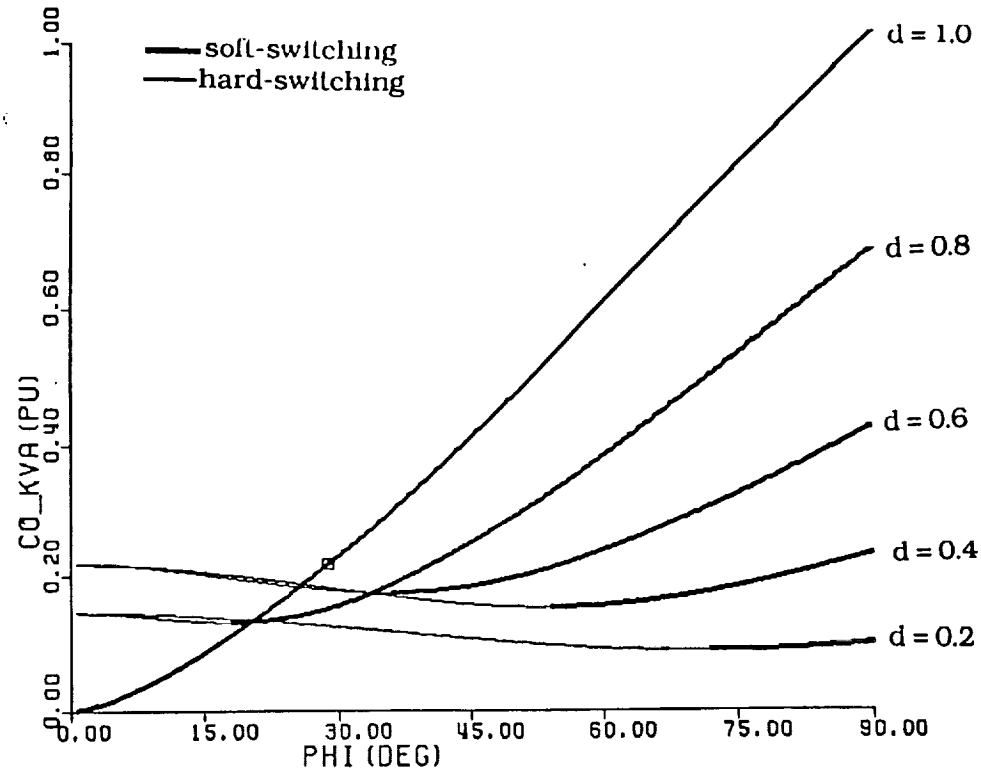


Figure 3.3.6a Output Filter Capacitor kVA vs Phi with d as a parameter(Topology B)

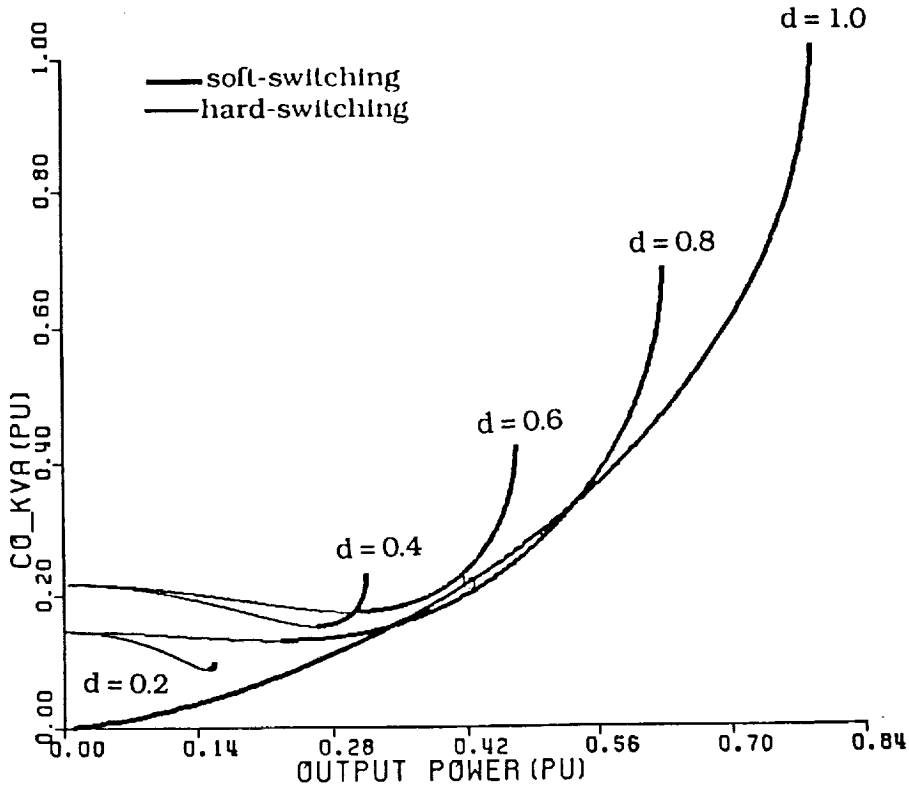


Figure 3.3.6b Output Filter Capacitor kVA vs Output Power with d as a parameter(Topology B)

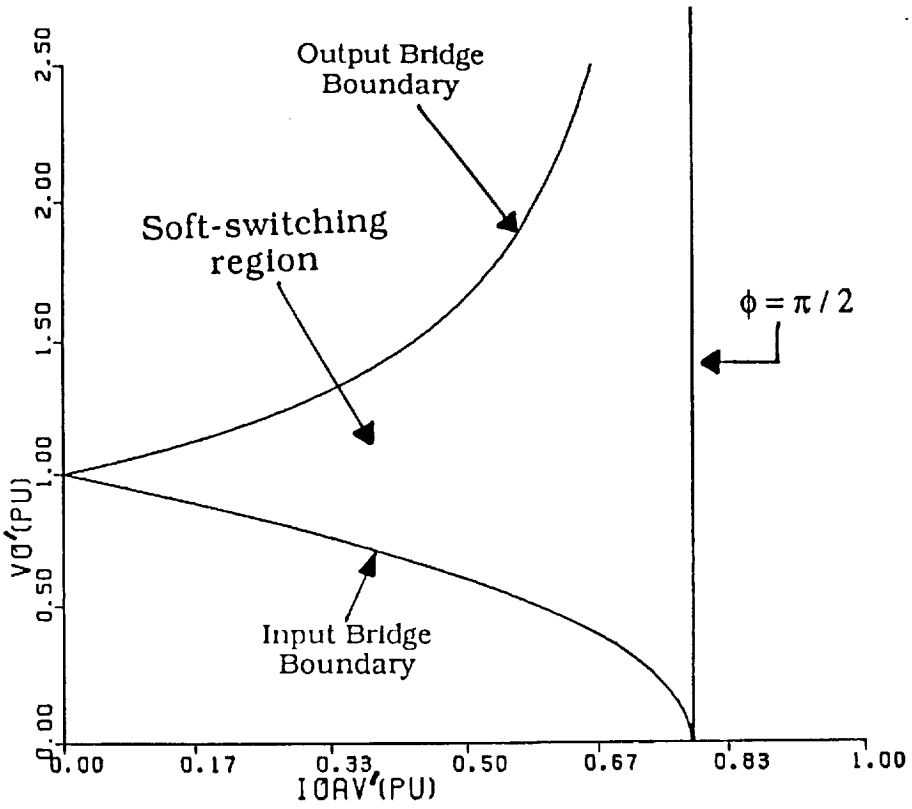


Figure 3.3.7 Output Voltage vs Output Current, showing soft switching Boundaries and Region(Topology B)

To reduce the harmonic content of the input and output bridge currents, and hence the filter sizes this topology can be extended to a 3-phase version, with the possible concomitant benefit of reduced VA stresses on the switching devices. The following section investigates this new extension of Topology B.

3.4 Three-Phase Dual Active Bridges DC/DC Converter(Topology C)

Figure 3.4.1(a) shows the circuit schematic of Topology C. It is simply a three-phase extension of Topology B. The two three-phase active bridges operate in a six-step mode at a fixed frequency. The controlled phase-shift, ϕ, between the bridges governs the amount of power flow. The high frequency ac link transformer is Y-Y connected and is three-phase symmetric with the leakage inductances used as the main energy transfer elements. The primary-referred equivalent circuit is shown in Figure 3.4.1(b). L is the total leakage inductance per phase referred to the primary side. Two distinct regions of operation, over the range of the control parameter, ϕ, are identified.

i) Region I : $0 \leq \phi < \frac{\pi}{3}$

ii) Region II : $\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$

Further, in each region <u>six</u> modes of operation exist. Figure 3.4.2 shows typical operating waveforms for Region I. In each mode, the inductor current of Phase-a, i_{ap} as a function of $\theta = \omega t$, where ω is the switching frequency, is given by,

$$i_{ap}(\theta) = \frac{\left[v_{ap}(\theta) - v_{as}'(\theta)\right]}{\omega L}(\theta - \theta_i) + i_{ap}(\theta_i) \qquad \theta_i \leq \theta < \theta_f$$

...(3.4.1)

where, θ_i and θ_f are the start and end of each mode respectively, v_{ap} is the Phase-a primary to neutral voltage, v_{as}' is the Phase-a secondary voltage referred to the primary side and $i_{ap}(\theta_i)$ is the initial current of each mode.

Region I (Figure 3.4.2) :

Mode 1 : $0 \leq \theta < \phi$

$$v_{ap}(\theta) = \frac{V_i}{3} \; ; \; v_{as}'(\theta) = -\frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i + V_o'}{3\omega L}(\theta) + i_{ap}(0) \qquad \ldots(3.4.2a)$$

Mode 2 : $\phi \leq \theta < \frac{\pi}{3}$

$$v_{ap}(\theta) = \frac{V_i}{3} \; ; \; v_{as}'(\theta) = \frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}(\theta - \phi) + i_{ap}(\phi) \qquad \ldots(3.4.3a)$$

Mode 3 : $\frac{\pi}{3} \leq \theta < (\phi + \frac{\pi}{3})$

$$v_{ap}(\theta) = \frac{2V_i}{3} \; ; \; v_{as}'(\theta) = \frac{V_o'}{3}$$

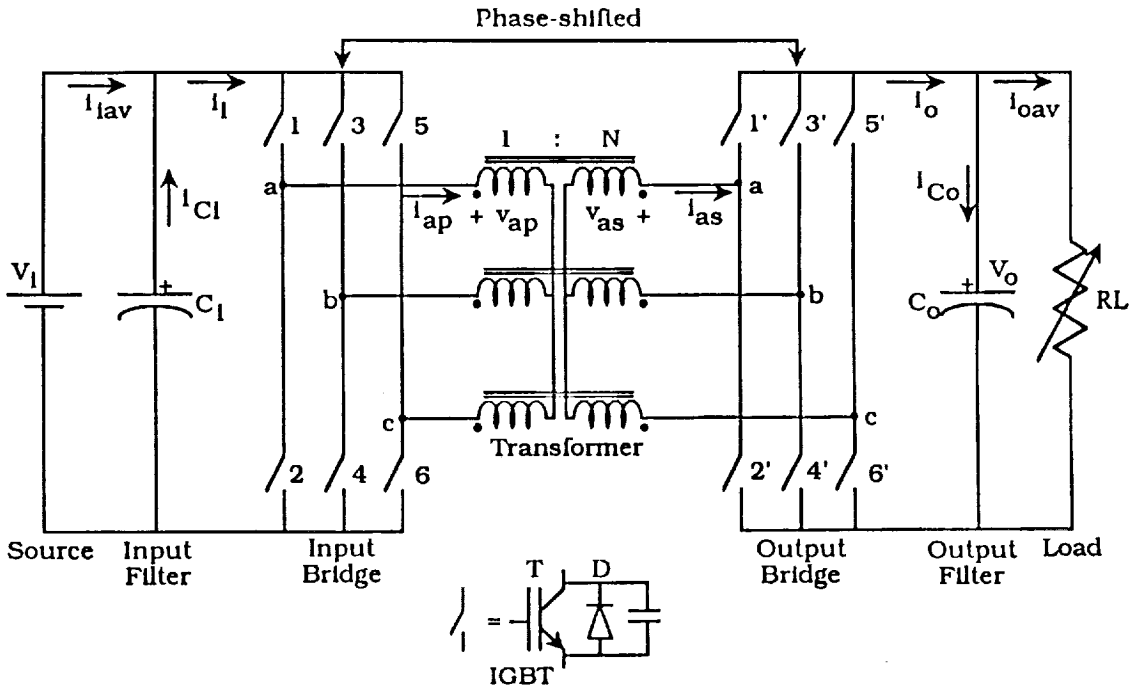


Figure 3.4.1a Schematic of Three Phase Dual Active Bridges DC/DC Converter(Topology C)

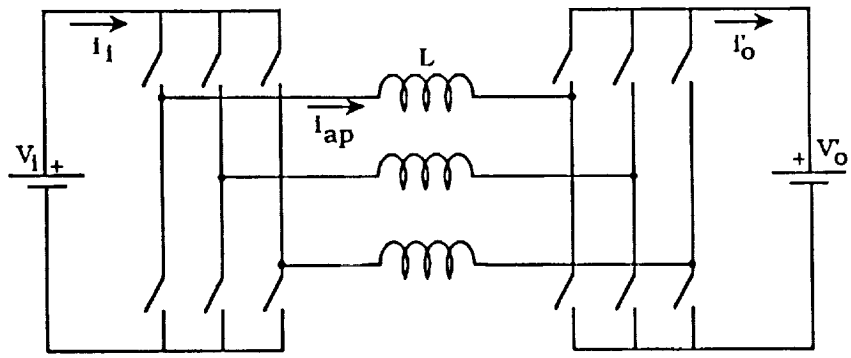


Figure 3.4.1b Primary-Referred Equivalent Circuit of Topology C

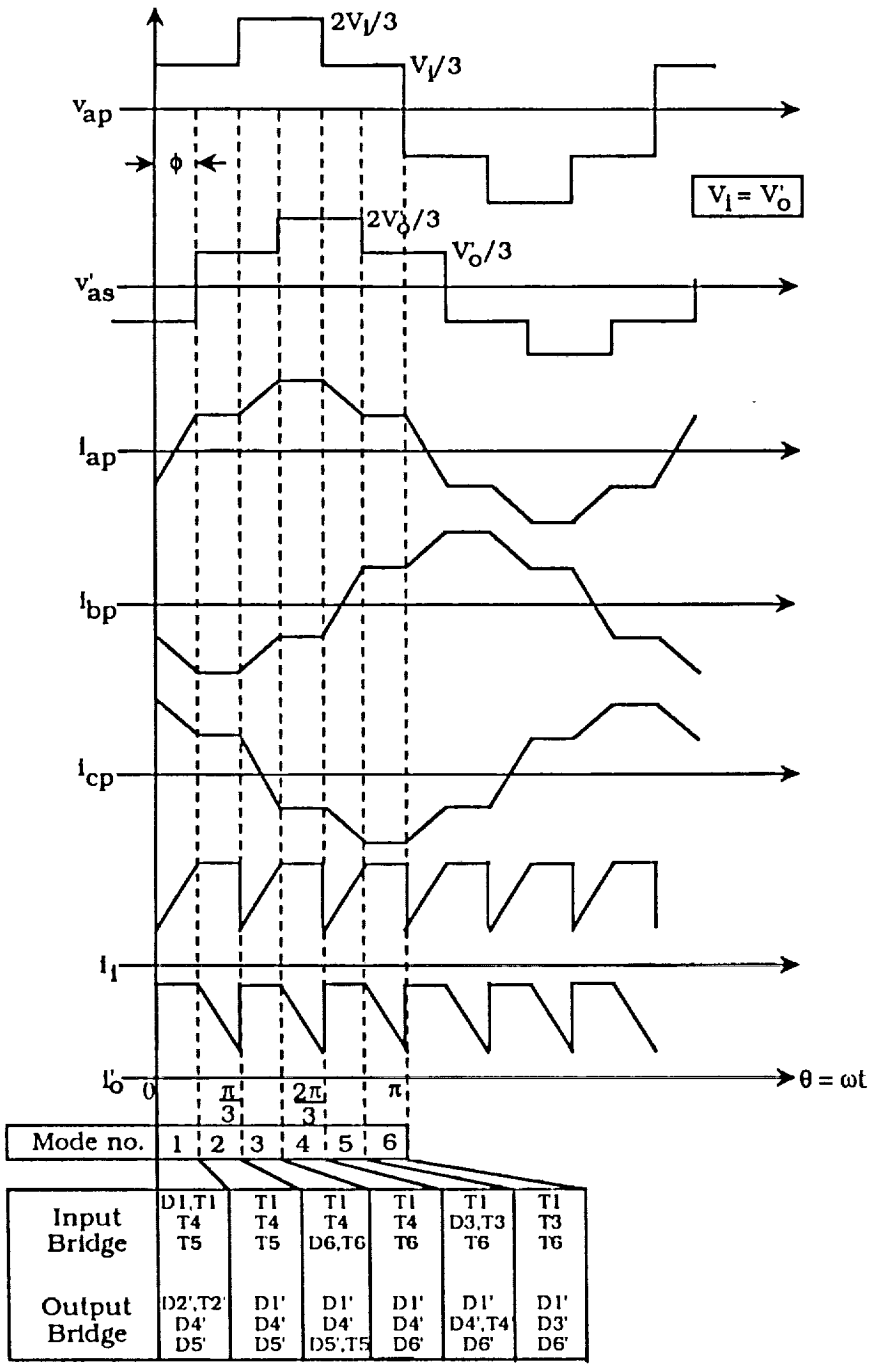


Figure 3.4.2 Idealized Operating Waveforms for Topology C

$$i_{ap}(\theta) = \frac{2V_i - V_o'}{3\omega L}\left(\theta - \frac{\pi}{3}\right) + i_{ap}\left(\frac{\pi}{3}\right) \qquad \ldots(3.4.4a)$$

Mode 4 : $\left(\phi + \frac{\pi}{3}\right) \le \theta < \frac{2\pi}{3}$

$$v_{ap}(\theta) = \frac{2V_i}{3} \; ; \; v_{as}'(\theta) = \frac{2V_o'}{3}$$

$$i_{ap}(\theta) = \frac{2(V_i - V_o')}{3\omega L}\left(\theta - \phi - \frac{\pi}{3}\right) + i_{ap}\left(\phi + \frac{\pi}{3}\right) \qquad \ldots(3.4.5a)$$

Mode 5 : $\frac{2\pi}{3} \le \theta < \left(\phi + \frac{2\pi}{3}\right)$

$$v_{ap}(\theta) = \frac{V_i}{3} \; ; \; v_{as}'(\theta) = \frac{2V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i - 2V_o'}{3\omega L}\left(\theta - \frac{2\pi}{3}\right) + i_{ap}\left(\frac{2\pi}{3}\right) \qquad \ldots(3.4.6a)$$

Mode 6 : $\left(\phi + \frac{2\pi}{3}\right) \le \theta < \pi$

$$v_{ap}(\theta) = \frac{V_i}{3} \; ; \; v_{as}'(\theta) = \frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}(\theta - \phi - \frac{2\pi}{3}) + i_{ap}(\phi + \frac{2\pi}{3}) \qquad ...(3.4.7a)$$

Again, from half-cycle symmetry conditions, and using Equations(3.4.2a) - (3.4.7a), $i_{ap}(0)$ and hence the complete current waveform can be obtained. Therefore,

$$i_{ap}(0) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} - d\phi - \frac{2\pi}{3}\right] \qquad ...(3.4.8a)$$

Also,

$$i_{ap}(\phi) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} + \phi - \frac{2\pi}{3}\right] \qquad ...(3.4.9a)$$

where, $d = \frac{V_o'}{V_i}$

Region II :

Mode 1 : $0 \leq \theta < (\phi - \frac{\pi}{3})$

$$v_{ap}(\theta) = \frac{V_i}{3} \; ; \; v_{as}'(\theta) = -\frac{2V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i + 2V_o'}{3\omega L}(\theta) + i_{ap}(0) \qquad ...(3.4.2b)$$

Mode 2 : $(\phi - \frac{\pi}{3}) \leq \theta < \frac{\pi}{3}$

$$v_{ap}(\theta) = \frac{V_i}{3} \quad ; \quad v'_{as}(\theta) = -\frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{V_i + V_o'}{3\omega L}(\theta - \phi + \frac{\pi}{3}) + i_{ap}(\phi - \frac{\pi}{3}) \qquad ...(3.4.3b)$$

Mode 3 : $\frac{\pi}{3} \leq \theta < \phi$

$$v_{ap}(\theta) = \frac{2V_i}{3} \quad ; \quad v'_{as}(\theta) = -\frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{2V_i + V_o'}{3\omega L}(\theta - \frac{\pi}{3}) + i_{ap}(\frac{\pi}{3}) \qquad ...(3.4.4b)$$

Mode 4 : $\phi \leq \theta < \frac{2\pi}{3}$

$$v_{ap}(\theta) = \frac{2V_i}{3} \quad ; \quad v'_{as}(\theta) = \frac{V_o'}{3}$$

$$i_{ap}(\theta) = \frac{2V_i - V_o'}{3\omega L}(\theta - \phi) + i_{ap}(\phi) \qquad ...(3.4.5b)$$

Mode 5 : $\frac{2\pi}{3} \leq \theta < (\phi + \frac{\pi}{3})$

$$v_{ap}(\theta) = \frac{V_i}{3} \quad ; \quad v'_{as}(\theta) = \frac{V'_o}{3}$$

$$i_{ap}(\theta) = \frac{V_i - V_o'}{3\omega L}(\theta - \frac{2\pi}{3}) + i_{ap}(\frac{2\pi}{3}) \qquad ...(3.4.6b)$$

Mode 6 : $(\phi + \frac{\pi}{3}) \leq \theta < \pi$

$$v_{ap}(\theta) = \frac{V_i}{3} \quad ; \quad v'_{as}(\theta) = \frac{2V'_o}{3}$$

$$i_{ap}(\theta) = \frac{V_i - 2V_o'}{3\omega L}(\theta - \phi - \frac{\pi}{3}) + i_{ap}(\phi + \frac{\pi}{3}) \qquad ...(3.4.7b)$$

From symmetry conditions, and Equations (3.4.2b) - (3.4.7b),

$$i_{ap}(0) = \frac{V_i}{3\omega L}\left[\pi d - 2d\phi - \frac{2\pi}{3}\right] \qquad ...(3.4.8b)$$

Also,

$$i_{ap}(\phi) = \frac{V_i}{3\omega L}\left[\frac{2\pi d}{3} + 2\phi - \pi\right] \qquad ...(3.4.9b)$$

Imposing the soft-switching constraints,we get,

For Input bridge $\quad i_{ap}(0) \leq 0$

Over Region I ($0 \leq \phi < \frac{\pi}{3}$), from Equation(3.4.8a),

$$d \leq \frac{1}{1 - \frac{3\phi}{2\pi}} \qquad \ldots(3.4.10a)$$

Over Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$), from Equation (3.4.8b),

$$d \leq \frac{1}{\frac{3}{2} - \frac{3\phi}{\pi}} \qquad \ldots(3.4.10b)$$

For Output bridge $\quad i_{ap}(\phi) \geq 0$

Over Region I ($0 \leq \phi < \frac{\pi}{3}$), from Equation(3.4.9a),

$$d \geq 1 - \frac{3\phi}{2\pi} \qquad \ldots(3.4.11a)$$

Over Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$), from Equation (3.4.9b),

$$d \geq \frac{3}{2} - \frac{3\phi}{\pi} \qquad \ldots(3.4.11b)$$

Moreover, in conjunction with the above constraints one must also keep in mind that,

$$d \geq 0$$

Again, violation of any of the above constraints leads to natural commutation of the active devices and, hence, undesirably high switching losses due to the snubber dump action. Also, the $d \geq 0$ constraint limits the range of ϕ upto $\pi / 2$, for realizing soft-switching.

With a knowledge of the primary current, $i_{ap}(\theta)$, and the converter switching functions the various quantities of interest defined in the previous sections are once again calculated, and are given below.

Output Power :

Over Region I ($0 \leq \phi < \frac{\pi}{3}$)

$$P_o = \left[\frac{V_i^2}{\omega L}\right] d\,\phi \left[\frac{2}{3} - \frac{\phi}{2\pi}\right] \qquad ...(3.4.12a)$$

Over Region II ($\frac{\pi}{3} \leq \phi < \frac{\pi}{2}$)

$$P_o = \left[\frac{V_i^2}{\omega L}\right] d \left[\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}\right] \qquad ...(3.4.12b)$$

Transformer kVA :

$$T\_kVA = \frac{3\,(v_{aprms} + v'_{asrms}) * i_{aprms}}{2} \qquad ...(3.4.13)$$

where, $v_{aprms} = \frac{\sqrt{2}\,V_i}{3}$

and $v'_{asrms} = \frac{\sqrt{2}\,V'_o}{3}$

The remaining quantities of interest are given as in Section 3.2. The steady state operating characteristics of each quantity of interest, normalized to the same base as defined in the previous sections, are plotted as a function of the control variable, ϕ, with d as a parameter.

Figure 3.4.3a shows the variation of output power as a function of ϕ, over the range 0 to π / 2, with d as a parameter. The trend is similar

to those of Topology B(Figure 3.3.3a). However, for each d < 1, soft-switching can be obtained over a marginally higher range of ϕ, as compared to Topology B. For d = 1, full control over ϕ is attainable, under soft-switching. Figure 3.4.3b shows the same for values of d > 1. This demonstrates boost mode of operation under soft-switching. Analysis has been carried out for operation in the first quadrant, only. But, given the symmetry of the converter, it can be shown that reverse power flow characteristics similar to those for Topology B(Figures 3.3.3a and 3.3.3b) can be realized.

Figures 3.4.4a and 3.4.4b show the variation of transformer kVA with ϕ and output power, respectively. Selecting the maximum power transfer point(0.267pu) on the output bridge constraint(which pertains to the output bridge operating as a diode bridge), the minimum transformer kVA required is 0.391pu, Figure 3.4.4b. This gives a transformer utilization of 0.683. Now, for the same transformer kVA, the output power can be increased to 0.351pu at d = 1(see point labelled X), by virtue of an active output bridge. Hence, transformer utilization has gone up to 0.898, an increase of 31%. Moreover, the transformer utilization is fairly constant over a wide range of ϕ at d = 1, a very desirable feature.

The variation of input and output filter capacitor kVAs with ϕ and output power are shown in Figures 3.4.5a,b and 3.4.6a,b. As expected, much lower filter kVAs are required as compared to those for Topology B.

Finally, Figure 3.4.7 depicts the region of soft-switching on the V_o' - i'_{oav} plane. Observations similar to that for Topology B can be made.

One might be tempted to further extend the three-phase version to a general n-phase system. This would certainly be advantageous as far as the filter size is concerned. However, the cost and design of an n-phase transformer and the increasing number of active devices with their control and drivers would soon offset the decrease in cost of the

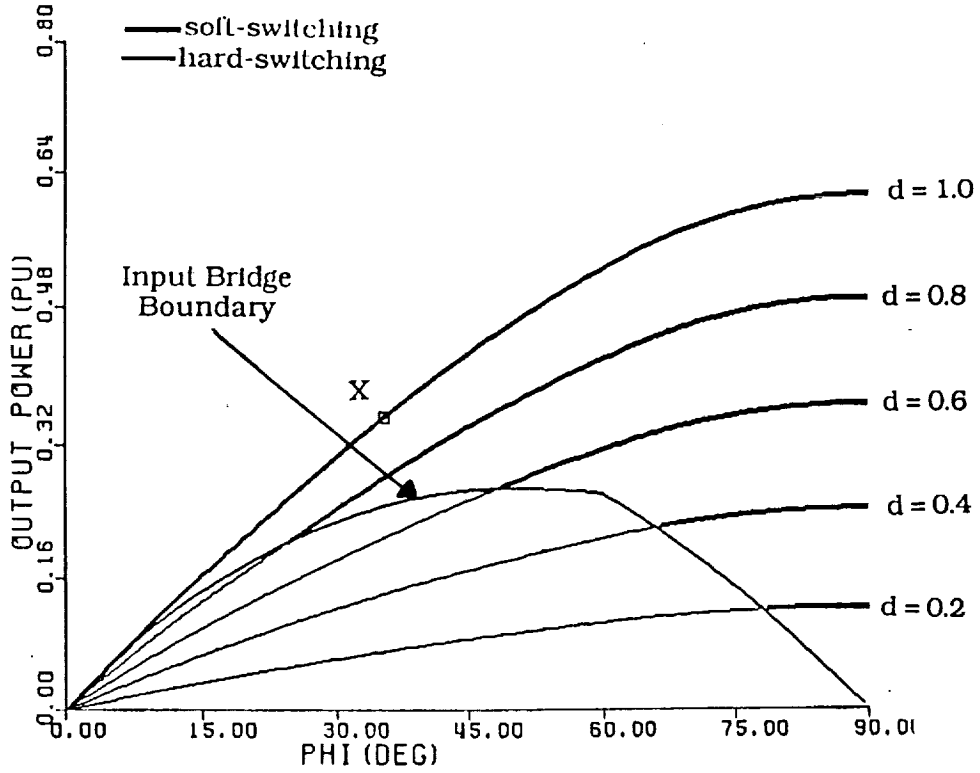


Figure 3.4.3a Output Power vs Phi with d as a parameter, showing buck characteristics(Topology C)

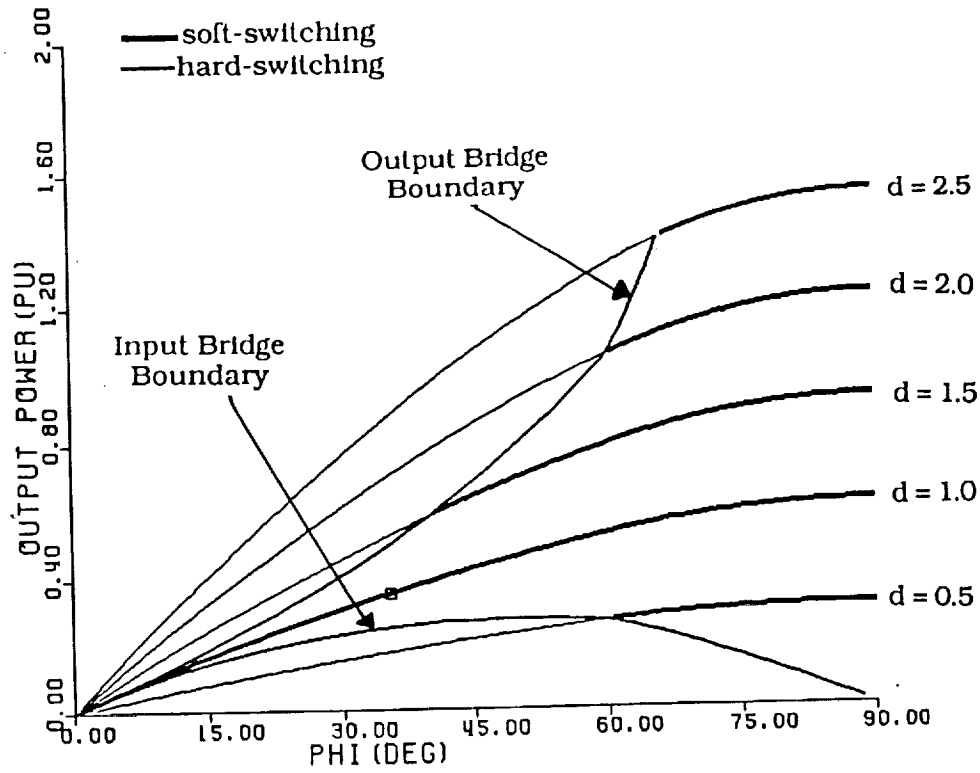


Figure 3.4.3b Output Power vs Phi with d as a parameter, showing buck-boost characteristics(Topology C)

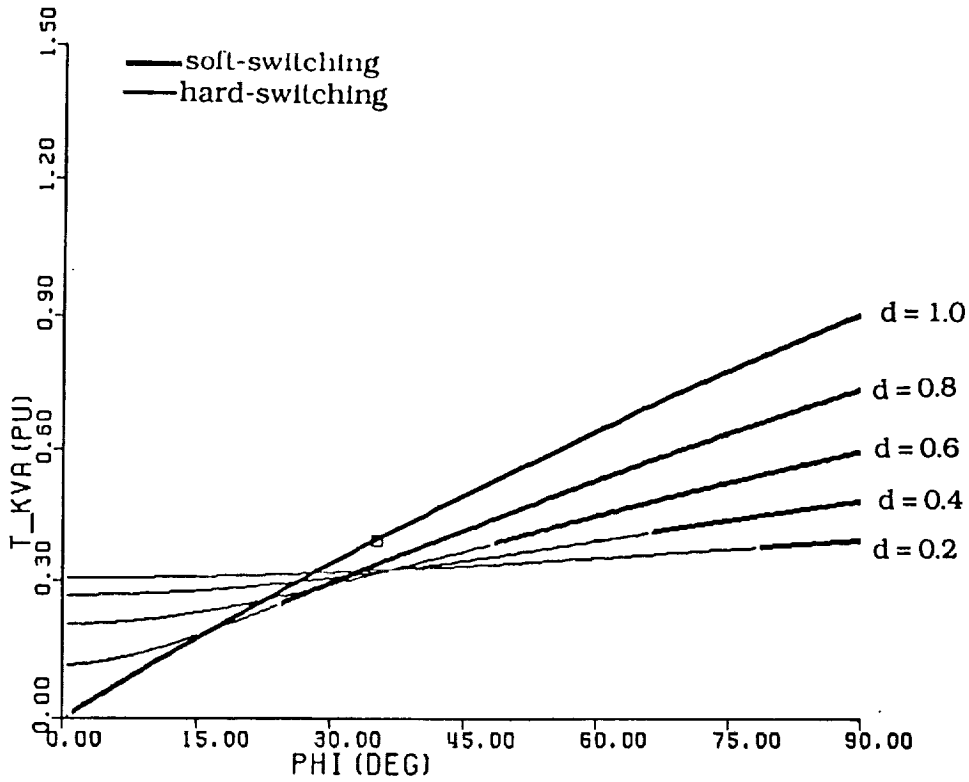


Figure 3.4.4a Transformer kVA vs Phi with d as a parameter (Topology C)

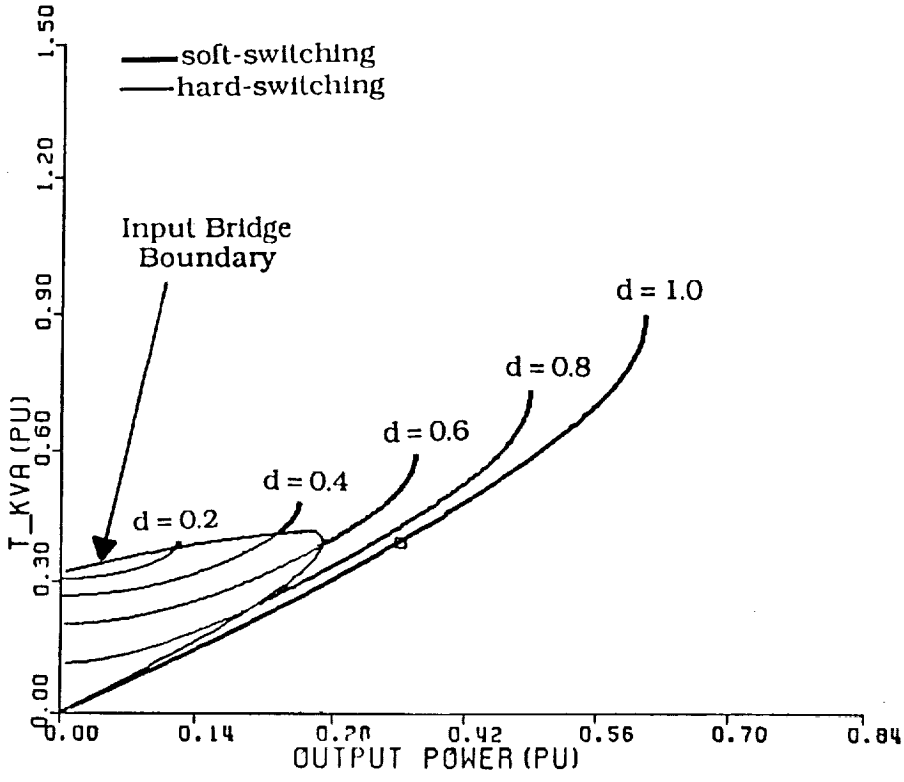


Figure 3.4.4b Transformer kVA vs Output Power with d as a parameter(Topology C)

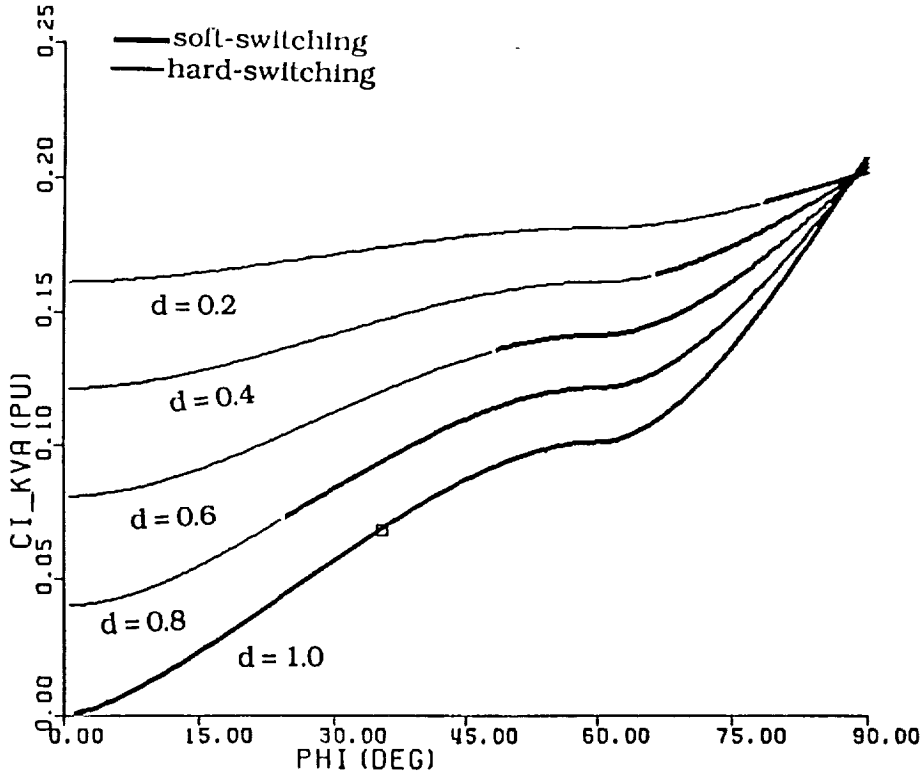


Figure 3.4.5a Input Filter Capacitor kVA vs Phi with d as a parameter (Topology C)

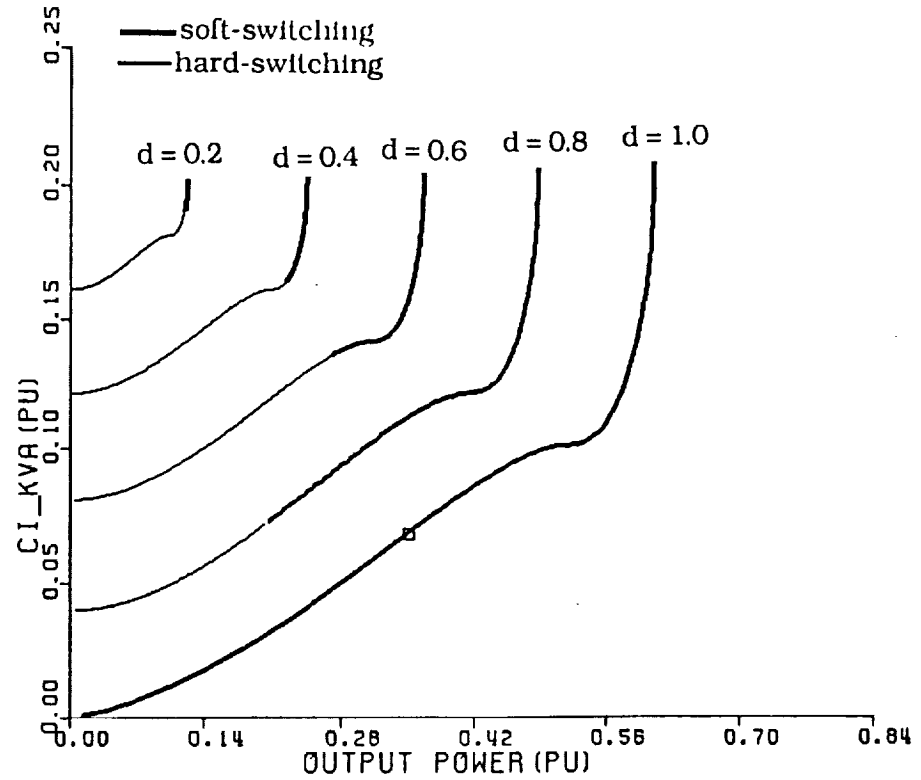


Figure 3.4.5b Input Filter Capacitor kVA vs Output Power with d as a parameter (Topology C)

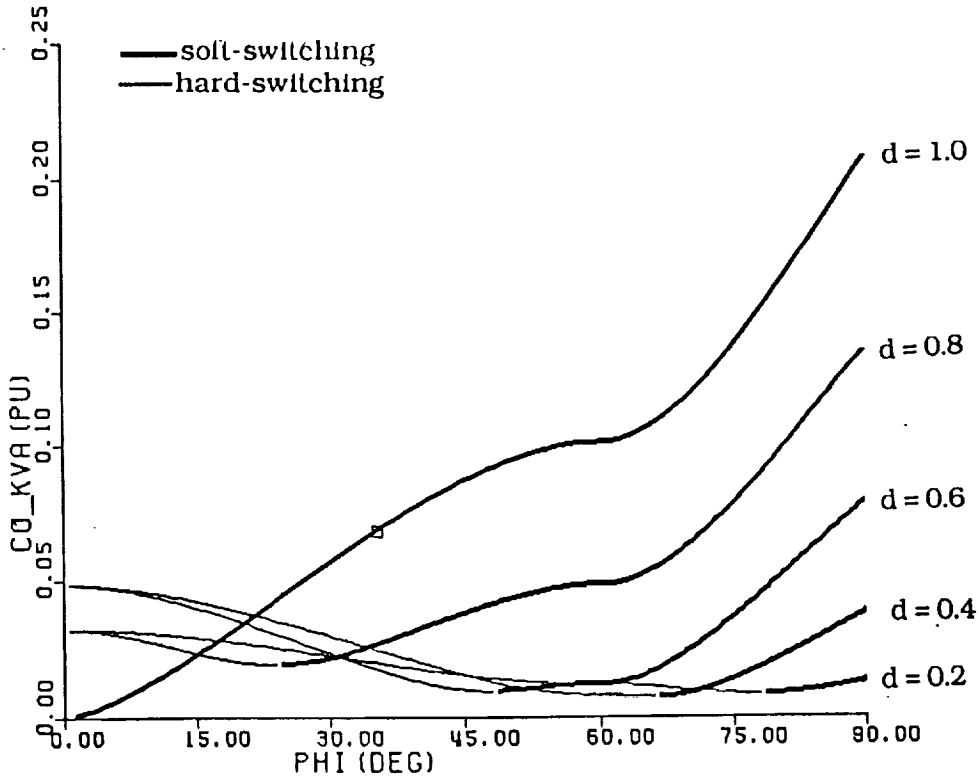


Figure 3.4.6a Output Filter Capacitor kVA vs Phi with d as a parameter(Topology C)

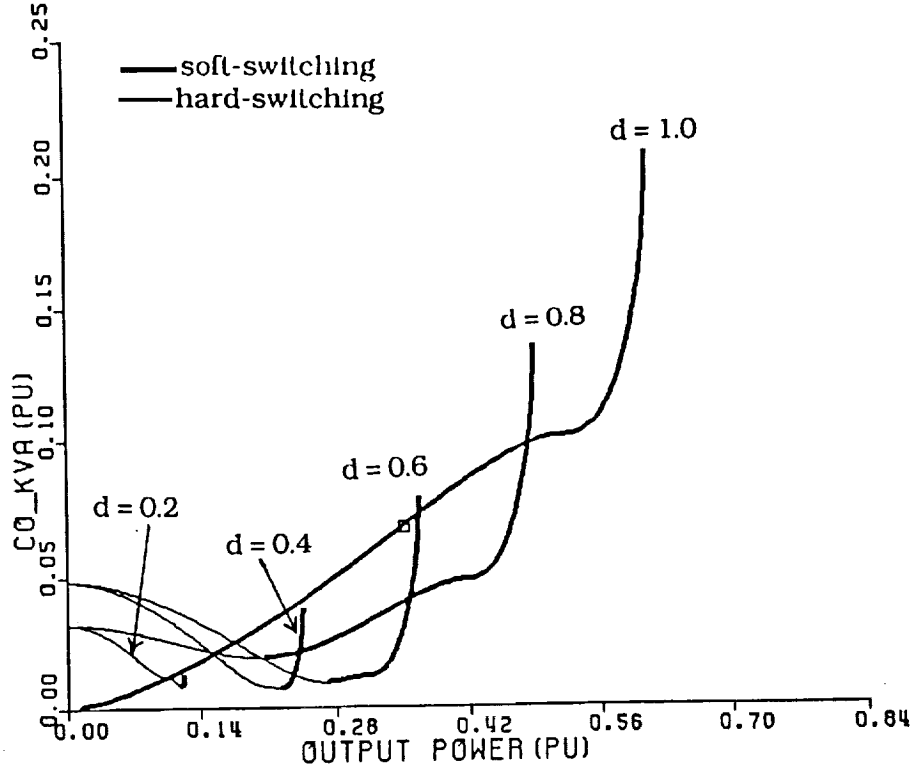


Figure 3.4.6b Output Filter Capacitor kVA vs Output Power with d as a parameter (Topology C)

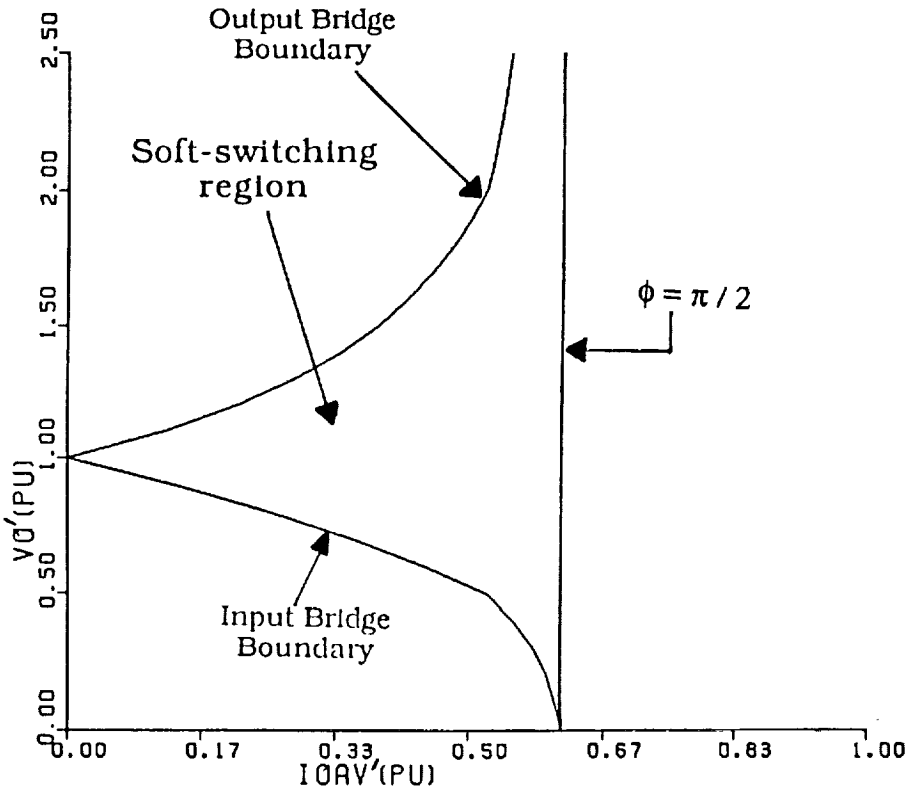


Figure 3.4.7 Output Voltage vs Output Current, showing soft switching Boundaries and Region(Topology C)

filters. Additionally, the analysis would become extremely tedious with the multiple regions and modes of operation.

To close this chapter, an elegantly simple model for Topologies A and B is presented in the following section, which will hopefully lead to a deeper understanding of the operation of these circuits.

3.5 Fundamental Model for Proposed Topologies A and B

Conceptually, each of these circuits can be viewed as an inductor(the transformer leakage inductance) driven at either end by a controlled square-wave voltage source. The voltage sources are phase-shifted from each other by a controlled angle, ϕ. To simplify the analysis, the square-wave voltage sources are replaced by their fundamental components. Figure 3.5.1a shows the fundamental model. Note, this model can also be treated as a per phase model for Topology C. The model is identified to the familiar synchronous machine equivalent circuit and may be expected to demonstrate similar properties. The inductance, L, is analogous to the series inductance of the machine. The input($\mathbf{V_{fi}}$) and output($\mathbf{V_{fo}'}$) voltage sources can be viewed as the internal e.m.f. and terminal voltage, respectively. The angle, ϕ, is commonly referred to as the torque angle. Since, all circuit quantities are sinusoidal at a single frequency(the switching frequency), a phasor analysis can be carried out. The steady state current phasor, $\mathbf{I_p}$, through the inductor, is given as,

$$\mathbf{I_p} = \frac{\mathbf{V_{fi}} - \mathbf{V_{fo}'}}{\mathbf{X_L}} \qquad \ldots(3.5.1)$$

where, $\mathbf{V_{fi}} = V_{fi}\angle 0\rangle$

$\mathbf{V_{fo}'} = V_{fo}'\angle -\phi\rangle$

$$\mathbf{X_L} = j\omega L$$

ω = switching frequency

Note, for a square-wave input voltage of peak amplitude V_i, the RMS fundamental component, V_{fi} is given as,

$$V_{fi} = \frac{2\sqrt{2}V_i}{\pi}$$

Similarly, for the output,

$$V_{fo} = \frac{2\sqrt{2}V_o}{\pi}$$

Hence, the output power is given as,

$$P_o = \text{Real part of}\left[\mathbf{V'_{fo}}\,\mathbf{I_p^*}\right]$$

$$= \frac{V_{fi}\,V'_{fo}}{\omega L}\sin(\phi)$$

$$= \frac{V_{fi}^2}{\omega L}\,d\,\sin(\phi) \qquad \ldots(3.5.2)$$

where, $d = \dfrac{V'_{fo}}{V_{fi}}$

Equation (3.5.2) is identical to that for a synchronous machine. Figure 3.5.1b shows a plot of the fundamental output power(normalized to the power base defined in Section 3.2) for d = 1. The actual output power

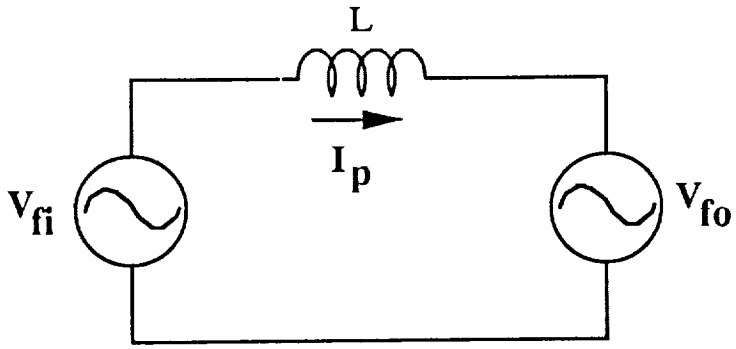


Figure 3.5.1a Per Phase Fundamental Model of Dual Active Bridges DC/DC Converters

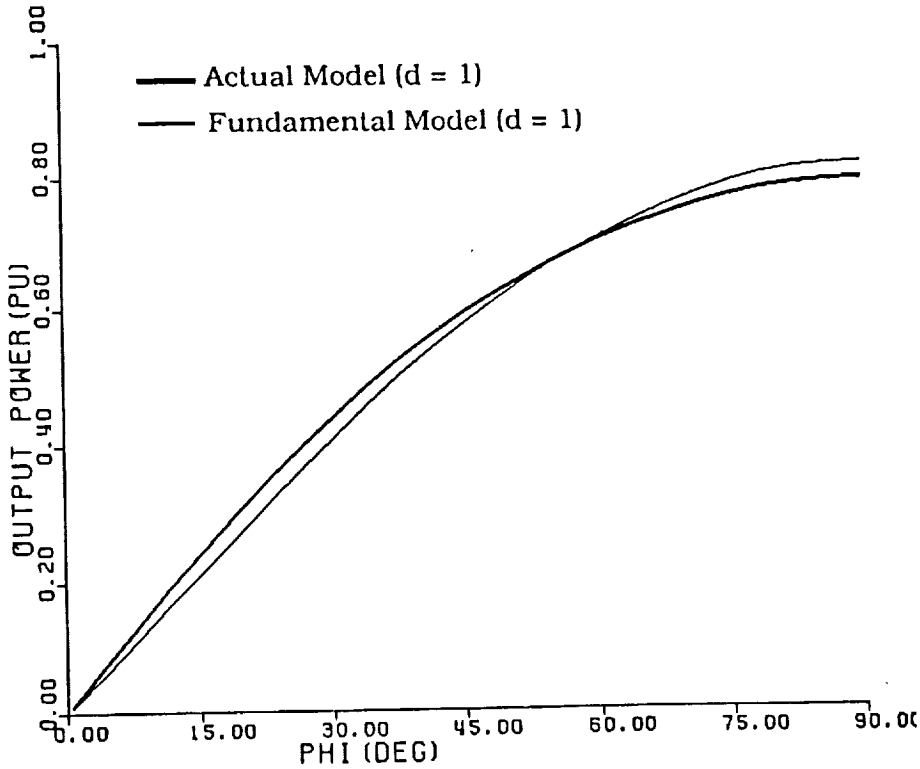


Figure 3.5.1b Output Power vs Phi for Actual and Fundamental Models at d = 1

for Topology B, for d = 1, is also shown on the same figure. The good correlation, justifies the validity of the fundamental model.

To appreciate the relationship between ϕ and d for soft-switching conditions, phasor diagrams based on the fundamental model can be very helpful. Again, as a reminder the soft-switching constraints dictate that the inductor current $\mathbf{I_p}$ lag the input voltage, $\mathbf{V_{fi}}$, and lead the output voltage, $\mathbf{V_{fo}'}$. For instance, Figure 3.5.2a shows the phasor diagram for d = 1. As ϕ is varied over the range 0 to $\pi/2$, the current phasor, $\mathbf{I_p}$ always remains between the phasors $\mathbf{V_{fi}}$ and $\mathbf{V_{fo}'}$, thus satisfying the above soft-switching constraints for this entire range of ϕ. This conforms to our actual model. Figure 3.5.2b shows another phasor diagram, where d < 1. As seen, ϕ must be greater than a certain minimum to achieve soft-switching on the output bridge. The input bridge constraint is always satisfied.

To conclude, this section presents a fundamental model for the dual active bridge topologies. The fundamental model shows good correlation in the dependence of the output power with d and ϕ, with that for the actual model. Hence, the simple analysis for the fundamental model can be used in making some first-pass predictions about the operation of the circuit. Moreover, the phasor diagrams are a convenient tool for appreciating the soft-switching constraints for the two bridges.

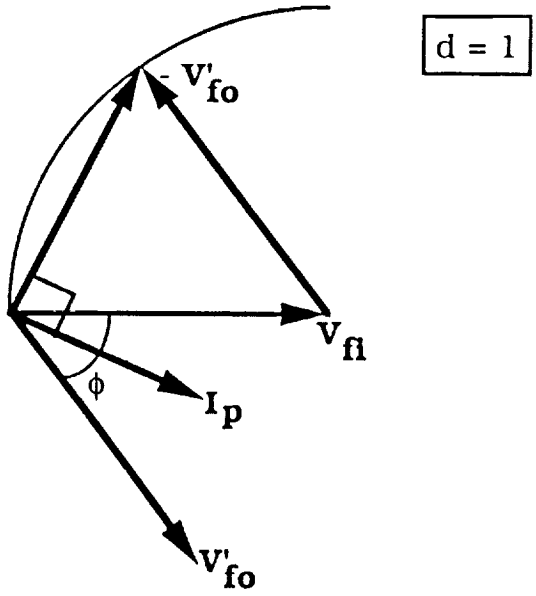


Figure 3.5.2a Phasor diagram for the Fundamental Model for d = 1

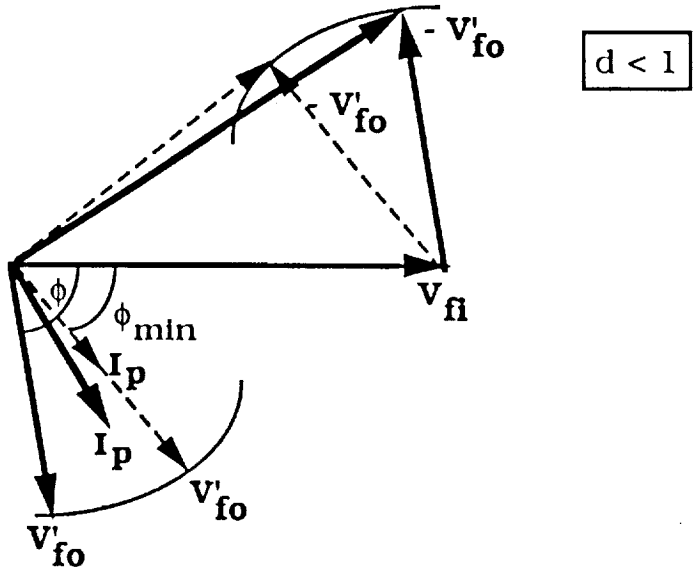


Figure 3.5.2b Phasor diagram for the Fundamental Model for d < 1

3.6 Summary

The main goal of this chapter has been to present the principle of operation along with a detailed steady state analysis for each of the three proposed topologies. The various operating characteristics including power transfer, transformer and filter kVAs, derived from this analysis, are shown, with their soft-switching and hard-switching regions. A fundamental model for the dual active bridges dc/dc converter is also presented, and is seen to give good insights into the operation of the converter through the aid of phasor diagrams.

The issue of selection of the optimum topology, based on the requirements of high power density, high reliability, and ease of control, is addressed in the following chapter.

CHAPTER 4

SELECTION OF FINAL CONVERTER TOPOLOGY

4.1 Introduction

With a knowledge of the performance characteristics of the various components in the three proposed topologies, presented in detail in the last chapter, we are now in a position to quantitatively assess the merits and demerits of these circuits. The final objective being to select one of these topologies which realizes the highest power density, under the given rated specifications, under minimal component stresses and control complexity.

The following section presents a table comparing the various component specifications in each topology. The comparison is based on the consideration that each topology operates at its optimum transformer utilization under rated conditions. The calculations are based on the equations and operating characteristics presented in the last chapter, and denormalized to conform to the rated specifications of 50 kW at an input dc voltage of 200V and an output dc voltage of 2000V. The switching frequency is tentatively selected as 50 kHz, with a hope of operating as high as 100 kHz.

4.2 Comparison of Proposed Topologies

Since high power density is the most stringent requirement, and the transformer is the biggest component in the system, it seems reasonable to design the circuit based on an optimum transformer utilization. For Topology A, this optimum operating point(see point labelled X on Figure 3.2.4b) is the minimum transformer kVA(0.475pu) required to transfer the maximum power(0.302pu). This corresponds to a phase-shift, $\beta = \pi$ and d = 0.58. As observed in Chapter 3, Topology B gives a 40% improvement in the transformer

utilizaton over that of Topology A for the same transformer kVA of 0.475pu at d = 1, by virtue of an active output bridge. Hence, for purpose of comparison, this seems like a reasonable operating point(see point labelled X in Figure 3.3.4b) for Topology B. The corresponding phase-shift, ϕ, turns out to be 28.78°. For Topology C, a similar design philosophy of choosing an operating point for d = 1(see point labelled X in Figure 3.4.4b), corresponding to the minimum transformer kVA required for the maximum power transfer on its output constraint(i.e., diode bridge constraint), leads to a design point corresponding to a ϕ = 35.41°.

The next step was to evaluate the various quantities related to the switching devices, filters and transformer, for each topology operating at its selected optimum operating point. These quantities were denormalized to conform to the given rated specifications and are tabulated in Table 4.2.1.

Examining the peak device stresses for each bridge, Topology C offers the lowest (V_{pk} * I_{pk} / P_o) stress at 1.17pu. However, Topology B shows a slightly higher stress of 1.19pu, with a saving of two devices on each bridge. Topology A exhibits very high device stresses on both the bridges. Infact, the 1.19pu device stress for Topology B compares favourably with the desired stress of 1pu, theoretically achievable with hard-switched pwm converters.

Comparing the transformer specifications, again Topology A seems to be poorest in regard to peak current stresses and transformer utilization. Both Topologies B and C offer almost identical performances. However, it must be emphasized that Topology C requires a three-phase transformer with identical equivalent leakage inductances in each phase. This is necessary for two reasons :

(i) Balanced three-phase currents, resulting in current components at multiples of six times the switching frequency only, at the dc sides of the bridges. Hence,

TABLE 4.2.1

(P_O = 50 kW ; V_I = 200 Vdc ; V_O = 2000 Vdc ; f = 50 kHz)

	Topology A	**Topology B**	**Topology C**
d	0.58	1	1
β(°)	180	-	-
ϕ(°)	-	28.78	35.41
Device Specs.			
Input Bridge			
No. of Active Devices	4	4	6
Peak voltage(V)	200	200	200
Peak current(A)	861.48	297.57	293.46
V_{pk}*I_{pk} / P_O	3.45	1.19	1.17
Output Bridge			
No. of Active Devices	4(diodes)	4	6
Peak voltage(V)	2000	2000	2000
Peak current(A)	50.68	29.76	29.35
V_{pk}*I_{pk} / P_O	2.03	1.19	1.17
Transformer Specs.			
1 : N	1 : 17	1 : 10	1 : 10(Y-Y)
Peak pri. volts(V)	200	200	133/ph
Peak pri. amps(A)	861.48	297.57	293.46
RMS pri. amps(A)	497.52	281.4	197.29/ph
Peak sec. volts(V)	2000	2000	1333/ph
Peak sec. amps(A)	50.68	29.76	29.35
RMS sec. amps(A)	29.27	28.14	19.73/ph
kVA	78.64	56.28	55.7
P_O / kVA	0.64	0.89	0.89
L(μH)	0.77	1.1	0.89/ph
Filter Specs.			
Input			
Cap. volts(Vdc)	200	200	200
Cap. RMS amps(A)	429.75	129.15	48.43
kVA	85.95	25.83	9.69
Output			
Cap. volts(Vdc)	2000	2000	2000
Cap. RMS amps(A)	14.63	12.92	4.84
kVA	29.26	25.83	9.69
Operation	1-Quadrant	2-Quadrant	2-Quadrant

reduction in the RMS-current ratings of the filter capacitors, and

(ii) The minimum current constraint for zero-voltage switching of the active devices at turn-off, is dictated by the value of the leakage inductance and snubber capacitance. Hence, for this minimum current to be identical for each device, it seems logical for the leakage inductance to be identical in each phase.

Figure 4.2.1 shows a possible construction of such a symmetrical three-phase transformer. In view of the constraint of high power density, the non-conventional core geometry requiring additional yokes would indeed be a difficult problem to resolve.

Finally, examining the input and output filter capacitor ratings, Topology C exhibits the lowest RMS-current stresses and hence, lowest kVA, for reasons mentioned above. Topology A is the worst with 9 times the kVA rating for that of the input capacitor for Topology C. However, the output filter stresses for Topology A are much lower than that of its input filter. This is because, the output bridge being a diode bridge allows the current on its dc side to be unidirectional only, resulting in lower ripple currents.

4.3 Final Topology

Of the three proposed topologies, B and C possess the following desirable attributes :

1) Good range of control, especially for a dc conversion ratio(d) of unity.
2) Buck/boost operation possible.
3) High transformer utilization.
4) Low device and transformer stresses.
5) Bidirectional power flow.

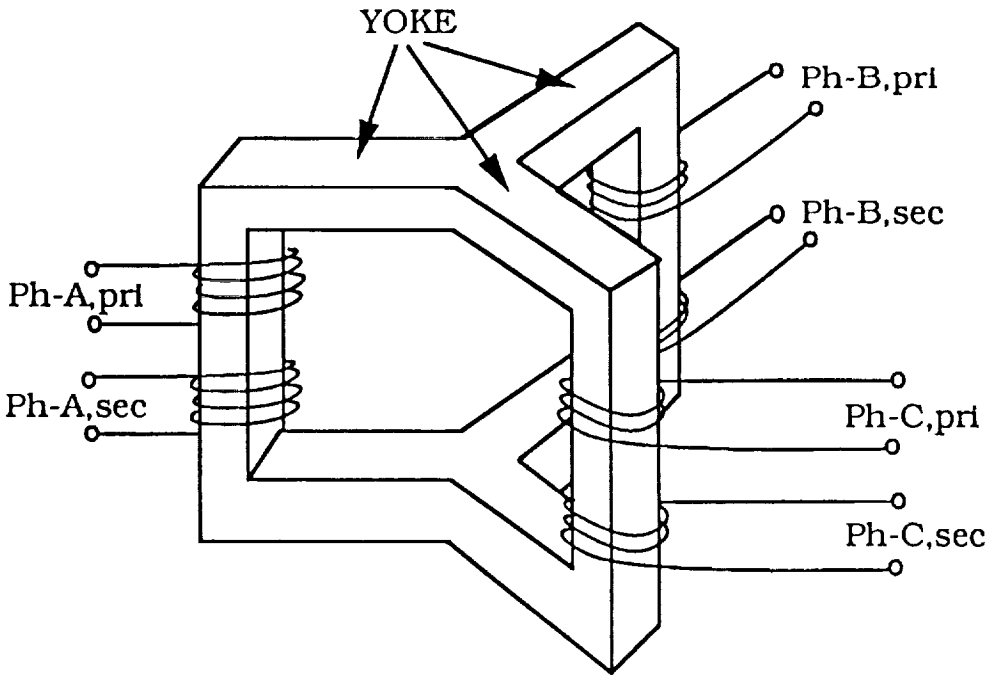


Figure 4.2.1 Schematic of a possible geometry of a Symmetrical 3-Phase Transformer

However, bearing in mind the requirement of high power density, Topology C suffers in the following aspects :

1) Requires 4 additional devices(2 on each bridge), with its associated gate-driver circuits
2) Complex transformer construction, with a weight penalty associated with the additional yokes required for symmetry

Moreover, the additional devices in Topology C, imply additional switching events per cycle and hence a more complex controller.

On the other hand, Topology C shows a distinct advantage over Topology B, in its lower filter kVA-ratings. However, with the state-of-the-art multi-layer ceramic capacitors(MLC) available, which offer much higher power densities than conventional commutation-grade or electrolytic capacitors, the total weight required for the filter capacitors for Topology B is seen to be marginally higher than that for Topology C.

Hence, on an overall basis, keeping in perspective the simpler and lighter transformer, and fewer switching devices, Topology B does seem to offer a higher power density than Topology C.

Finally, since the control methodology for Topology A can also be incorporated in Topology B, a wider range of control is possible when their V_o' - I'_{oav} operating characteristics are superimposed, as shown in Figure 4.3.1. It should be remembered that the $\beta = \pi$ boundary for Topology A is identical to the diode bridge constraint for Topology B, hence they overlap. Now for instance, at higher load currents one could maintain tight control over this current as the output voltage is reduced, by essentially switching from Topology B mode of operation to Topology A mode as the overlapping boundaries for the two topologies is crossed. A significant implication of this is that the load current could be held constant even under short-circuit faults, and with all the devices always operating under soft-switching conditions.

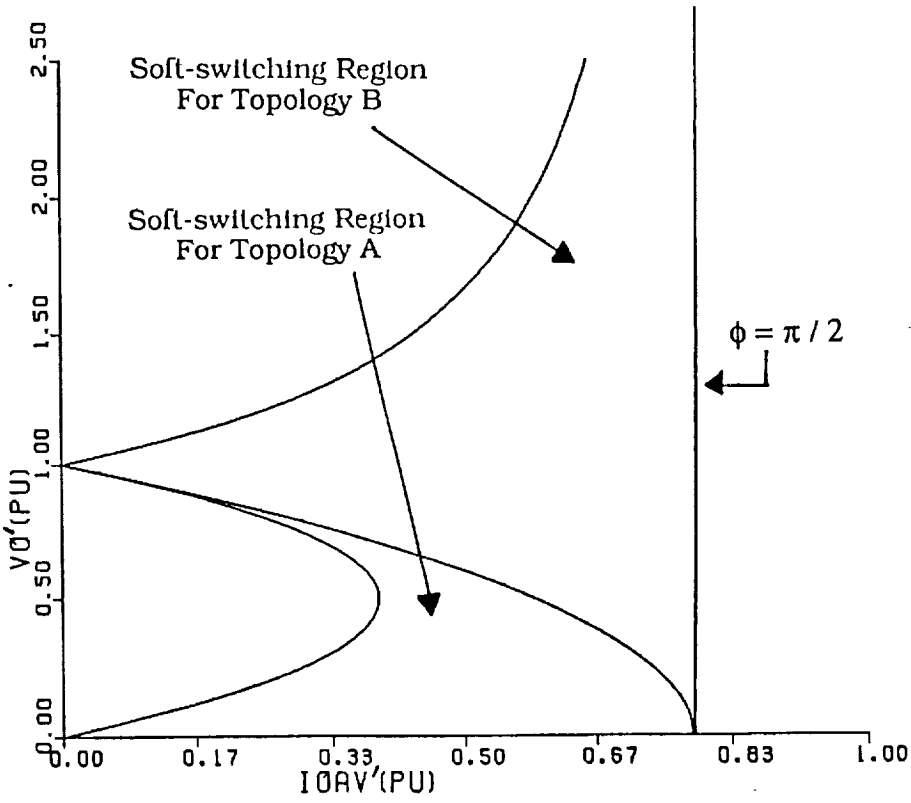


Figure 4.3.1 Superposition of the soft switching regions for Topologies A and B on the Output Voltage vs Output Current plane

In conclusion, considering the various desirable features of Topology B, it seems like the most viable choice as the final topology. However, the high output voltage requirement(2000 Vdc) seems to make the use of active output bridges difficult, as devices rated in the kilovolt range are limited in terms of switching speed. Also, the high power density needed mandates a high switching frequency. Thus, a modular approach is necessary for realizing high power at the high output voltages. For the specified output voltage, a series connection of two active half-bridges, as shown in Figure 4.3.2, is a possible solution. These aspects of circuit operation will be examined in the next phase of the project.

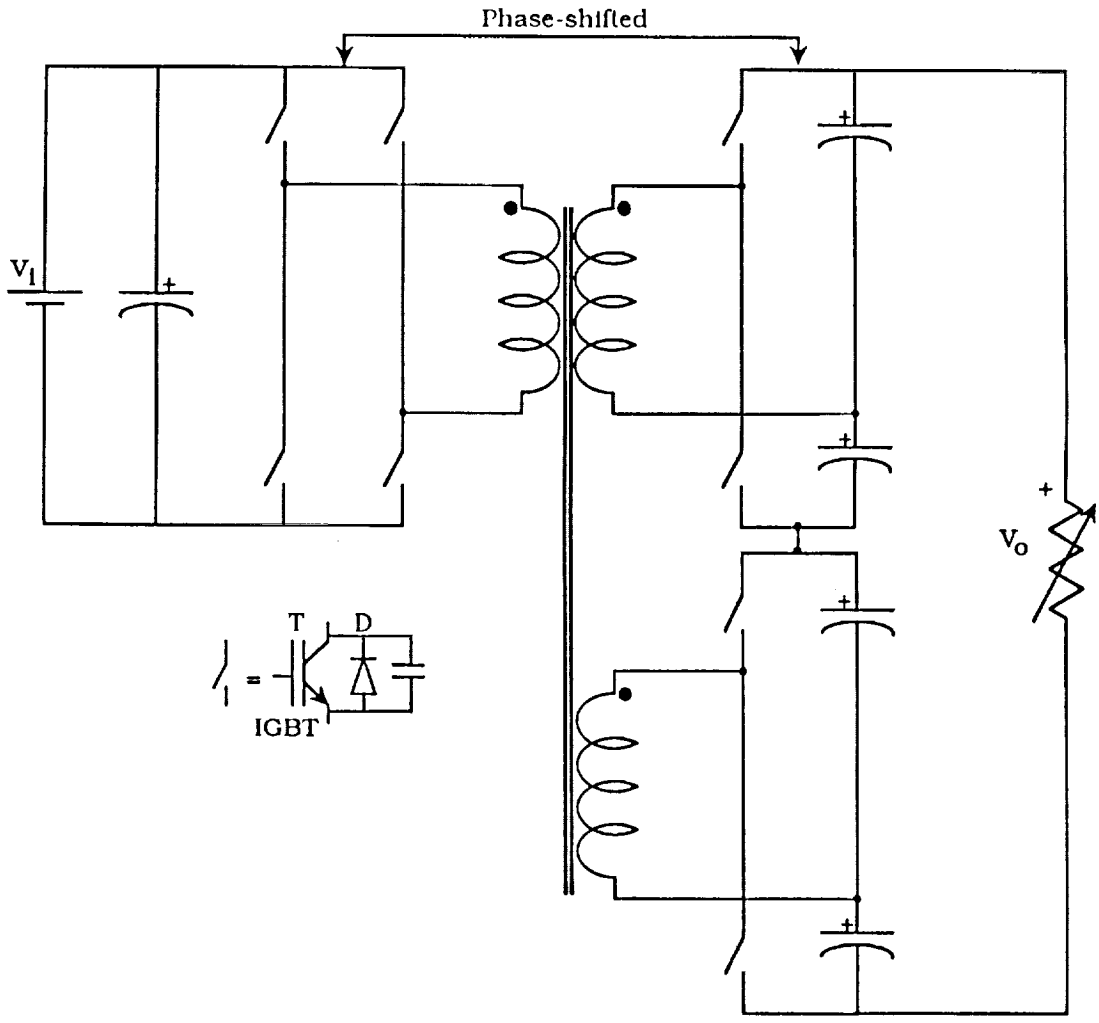


Figure 4.3.2 Schematic of Series Connected Single Phase Dual Active Bridges DC/DC Converter for High Voltage Outputs (Outputs are Half Bridges)

CHAPTER 5

CONCLUSIONS

5.1 Summary

The goal of this project is the development of a high power density, high power dc/dc converter for aerospace applications. The rated specifications are an output power of 50 kW, at an input voltage of 200 Vdc, output voltage of 2000 Vdc, with a power density of 0.2 - 0.3 kg/kW. The switching frequency will be in the order of 50 - 100 kHz. This report describes the work involved in the identification and selection of a suitable converter topology, as a first task of an on-going research project.

Three new dc/dc converter topologies are proposed, namely

a) Phase-Shifted Single Active Bridge DC/DC Converter(Topology A)
b) Single Phase Dual Active Bridges DC/DC Converter(Topology B)
c) Three Phase Dual Active Bridges DC/DC Converter(Topology C)

The salient features of these topologies are :

1) All are minimal in structure, i.e., each consists of an input and output bridge, input and output filter and a transformer, all components essential for a high power dc/dc conversion process.

2) All devices of both the bridges can operate under near zero-voltage conditions, making possible a reduction of device switching losses and hence, an increase in switching frequency.

3) All circuits operate at a constant frequency, thus simplifying the task of the magnetic and filter elements.

4) Since, the leakage inductance of the transformer is used as the main current transfer element, problems associated with the diode reverse recovery are eliminated. Also, this mode of operation allows easy paralleling of multiple modules for extending the power capacity of the system.

5) All circuits are least sensitive to parasitic impedances, infact the parasitics are efficiently utilized.

6) The soft switching transitions, result in low electromagnetic interference.

In addition, the dual active bridge topologies can realize,

1) Two-Quadrant operation
2) Buck-boost characteristics
3) Low device and component stresses.

A detailed analysis of each topology has been carried out. The various steady state operating characteristics including, output voltage, power transfer, transformer utilization and filter capacitor kVA ratings as a function of the control and load parameters are presented for soft-switching conditions.

Based on the analysis, the various device and component ratings for each topology operating at an optimum point, and under the given specifications, are tabulated in Table 4.2.1. Topology A offers the possibilty of realizing high output voltages given the fact that the output is a diode bridge. However, the input filter capacitor ratings and device stresses are much higher than those for Topologies B and C. Moreover, the transformer utilization is the poorest. On the other hand, Topologies B and C exhibit device VA stresses which are only 20% higher than that of an ideal conventional hard switched pwm converter. Topology B gives a 40% improvement in the transformer utilization over that of Topology A. Topology C shows a similar

improvement in the transformer utilization, at the expense of a more physically complex symmetrical three phase transformer. As expected, the filter capacitor ratings for Topology C are the lowest.

Based on the following considerations, Topology B is selected as the final converter topology :

1) Allows better control range, under soft-switching conditions, as compared to Topology A, especially at a dc conversion ratio of unity

2) Relatively, simpler transformer design as compared to Topology C

3) Given the state-of-the-art in the high power density multi-layer ceramic capacitors, it is seen that very little or no weight penalty will be incurred, although the filter kVA requirements are higher than that those for Topology C

4) Requires fewer active devices compared to Topology C, and hence fewer drive circuits

5) Since the control methodology for Topology A can also be incorporated in Topology B, a much wider range of control can be achieved.

A fundamental component for the dual active bridge topologies is also presented, and it shows good correlation to the actual model. This model allows a better appreciation of soft switching constraints through phasor diagrams.

5.2 Future Work

A proof-of-concept experimental unit for Topology B, rated for 1 kW at a switching frequency of 20 kHz has been built and tested. The

experimental unit along with simulated and actual waveforms showing soft-switching characteristics will be presented in the next report. The experimentally obtained power transfer characteristics will also be presented to corroborate theoretical results.

The tasks involved in the next phase of this project include the following:

1) Converter Design Issues
   a) Choice of device type, based on trade-offs between speed and conduction losses
   b) Computer simulation results with realistic device models, snubber capacitances and ESRs of filter capacitors

2) Transformer Design Issues
   a) Choice of core material based on trade-offs between core losses, switching frequency and operating flux levels
   b) Estimation of copper losses arising from skin and proximity effects, and investigation of winding geometries to minimize these losses
   c) Investigation of fabrication techniques to control leakage inductance

3) Overall Circuit Layout Issues
   a) For good thermal management
   b) For minimization of parasitic impedances
   c) For low volume

4) Projected Performance-Measures
   a) Power Density
   b) Efficiency

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