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Magellan/Galileo Solder Joint Failure Analysis and Recommendations

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ABSTRACT

On or about November 10, 1988 an open circuit solder joint was discovered in the Magellan Radar digital unit (DFU) during integration testing at Kennedy Space Center (KSC) in Florida. A detailed analysis of the cause of failure was conducted at the Jet Propulsion Laboratory during November 1988 leading to the successful repair of many pieces of affected electronic hardware on both the Magellan and Galileo spacecraft. The problem was caused by the presence of high thermal coefficient of expansion heat-sink and conformal coating materials located in the large (0.055") gap between Dual Inline Packages (DIPS) and the printed wiring board. This publication describes the details of the observed problems and makes recommendations for improved design and testing activities in the future.

ACKNOWLEDGEMENT

The results described in this publication reflect the contributions of a number of individuals who supported the Tiger Team activity. Key contributors included:

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Genji Arakaki	Electronic Packaging
Bob Bamford	Stress Analysis
Pradeep Bhandari	Thermal Analysis and Test
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Tom Borden	Electronic Packaging
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Ken Evans	SEM Analysis
Ray Garcia	Thermal Testing
Mark Gibbel	Thermal Analysis and Test
Don McQuarie	Quality Assurance
Dr. Gordon Mon	Temperature Cycle Testing
Dick Rathcke	AACS Testing
John Shepherd	Solution Development
Phil Stevens	Material Properties
Jerry Swanson	Reliability

In addition, many thanks are due the many technicians and specialists that worked long hours to generate the data presented. Special thanks are due J. Gerpheide, A. E. Cherniack, B. Brown and D. Hess for their unwavering support and guidance.

Hughes Aircraft, as builder of the balance of the Magellan radar, contributed many test articles to confirm that problems observed in the JPL-built hardware were not also present in the Hughes-built hardware. As noted in the findings, the Hughes-built hardware utilized slightly different processing procedures and materials and was found to be free of the problems observed in the JPL-built hardware. Many thanks are extended to the Hughes personnel for their cooperation in this effort.

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INTRODUCTION

Immediately following the finding of the failed solder joint in the Magellan Radar DFU, a Tiger Team of technical specialists was assembled at JPL to determine the exact cause of failure and to develop recommended fixes. A one-month indepth activity was carried out involving detailed parts failure analysis, structural analysis and testing, thermal analysis and testing, materials evaluations, and numerous thermal-cycle tests [1,2]. Thousands of solder joints were inspected on dozens of flight and engineering-mockup boards. The activity resulted in a much improved understanding of many issues related not only to solder joint integrity, but also to a variety of other packaging and test verification issues.

ELECTRONIC PACKAGING OVERVIEW

A circuit board of the Magellan Radar DFU, as pictured in Fig. 1, is fairly typical of JPL electronic packaging; it is fabricated using surface-mounted components that are hand soldered to the top surface of the 8-Layer G-10 printed wiring board (PWB) that is bonded to the chassis web. A second board is bonded to the opposite side of the web, directly beneath the pictured board, facing in the opposite (back-to-back) direction. Part cooling is provided by conducting the part heat through the board to the central web, then laterally in the web plane to the chassis edge (base plate) opposite the connectors; the base plate edge is bolted to the spacecraft external heat transfer surface (shear plate).

For compatibility with surface mounting, most integrated circuits are obtained and used in "flat-pack" packages. Although there is considerable variability in flat-pack package size and configuration, the leads of this style part exit horizontally, parallel to the board surface. They are subsequently bent, as shown in the left side of Fig. 2, to provide for a positive spacing between the part and the board. The horizontal lead attachment allows for the easy incorporation of part-board strain relief, both in the plane of, and normal to the board.

With increasing frequency in recent years, parts have been unavailable in flat-packs, and have had to be obtained in Dual-Inline-Packages (DIPS). This part style, although not intended for surface mounting, can be converted for surface mounting by bending the leads into the "gull-wing" configuration illustrated in the right side of Fig. 2. This is done at JPL with a special lead bending and trimming tool.

Unfortunately, the DIP lead geometry prevents the leads from being bent adjacent to the part body; this results in the part standing off the boards with a typical part-board spacing of around 0.055". This space has either ended up being filled with Solithane 113/300 during conformal coating, or,

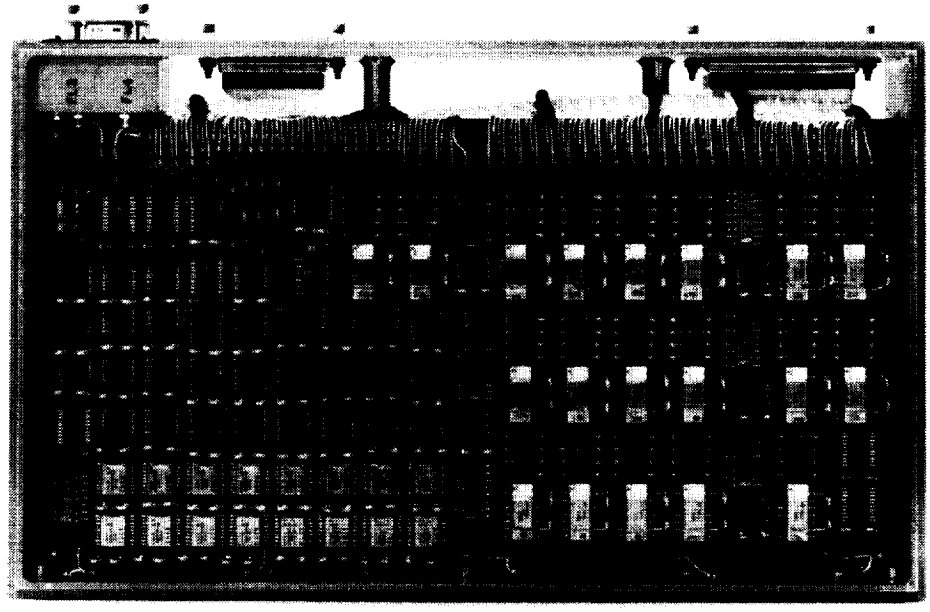


Fig. 1. Typical Magellan Radar Digital Unit (DFU) circuit board

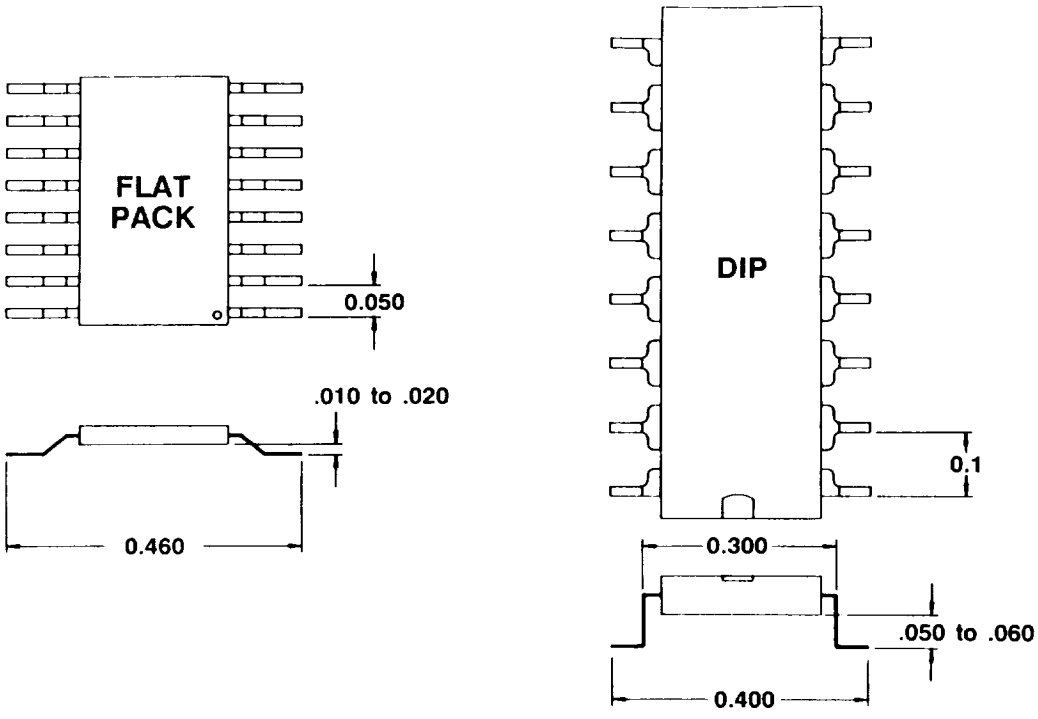


Fig. 2. Comparison of DIP and Flat-pack electronic part packages

for improved heat conduction, has been intentionally filled with one of several heat transfer compounds, aluminum, or copper heat sinks. An historical problem with the DIP package is that the configuration does not provide any lead flexibility in the normal-to-the-board direction.

REPORT ORGANIZATION

This report summarizes the findings of the Tiger Team solder joint investigation starting first with an overview in Section 2 of the DIP soldering and attachment problem and recommendations. Next, related packaging-design and verification-process issues are addressed in Section 3; these issues perhaps contributed to the problem not being caught earlier in the hardware design and qualification phases. Because rework played an important part in generating the fixes, Section 4 deals with a number of rework process sensitivities that fall into the context of lessons learned or re-learned. The final section, Section 5, attempts to concisely summarize the key recommendations. Important references released during the course of the investigation, or found to be particularly relevant, are listed at the end.

SECTION 2

DIP SOLDERING AND ATTACHMENT PROBLEMS

PROBLEM DESCRIPTION

As noted above, the specific failure that led to this investigation was a cracked, open-circuit solder joint that occurred in a dual-inline-package integrated circuit during hardware integration testing of the Magellan Radar Digital Unit (DFU) at KSC. A closeup photograph of the open-circuit solder joint is shown in Fig. 3. This particular part was configured with alumina-filled Solithane applied beneath the part (prior to soldering) to enhance its heat transfer performance.

The most influential finding came directly from visual examination of the failed part. Following removal of the problem lead (pin-15) for analysis, the solder socket remaining on the pad was found to be filled with clear Solithane, indicating that the solder joint had actually fractured early in the hardware fabrication phase, prior to conformal coating, and prior to qualification testing. All of the leads (pins 9 through 16) on the same side of the DIP were found to be heavily fractured, and, as shown in Fig. 4, all were filled with clear Solithane.

In the subsequent scanning electron microscope (SEM) analyses of the failed leads, the solder fracture surfaces displayed good lead wetting and good elongation at break (Fig. 5). This indicates that the solder joints themselves were not at fault, but that excessive forces are the most likely cause of failure. Another interesting finding was that all of the leads on the opposite side (pins 1 to 8) of the failed DIP were in excellent condition as shown in Fig. 6.

Upon detailed examination of the other DIPs on the DFU, and on many other Magellan and Galileo flight boards, it was found that most DIPs had significant numbers of cracks and/or heavy stressing in their solder joints. Heavy stressing is the presence of large numbers of micro cracks visible in the shiny solder fillets; these give the solder surface a frosty granular appearance, and are the precursor to actual cracking.

The observed cracks and stressing, schematically illustrated in Fig. 7, invariably initiated at the heel of the solder joints, and gradually progressed toward the toes. There was a general trend for all, or most of the leads on one side of the DIP, to be significantly worse off than those on the other side, and no particular trend for end leads to be worse than middle leads, or vice versa. It is hypothesized that one weakest lead fails first thus transferring mechanical loads it was carrying to its nearest neighbors, and thereby cascading into an unzipping action for all the leads on a single side. Once the leads on one side (eg. pins 1 through 8) yield, the leads on the other side (pins 9 through 16) will be relieved of their load and will remain in good condition.

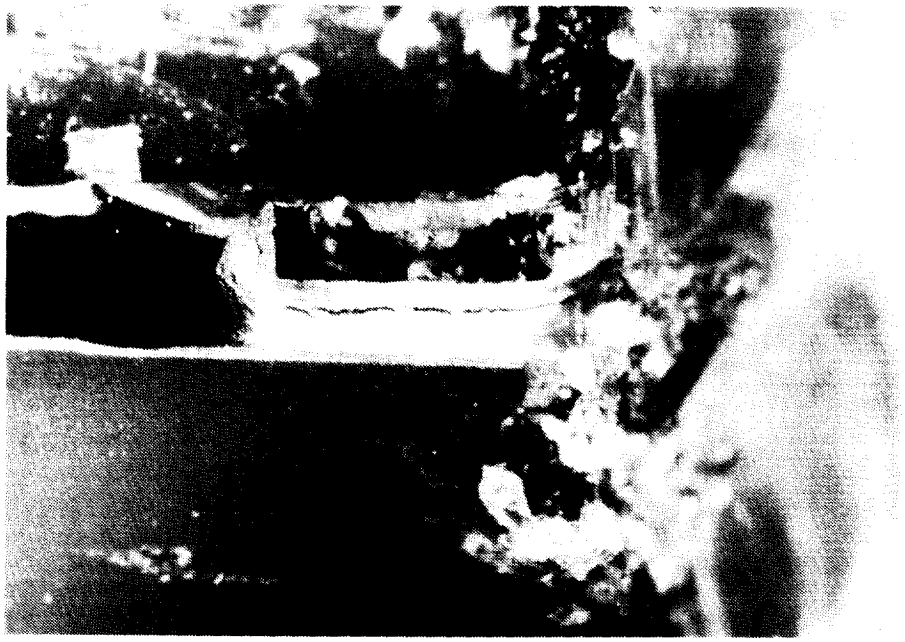


Fig. 3. Cracked solder joint of DIP in Magellan Radar Digital Unit (DFU)

Fig. 4. Clear Solithane found in solder-joint fractures of DFU part that failed open-circuit

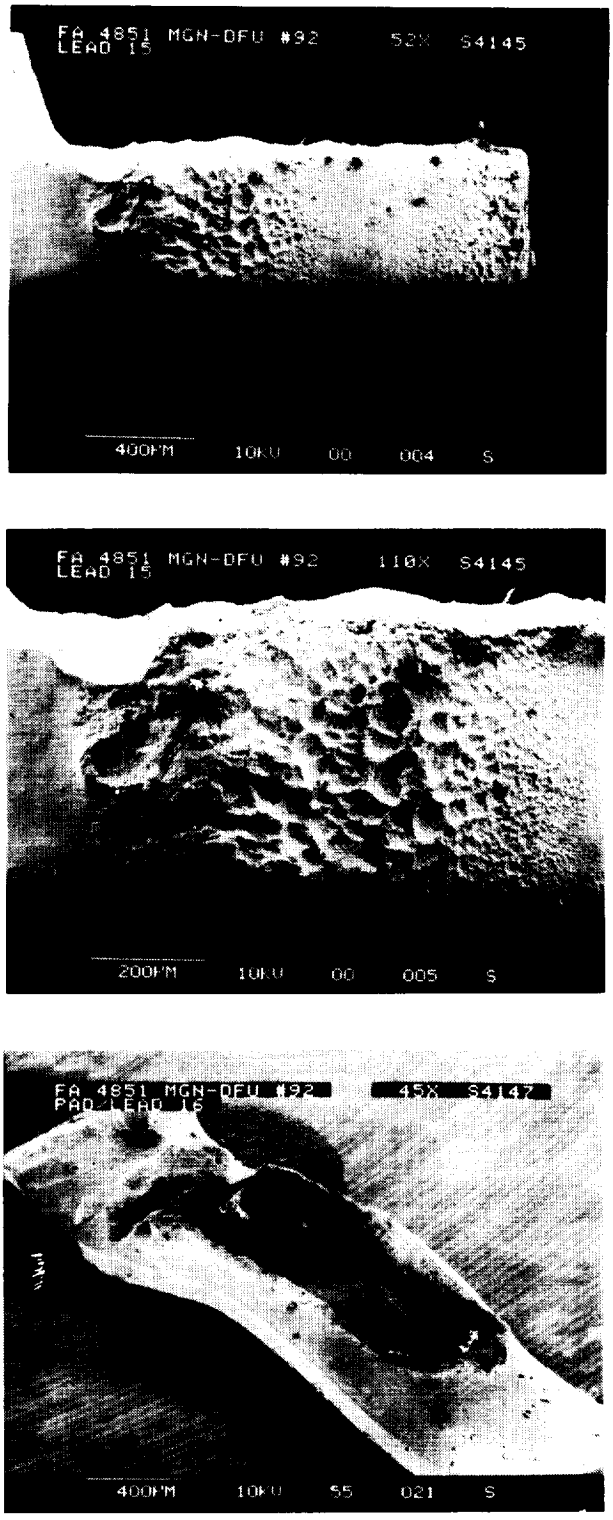


Fig. 5. SEM photographs showing good solder fracture properties of foot and pad from failed (pin 15 and 16) solder joints

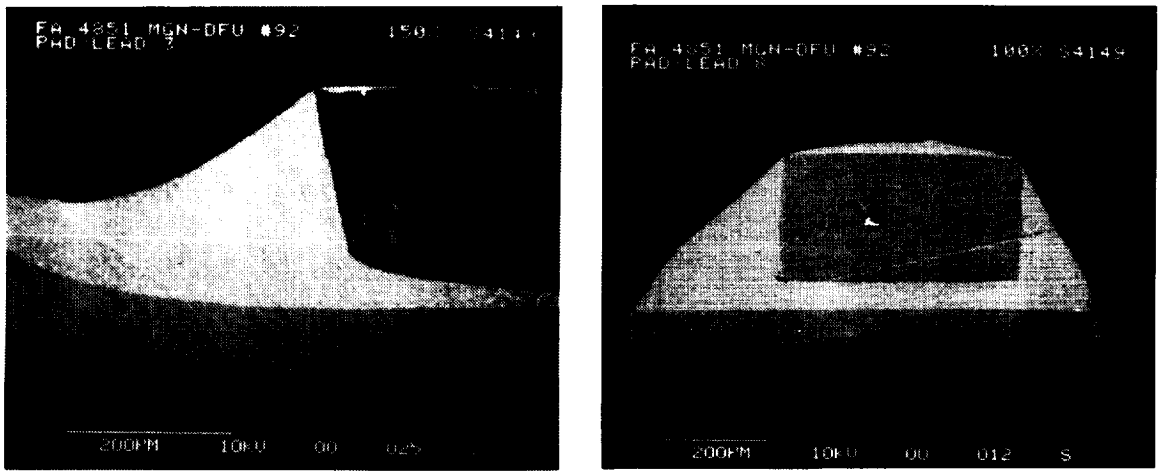


Fig. 6. SEM cross-sections showing excellent solder joints on opposite side (pins 3 and 8) of DFU part that failed open-circuit

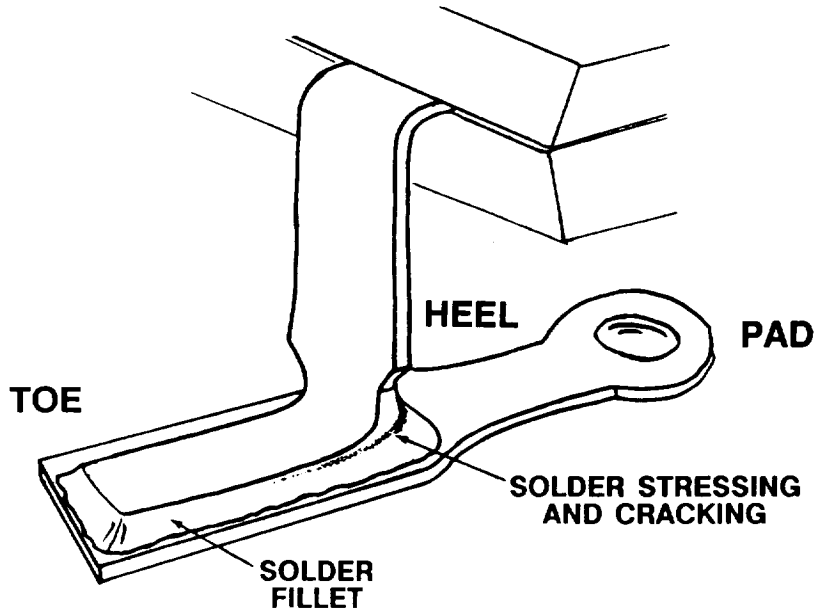


Fig. 7. Solder joint nomenclature

The detailed investigation of the failures demonstrated that **it was not the solder joints or soldering that was at fault, but was instead excessive mechanical loads applied to the solder joints** by conformal coating and heat-sinking materials located in the relatively large (0.050" to 0.080") gap between the DIP body and the printed wiring board (PWB). The principal damage mechanism was identified as **differential thermal expansion** of the gap material. Expansion of the gap material due to absorption of cleaning solvents was identified as a possible contributing factor. The solvent swelling issue is described in detail later in this publication under rework issues.

Among the various flight boards there were several gap filling materials and processes used [3]; these different materials and processes led to different levels of observed damage as noted in Table 1. The detailed compositions of the Solithane materials are enumerated in Table 2 and were carefully characterized during the course of the investigation [4].

Detailed technical descriptions of each of these constructions are reviewed below:

Clear Solithane (Beneath DIP) - As shown in Fig. 8, very severe stressing occurs when the large (0.055") gap beneath the DIP is completely filled with clear Solithane. Although the critical parameter is the very high coefficient of thermal expansion (CTE) of the Solithane (Fig. 9), the problem is further aggravated by the confining geometry of the gap beneath the DIP. This confined-space geometry prevents the lateral expansion of the Solithane and encourages it to grow vertically proportional to its volume expansion coefficient--this is three times the linear CTE. Further compounding the problem, there is some indication that the high-stress condition is aggravated by elevated-temperature ($140^{o}F$) curing of the Solithane, as opposed to room-temperature curing. Also, vacuum application during curing tends to draw Solithane into the gap; however, the vacuum is not implicated as having any other effect, good or bad. **The high level of stressing observed with this conformal coat application requires that more detailed procedures be developed to insure that confined spaces (such as the space under DIPS) not be filled with Solithane during the conformal coating operation; simultaneously the procedures must assure that complete coverage is achieved of the active circuit elements under the part.**

Pre-applied Alumina-Filled Solithane - Very severe stressing occurs when a bead of alumina-filled Solithane is applied beneath the part prior to part placement and soldering--even with no clear-Solithane over-coat. This mounting configuration, shown in Fig. 10(a), is the one that was used with the part that failed at KSC. A particularly stressful aspect of this mounting approach is the fact that the pre-application of the Solithane, prior to soldering, requires that the Solithane be exposed to the high part temperatures that can occur during soldering, and be exposed to multiple applications of solder-flux cleaning solvents. There is also evidence that this filled Solithane expands slightly when cured, perhaps due to the presence of, or generation of entrapped gas in the Solithane [4]. Fig. 11 shows the foamy nature of this material as it was found under the failed

Table 1. Level of Solder Joint Stressing After 24 Thermal Cycles from -25 to +100°C versus DIP Gap-filling Material

GAP MATERIAL	LEVEL OF SOLDER STRESSING
Clear Solithane Only	Severe
Pre-applied Alumina-Filled Solithane	Severe
Post-applied Alumina-Filled Solithane	Unknown (Not Severe)
G-10 Fiberglass Spacers	Severe
Alumina Ceramic Spacers	Modest
Copper Heat Sinks	Modest
Alumina-Filled Polysulfide	Slight
Radiation Shields	Slight
Interface Transformer	Slight
No Solithane Under Part	None

Table 2. Composition and Formulation of Clear and Alumina-Filled Solithane*

CLEAR, UNFILLED VERSION FOR CONFORMAL COATING

Ingredient	Type	Parts-by-Weight
Solithane 113	Resin	100
C113-300	Catalyst	74
T-12	Accelerator	.036

Cure Schedule: 3 hours at Room Temperature, plus 3 hours at 140°F

AL_2O_3 FILLED VERSION FOR THERMAL CONDUCTIVITY

Ingredient	Type	Parts-by-Weight
Solithane 113	Resin	46
C113-300	Catalyst	35
T-12	Accelerator	.036
Al_2O_3	Filler	154

Cure Schedule: 24 hours at Room Temperature

* Solithane 113 and Catalyst C113-300 are marketed by the Morton Thiokol Chemical Division.

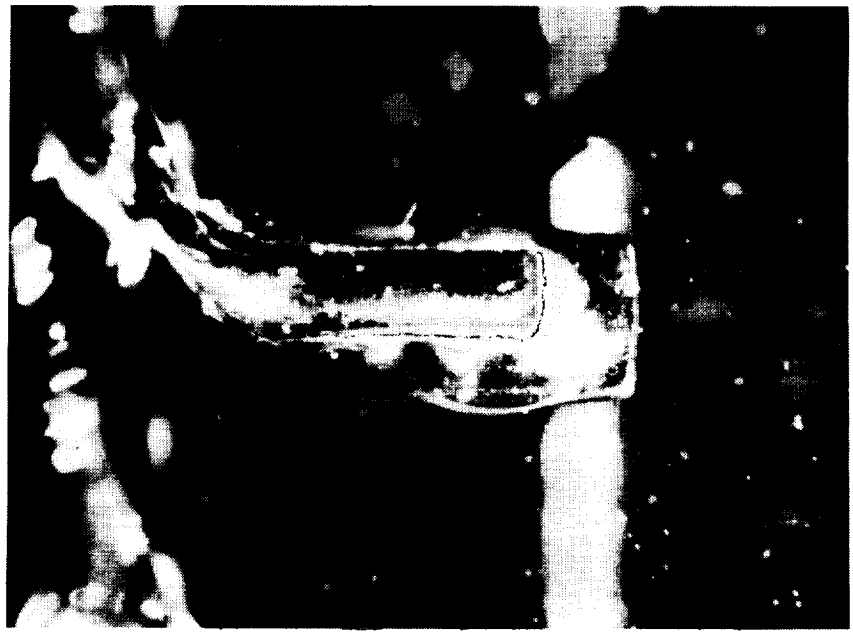


Fig. 8. Typical solder-joint failure caused by clear Solithane in space between DIP and PWB

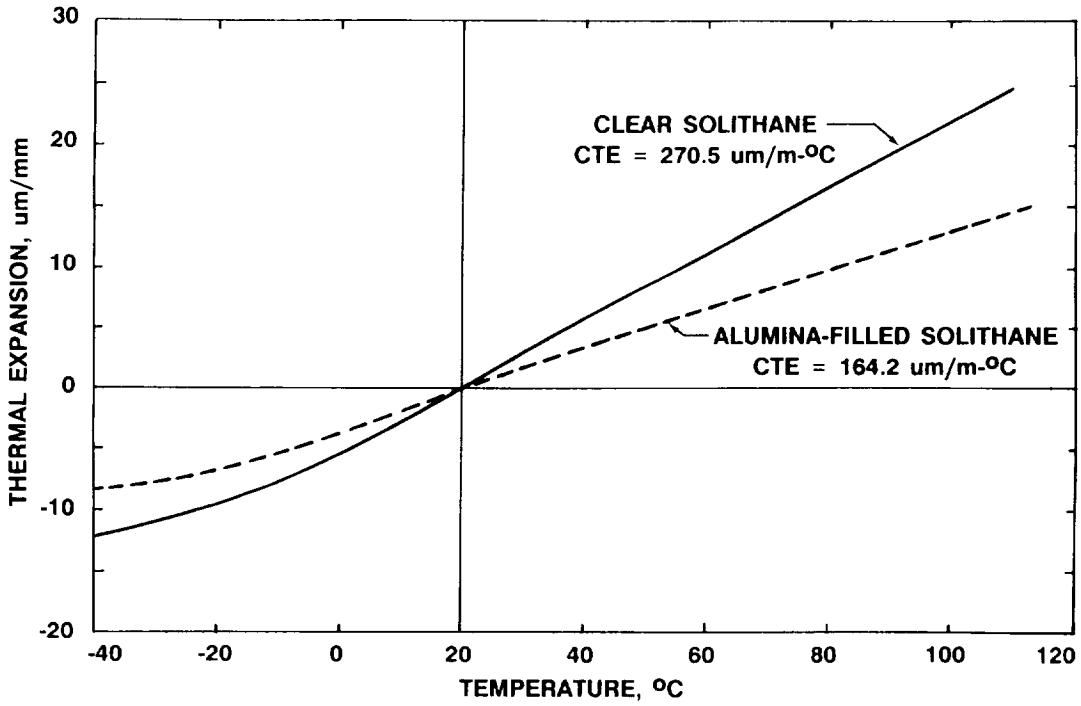
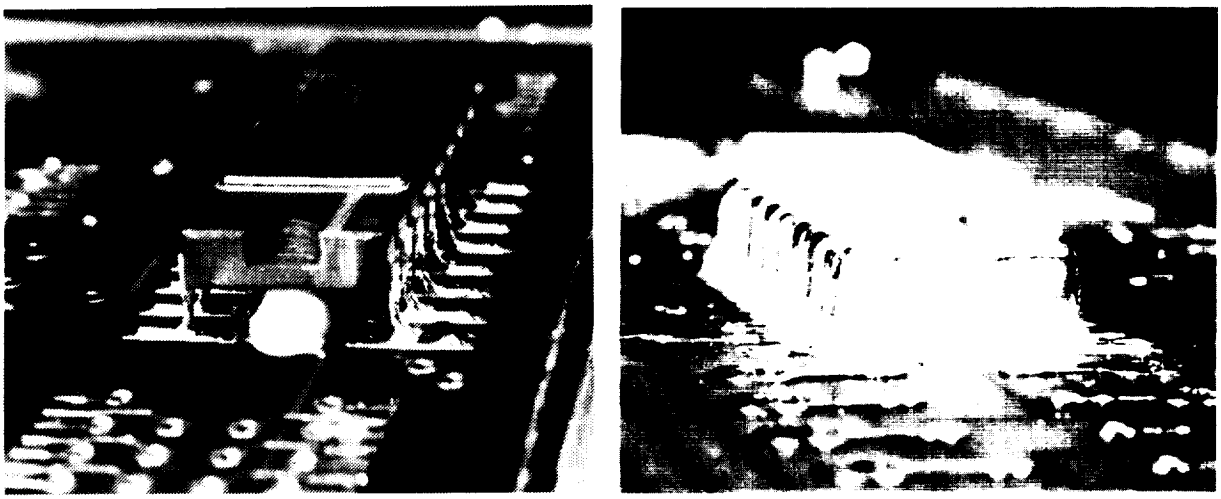


Fig. 9. Thermal expansion versus temperature for clear and alumina-filled Solithane



(a) Pre-applied (b) Post-applied

Fig. 10. Typical DIP configuration with part-board gap filled with alumina-filled Solithane for improved part heat sinking

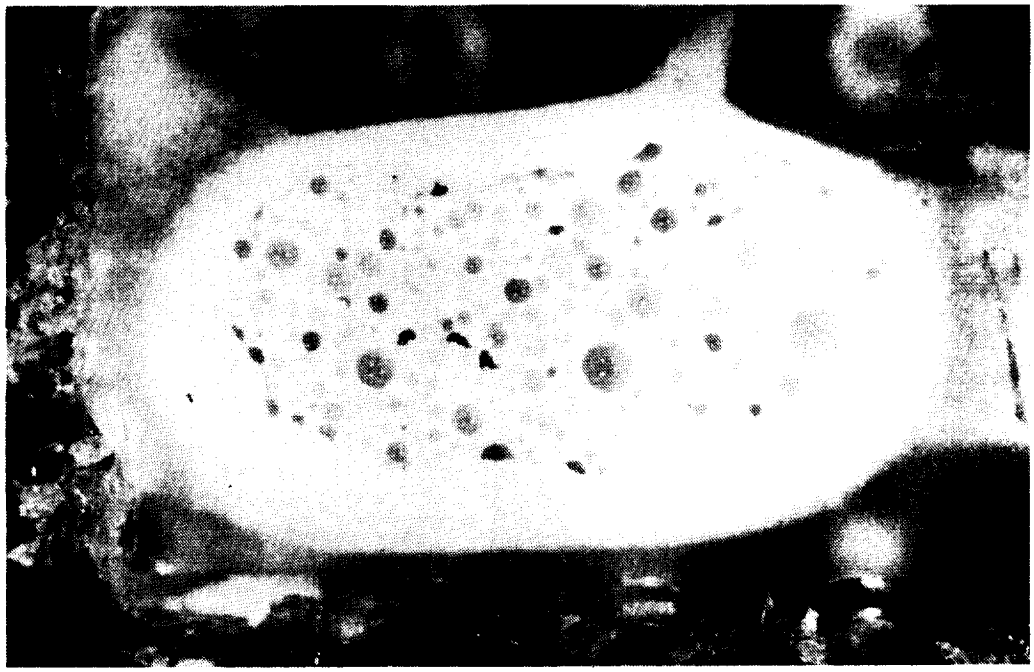


Fig. 11. Foamy nature of alumina-filled Solithane under flight DIP

flight part. Although it was determined that most of the observed foaming is due to air entrapped during mixing, entrained moisture (either adsorbed from the air during mixing, or desorbed from the alumina filler powder) can cause a chemical reaction with the Solithane that produces CO_2 gas evolution similar to that in a rising cake [4]. Although this application technique leaves the solder joints easily inspectable, which was the reason behind its original choice, **the high level of stressing associated with this process as it is presently implemented makes it unsuitable for further use.**

Post-applied Alumina-Filled Solithane - No severe stressing (no stress visible in the toe region) was found in those cases where alumina-filled Solithane was post-applied after the DIP is soldered to the board and cleaned. However, the Solithane invariably covers a large fraction of each solder joint, as shown in Fig. 10(b), making inspection of possible heel stressing impossible; in addition, cleanup and removal of excess Solithane prior to curing generally scratches the solder fillets (the filled Solithane is very abrasive) so that inspection of solder stressing elsewhere on the joint is also difficult. Despite the difficulty of inspection, this post-soldering application of alumina-filled Solithane appears to in fact lead to lower solder stress levels than either the clear Solithane, or the pre-applied alumina-filled Solithane. The lower stress than the clear Solithane is most likely attributable to the lower CTE of the alumina-filled Solithane, as noted in Fig. 9, and the fact that room-temperature curing was always used with this material.

The lower stress than the pre-applied alumina-filled Solithane is not well understood, but probably relates to the fact that the post-applied material is not exposed to the part-heating and solvent-cleaning of the soldering process. It is also probable that the excessive Solithane covering the solder joints slows the rate at which solvents can be adsorbed in the critical space directly beneath the part during rework, and may prevent later applications of clear Solithane from entering cracks under the heel of the solder joints. Although the exact role of Solithane in the heel cracks is unclear, there is strong suspicion that this material is a major contributor to the failure mechanism, not just a passive indicator of when the crack occurred. In short, the application of alumina-filled Solithane covering the leads may result in protecting the part from damage caused by nearby rework (reapplications of solvents and conformal coat).

Continued use of this DIP mounting method is discouraged until further research can clarify its uncertain reliability and improve its inspectability.

G-10 Fiberglass Spacers Beneath DIPs - The level of stressing with this construction was quite high, reflecting the relatively high CTE of the G-10 board (70 uin/in-^{o}C) in the direction normal to the glass-fiber plane. This construction is also exposed to heating during soldering, and is subjected to multiple solder-flux cleaning solvent applications. **Its use should be discontinued.**

Alumina Ceramic Spacers Beneath DIPS - The level of stressing observed with this construction was modestly high--a surprise in light of the desirably

low CTE of the alumina material. However, the observed stressing tends to propagate only slowly along the foot, and then to stop short of the toe region--even after prolonged thermal cycling (see Fig. 12). This is probably due to the more limited total strain (stroke) associated with the fact that there are only 10 to 20 mils of clear Solithane in the alumina-spacer stack-up. The fact that the entire stackup is heated during soldering, and then subjected to multiple solder-flux cleaning solvent exposures, may account for the modestly high level of stressing observed with this mounting approach. **This construction technique is considered marginal, but acceptable for flight environments with minimal thermal cycling. Research should be carried out to further reduce the modest levels of observed stressing with this construction.**

Copper Heat Sinks beneath DIPs - This construction, shown in Fig. 13, behaved almost identically to the alumina spacers--modest stressing with the stress propagating along the foot, but generally stopping short of the toe region. **Like the alumina spacers, this construction technique is considered marginal, but acceptable for flight environments with minimal thermal cycling. Research should be carried out to further reduce the modest levels of observed stressing with this construction.**

Pre-applied Alumina-filled Polysulfide under DIPs - Some of the Magellan radar boards manufactured by Hughes Aircraft used this construction. Although this material has a CTE similar to that of alumina-filled Solithane (133 uin/in-^{o}C) [4], the solder joints exhibited no significant signs of stressing. Possible explanations include the fact that trichloroethane and Freon vapor-degreasing were not used for solder flux cleaning on the tested boards, and/or it is likely that the polysulfide material shrinks somewhat during curing--this would preload the solder joints in compression and greatly minimize the chance of tension-induced solder joint cracking.

Radiation Shields - This construction, shown in Fig. 14, exhibited no significant solder-joint stressing, i.e. it was similar to the post applied alumina-filled Solithane. Inspection of the solder-joint heels was obscured by alumina-filled Solithane that extrudes from beneath the package.

Interface Transformers - Interface transformers, shown in Fig. 15, are packaged in a special 16-pin DIP with a different high-compliance lead bend as compared to conventional IC DIPs. As a result, the package sits much closer to the board (only 0.020" to 0.030"gap) and can accommodate some vertical (normal to the board) motion. Although heavy stressing of end leads (typically pins 1, 8, 9 or 16) was sometimes observed, the problem could not be reproduced in testing. Most flight interface transformers were found to be free of stressing. It is suspected that the random cracking of end leads with this construction may be caused by the manner in which the leads were held during soldering; it is well known that if leads are held down (elastically deformed) during soldering, they are likely to subsequently crack due to creep-rupturing of the solder under the applied spring load as the leads attempt to return to their unstressed position. This type of failure is generally of a random nature (individual isolated leads), and the crack generally initiates at the toe and progresses toward the heel.

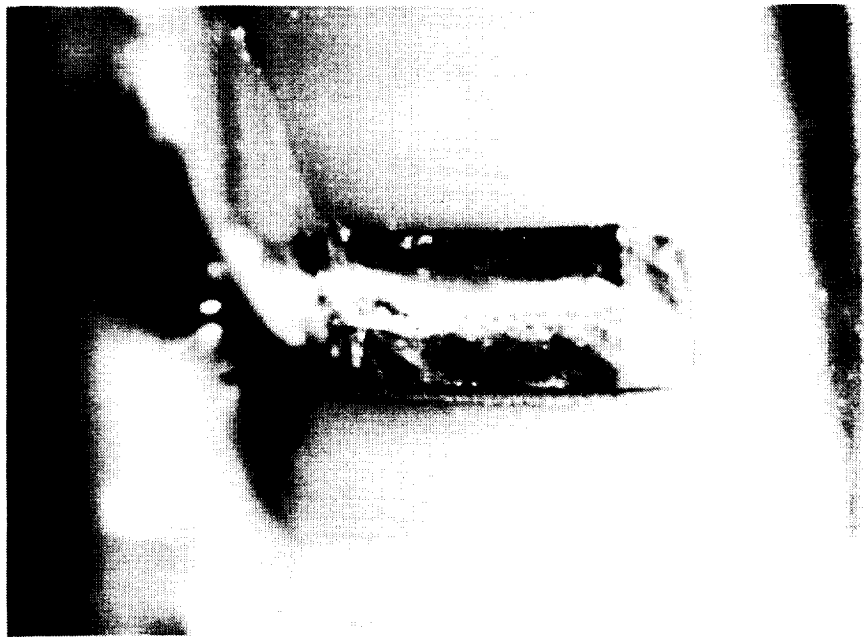


Fig. 12. Limited crack growth into toe region as generally observed with low-CTE spacers or copper heat sinks under DIPs

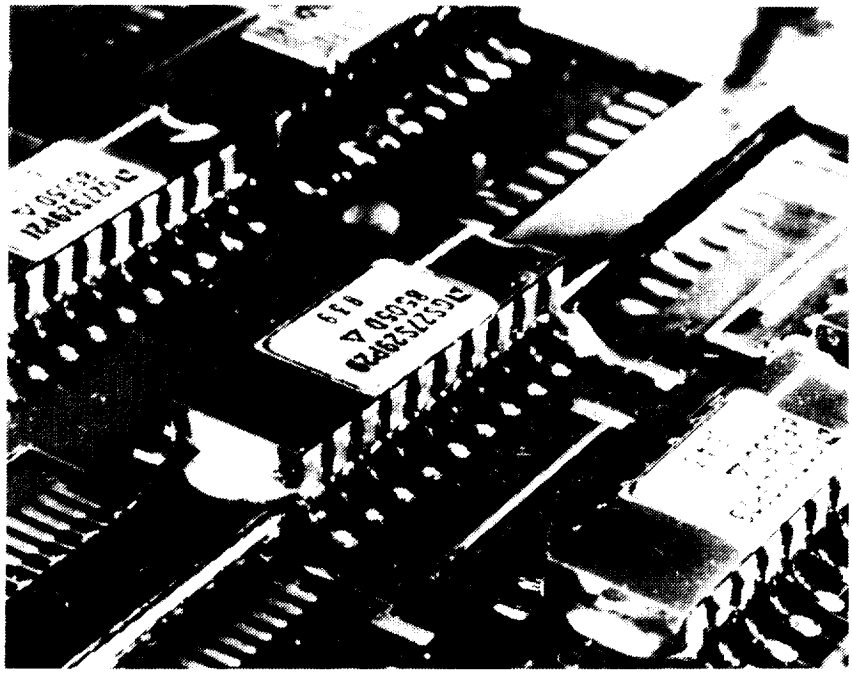


Fig. 13. DIPs mounted over 0.060" copper heat sinks

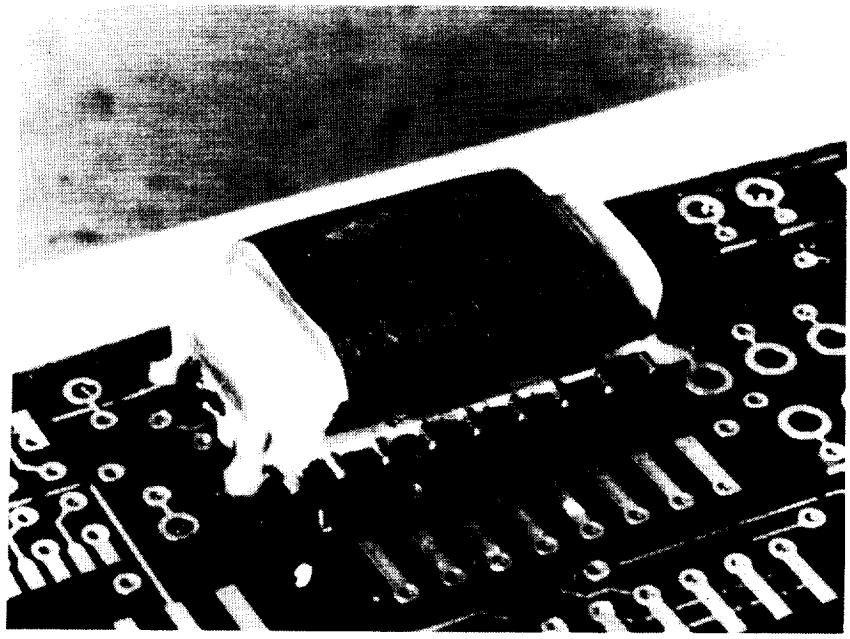


Fig. 14. DIP mounted with Tantalum radiation shield

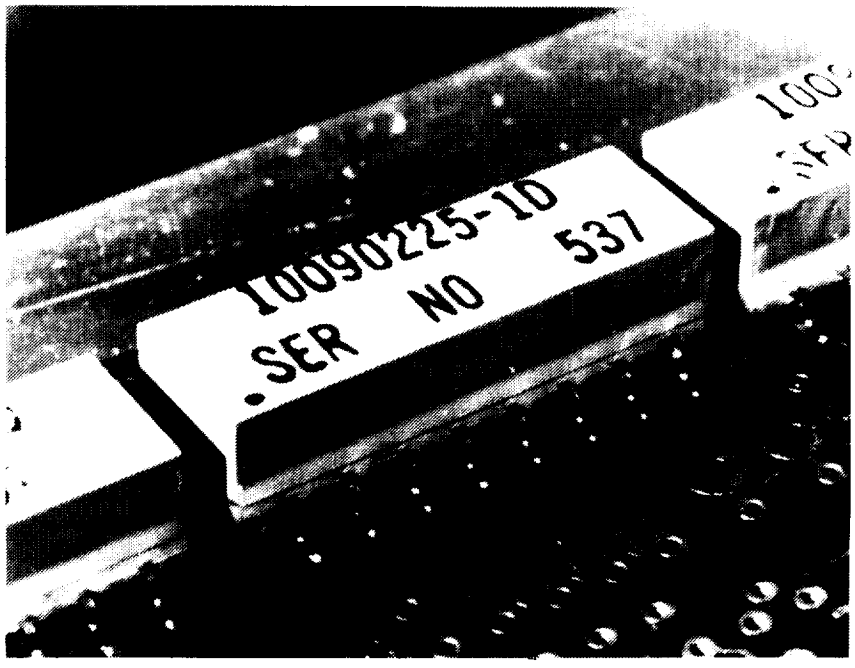


Fig. 15. JPL DIP interface transformer package

CANDIDATE SOLUTIONS TO PREVENT DIP SOLDER-JOINT FAILURES

Because the fundamental problem is solder-joint mechanical fatigue due to excessive strain cycling, the fundamental solution must involve reducing the level of mechanical strain generated in the solder joints. From the above discussions it is clear that this is not a simple task, for many variables play complex and synergistic roles in establishing the levels of applied strain. Solutions must be carefully defined in terms of exact sequences of operations, cure temperatures and times, cleaning solvent exposures, rework techniques, etc. It is not just a particular construction configuration that must be qualified, but an entire processing sequence including likely deviations such as operator-to-operator differences and anticipated rework scenarios.

An important first step is of course to minimize the strain by strictly limiting excessive thermal-cycle and solvent exposures. Once this is done, further improvements require fundamental design modifications in the way the DIPs are mounted. Candidate approaches range from removing the high-CTE material from beneath the DIPs, to accommodating the strain through the use of add-on stress relief loops. Whichever technique, or combination of techniques is adopted, the solution must be thoroughly tested and qualified, not only against the anticipated stress environments, but also against the likely variations in the processing variables.

The Tiger-team activity identified four broad classes of candidate design approaches to eliminate the mechanical fatigue failures:

Removing the high CTE Solithane from beneath the DIPs - Removing the Solithane from large confined spaces, such as from under the DIPs, and replacing it with a void, is a workable design alternative. The key problem with this technique is achieving a 100% conformal coating of the electrical leads and PWB conductors under the component. Thin brush or spray coating has been demonstrated, but is time consuming and difficult to inspect. This technique is also not compatible with high levels of heat transfer from the part.

Replacing the high-CTE Solithane with a low-CTE, high thermal conductivity material - This option is ideal from the point of improved heat transfer and low strain, and encompasses two of the mounting approaches currently in use: alumina spacers and copper heat sinks. However, additional research is needed to understand and correct the modest stressing observed with these designs. For example, similar boards manufactured by Hughes Aircraft with aluminum heat sinks and polysulfide adhesive did not exhibit any detectable solder-joint stressing.

Add a material that shrinks slightly beneath the part so as to draw the part toward the board and preload the solder joints in compression - This is only a conceptual solution that requires considerable research and study. The controlled-shrinkage material should provide both the necessary voltage isolation and heat transfer functions, as well as preload the solder joints in compression. However, its modulus must be low enough, and its bond

strength high enough to prevent delamination; at the same time, the bond strength must be weak enough to allow easy rework and not to cause damage to the part under any environmental extremes. The Hughes thick (0.080" to 0.090") alumina-filled polysulfide material may fall into this category.

Add mechanical flexibility in the component leads so that vertical motion due to applied loads is accommodated as strain in the leads, not in the solder joint - This alternative has been explored by many other organizations--examples of typical strain relief configurations are illustrated in Fig. 16. This technique has a proven success record, but requires extensive modification of the as-delivered DIPs. Dead-bug mounting also falls into this general category. For high-heat-transfer applications, the flexible leads must be combined with a high thermal conductivity heat-sink material.

SOLUTIONS IMPLEMENTED ON MAGELLAN AND GALILEO

For the Magellan and Galileo flight hardware, the chosen solution was to totally rework all DIPs that had clear Solithane, pre- or post-applied alumina-filled Solithane, or G-10 fiberglass spacers beneath them. All material was removed from beneath these parts except for a thin non-filling coat of clear Solithane to shield circuit elements. On one board the original Solithane was left beneath the parts, and hay-wire stress relief loops (shown in Fig. 17) were added to the DIP leads to accommodate the vertical motion resulting from Solithane swelling. Although the hay-wire approach did not require removal of the parts from the boards, it was found to be extremely labor intensive and was abandoned after a single board. Extensive testing demonstrated that both approaches were excellent solutions to the problem (neither had any significant solder-joint stressing after 110 cycles from $-25^{o}C$ to $100^{o}C$) [5]. However, both techniques were very labor intensive and difficult to inspect.

For DIPs with the other mounting configurations (alumina ceramic spacers, copper heat sinks, radiation shields, and interface transformers) the decision was to use as is. This decision was based on: 1) extensive testing that demonstrated that heel cracks propagate only slowly into the toe region of these constructions, 2) the fact that the flight hardware only exhibited solder joints in the early stages of cracking (1/4 the distance from heel to toe), and 3) the fact that the flight boards containing these DIP constructions had already experienced as much as 90% of the total thermal cycle exposure that the boards would see by the end of mission (See Table 3 and its accompanying discussion in Section 3).

Other Magellan radar boards, manufactured by Hughes Aircraft, used alumina-filled polysulfide or aluminum heat sinks under the DIPs. These parts exhibited no visible stress during thermal-cycle testing and were also used as is.

Although workable fixes were developed and successfully implemented as part of the Tiger-team activity, **there is a clear need for improved DIP mounting techniques in the future.**

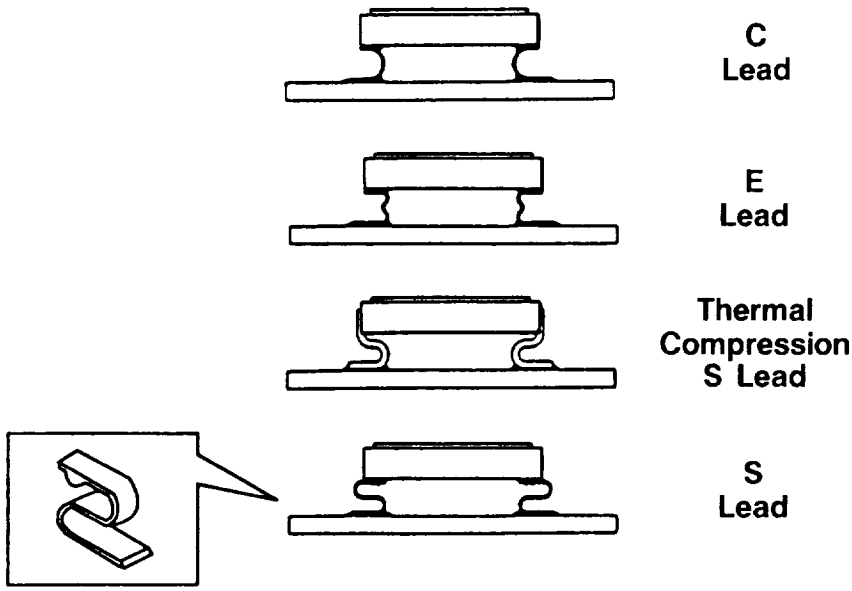


Fig. 16. Candidate strain relief modifications for DIP packages

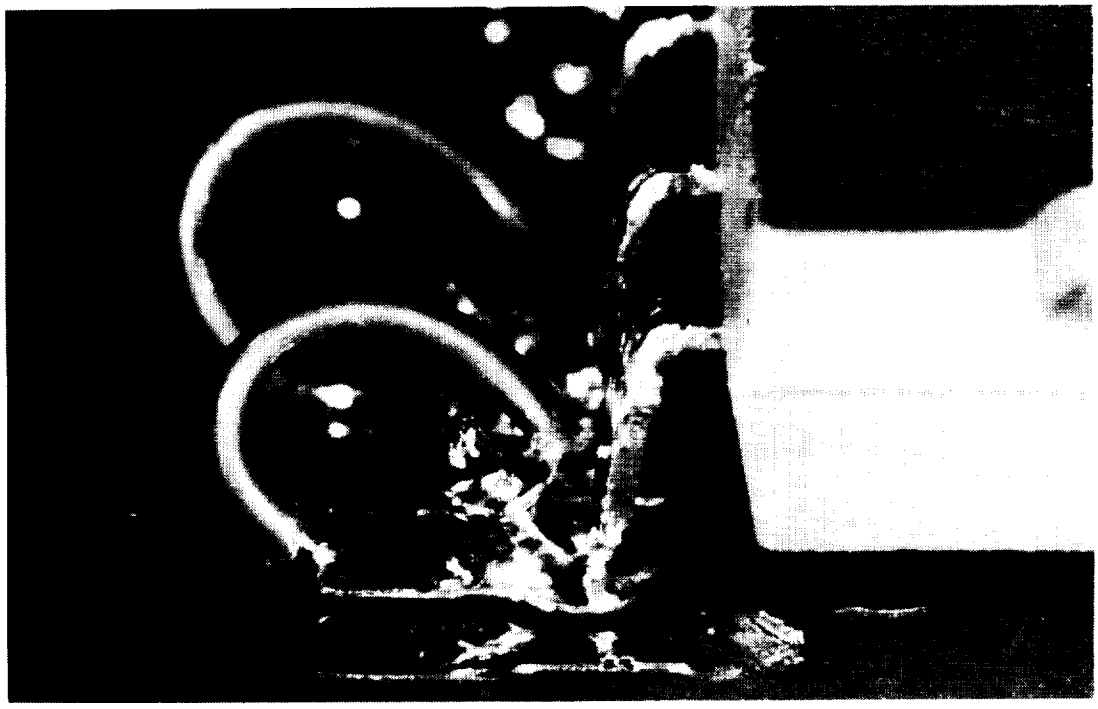


Fig. 17. Application of hay-wire strain relief loops on Magellan DIPs

SECTION 3

PACKAGING DESIGN AND VERIFICATION PROCESS DEFICIENCIES

The fact that the extensive solder-joint cracking occurred and was not caught until system level testing at the Cape suggests that important deficiencies exist in the basic design, testing, and inspection processes being applied to electronic packaging. Over the past year, similar failures occurred in the CDS edge-clip solder joints, and in DFU PROM solder joints [6,7]. This section divides these issues into three broad categories: Thermal-cycle Fatigue Issues, Part Temperature Control Issues, and Inspection Issues.

THERMAL-CYCLE FATIGUE ISSUES

The common thread among these problems is that they all involve solder joint failures due to excessive differential expansion forces from mixtures of high- and low-CTE materials. At this point the nature of the mechanism is well understood--it is classical metal fatigue combined in many cases with long-term creep rupture.

Figure 18 presents representative fatigue-life data for 63-37 SnPb solder joints taken from IBM test results [8]. The plot illustrates the typical dependency between cycles-to-failure and the level of mechanical strain introduced into the solder joint. Such a mechanism is called an accrued damage mechanism because failure occurs after a number of strain cycles have been accumulated. Note that the level of damage (number of cycles to failure) is an extremely strong function of the strain level. Doubling the strain (for example doubling the Solithane thickness) can reduce the fatigue life by nearly an order of magnitude.

In most electronic packages, the principal strain in solder joints is caused by differential expansion between the part and its mounting environment due to temperature gradients between the part and the board and/or due to changes in temperature (thermal cycles). Because the strain is generally linearly dependent on the temperature swing, solder joint fatigue test data can be equally well plotted as cycles-to-failure versus temperature swing (T). Figure 19 presents example temperature-cycle data gathered by TRW on actual electronic circuit board solder joints [9]; note that these data exhibit the same characteristic log-log slope for solder as the IBM data in Fig. 18. The proportionality between T and strain in these two plots describes the level of strain being introduced into the TRW solder joints by the temperature cycling. In general, this strain- T proportionality will vary from design to design, reflecting the degree of CTE matching, and/or the level of stress relief obtained from stress-relief features such as flexible metal connections between the electronic components and the PWB.

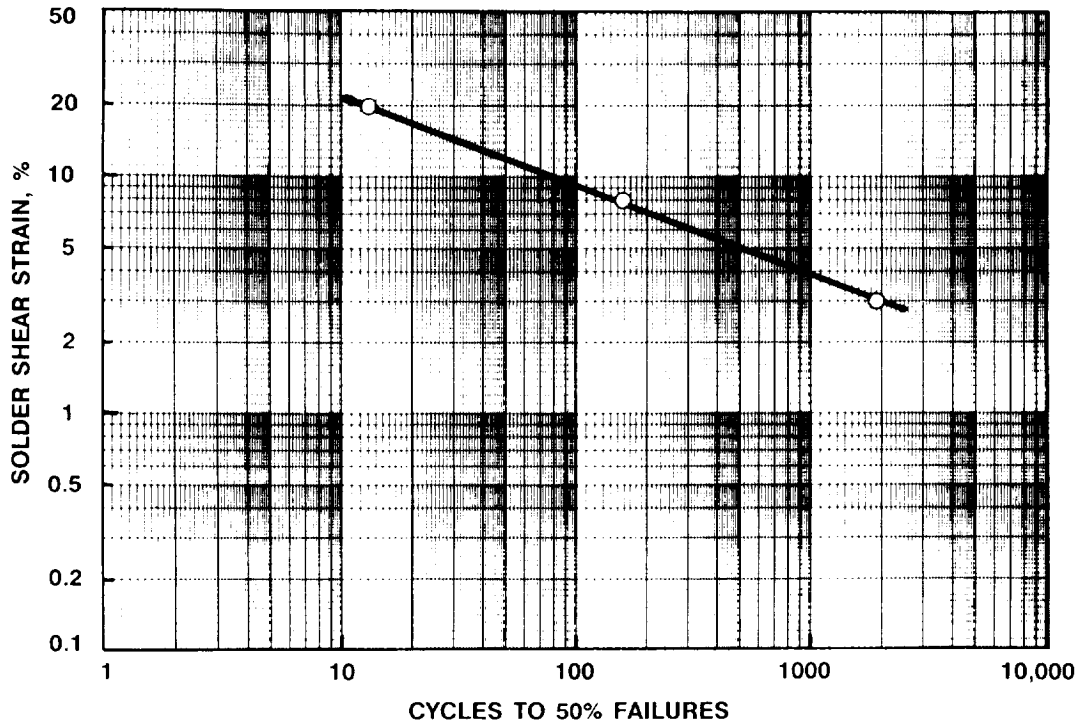


Fig. 18. Solder-joint fatigue life versus cyclic strain level at 25°C (IBM data using 15 minutes per strain cycle [8])

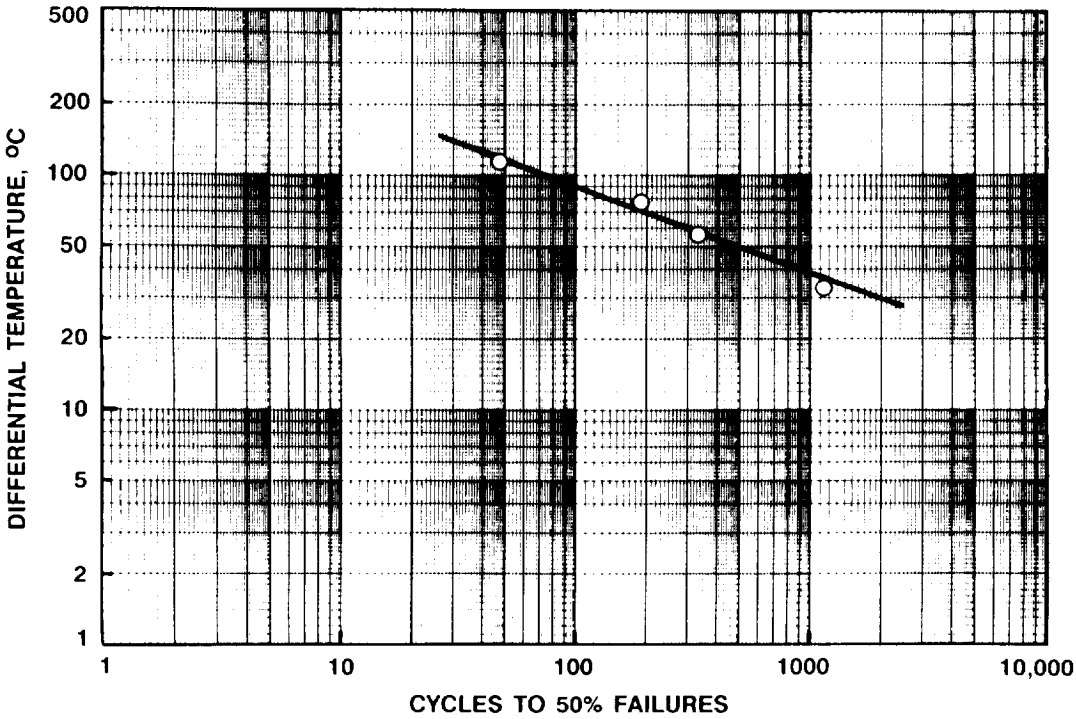


Fig. 19. Example solder-joint fatigue life versus temperature cycle depth (TRW data for Solithane encapsulated parts [9])

Because this characteristic strain-cycle slope of the solder fatigue curve is invariant, one can readily establish a fatigue tolerance requirement for any given electronic packaging flight application. This is done based on the total number of temperature cycles the hardware is expected to see of various cycle depths during both **ground testing** and the flight mission. Figure 20 represents an example electronic packaging fatigue requirement for a hypothetical ground/mission environment equivalent to 2500 cycles with a 15°C temperature swing. Packaging designs with a fatigue performance above the line are adequate for this application--those below the line are inadequate.

When establishing the level of fatigue endurance of an electronic packaging concept it is most economic to use a thermal-cycle test with a relatively deep cycle; this minimizes the number of cycles that must be run. For example, the thermal cycle requirement in Fig. 20 is equivalent to 10 cycles with a depth of 125°C--this is easily implemented by cycling between -25°C and +100°C, thus avoiding both unrealistic environments significantly below the Solithane glass-transition temperature at -15°C, and elevated temperatures above 100°C, where solder strength decreases precipitously.

Such a cycle, shown in Fig. 21, was used extensively during this Tiger-Team effort to quantify the fatigue resistance of the various packaging DIP mounting techniques contained in the flight hardware, as well as alternatives proposed as fixes. Note that the cycle shape contains a significant (2 hour) dwell at 100°C to accelerate creep-rupture failures, and turns around quickly at -25°C, where creep is negligible, to conserve test time. The ramp rate between extremes is chosen slow enough to negate thermal shock effects caused by excessive thermal gradients.

RECOMMENDATIONS FOR IMPROVED FATIGUE ENDURANCE

Although the issues of solder-joint fatigue and creep-rupture were fully incorporated into the recent packaging failure analysis and fixes, the fact that the recent failures occurred suggests that there is need for broader understanding and incorporation of these principles into the flight design and verification process. An important element of the problem is the fact that the failure mechanism is an accrued damage mechanism; thus the hardware's tolerance to thermal-cycle environments should generally be tested on flight-like hardware that is <u>not flown</u>.

Figure 22 illustrates the flight mock-up test boards that were used during the Tiger-team investigation to evaluate the many part and material combinations that required examination. These were fabricated with flight-reject boards bonded to rigid 1/2"-thick aluminum substrates to duplicate the actual pad heat-sinking and board thermal expansion characteristics as well as possible.

Because solder joint failures of the type encountered tend to be generic, affecting many similar parts in various subsystems, it is critical that generic flight qualified design approaches be developed off-line, prior to building and testing the flight hardware. It is also very important that

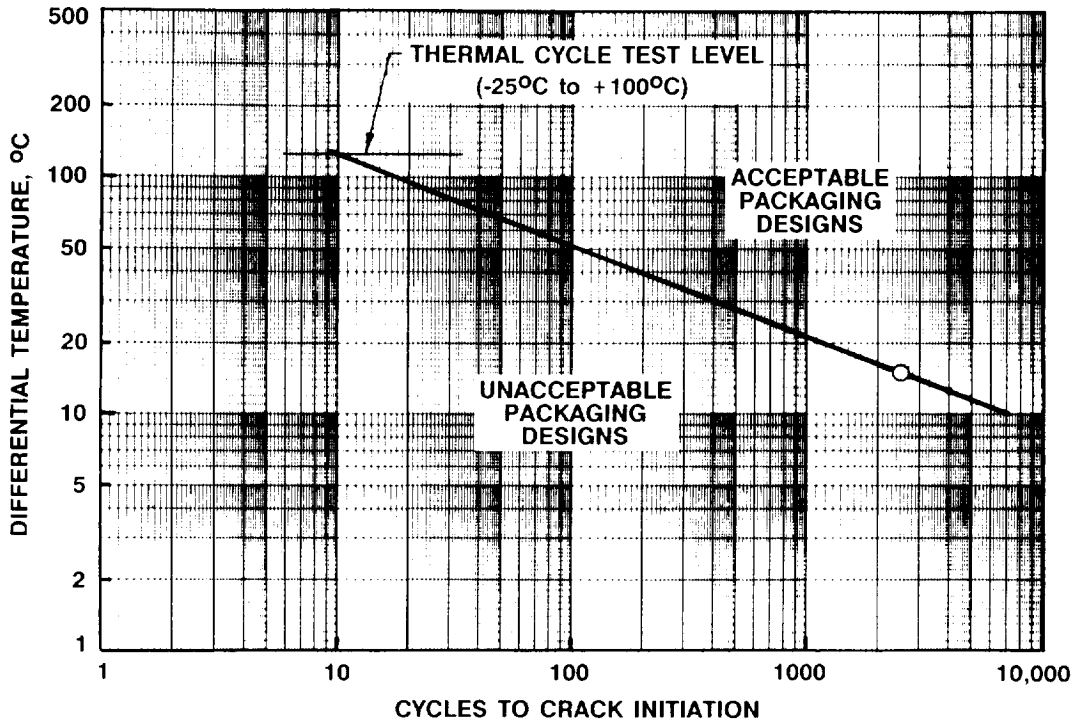


Fig. 20. Example solder-joint thermal-cycle fatigue-life requirement for a spacecraft electronic package

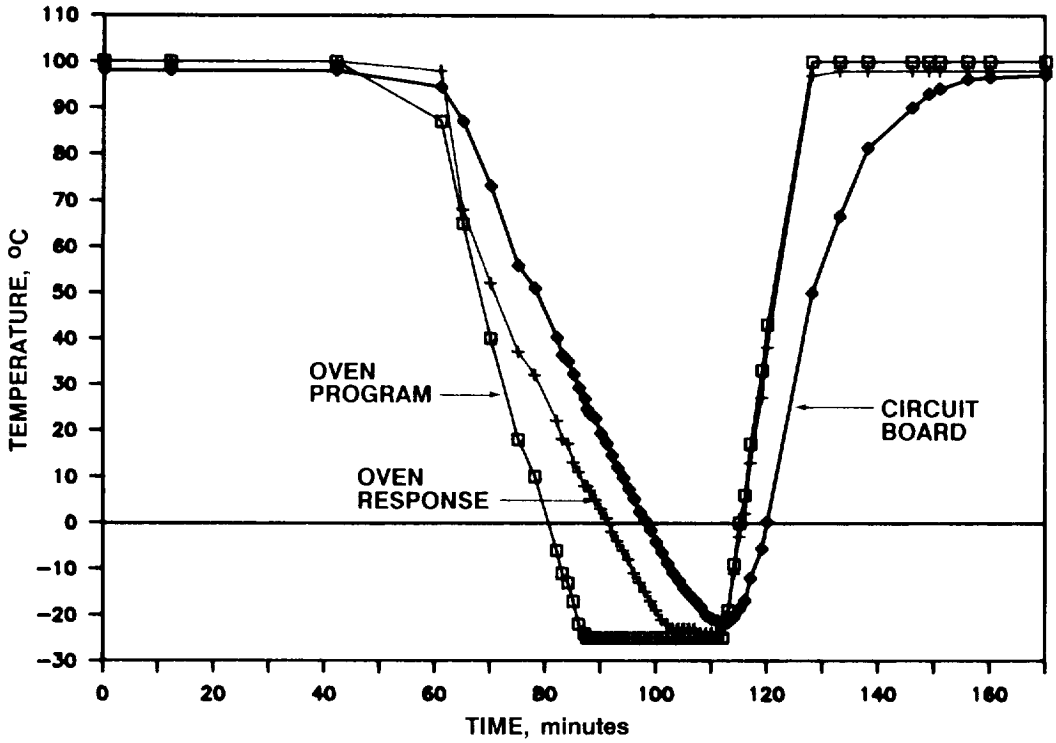


Fig. 21. Thermal cycle used to characterize and qualify Magellan and Galileo solder-joint fixes

Table 3. Example Thermal-Cycle Exposure for Magellan Flight Electronics

Cause of Temp Cycles	Temp Cycle ΔT (°C)	Number of ΔT Cycles	Cycles* to Failure Ratio (15°C vs ΔT)	Equivalent Number of 15°C Cycles	Percentage Exposure per Environment
Qual Tests	85	9	91.55	824	33
Qual Tests	65	8	45.53	364	15
Thermal Tests	50	1	23.00	23	1
Thermal Tests	40	1	12.86	13	1
Oven Curing	25	25	3.78	95	4
On/Off Testing	15	1075	1.00	1075	44
Flight Mission	3	4000	0.0151	61	2
			TOTAL	2455	100

* $\text{Ratio} = \frac{\text{Cycles for equal damage at } 15^{\circ}C}{\text{Cycles at } \Delta T} = \left(\frac{\Delta T}{15}\right)^{2.6}$

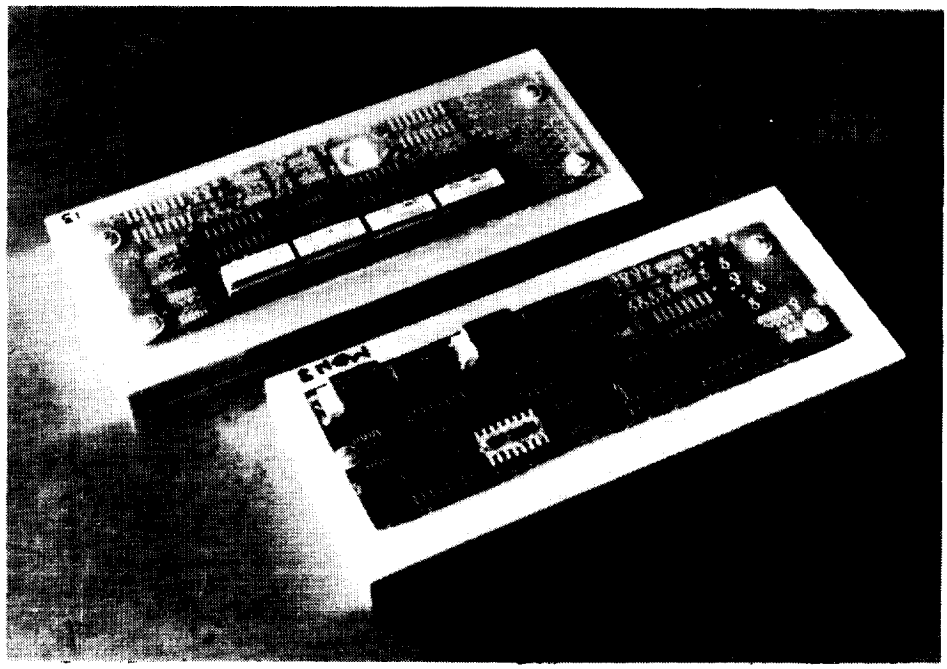


Fig. 22. Mockup printed wiring boards used for thermal cycle testing

generic multi-mission thermal-cycle endurance requirements be established to guide the development process and allow generic design approaches to be developed for a whole class of likely applications. There are far too many part-specific electronic packaging technologies to be able to qualify each one for each mission.

Even for subsystems with minimal mission thermal-cycling environments, the ground test environment presents a significant stress level. As an example, Table 3 articulates the relative levels of thermal-cycle stress applied to recent Magellan attitude control boards by the functional testing and proto-flight qualification program as compared to the projected flight environment [10]. Note that the pre-flight test environment is 50 times as stressful as the projected mission environment. **The need for this extensive testing of flight hardware needs to be carefully examined, and where found necessary, needs to be thoroughly factored into the requirements for the electronic packaging design.**

PART TEMPERATURE CONTROL ISSUES

Another design and test issue surfacing during the investigation was that of controlling part junction temperature to meet Project derating requirements on maximum allowable temperature levels (typically 110°C to 125°C) so as to insure long-term reliability. This common industry-wide practice has excellent justification for controlling typical material degradation and semiconductor failure mechanisms that exhibit Arrhenius temperature-rate dependencies. The standard practice is to insure that junction temperatures remain below 125°C under realistic worst-case long-term operating conditions. Keeping the part temperature low also reduces the level (depth) of thermal cycling if the electronics are subjected to on/off cycling.

At issue is the observation that the manner in which the design and specification process is being conducted is leading to considerable conservatism in the actual operating temperatures obtained. Unfortunately, the design conservatism in this area may lead to unacceptable levels of risk with respect to other failure mechanisms, such as solder-joint fatigue stress, that have no design requirements.

During the Tiger-team activities it was necessary to assess if the Solithane could be safely removed from beneath the DIPs without causing excessively high temperatures. This led to a detailed analytical and experimental testing program to accurately quantify and verify the part temperatures under anticipated flight operating conditions [11,12]. Fig. 23 displays the thermal test mockup that was assembled using flight-like parts and board components, and was specially instrumented with 36-gage thermocouples and 30-gage Constantan wire to power the individual DIPs. The detailed results of the study, documented in Refs. 11 and 12, are summarized in Fig. 24.

Examination of Fig. 24 reveals that the rework design with no Solithane under the parts has excellent margin; the predicted junction temperature is only 55°C for the expected flight baseplate temperature of 30 to 35°C, and is below 70°C at the maximum allowable flight baseplate temperature of 45°C.

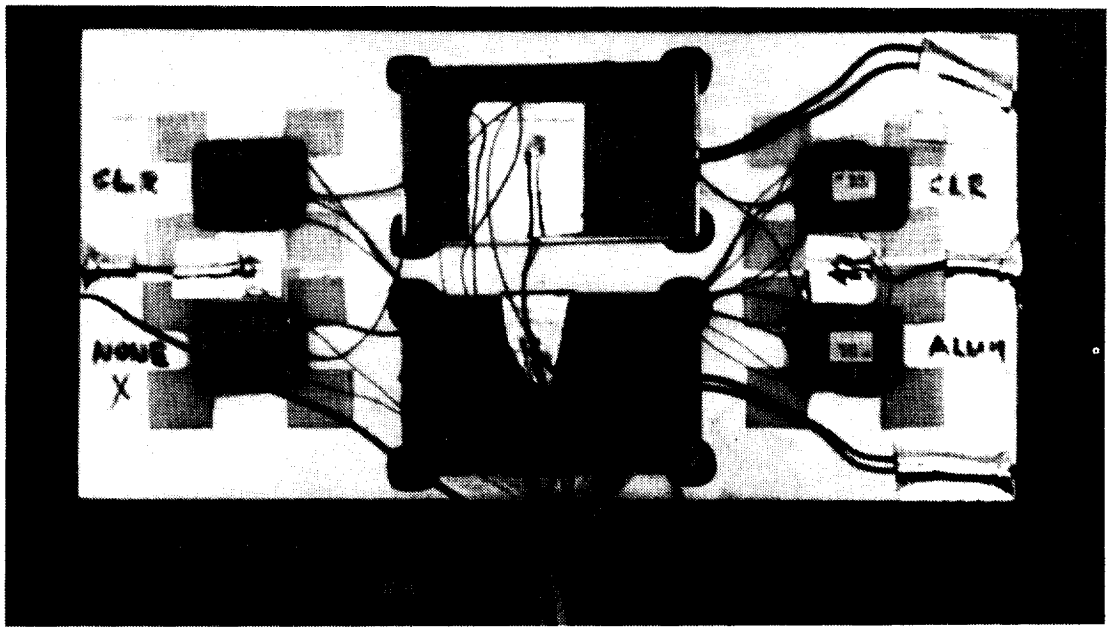


Fig. 23. Thermal test mockup of electronic-part-to-chassis thermal resistances

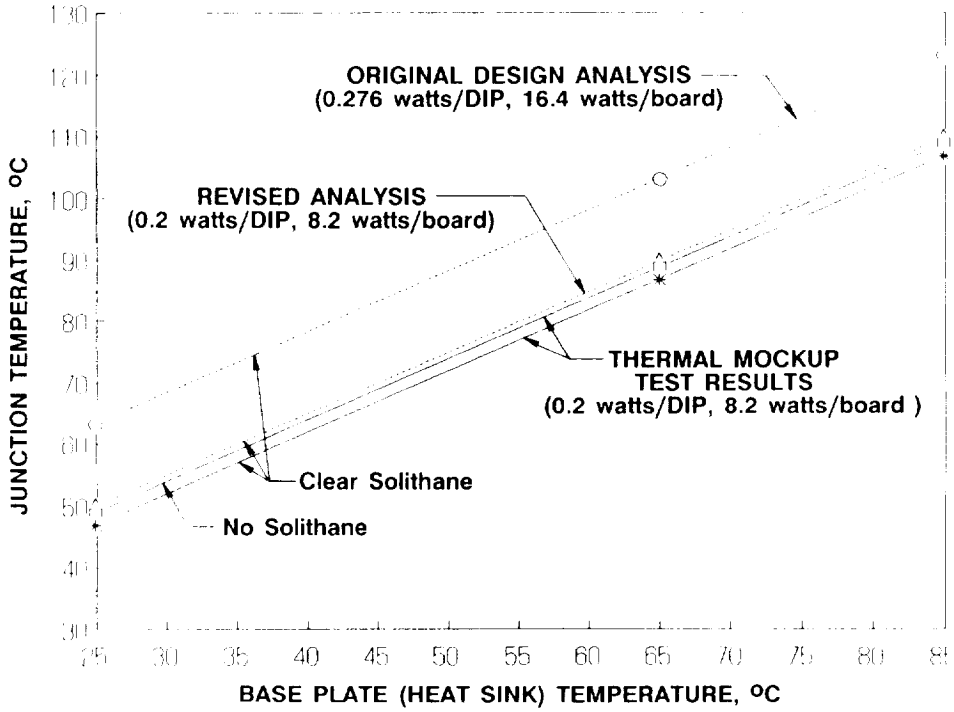


Fig. 24. Comparison of analysis and test data on DIP junction temperature in vacuum as a function of circuit board heat-sink temperature

The test data also demonstrate that the presence of clear Solithane beneath these parts only lowers the part temperature by 2°C (3°C for alumina-filled Solithane). This temperature reduction would increase proportionately for parts with higher power dissipations, or for parts such as flat-packs, which have much greater thermal resistance in their leads.

The largest difference between the original flight design analysis and the Tiger-team analysis is more accurate power dissipation estimates for both the part, and the total module (the module is the two back-to-back boards combined). The test and analysis data in Fig. 24 are based on a measured power dissipation for the module of 8.2 watts, compared to a previously assumed value of 16.4 watts, and a measured worst case part power dissipation of 0.2 watts for the optical isolator DIP (compared to 0.276 watts). Even the present 0.2 watt estimate is very conservative; it assumes a manufacturer's maximum 25 mA LED drive current and 100% duty cycle (fraction of time in the on state), as opposed to the flight application, which uses a 15 mA drive current, and a duty cycle closer to 50%.

RECOMMENDATIONS FOR IMPROVED THERMAL DESIGNS

From an overall systems point-of-view it is important to carefully moderate design conservatism where increased conservatism in one area leads to increased risk in another. Because packaging techniques that enhance part cooling often result in increased design complexity, it is important that design augmentations for improved heat sinking be thoroughly analyzed and tested, and be carefully balanced with the risks associated with the increased complexity.

Two additional areas were highlighted by the Tiger-team activity as deserving improvement:

1. <u>There is need for more realistic electronic part power dissipation levels</u>. In many cases manufacturers' maximum power dissipation levels are used in instances where the actual circuit application limits the component power to a small fraction (1/4 to 1/2) of this maximum. The excessively conservative part power dissipations have a double impact: the first is in exaggerating the total power dissipation on each module (this exaggerates the predicted thermal rise of the overall board), and the second is in exaggerating the predicted board-to-junction thermal rise of the individual parts. **Realistic power dissipation levels need to be provided to the electronic-packaging and thermal-analysis personnel for both the overall board, as well as for any components requiring special thermal control treatment.**

2. <u>There is need for improved analytical tools and test data to allow improved estimation of part operating temperatures</u>. Thermal conductance data were found to be inadequate in several areas such as part lead conductances, PWB conductances and heat spreading, and Solithane conductances. Although the developed data allowed predictions that agreed with the experimental results within 1 to 2°C, improved data should be developed in additional areas.

INSPECTION ISSUES

The fact that the DFU solder joint fractures initiated prior to conformal coating, and therefore prior to qualification testing, but were not caught in inspection, prompted a detailed look at the inspection process. In general, flight electronic hardware that is assembled at JPL undergoes detailed inspection after every major process step or testing activity. Examples of process steps and tests that require inspections include:

- Component soldering
- Subassembly-level testing
- Rework or design change
- Component spot bonding
- Conformal coating
- Qualification testing

Historically, the focus of the process-related inspections has been limited to the particular element of the board that was the subject of the latest process step; thus, among the process inspections, the only one that critically examined the solder joints was the inspection immediately following the soldering operation. Following conformal coating, none of the inspections dwelled on the solder joints because of the poor visibility caused by the optical distortion and reflections from the coating material. The heel fillet is particularly difficult to inspect, as it can only be viewed indirectly from the side at an angle of approximately 80^{o}.

Another complicating factor was that prior to the recent Magellan/Galileo solder cracking problems, JPL did not have inspection criteria for visual stress in solder joints. Experience over the Tiger-team activity has shown that stress, if it exists, is highly visible in shiny solder fillets, and is much more easily quantified than the presence of cracks; cracks in solder joints can be extremely difficult to see, even by a trained eye at 50x, unless either: 1) the crack is mechanically held open, or 2) the crack is substantially burnished around the edges through repeated open-close cycles. This cyclically burnished crack is unlikely to be visible until sometime considerably after the original cracking occurs.

It was found that cracks are particularly visible and easy to see when mechanically held open while the break is still fresh and sharply defined. This situation existed when boards were inspected at elevated temperatures, where the Solithane is in an expanded state. Test boards were readily inspectable when withdrawn from thermal cycling at the maximum ($100^{o}C$) temperature extreme. Cracks that were readily visible at $100^{o}C$ were often impossible to confirm after the board cooled to room temperature. Because of the extreme difficulty in quantifying the existence and extent of cracks, electrical means of identifying major cracks through significant solder joint resistance changes are presently under investigation at JPL. It is recommended that these development efforts be continued.

Because solder joints on flight boards are not easily inspected at elevated temperatures, they present a particularly challenging inspection problem.

The best indication of a possible partial crack appears to be the existence of severe stressing; the absence of stressing generally rules out the possibility of cracks.

During the Tiger-team activity, inspectors were further trained in the visual appearance of solder joint stressing and cracking using optical microscopes at 12 to 50 X to view examples of stressed and cracked solder joints, as well as with diagrams such as that shown in Fig. 7. In general, 12 to 30 X was found to be the most useful magnification level. A total of several thousand solder joints, ranging from pristine to severely cracked, were inspected over the two month activity period.

Because major questions sometimes arose in interpreting the visual observations, pull tests were conducted to quantify the relationship between the visual appearance of solder joints with various degrees of stressing and their pull strength. Good unstressed joints generally pulled in the range of 4 to 8 pounds, with weaker joints in the 2 to 4 pound range. Joints that pulled at 1 pound or less were considered unacceptable for flight and generally corresponded to ones that were visibly severely cracked. In rough terms, joints that were visually similar to ones that pulled at loads of approximately 2 pounds or less were always reworked.

Looking back, it is clear that solder joints are both very difficult to inspect, and additional and improved means of inspecting solder joints are needed. It is particularly important to consider adding a thorough detailed inspection of the solder joints of flight hardware following qualification testing, and prior to delivery to system integration testing. This inspection would provide a critically needed screen for bad solder joints after completion of the hardware fabrication, rework, and assembly-level ground-testing phase. The environmental exposure associated with these activities plays a critical role in making visible marginal solder joints that are in the process of failing due to prolonged creep-rupture or cyclic fatigue.

SECTION 4

REWORK PROCESSING SENSITIVITIES

Although many of the recently observed packaging problems were directly associated with basic design and qualification deficiencies, several others were associated with rework processes and fixes. The rework process is particularly challenging because, by definition, it generally implies inventing spur-of-the-moment fixes to problems invariably encountered during the course of building and testing of flight hardware. The challenge is to fix the identified problem without causing another.

A particularly troublesome part of rework is that highly synergistic process steps such as soldering, cleaning and conformal coating are applied out of sequence, often in untested ways. A few of the most troublesome problem areas identified include:

SOLVENT/CONFORMAL-COAT INTERACTIONS

Normally, cleaning solvents such as Trichloroethane, Freon and Alcohol are applied only prior to conformal coating. This precludes negative interactions between the solvents and the polymeric materials. Unfortunately, in the rework setting, cleaning solvents are often required to be used after the conformal coat or heat-sink compound is applied and cured in place. During rework cleaning, the solvent will be adsorbed by any contacted polymeric material and cause the polymer to swell. The amount of swelling is very dependent on which solvent is used, and the length of solvent exposure. Fig. 25 illustrates the dramatic swelling of 5/8" cubes of clear Solithane after reaching equilibrium during room temperature immersion in the noted solvents: water, Ethyl alcohol, Freon TE and 1,1,1-Trichloroethane; Figure 26 presents quantitative data for the same cubes. Note that the alumina-filled Solithane exhibits a much faster time constant than the clear Solithane (probably because of its foamy porosity), but reaches a lower equilibrium level of swelling due to the presence of the alumina filler.

As might be expected in light of their much shorter time constant for diffusion, thin sections of Solithane are found to expand much more rapidly than these bulk samples. For example, 0.030" thick samples of clear Solithane reached 30% volume expansion in Trichloroethane in 5 minutes, and 10% volume expansion in boiling Freon TE (43^{o}C vapor degreaser) in 4 minutes [4].

It is clear from these experiments that Trichloroethane is extremely reactive with the Solithanes, and causes enormous swelling; under no circumstances should it be used in the presence of the Solithanes. Freon TE and Ethanol are much less reactive. Considering the fact that Freon

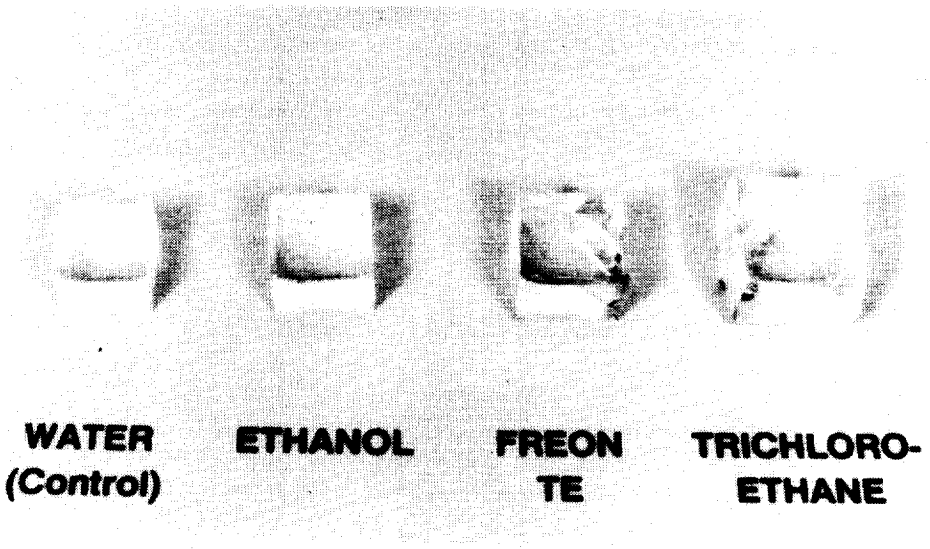


Fig. 25. Visual appearance of 5/8" clear Solithane cubes after immersion in solvents. Before solvent exposure, all cubes were identical in size to the cube labeled "control"--water immersion had no swelling action. After withdrawal from the solvent, the cubes return to their original size

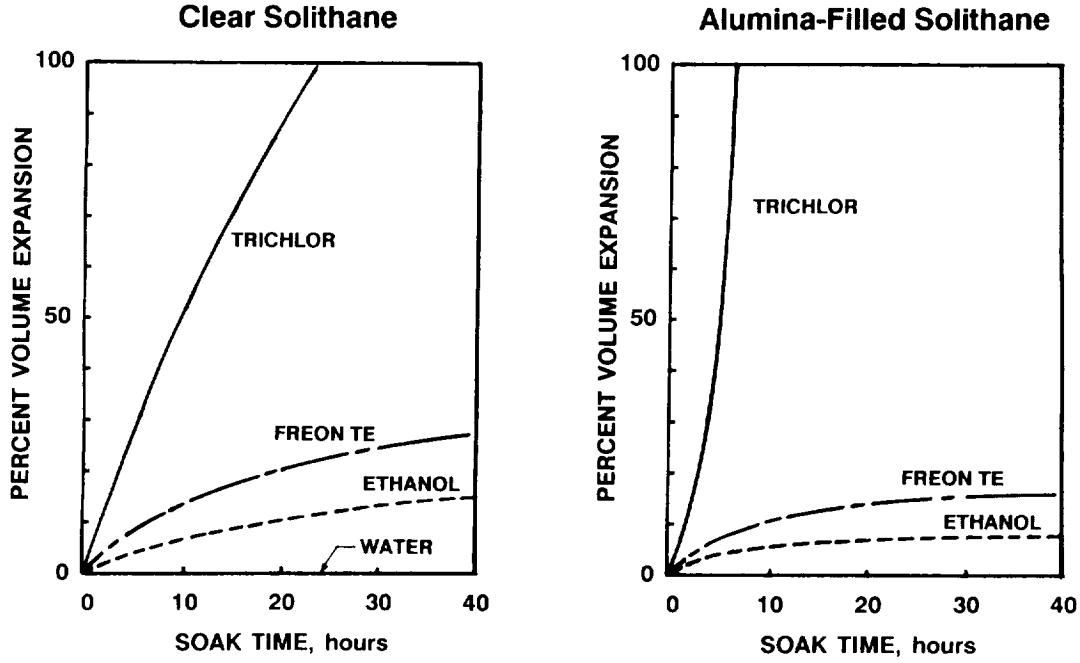


Fig. 26. Volume percent expansion of clear and alumina-filled Solithane (5/8" cubes) during immersion in solvents

evaporates much faster than Ethanol, its use should shorten the exposure period. Although brief (less than 5 minutes) exposure of Solithane to Freon TE and Alcohol is relatively benign, prolonged exposures to even these solvents can cause significant damage to parts with trapped Solithane, such as under DIPs and flat packs.

COATING OF PARTIALLY-CRACKED SOLDER JOINTS

Another sensitive rework issue is that of reapplying conformal coat to electronic parts, such as DIPs and flat-packs, that have had previously applied conformal coat removed to facilitate rework and/or inspection. If the new coating is applied with an elevated temperature cure, it is likely to penetrate any partially cracked solder joints, and result in a cured wedge of Solithane inside the cracks. After cool-down the wedge prevents the solder-joint crack from closing and may lead to a complete creep-rupture failure of the solder joint over time. All of the dozens of badly cracked solder joints found in this study had substantial amounts of Solithane in the crack as shown in Fig. 4. Many were adjacent to rework areas. **It is best to completely remove and replace any exposed parts and to use room temperature, ambient pressure curing of the new conformal coat in rework areas.**

STUB-MOUNT SOLDERING OF PARTS

Under special circumstances, certain electronic parts were installed to the Galileo and Magellan boards using a "stub-mount" solder joint; this mounting technique, illustrated for discrete diodes in Fig. 27, was typically used when the correct size part was not available for the as-fabricated boards. Because the pad size was insufficient for a normal gull-wing type lead bend, the lead was soldered normal to the board in the stub-mount configuration. In the case of the pictured diodes, the original diode flat-pack package became unavailable from the manufacturer and necessitated the use of the discrete diodes.

During the last year many of these stub-mounts were found to have cracked or heavily stressed solder joints [13]. In each case of a stub-mount solder joint failure, the lead had risen off the soldering pad during soldering, resulting in little or no solder fillet as shown in Fig. 28. Of particular concern is that the fillet appeared adequate in inspection. The problem is that the position of the lead within the solder joint cannot be judged by either the soldering technician or the QA inspector. **This mounting technique should either be made inspectable or abandoned.**

ELECTRONIC-PART SOLDERING COMPATIBILITY

In the course of this packaging failure investigation, other important issues arose relative to the compatibility of electronic parts with common soldering and lead-tinning practices. Of particular concern to this investigation was the open-circuit failure of DIP resistor packs during

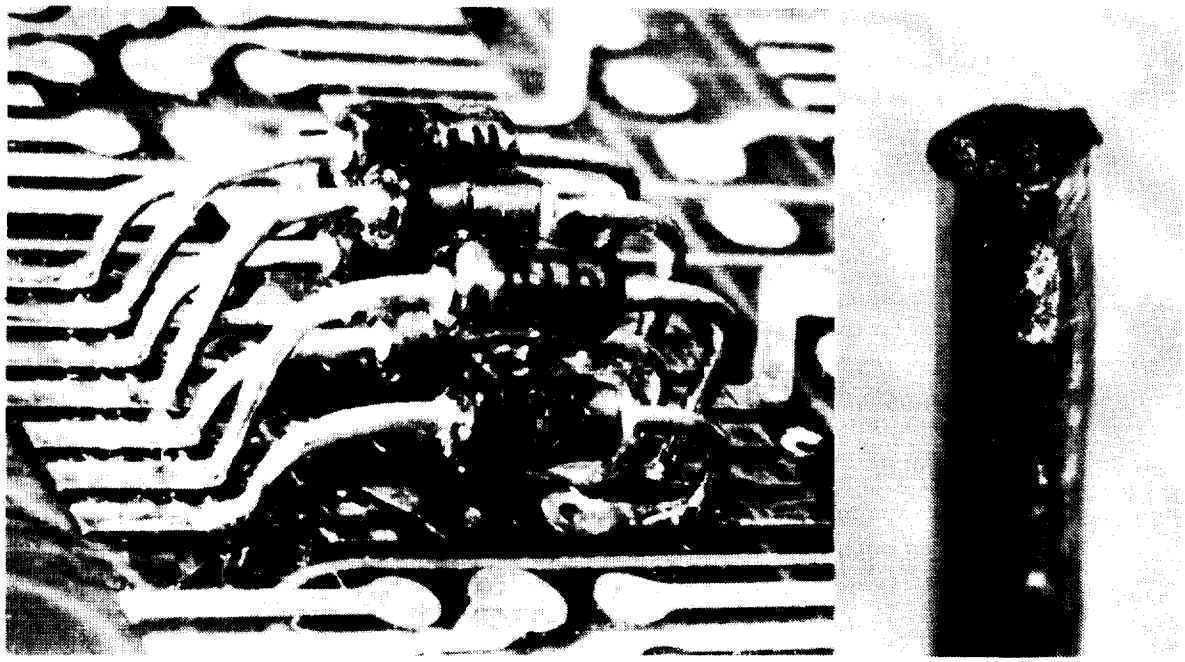


Fig. 27. Stub-mounted diodes used as substitute for unavailable diode flat-pack, and example of failed lead with no solder fillet

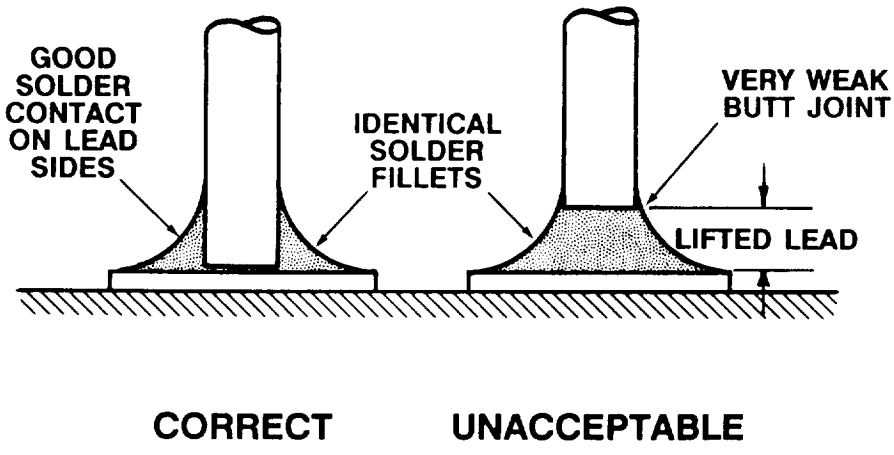


Fig. 28. Problem of poor inspectability of solder fillet on stub-mounted lead

exposure to lead-tinning and solder-wicking processes [14]. Measurement of part temperatures during typical JPL lead tinning operations indicates that internal resistor elements often reach 240°C. Alarmingly, however, the resistor packs were found to exhibit internal solder reflow at as low as 230°C. There is an urgent need to either bring the solder temperature exposures down, or to verify that electronic parts are compatible with the higher temperatures.

SECTION 5

SUMMARY RECOMMENDATIONS

Various recommendations have been highlighted throughout this publication in areas where improvements are felt to be necessary or desirable. This section attempts to briefly summarize these findings under three sub-headings:

- Packaging Requirements
- Packaging Methods
- Management and Review

PACKAGING REQUIREMENTS

- Establish generic electronic packaging thermal-cycle fatigue endurance requirements that envelop the vast majority of JPL missions; the requirements must reflect the total environment seen by flight hardware including fab, rework, functional testing, qualification testing, launch and flight. A recommended approach is shown in Fig. 20. Such requirements are critically needed to measure the acceptability and focus the development of present and future electronic packaging concepts. No thermal cycle fatigue requirements presently exist.

- Develop test methods to verify the conformance of all electronic packaging concepts to cyclic-temperature and solvent-exposure fatigue requirements. A recommended thermal cycle is shown in Fig. 21.

- Critically assess allowable part operating temperature requirements (and design and confirmation procedures) to remove excessive conservatism in this area.

PACKAGING METHODS

- Develop a family of mounting techniques with increased thermal cycle endurance for DIPs and similar components; the family should include designs for various part power-dissipation levels (heat sinking).

- Critically evaluate the stub-mounting concept and either make it inspectable with suitable process controls, or abandon it.

- Develop improved electronic part operating temperature calculation procedures including improved data for thermal properties of typical packaging constructions and materials.

- Develop improved solvent exposure control procedures to prevent solvent induced damage to flight hardware.

- Develop Solithane application procedures to prevent unacceptable part stressing from thermal and solvent expansion.

MANAGEMENT AND REVIEW

- Assure that the complete family of electronic packaging techniques used is fully consistent with the demands on the technology including:

  - Fully qualified for all expected environmental exposures--with the assumed exposure levels well defined so that missions with higher levels will know that requalification is required.
  - Fully inspectable so that failure to be built to print or failure during qualification testing is determinable.
  - Tolerant to process variabilities due to normally expected person-to-person and lab-to-lab differences in carrying out well documented processing procedures.
  - Tolerant to normal rework procedures.

- Develop improved procedures for the review and verification of rework approaches and processes. Many of the observed problems appeared to be directly tied to marginal rework designs or increased stressing caused by rework.

- Develop packaging design review procedures at appropriate steps in the design process. The electronic packaging design is not covered in the present JPL series of design reviews.

- Implement improved inspection methods and procedures to insure that solder joints are of flight quality prior to shipment of hardware for final spacecraft integration, and at other points in the hardware build cycle as deemed appropriate.

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