Direct Detection Optical Intersatellite Link at 220 Mbps Using AlGaAs Laser Diode and Silicon APD with 4-ary PPM Signaling

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ABSTRACT

A newly developed 220 Mbps free-space 4-ary pulse position modulation (PPM) direct detection optical communication system is described here. High speed GaAs integrated circuits from GigaBit Logic were used to construct the PPM encoder and receiver electronic circuits. Both PPM slot and word timing recovery were provided in the PPM receiver. The optical transmitter consisted of an AlGaAs laser diode (Mitsubishi ML5702A, λ=821nm) and a high speed driver unit. The photodetector consisted of a silicon avalanche photodiode (APD) (RCA30902S) preceded by an optical interference filter ($\Delta\lambda$=10nm). Preliminary tests showed that the self-synchronized PPM receiver could achieve a receiver bit error rate of less than 10^{-6} at 25 nW average received optical signal power or 360 photons per transmitted information bit. The relatively poor receiver sensitivity was believed to be caused by the insufficient electronic bandwidth of the APD preamplifier and the poor linearity of the preamplifier high frequency response.

1. Introduction

Direct detection optical communication systems that use a semiconductor laser diode and silicon avalanche photodiode (APD) have the greatest advantages in system simplicity, small size, and power efficiency. A test system based on this technology has been proposed as a payload on Space Station Freedom to be launched in the near future [1]. Direct detection 4-ary pulse position modulation (PPM) systems at data rates of 25 Mbps and 50 Mbps have been developed in the past several years which achieved receiver sensitivities of about 50 detected signal photons per transmitted information bit at a bit error rate (BER) of 10^{-6} [2]-[5]. However, the data rates need to be increased to beyond 100 Mbps in order to demonstrate the advantage of an optical communication system over conventional microwave intersatellite links currently in use. We report here a 220 Mbps 4-ary PPM direct detection optical communication system and the preliminary test results.

As the data rate becomes higher, especially beyond 100 Mbps, the electronic circuits required becomes much harder to build and GaAs devices may have to be used to achieve sufficiently high speed operation. Since 4-ary PPM signaling requires the receiver to have an electrical bandwidth which is four times that of the data rate, identifying suitable amplifiers and filters for use in the receiver to accomplish the received signal processing becomes a challenge. Furthermore, circuit noise cannot be assumed as white since the power spectral density becomes proportional to frequency or even to the square of frequency beyond 100 MHz [6]. The mathematical model developed for the lower data rate system described in [2] may have to be modified to cope with the nonwhite noise. Effects of high frequency noise on system performance need to be studied and measured.

The rest of this report is organized as follows. The overall system description, including key optical and opto-electronic components, are given in the next section. Section 3 contains a detailed description of the PPM encoder and PPM receiver electronics circuits. Preliminary test results are presented in Section 4.

2. System Description

The system setup is shown in Figure 1. The binary source data consisted of a 220 Mbps pseudo random binary sequence (PRBS) 2^7–1 bits long which was generated by a seven bit shift register with feedback as described in [7]. This simple shift register PRBS generator was included in the PPM encoder unit as an optional binary data source. The PPM encoder converted the binary data into PPM format and the resultant PPM pulsewidth was $1/(440\times10^6)\approx2.27$ nanoseconds. An AlGaAs laser diode (Mitsubishi ML5702, λ=821nm, P_{max}=30mW CW) was used as the optical transmitter which was mounted on a temperature stablized mount operated at 25 °C. The laser diode (LD) driver and temperature control unit was developed by NASA Goddard Space Flight Center (GSFC). The rise and fall times of the laser diode using this driver unit were measured to be about 500 picoseconds. The bias level of the laser diode was set to near its threshold level ($\sim$55mA) and the modulation depth was set to 50mA (I_{max}=105mA). A set of neutral density attenuators ($\sim$50dB) were used to simulate the losses between the transmitter and receiver in free space. The maximum allowed transmission loss could be increased by raising the laser diode output power to its full capacity.

The receiver optics consisted of two interference filters in cascade, a focusing lens, and an APD preamplifier module. The interference filter was used to block broadband background radiation and noise emission from the laser diode. The combined passband of the two filters at full width half maximum (FWHM) was about 10 nm which contained nearly the entire emission band of the laser diode, including the chirping effects. The peak transmission coefficient of the filter was 38% based on the data sheet given by the manufacturer. The photodetector consisted of a low noise silicon APD (RCA 30902S) which was measured to have an ionization coefficient ratio of $k_{eff}\approx0.010$ [2]. The transimpedance preamplifier had a GaAs FET as the first stage and a feedback resistance (APD load resistance) of 1030Ω. The total electrical bandwidth was from 45KHz to 440MHz and the total preamplifier gain was 28.9 mV/μA. The signal output from the APD preamplifier module was fed into the PPM receiver which recovered the PPM signal from the noise corrupted waveforms using a

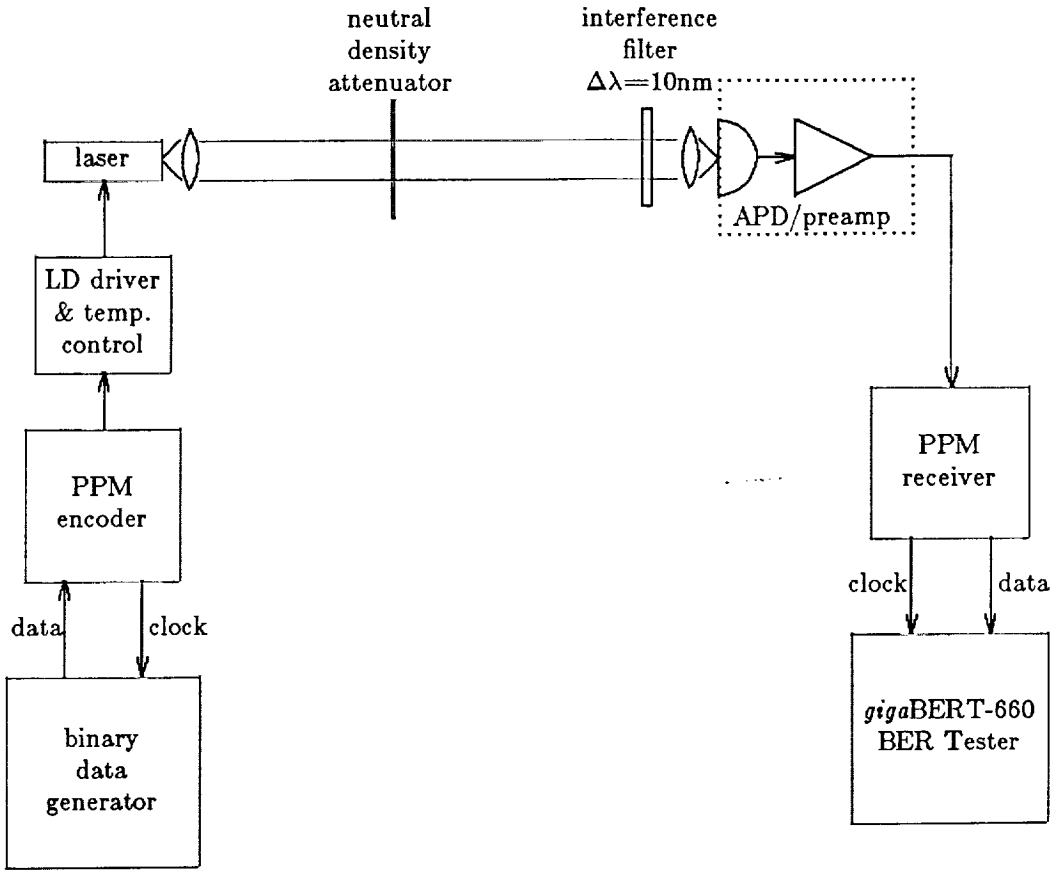


Figure 1. System setup.

maximum likelihood detection scheme. The detected PPM signal was then converted back into the corresponding binary sequence. The output binary data and the recovered binary clock from the PPM receiver were sent to the BER tester (Microwave Logic gigaBERT-660). The BER tester recognized the format of the received PRBS and then actived its own shift register PRBS generator in synchronization with the transmitted sequences. The receiver BER was determined by comparing the received binary data, bit by bit, with the error free PRBS generated in the BER tester.

3. PPM Encoder and Receiver Electronics Circuits

3.1. PPM Encoder Circuit

The design of the PPM encoder electronic circuit is similar to that of the existing 25 and 50 Mbps Q=4 PPM system described in [5]. A schematic circuit diagram is shown in Figure 2. The circuit was constructed on a prototyping circuit board (GigaBit Logic 90GUPB) with both 10G PICOLOGIC^{TM} GaAs logic circuits [8] and Motorola MECL III logic circuits [9]. The circuit board contained several metal layers which provided various DC power supply voltages to the sites of the IC's. High frequency signals between the IC's were carried by semirigid coax cables (Precision Tubes CE50034). The ECL logic circuits were easy to use but they were not fast enough ($\sim$1.3ns rise and fall times) for the part of the circuit that processed the PPM signal and the timing signal. A 4-ary PPM transmitter operating at a binary source data rate of 220Mbps required a slot clock of 440MHz and a PPM pulsewidth of only 2.27ns. GaAs circuits are able to operate at much higher speeds than ECL circuits so they were used where ECL circuits were inappropriate. The transmitter electronics were able to operate with an external slot clock source over a frequency range of 150MHz to 580MHz (75-290Mbps source data rate). The measured pulse rise and fall times were less than 400ps.

The circuit works as follows. The binary data are first stored in a two bit shift register. The two parallel outputs, Q0 and Q1, are fed into a 2-to-4 line decoder which translates the two binary bits into a single PPM word in parallel form. The PPM word is loaded into another shift register and then shifted out

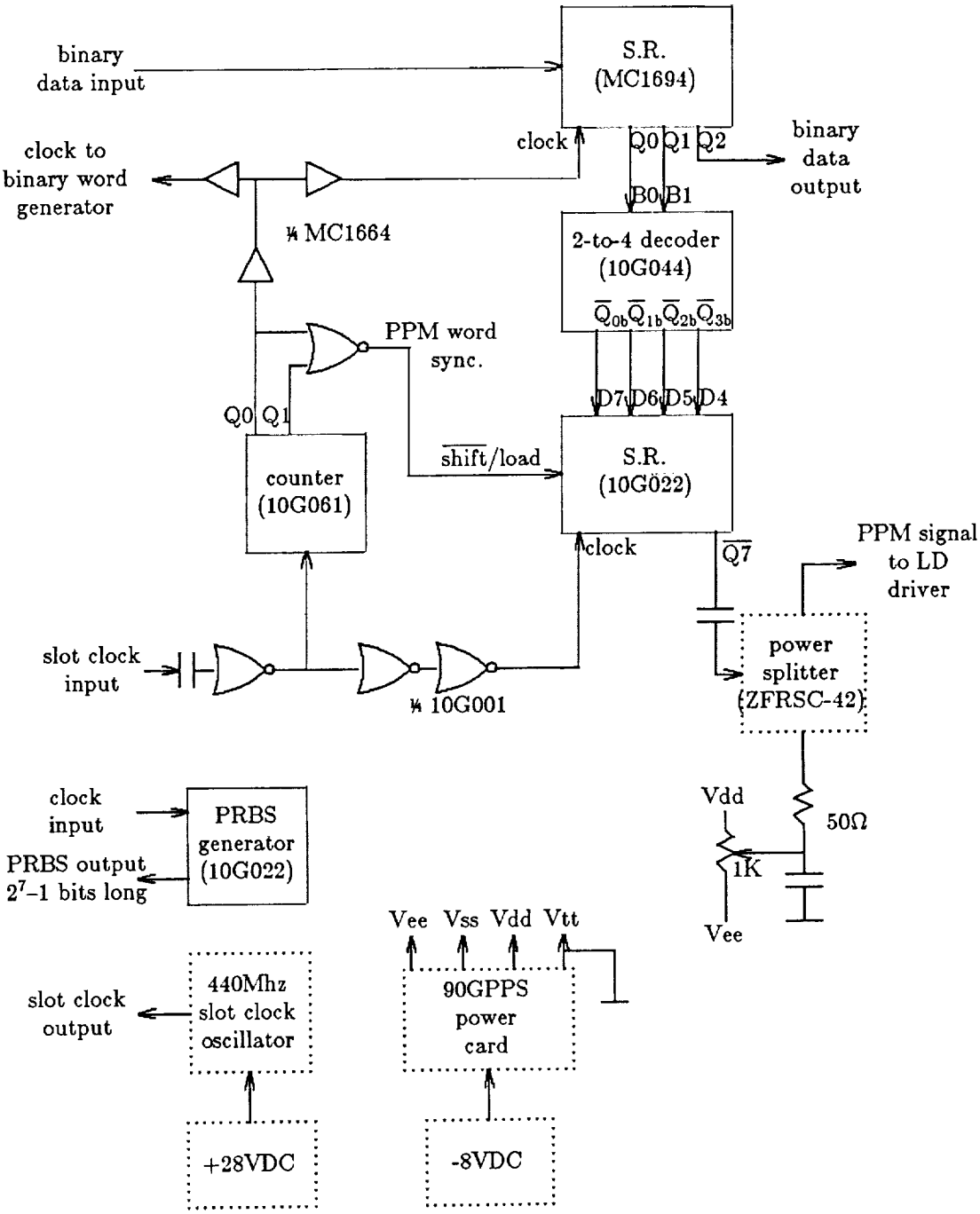


Figure 2. Transmitter circuit diagram. The dotted boxes represent separate components off the circuit board.

in series. The counter in Figure 2 divides the slot clock by two to generate another clock waveform for the binary data. The NOR gate outputs a pulse when the counter state is "00". These pulses form the the PPM word synchronization signal which controls the load and shift states of the shift register. The correspondence between the PPM word patterns and the two binary bits is shown in Figure 3. The circuit was configured such that the output signals require 50Ω termination to ground (Vtt=gnd) so that they may be directly monitored by an oscilloscope. The only exception is the PPM output signal which is AC coupled. The resistive power splitter (Mini-Circuit ZFRSC-42) and the multiturn potentiometer of Figure 2 are used to shift the DC level of the output PPM signal so that it may interface with an ECL level laser diode driver. Since the input threshold level of a laser diode driver is usually fixed, the pulse width of the laser may be adjusted slightly by changing the DC level of the signal. The power splitter also serves as an attenuator which reduces the excessive signal voltage swing between "HIGH" and "LOW" states output by a GaAs device (V_{OH}–V_{OL}=1.9V) to a standard ECL level voltage swing (V_{OH}–V_{OL}≈0.9V).

The transmitter circuit contains a 440MHz crystal oscillator (Greenray T–316JG6) which may be used as a slot clock source. As mentioned in the previous section, a PRBS generator (2^7–1=127 bits long at a data rate of up to 690Mbps) is also included in the PPM encoder as an optional binary data source.

3.2. PPM Receiver Structure

A block diagram of the entire receiver electronics is shown in Figure 4. The signal output from the APD preamplifier was further amplified by a low noise wideband amplifier (Avantek-GPD311/321, 100KHz-800MHz, 28dB). The amplified signal was then split with a 2-way power splitter. One half of the signal was sent to the PPM slot and word timing recovery circuit and the other half was amplified again with a power amplifier (Avantek-UTO-1005, 5-1000MHz, 11dB) before being sent to the matched filter for PPM detection and demodulation. The 1-to-2 power splitters (Mini-Circuits ZFSC-2-1) limited the

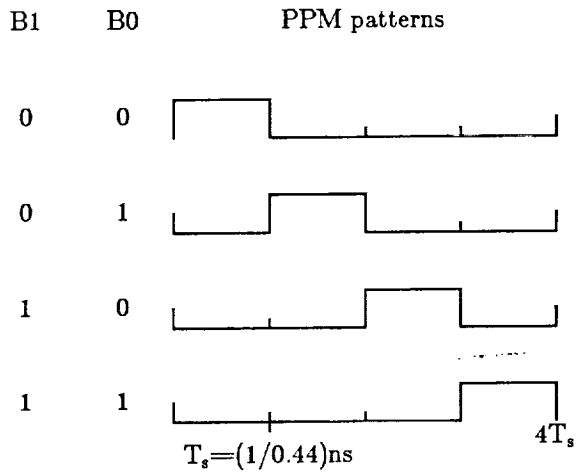


Figure 3. Binary patterns and the corresponding 4-ary PPM patterns.

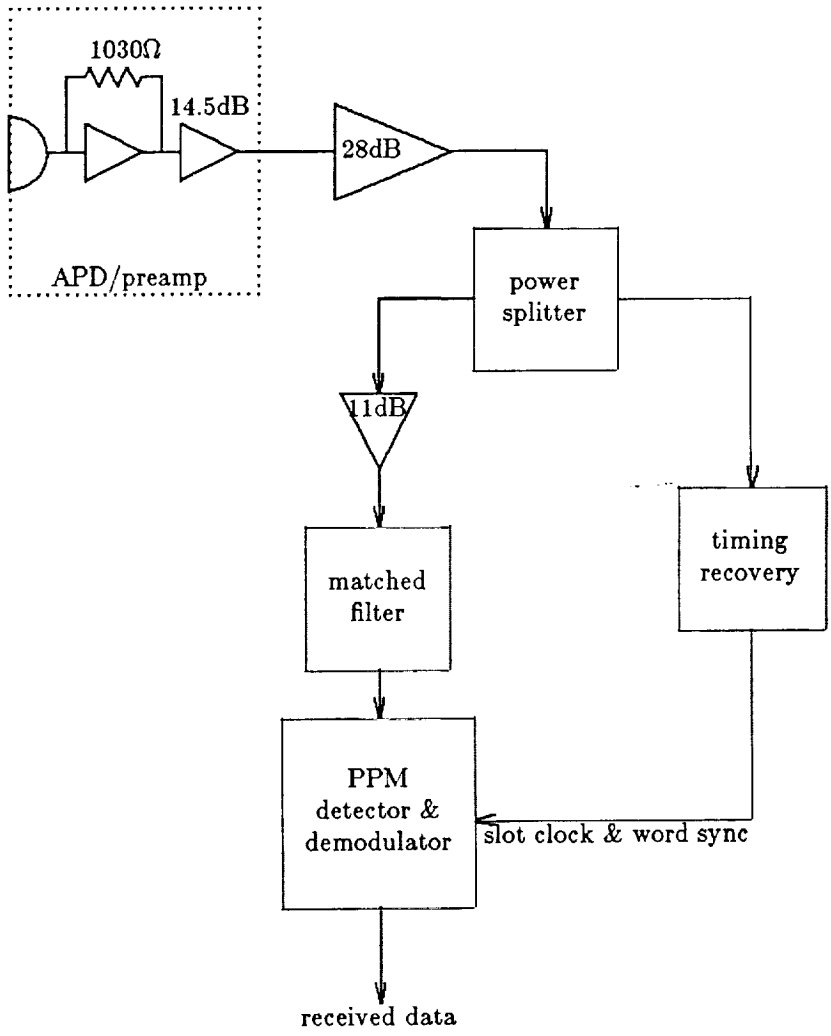


Figure 4. PPM receiver block diagram.

lower cutoff frequency of the entire circuit to 1 MHz, and therefore, the effects of low frequency 1/f noise could be neglected.

The integration of the APD output photocurrent over each time slot required by the maximum likelihood PPM receiver was realized by sampling the output of a matched filter. If the APD output pulses are assumed to have a rectangular pulse shape, the output waveform of an ideal matched filter in response to an input rectangular pulse should be a triangle of equal sides and a base which is proportional to twice the input pulsewidth. If the filter is sampled every T_s seconds at the PPM slot boundaries, each sample is equal to the integration of the APD output photocurrent over the previous time slot without intersymbol interference. The matched filter used in our system, shown in Figure 5, had a well known tapped delay line structure [10]. The time delays consisted of RG316 coax cables cut to the proper lengths. The power splitter and the power combiner in Figure 5 were Mini-Circuit ZFSC-4-1 power splitters which had a bandwidth of 1-1000MHz. The lowpass filter, drawn in dashed box, was used to smooth out the staircase like waveform output from the power combiner of Figure 5. Since the required bandwidth of the lowpass filter was just about the same as the upper cutoff frequency of the first amplifier of Figure 4, no separate lowpass filter was actually used in the circuit.

3.3. PPM Slot and Word Timing Recovery

The timing recovery circuit consists of mainly two phase lock loops (PLL), one for PPM slot timing recovery and one for PPM word timing recovery. The circuit design was based on that of the existing 25 Mbps Q=4 PPM system described in [3] and [4]. The only major change was the use of digital phase/frequency comparators instead of analog mixers as the phase detectors.

A schematic circuit diagram of the entire timing recovery circuit is shown in Figure 6. The detailed PLL circuits and loop filters are shown in Figure 7 and 8. The dotted boxes in the diagrams represent the circuit components which are separate from the circuit board due to their sizes. The component values and design parameters of the two PLLs are also listed in Figure 7 and 8.

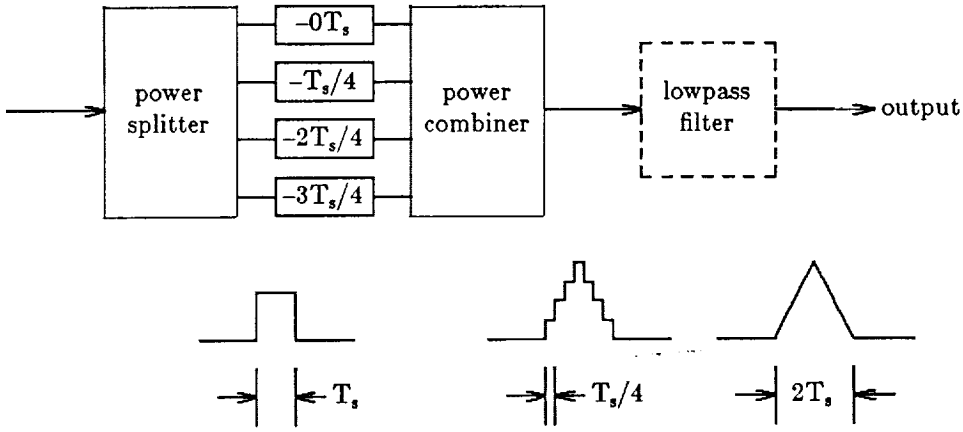


Figure 5. The matched filter in the PPM receiver.

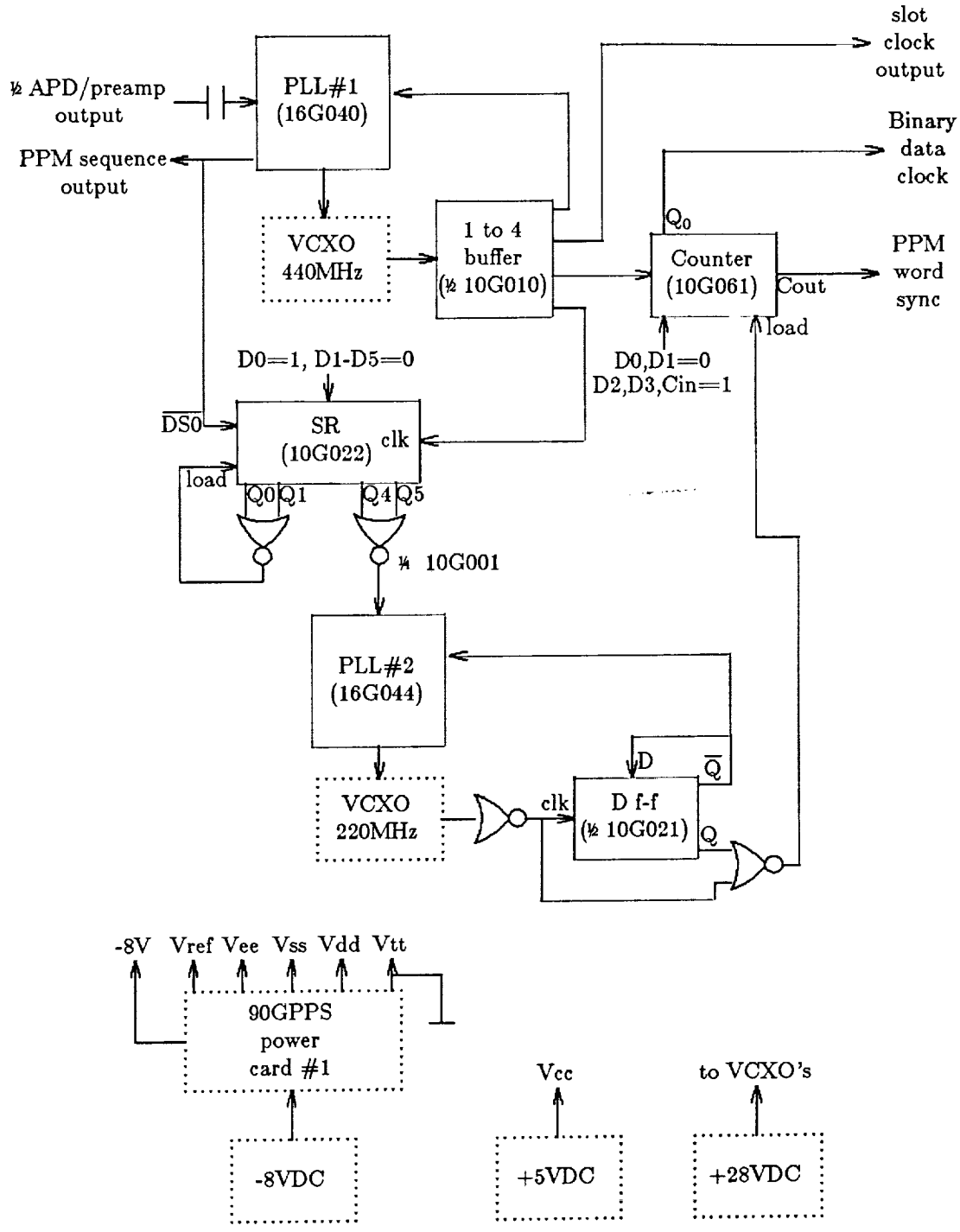
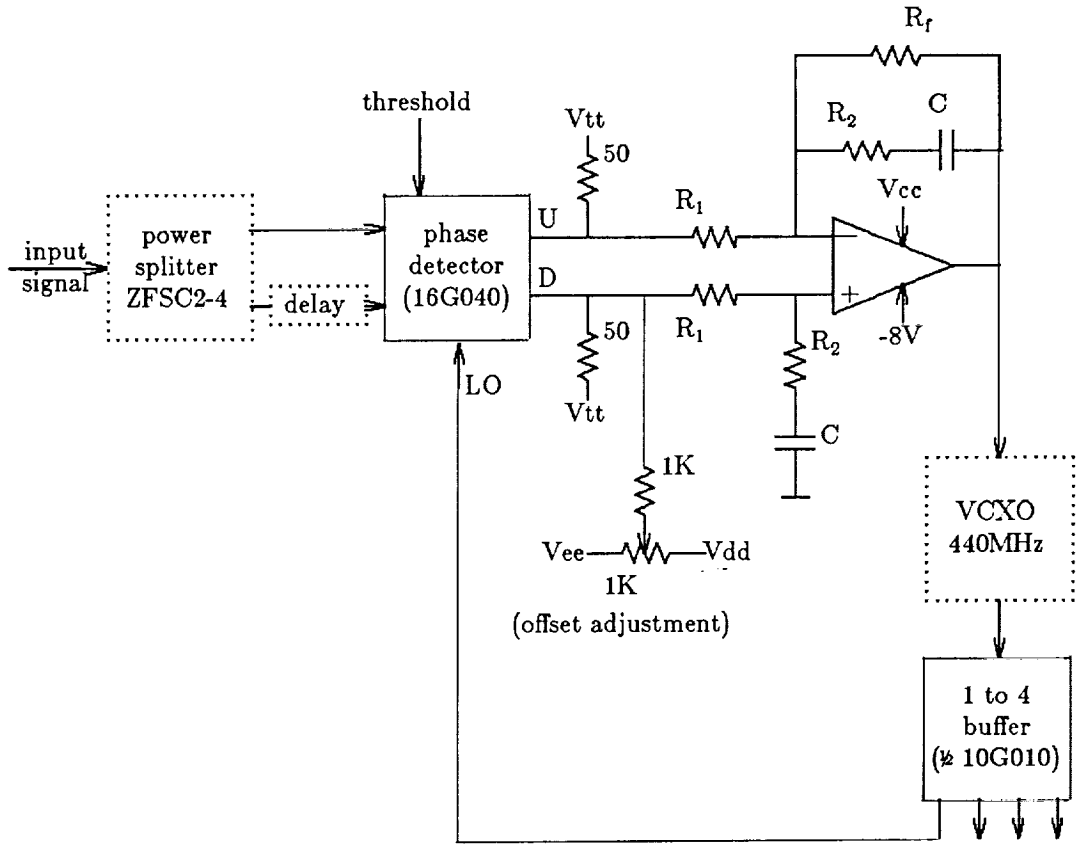
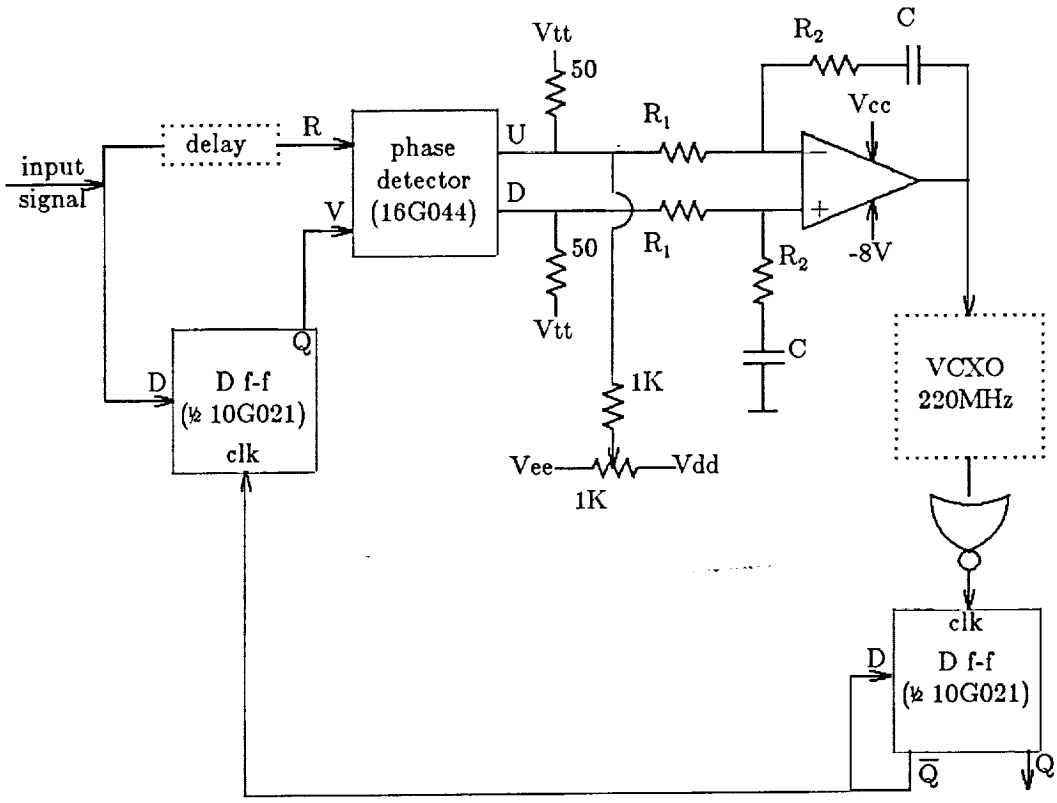


Figure 6. Timing recovery circuit diagram. The dotted boxes represent separate components off the main circuit board.



R_1=1.5KΩ, R_2=15KΩ
C = 1000 pF
R_f = 1MΩ
phase detector gain: K_d = 95.5 mV/rad.
VCXO gain: $K_o = -2\pi \times 15 \times 10^3$ rad/sec./V
nature frequence $\omega_n \simeq$ 12.3 KHz
damping factor $\zeta \approx 0.58$
loop noise bandwidth $B_L \simeq$ 39 KHz
op-amp: Burr-Brown OPA2107
VCXO: Greenray N-423

Figure 7. Detailed circuit diagram of PLL#1.



R_1=820Ω, R_2=22KΩ
C = 1000 pF
phase detector gain: K_d = 23.9 mV/rad.
VCXO gain: $K_o = -2\pi \times 7.3 \times 10^3$ rad/sec./V
nature frequence $\omega_n \simeq 5.82$ KHz
damping factor $\varsigma \approx 0.40$
loop noise bandwidth $B_L \simeq 19$ KHz
op-amp: Burr-Brown OPA2107
VCXO: Greenray N-420

Figure 8. Detailed circuit diagram of PLL#2.

The circuit was constructed on a prototyping circuit board (GigaBit Logic 90GUPB) with GigaBit Logic 10G PICOLOGIC^{TM} family GaAs integrated circuits. The two voltage controlled crystal oscillators (VCXO) (Greenray N-423A and N-420A) in the PLLs have center frequencies 440MHz and 220MHz, respectively, and tuning ranges of 0.01%. Both PLL's contained a second order active loop filter with a Burr-Brown OPA2107P operational amplifier (op-amp). The slot clock PLL was designed such that the product of the loop noise bandwidth B_L and slot time T_s was less than 10^{-4}, which corresponded approximately to a 0.1% jitter in the recovered slot clock. This choice of loop noise bandwidth ensured the PLL to have a capture (or pull-in) range equal to the tuning range of the VCXO while still maintaining a negligible slot clock jitter. The word clock PLL was designed in a similar way with the center frequency equal to 110MHz (1/Q of slot clock rate). The damping factors of both PLL's were about 0.5.

The operation of the circuit is described as follows. As shown in Figure 6, the VCXO output is buffered with an 1-to-4 fan-out buffer. One output of the buffer is used to drive a four bit counter which divides the slot clock by two to form a binary data clock. The counter is loaded with state "1100" at the end of every PPM word and the carrier signal is used as the PPM word synchronization signal. The regenerated PPM sequence (a byproduct of the phase detector chip of the slot clock PLL) is inverted and shifted into a 8 bit shift register. Back-to-back PPM pulses (i.e. PPM word "4" followed by a "1") are detected by a NOR gate whose input consists of the first two stage outputs of the shift register. When back-to-back pulses occur, the NOR gate outputs a pulse which causes the shift register to load with the state Q0,...,Q5=100000 on the next clock rising edge. The output Q4 and Q5 of the shift register are fed into another NOR gate. The NOR gate, in turn, generates a pulse of four PPM slot time wide in response to every appearance of a back-to-back PPM pulse pair as required by the PPM word clock PLL. The VCXO of the word clock PLL has a center frequency equal to twice the word clock frequency and a D flip-flop has to be used to scale it down by a factor of two. The VCXO output and the D flip-flop output are input to a NOR gate. The output of the NOR gate is a

pulse of one slot time wide at the end of every PPM word. Since the occurrences of back-to-back PPM pulse pairs are random, the VCXO output always contains jitters. This is why this NOR gate output is not directly used as the PPM word synchronization signal but as the load signal for the counter driven by the slot clock. As a result, the PPM word synchronization signal generated by the counter is always perfectly aligned with the slot clock and the tolerance for the recovered PPM word clock is as large as half a slot time.

Digital phase/frequence comparators as phase detectors are only sensitive to rising edges of the input signals and the resultant PLL's are the same as the transition detector type timing recovery circuit described in [3]. This type of phase detector is simple to use and immune to pulse amplitude noise. However, missing pulses cannot be tolerated in either of its inputs. The slot clock PLL shown in Figure 7 consists of a phase/frequency comparator (16G040) which has one local oscillator input and two signal inputs with one being delayed by half of a clock cycle. The threshold levels for both the signal inputs are identical and set to near the midpoint of the rising edges of the input PPM pulses. The undelayed signal is used to gate the local oscillator output so that the number of pulses at the two phase detector inputs are always equal and there are no missing pulses.

When the input signal to the PLL is not connected, the outputs of the digital phase/frequency comparator are left randomly in a LOW or HIGH state and the op-amp will be driven to saturation. When the input signal is connected, the phase detector first generates a signal at the beating frequency of the input signal and VCXO output. If the VCXO can respond to the beat signal, the PLL will gradually come to lock [11]. However, since the VCXO has been driven by a saturated op-amp and consequently operated at its extreme oscillation frequency, the frequency differency between the VCXO and the input signal ($\sim$50KHz) is too high for the slot clock VCXO to respond. Furthermore, if the DC gain of the loop filter is too high, the op-amp still may not be able to recover from saturation after the input signal is connected because of the small DC offset in the phase detector outputs. As a result, when the input signal is first connected, the PLL may not always lock in without further assistance. To

avoid this hang-up problem, a relatively large feedback resistor is used across the op-amp to reduce the DC gain of the loop filter. The resultant increase of the static phase error in the PLL output is usually negligible. The operation of the word clock PLL shown in Figure 8 is similar to the slot clock PLL, although it uses a different phase detector chip (16G044) and a D flip-flop to gates the local oscillator signal. The frequency of the beating signal ($<$15KHz) when the PLL is out of lock is within the maximum modulation rate of the VCXO. It is therefore not necessary to use the feedback resistor for the op-amp as in the slot clock PLL.

3.4. PPM Detection and Demodulation

A maximum likelihood (ML) scheme was used to detect the received PPM sequence. The received photodetector output signal was integrated over each PPM time slot and then compared to find the slot that contained the largest amount of signal energy in the PPM word.

The integration, as mentioned earlier, was realized by sampling the output of the matched filter at the end of each time slot. The circuit which performed the ML PPM detection and demodulation is shown in Figure 9. It works as follows. The signal output from the matched filter is first split into four branches by a power splitter (MiniCircuit ZFSC4-1) and then delayed 0, 1, 2, and 3 PPM time slots. Those four signals are compared with six high speed comparators as shown in Figure 9. The resultant PPM word then appears in parallel form at the outputs of the four 3-input NOR gates. The two 2-input NOR gates decode the PPM word into the two binary bits which are then loaded into the shift register and shifted out in series afterwards. The sampling of the signal at the end of each PPM word is done equivalently by loading the shift register in Figure 9 at correct moments. The sampling times are controlled by the phases of the slot clock and word synchronization (shift/$\overline{\text{load}}$) signal.

Since the speed of the signal is relatively high, 50Ω coax cables have to be used to connect and distribute signals on the circuit board. The delayed signal from each output of the 1-to-4 power splitter of Figure 9 are distributed to the

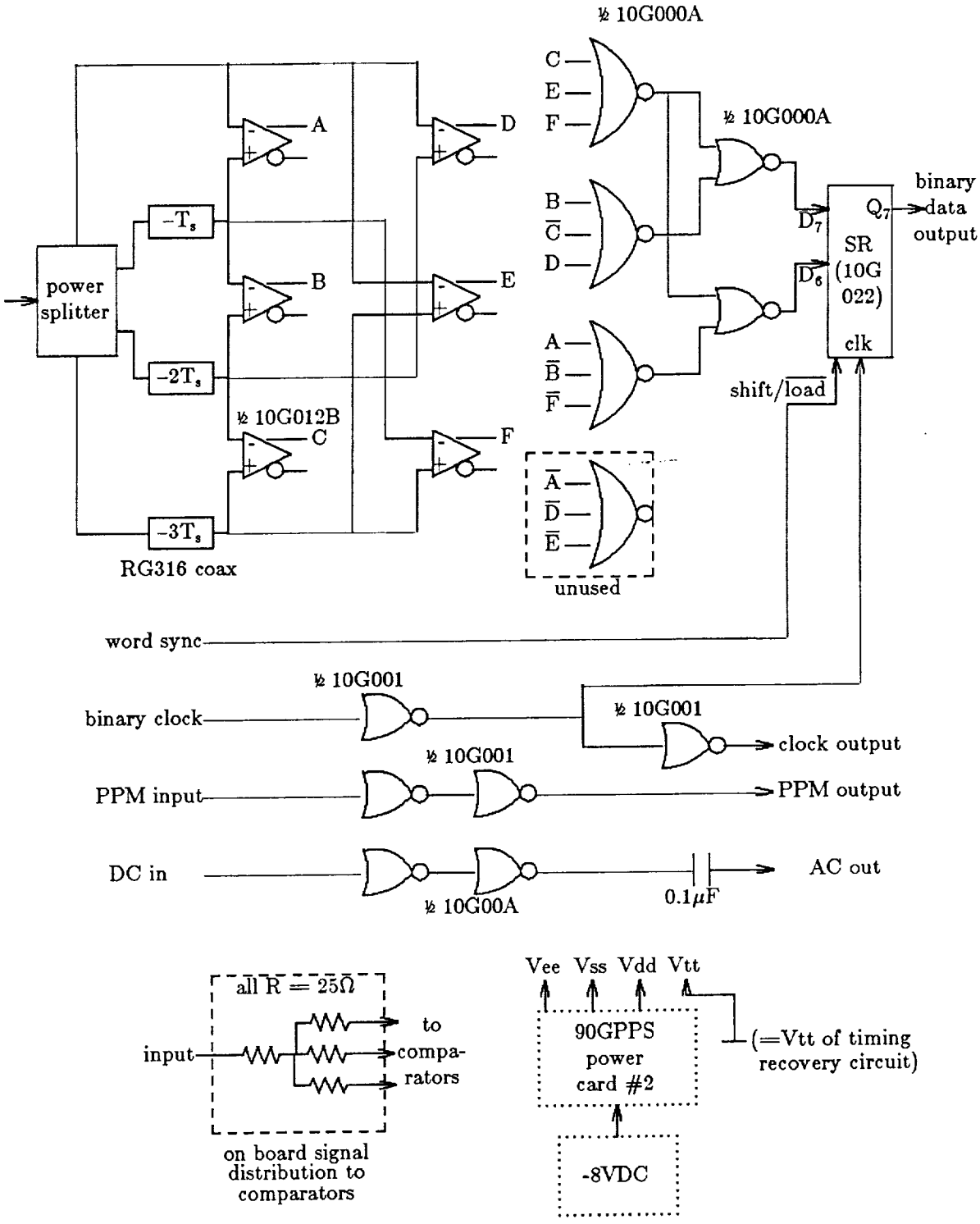


Figure 9. PPM detection and demodulation circuit.

inputs of the three comparators through a resistive power splitter shown in the lower left corner of Figure 9. The circuit is configured such that the outputs require 50Ω resistor termination to ground. A DC-to-AC conversion circuit is added for convenience when a test instrument such as a counter has to be AC coupled. The PPM detection and demodulation circuit uses a separate multivoltage DC power supply card (GigaBit Logic 90GPPS) with common Vdd and Vtt (case ground) from those of the timing recovery circuit.

4. Preliminary Test Results

The electronic circuits of the PPM encoder and receiver were fully assembled and packaged and the entire system was setup as shown in Figure 1. The pulse shape of the PPM sequence output from the PPM encoder was first measured. The output pulse shape of the laser was then measured by a high speed APD (Newport 877) followed by a wideband amplifier (Avantek AV-9T). The laser was biased at 55mA. The modulation signal was DC coupled and the modulation current was set to 50mA (I_{max}=105mA). The measured average optical power in front of the laser diode when the modulation signal was ON and OFF were 3.7mW and 0.1mW, respectively. Figure 10 shows the PPM encoder output waveform (top trace) and the laser diode output waveform (bottom trace). The rise and fall times of the PPM encoder output, as shown in Figure 10, were less than 400ps. The rise and fall times shown by Figure 10 were 700ps and 800ps, respectively, which was believed to be limited by the amplifier following the APD rather than the laser diode itself.

The preamplifier of the APD used in our system was shown to have an insufficient bandwidth and poor response at high frequencies. Figure 11 shows the waveform output from the preamplifier (top trace) and the envelope of the noise fluctuation (lower trace) under an incident optical power of 25 nW and an APD gain of G≈65. As it is shown in Figure 11, the pulse shape became triangular due to the limited bandwidth (440MHz) and there was significant ringing and overshoot. The envelope of the noise fluctuation of Figure 11 shows severe jitter in the received pulses. Idealy, the waveform should have small noise when pulses were absent and much bigger noise fluctuations when pulses

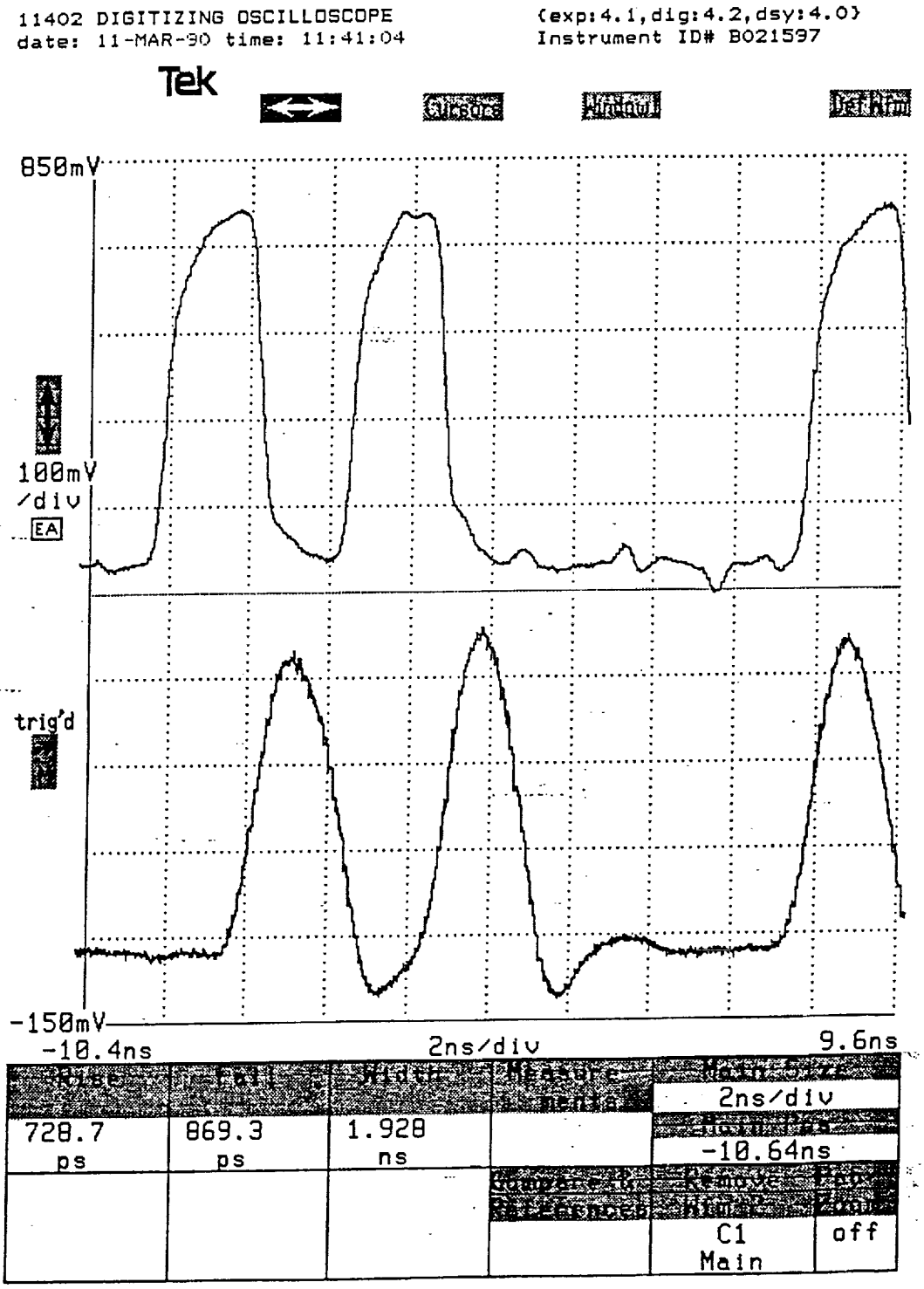


Figure 11. Waveforms output from the APD preamplifier at an input average optical signal power of 25nW (360ph/bit) and an average APD gain of G≈65. The waveform in the lower graticule (2ns/div) shows the envelope of noise fluctuations over 102 displayed waveforms (~30sec).

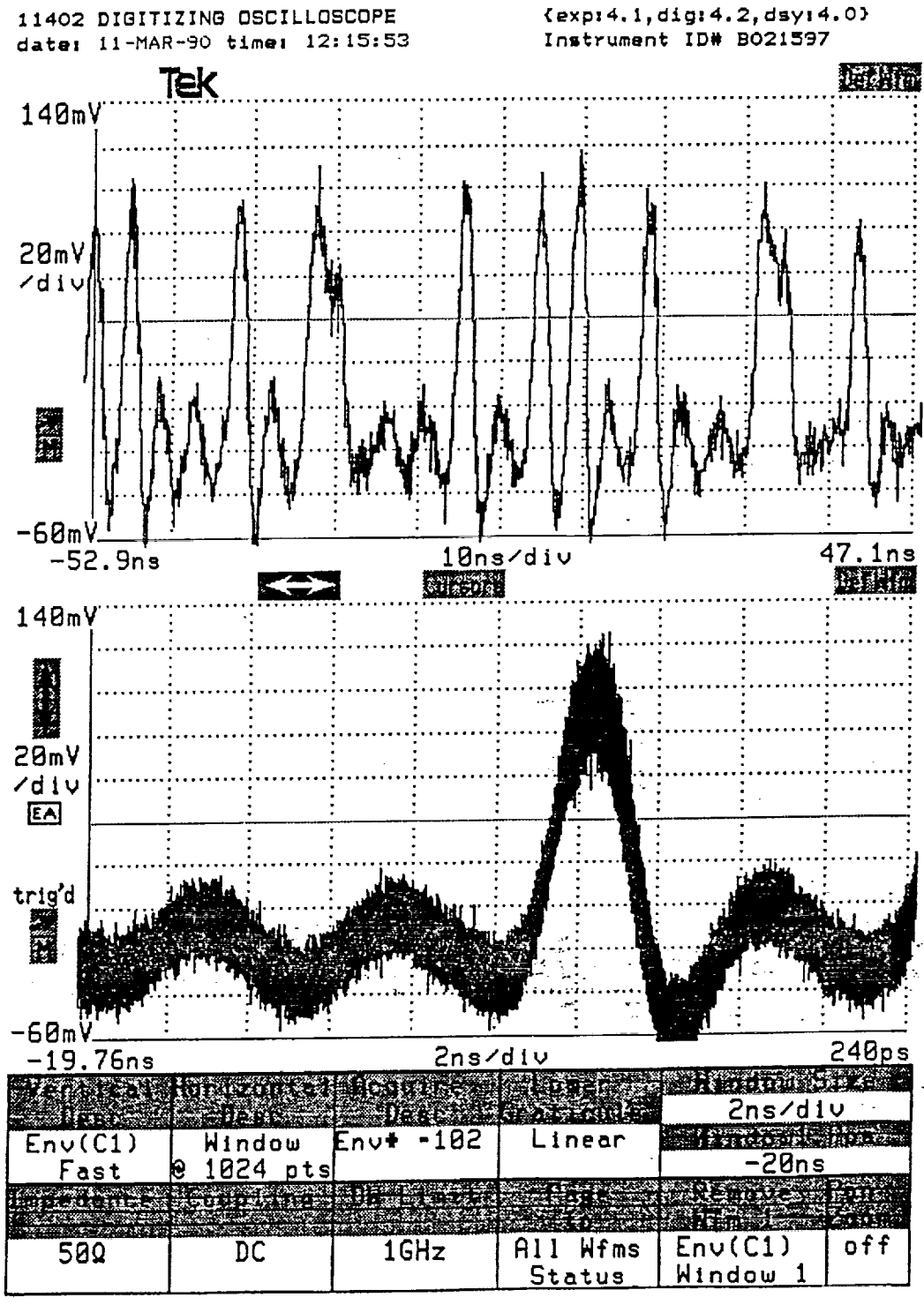


Figure 10. Waveforms output from the PPM encoder (upper trace) and from the laser diode (lower trace). The measured rise and fall times shown in the boxes at the bottom are for the lower trace.

were present because of the multiplicative nature of the APD noise. The noise should have appeared mainly as pulse amplitude fluctuation rather than jitter in rise and fall edges. The poor waveform shown in Figure 11 may be explained by the poor linearity of the preamplifier so that amplitude fluctuation was converted into phase noise. It was found that the jitter of the pulses became intolerable for the PPM receiver to synchronize itself when the APD gain was increased to greater than G=65.

The measured receiver performance with the current APD preamplifier was 360 detected signal photons per information bit or 25nW average received optical signal power at a BER of 10^{-6}. The APD preamplifier was believed to be the major obstacle to achieving a higher receiver sensitivity. The ringing and overshoot on the waveform behaved as a major noise source. Severe phase jitter converted from pulse amplitude fluctuation made it impossible to increase the average APD gain to the optimal value ($\sim$300) as predicted by the theoretical analysis given in [2]. Since the PPM receiver was designed for rectangular input pulses, the insufficient preamplifier bandwidth caused degradation in both PPM signal detection and timing recovery.

A new APD preamplifier is currently being constructed using a different transimpedance amplifier (GigaBit Logic 16G071) which has a 3dB bandwidth of 600MHz and a 6dB bandwidth of 830MHz. The receiver performance is expected to improve significantly with the new APD preamplifier.

5. References

[1] B. D. Seery and M. W. Fitzmaurice, "Overview of NASA Goddard's laser communication program," in *Free-Space Laser Communication Technologies II*, D. Begley and B. Seery Eds, SPIE proceedings vol. 1218, January 1990.

[2] F. M. Davidson and X. Sun, "Gaussian approximation versus nearly exact performance analysis of optical communication systems with PPM signaling and APD receivers", *IEEE Trans. Commun.*, vol. COM-36, pp. 1185-1192, Nov. 1989.

[3] F. M. Davidson and X. Sun, "Slot clock recovery in optical PPM communication systems with avalanche photodiode photodetectors," *IEEE Trans. Commun.*, vol. COM-37, pp. 1164-1172, Nov. 1989.

[4] X. Sun and F. M. Davidson, "Word timing recovery in direct detection optical PPM communication systems with avalanche photodiodes using a phase-lock loop," to appear in *IEEE Trans. Commun.*, vol. COM 38, May 1990.

[5] X. Sun, F. Davidson, and C. Field, "50Mbps free space direct detection laser diode optical communication system with Q=4 PPM signaling," in *Free-Space Laser Communication Technologies II*, D. Begley and B. Seery Eds, SPIE proceedings vol. 1218, January 1990.

[6] R. G. Smith and S. D. Personick, "Receiver design for optical fiber communication systems," in *Semiconductor Devices for Optical Communication*, H. Kressel Ed., ch. 4, Spring-Verlag, New York, 1980.

[7] P. Horowitz and W. Hill, *The Art of Electronics*, pp. 438-440, New York: Cambridge University Press, 1980.

[8] *GaAs IC Data Book & Designer's Guide*, GigaBit Logic Inc., 1988.

[9] *MECL Device Data*, Motorola Inc., 1987.

[10] M. I. Skolnik, *Introduction to Radar systems*, p. 415, McGraw-Hill, New York, 1962.

[11] F. M. Gardner, *Phaselock Techniques*, John Wiley & Sons, ch. 5, New York, 1979.