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ABSTRACT

A number of basic building blocks i.e. rectifying and ohmic contacts, implanted junctions, MOS capacitors, pnpn diodes and devices, such as MESFETs on both α- and β-SiC films have been fabricated and characterized. Gold forms a rectifying contact on β-SiC. Since Au contacts degrade at high temperatures, these are not considered to be suitable for high temperature device applications. However, it has been possible to utilize Au contact diodes for electrically characterizing SiC films. Preliminary work indicates that sputtered Pt or Pt/Si contacts on β-SiC films are someways superior to Au contacts. Sputtered Pt layers on α-SiC films form excellent rectifying contacts, whereas Ni layers, following annealing at ~1050° C, provide an ohmic contact. It has also been demonstrated that ion implantation of Al in β-SiC substrates held at 550° C can be successfully employed for the fabrication of rectifying junction diodes. Feasibility of fabricating pnpn diodes and platinum-gated MESFETs on α-SiC films has also been demonstrated.

1.0. INTRODUCTION

Silicon carbide is the only compound species that exists in the solid-state in the Si-C system; however it can occur in many polytype structures. The lone cubic polytype crystallizes in the zincblende structure and is denoted as β-SiC. The approximately 170 known additional hexagonal and rhombohedral polytypes are collectively referred to as α-SiC. The most common of these latter polytypes is 6H-SiC where the 6 refers to the number of Si-C bilayers along the closest packed direction and H the hexagonal crystal structure. It is these two polytypes of SiC in monocrystalline forms which have assumed primary importance in renewed SiC electronics research and technology.

In this research beta-SiC films were epitaxially grown at NASA-Lewis on nominal (100) and on off-axis (<100> oriented 2-4° toward <011>) silicon substrates by chemical vapor deposition (CVD). These layers were not doped intentionally; however, a net electron concentration of ~$1x10^{17}$ cm^{-3} was measured in these films. The alpha(6H)-SiC wafers used in this study were cut from boules of material produced at Cree Research Inc. via seeded sublimation at temperatures in excess of 2000°C using SiC powder and a 6H seed crystal oriented in the <0001> direction. The wafers were cut, polished, cleaned, oxidized in dry oxygen and etched in buffered HF. Details of the contact fabrication processes and results pertaining to electrical characterization are furnished in the following sections.

2.0. Rectifying Contacts on Beta Silicon Carbide Thin Films

2.1. Au Contact Diodes

Fabrication. To prepare the surface for diode fabrication, the grown films were polished with 0.1 μm diamond paste for 48 hr. The mounting wax residue was removed with hot concentrated H_2SO_4. A final cleaning was conducted in a 1:1 mixture of H_2SO_4 : H_2O_2 followed by a 2 min buffered oxide etch. In order to remove the damage caused by the polishing process, an ~1000Å thick oxide layer was thermally grown in a dry oxygen ambient at 1200°C. The oxide layer was etched and a layer of gold, ~2000Å in thickness, was thermally evaporated onto the samples to form a metal-semiconductor contact. Active diode areas, 100 μm diameter, were delineated by photolithography and gold etching in a $KI:I_2:H_2O$ solution, 4:1:40 by weight. The diodes were separated from the field region by a 100 μm wide annular ring. The structure of these diodes were similar to those reported by Ioannou *et al.* [IEEE Trans. Electron Devices, ED-34, 1694 (1987)]. The infinitely large area of the field-region ensured an adequate 'back contact' with required current handling capability. A measurement of I-V characteristics between the active device and the field region was conducted using an HP 4145A Semiconductor Parameter Analyzer. Current-voltage measurements as a function of temperature between 25°C - 150°C were obtained for the diodes on NCSU 870626/1 (since these diodes did not exhibit ohmic conduction at low biases), in order to establish whether thermionic emission was the prevailing conduction mechanism. This procedure was also expected to yield the barrier height and the modified Richardson's constant. However, at temperatures of 50°C and above, ohmic conduction at low forward biases was observed indicating the non-thermionic character of the contact diodes.

Characteristics. Logarithmic plots of the I-V characteristics in the forward direction indicate space charge limited current conduction through the active volume of the diodes. The β-SiC films grown on nominally (100) oriented substrates show the presence of two deep levels located approximately between 0.26 eV and 0.38 eV below the conduction band edge. In some films on nominal (100) substrates, the I-V characteristics are also influenced by additional traps which are exponentially distributed in energy with a maximum occurring at the conduction band edge. In contrast, the films deposited on off-axis substrates have only one deep level located at approximately 0.49 eV for the 2° off (100) substrates and 0.57 eV for the 4° off (100) substrates. Previous microstructural analysis revealed that the nature and density of defects in the β-SiC heteroepitaxial films on both nominal and off-axis (100) silicon are similar except that the films on nominal (100)

substrates have a high density of inversion(a.k.a. antiphase) domain boundaries. Therefore, the presence of the shallower deep-level states observed in the β-SiC films grown on nominal (100) substrates is speculated to be due to the electrical activity of antiphase domain boundaries. These results have been presented at the Fall 1989 meeting of the Materials Research Society. A preprint of the paper is included in Appendix 1. A detailed version of the paper has been accepted for publication in the Journal of the Electrochemical Society.

2.2 Platinum Contact Diodes

Platinum contact diodes were formed by sputtering a layer of platinum ~ 2000Å in thickness. A lift-off technique was used to define the active diode areas. The SiC was oxidized at 1200°C for 1 hr in order to grow a layer approximately 1000Å in thickness. The metal contact areas were opened, using the mask that was employed for defining the Au pattern (see section 2.1). A pattern reversal process was then utilized with a positive resist and the dark-field mask. The oxide in the contact areas was subsequently etched in buffered oxide for 10min (this overetching ensures good contact with subsequently deposited metal film) and the samples baked at 120° C for 10 min. A layer of Pt ~ 2000Å in thickness was sputtered onto the sample and a contact pattern defined by photoresist lift-off in acetone with ultrasonic agitation. Finally the samples were cleaned in acetone followed by a methanol rinse.

The as-deposited Pt contact diodes were near ohmic, however, rectification was observed on annealing at 400°C for 30min. The annular space between the active device and the field region was protected by a thermally grown layer of oxide. The oxide layer appeared to eliminate edge effects, thereby contributing to characteristics in some ways superior to Au contact diodes. In particular Pt diodes are not degraded as a result of bias stressing, although for -5V to 5V operation, Pt diodes have a higher leakage current than Au diodes. The device structure and current voltage characteristics are shown in Figs.1 and 2, respectively. Interaction between Pt and SiC appears to introduce a distribution of deep-level states in the band-gap of the semiconductor resulting in a slow rise in the forward current. It is speculated that these deep states also serve as the origin of the high reverse-leakage. It is considered that a sandwich-type structure composed of a layer of silicon between the SiC and Pt would provide the Si needed for the interface reaction and thereby contribute to a better contact than Pt alone.

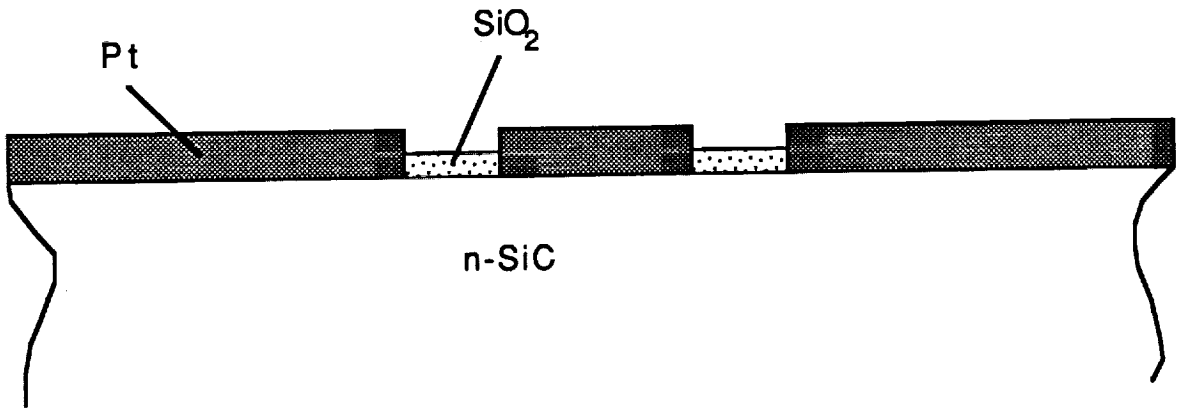

Fig. 1. Schematic of the Pt/SiC contact diode.

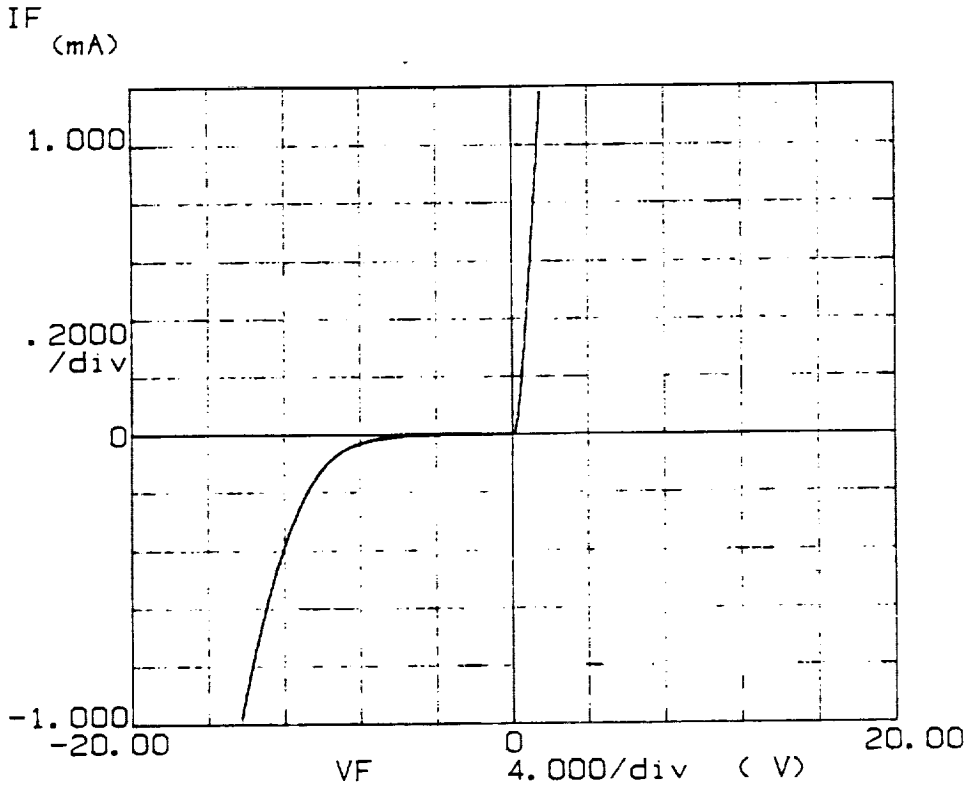

Fig. 2. Current-voltage characteristics of the Pt/SiC contact diode

2.3 Platinum Silicide Contact Diodes

Platinum silicide contacts were formed by depositing a layer of CVD polycrystalline silicon and reacting with a sputtered layer of platinum at a temperature of 450°C. The active diode areas were defined by a triple masking sequence employing a single bright-field mask involving a mask-reversal stage. The complete devices have the same dimensions as the Au contact diodes except that the annular area between the active diode and the field region is protected by a layer of thermally grown oxide, as shown schematically in Fig. 3. A preliminary study of I-V characteristics, as shown in Fig. 4, indicates that these present diodes are potentially superior to those formed by sputtered layers of platinum alone. A sputtered layer of Si followed a layer of Pt had the advantage of a single mask process. However, the thickness of the layers and anneal treatment have to be optimised. A detailed study is being conducted currently.

3.0 Ohmic and Rectifying Contacts on Alpha Silicon Carbide

3.1 Ohmic Contacts

Preliminary work on ohmic contacts on n-type α-SiC has been performed. Process steps similar to those described in Sections 2.1 and 2.2 were employed for the fabrication the test devices. It was observed, as reported by other workers, that ohmic contacts can be formed with sputter-deposited Ni subsequently annealed at a temperature between 1035°-1050°C at a pressure of ~ 5×10^{-5} torr. Fig. 5 shows the I-V characteristics of an annealed Ni contact dot of 100 μm in diameter separated from a Ni field region by a 100 μm wide annular ring.

3.2 Rectifying Contacts

Sputter-deposited Pt was found to form rectifying contacts. Process steps similar to those described in Sections 2.1 and 2.2 were employed for the fabrication the test diodes. Current-voltage characteristics of 100 μm diameter Pt dots as a function of temperature and following a 400°C anneal are shown in Fig. 6. Annealing of Pt contacts at temperatures in the range between 400°-600°C tends to degrade the forward characteristics. For both Ni and Pt contact studies, substrates with a carrier concentration of ~$2X10^{18}$ cm^{-3} were employed.

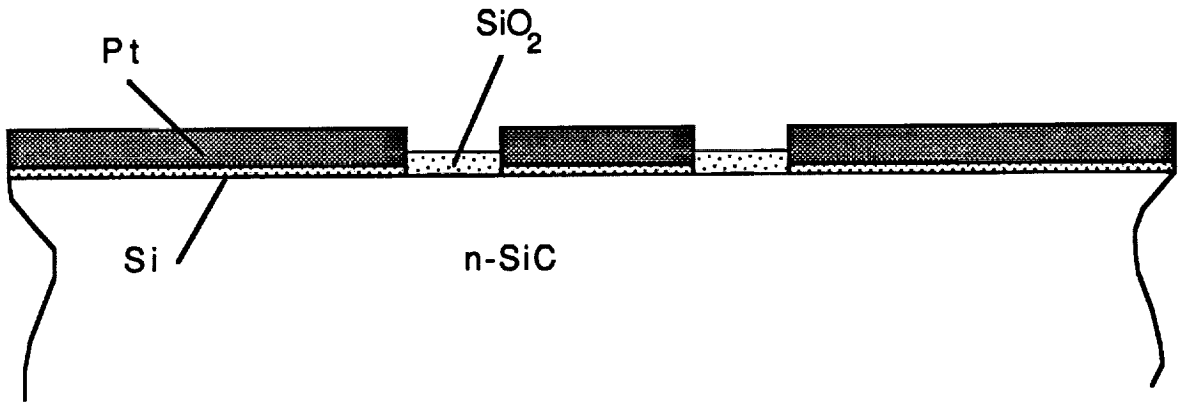

Fig. 3. Schematic of the Pt/Si/SiC contact diode.

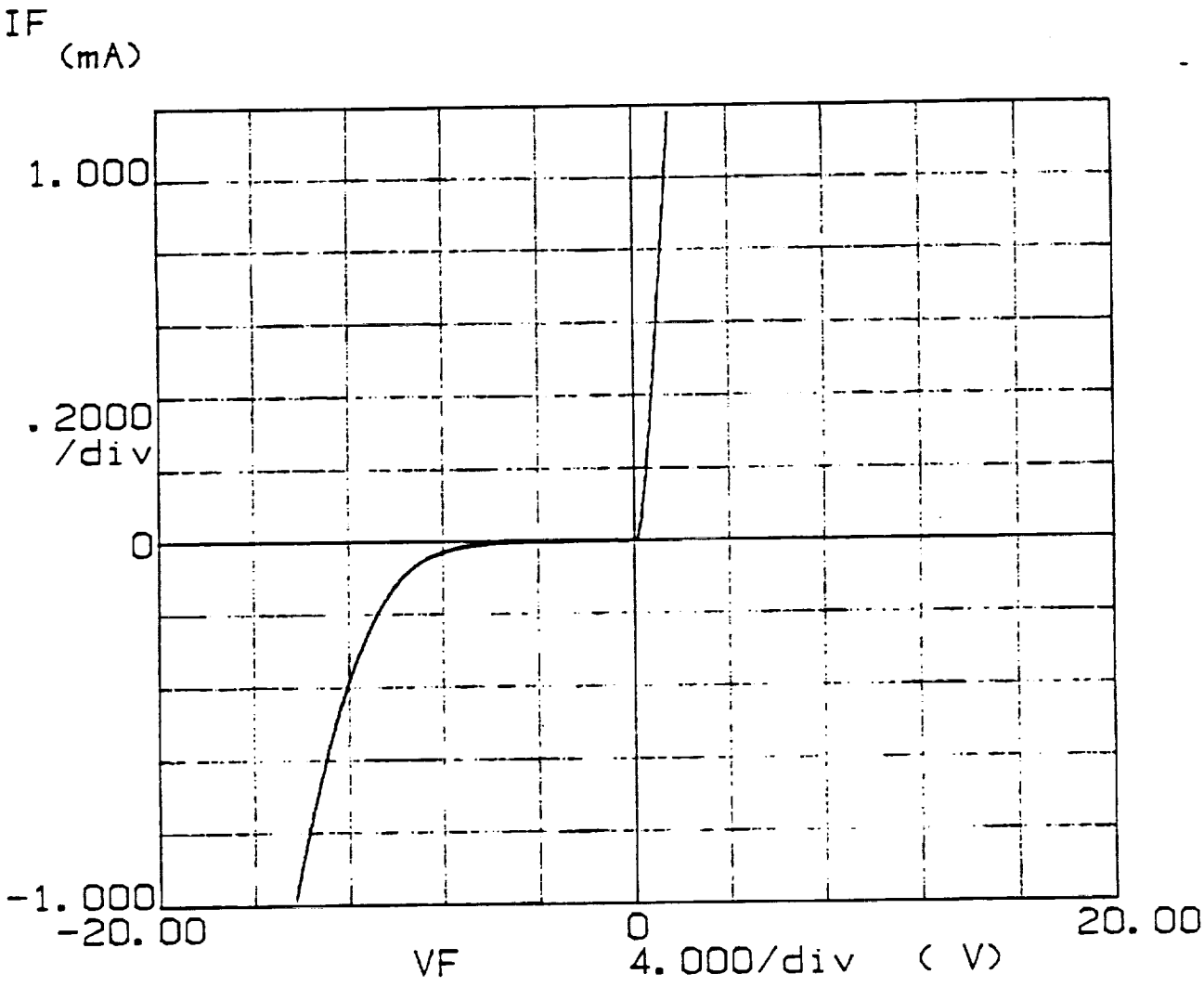

Fig. 4. Current-voltage of the Pt/Si/SiC contact diode.

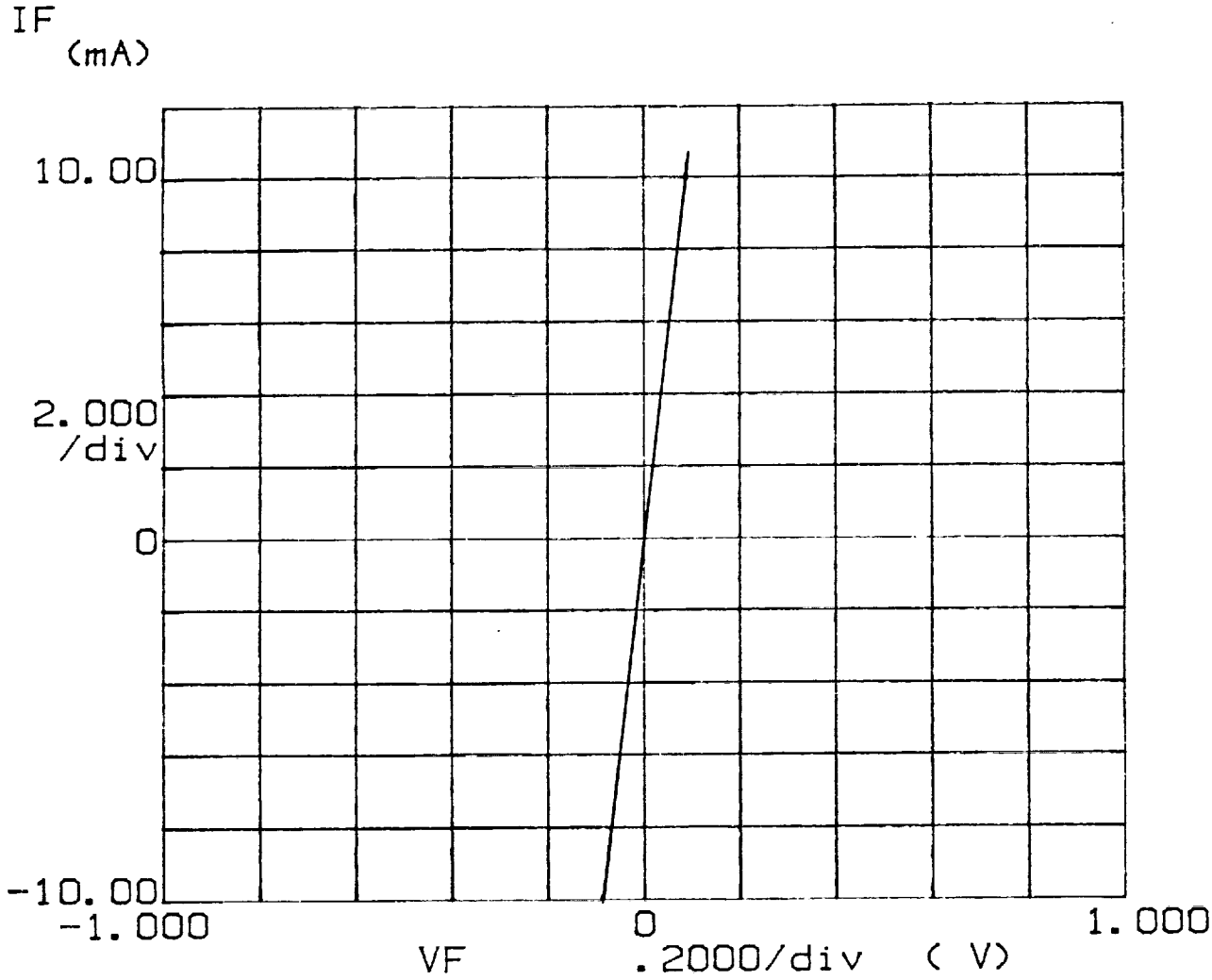

Fig. 5. Current-voltage characteristics of annealed Ni contacts on n^+ α SiC

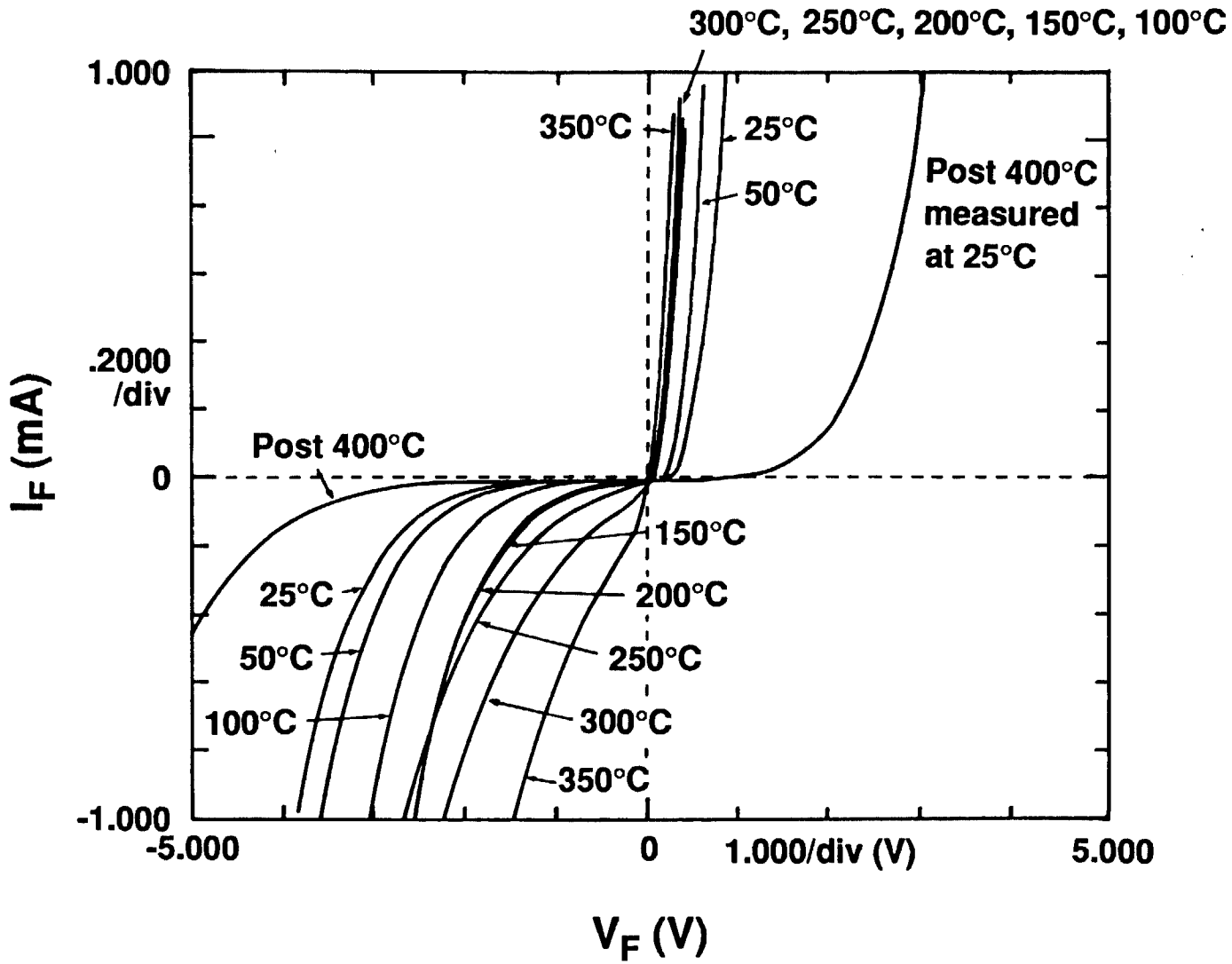

Fig. 6. Rectifying characteristics of Pt contacts on n^+ α SiC as a function of temperature.

4.0 Ion Implanted Junction Diodes on Beta-SiC

4.1 Introduction

Implantation of Al ions in β-SiC has been conducted for the fabrication of junction-diodes with reproducible characteristics and also for the formation of a uniform p-type doped layer. The uniform p-doped layer, if successfully formed, should serve as a substrate for further growth of an n-type layer thereby permitting the fabrication of MESFETs. The uniform p-layer may also enable the fabrication of NMOSFETs.

4.2 Fabrication steps

Fabrication of the implanted junction diodes involved the following process steps:

1. Implant Al^+ in β- SiC substrate held at ~550°C

Sample (i)	single implant : dose :	7.8×10^{14} cm^{-2}	100keV.
Sample (ii)	double implant : dose :	1.25×10^{15}cm^{-2}	180keV and
		6.7×10^{14}cm^{-2}	80keV
Sample (iii)	triple implant : dose :	1.9×10^{15} cm^{-2}	350 keV (twice this dose for 175keV Al^{++})
		1.25×10^{15} cm^{-2}	180 kev and
		6.7×10^{14} cm^{-2}	80 keV.

2. RCA clean.
3. Anneal at 1200°C: 30min in oxygen, 30min in argon
4. Etch oxide in buffered oxide etch(BOE) for 10 min.
5. Sputter deposit: 2500Å Al+11%Si + 2500Å Al.
6. Photolithography: define Al dots for active diodes.
7. Wet chemical etch Al.
8. Reactive ion etch SiC ~1μm.
9. Photolithography: pattern reversal to open ring-shape window area around Al dots for ohmic contact to n-type substrate.
10. Buffered HF etch to remove native oxide from contact window area.
11. Sputter deposit tantalum silicide.
12. Lift-off resist to define ohmic contact.
13. Clean in acetone and methanol.
14. Anneal contacts in argon ambient at 900°C for 2min.
15. Test at temperatures ranging from room-temperature to 550°C.

4.3 Characteristics of the Implanted Diodes

The structure of the fabricated devices and their characteristics obtained from sample (i) (single dose of 7.8 X 10^{14} cm^{-2} at 100keV) are shown in Figs.7 and 8. These characteristics compare very favorably with similar devices fabricated earlier in the Principal Investigator's laboratory. However, diodes fabricated on the doubly and triply implanted substrates which were processed separately failed to show desired characteristics in one case due to insufficient RIE etch-depth and in a second batch due to problems associated with Al metallization anneal.

Characteristics of implanted junction diodes with a dose of 7.8 X $10^{14}cm^{-2}$ at 100keV were obtained as a function of temperature. Rectifying properties were maintained to a temperature of 250°C; above this temperature the diodes became ohmic. Between room temperature and 100°C the diode forward characteristics were dominated by a 'shallow level' state located ~0.16eV above the valence band-edge with a concentration of ~1X10^{15} cm^{-3}. An analysis similar to that reported by Edmond, Das and Davis, (J.Appl. Phys., 63(3) pp. 922-929, 1988) has been used to obtain the shallow level parameters. Charge storage effects were not observed in the diodes indicating 'instant switching' from forward state to reverse blocking state.

5.0 MESFETs in Alpha and Beta Silicon Carbide

5.1 Introduction

MESFETs are normally fabricated on a thin n-type epitaxial layer on p-type material. For SiC a p-layer, several microns in thickness is initially grown, followed by a thin n-lyer in which the active MESFET is fabricated. Early experiments were conducted on heteroepitaxial β-SiC films. Considering the initial problems associated with the growth of reproducible quality p-type material by CVD, a buried layer was formed by ion implantation. MESFETs were fabricated on the top layer that had relatively low concentration of aluminum and retained n-type conductivity. MESFET devices have also been fabricated on recently available α- and β- films on α-SiC substrates. Process steps involved in the fabrication of these devices are given in the following section.

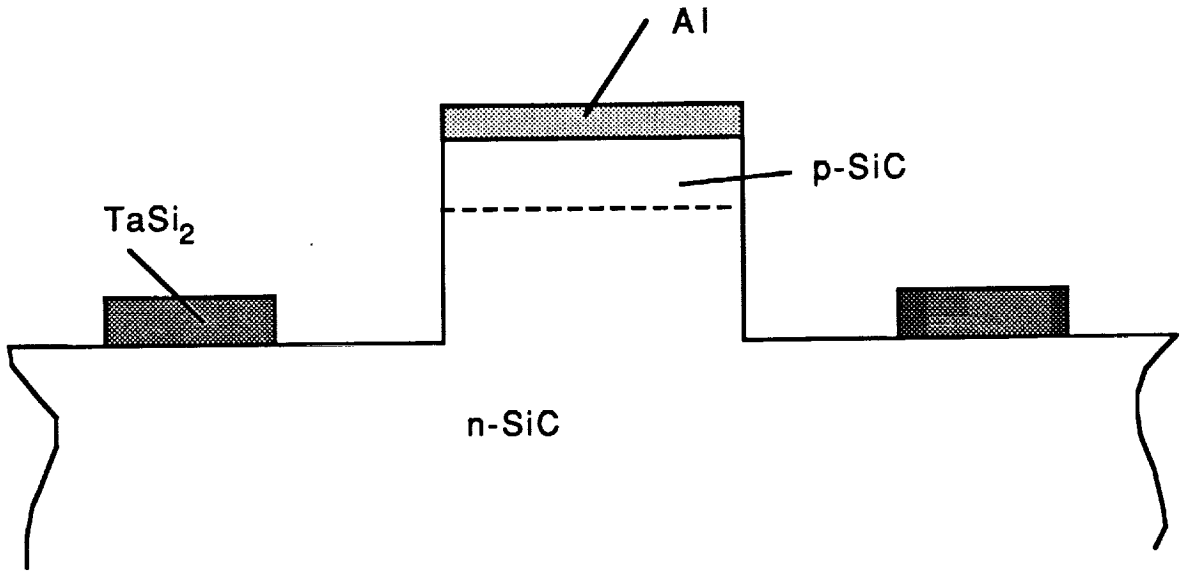

Fig. 7. Schematic of the Al ion implanted junction diode.

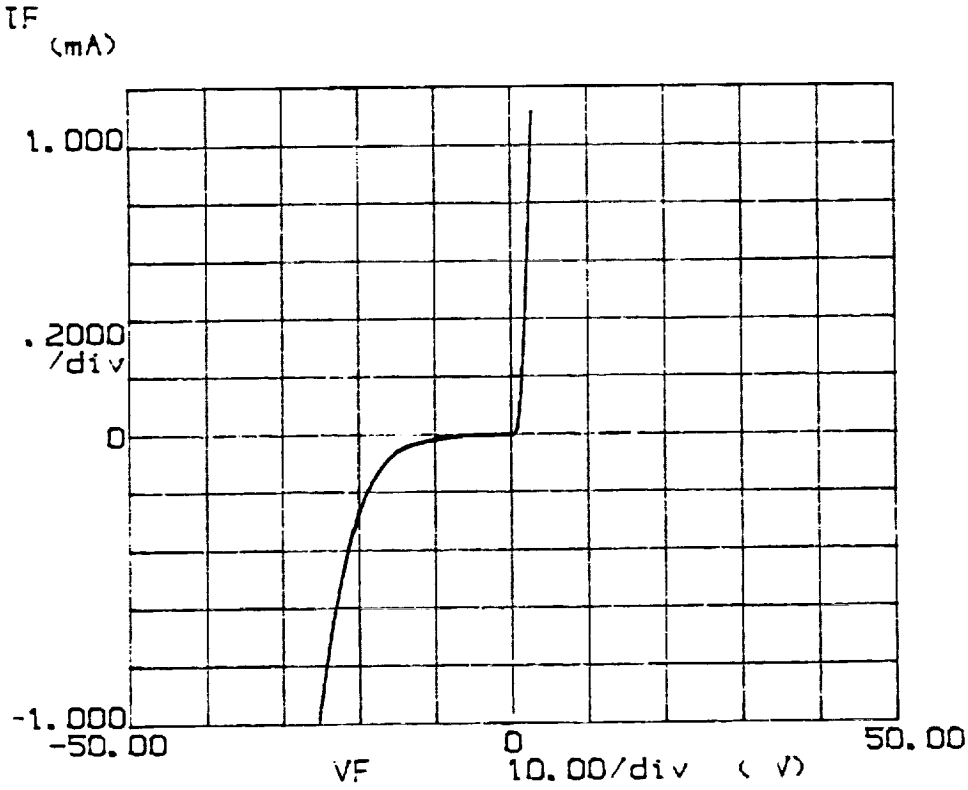

Fig. 8. Current-voltage characteristics of the Al ion implanted junction diode

5.2 MESFET Fabrication Steps for Beta-SiC Films on Silicon

1 Implant 175 keV Al^{++} ions at a dose of 1×10^{15} cm^{-2} at a substrate temperature of 550° C.

2 RCA clean.

3 Anneal at 1200° C for 30 min in dry oxygen and 30 min in argon

4 Etch oxide in BOE.

5 Define source/drain contact areas using a pattern reversal process employing a positive resist with a bright field mask.

6 Sputter $TaSi_2$. Source/drain pattern defined by photoresist lift-off in acetone with ultrasonic agitation.

7 Clean sample in acetone and methanol.

8 $TaSi_2$ contacts annealed for 3-5 min at a temperature of 900° C at a pressure of ~ 5×10^{-5} torr.

9 Deposit ~2000Å thick layer of Au by resistive heating.

10 Define gate pattern using bright-field masking with positive photoresist.

11 Etch Au from areas unprotected by photoresist.

12 Remove photoresist in acetone. Clean in methanol.

13 Test and characterize.

5.3 MESFET Fabrication Steps for Alpha and Beta Films on Alpha-SiC

1 Oxidize SiC at 1200°C for 1hr to grow a layer approximately 1000Å in thickness.

2 Source drain contact windows were opened in the oxide using a pattern reversal process employing a positive resist with a bright field mask.

3 Oxide etched in buffered oxide etch for 10min (this overetching ensures good contact with subsequently deposited metal film).

4 Source/drain contact metallization by sputter deposition. Pattern defined by photoresist lift-off in acetone with ultrasonic agitation. For α-SiC, Ni was employed, whereas $TaSi_2$ was used for β SiC.

5 Samples cleaned in acetone followed by a methanol rinse.

6 Source/drain contact annealing: Ni contacts for 3-5 min at a temperature of 1050°C at a pressure of ~ 5 x 10^{-5} torr and $TaSi_2$ for 3-5 min at a temperature of 900° C at a pressure of ~ 5 x 10^{-5} torr.

7 Gate metallization window was defined by a pattern reversal step with positive photoresist and a bright-field mask. The oxide film in the window area was removed by BOE etching for 10 min.

8 Samples baked at 120° C for 10 min.

9 2000Å thick layer of Pt was sputter deposited and the gate pattern defined by photoresist lift-off in acetone.

10 Devices on α films are ready for electrical evaluation at this stage since as-sputter-deposited Pt establishes a rectifying contact.

11 Pt contact on β films become rectifying following anneal treatment at 400° C for 30 min.

5.4 Characteristics

Characteristics of devices fabricated on n-type β films with an implanted buried p-layer are shown in Fig. 9. These devices did not show saturation, conducted relatively low currents and could not be turned off by applying a negative gate-bias.

Devices fabricated on 1 μm n-type (n = 1 X 10^{17} cm^{-3}) on 2 μm p-type (p = 1 X 10^{17} cm^{-3}) α films grown on an Acheson crystal with gate-lengths down to 3.5 μm showed reasonable transistor characteristics. Current-voltage characteristics of a 10 μm gate-length device are shown in Fig.10. It was not possible to turn-off the 3.5 μm and the 5 μm devices completely. A leakage current of 3-7 μA was observed in these devices for a gate voltage of -6 V. In contrast the 10 μm device had a leakage current of 0.2 μA for a gate voltage of -5 V. Current handling capability of these devices on was low, however, no breakdown was observed to a drain voltage of 70 V for the 10 μm gate-length device (not shown in Fig. 10). Substantial improvement in the current handling capability was observed in devices fabricated on films grown on substrates obtained from Cree Research as shown in Fig. 11. However, it was not possible to turn the device off with a negative bias.

It is believed that the thickness and carrier concentrations of the buried p and the active n layer are absolutely critical for enhancing device performance. Shorter gate length devices with gate lengths of the order of 1 μm are expected to perform much better.

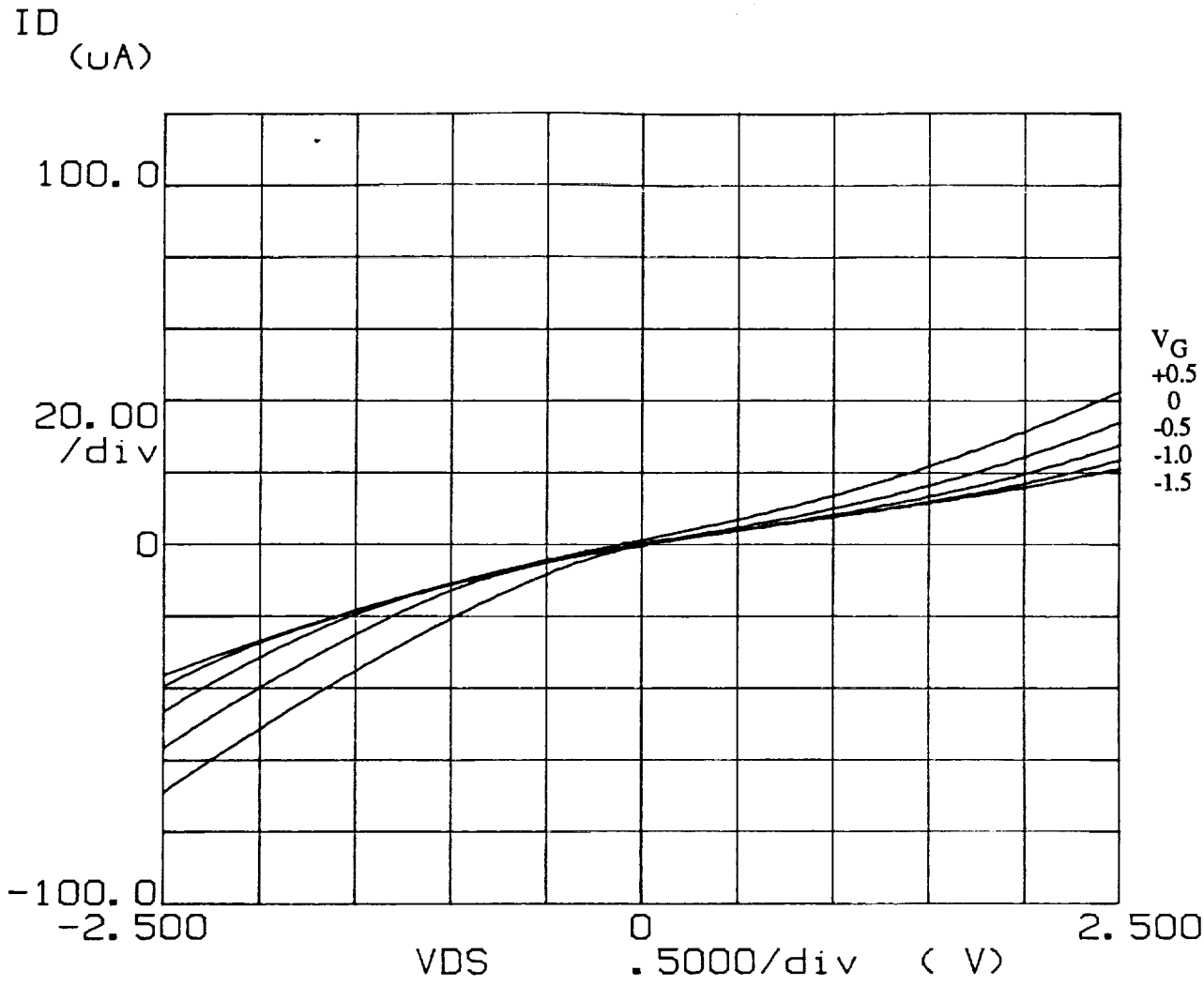

Fig. 9. Drain characteristics of Au gate MESFETs fabricated on n β SiC film with a buried implanted p layer.

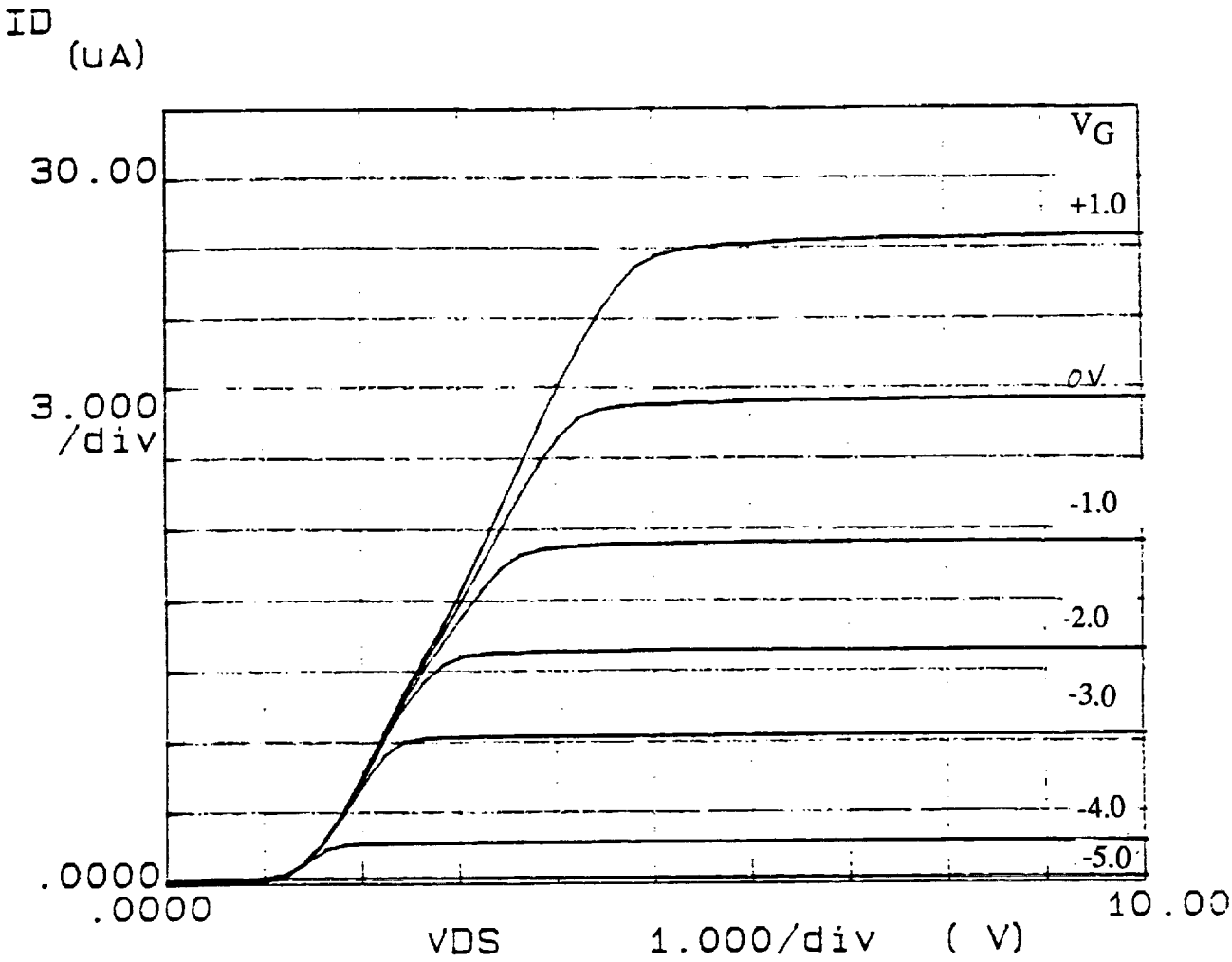

Fig. 10. Drain characteristics of a 10 μm Pt gate MESFET fabricated on 1 μm thick n on 2 μm p film grown on an Acheson crystal.

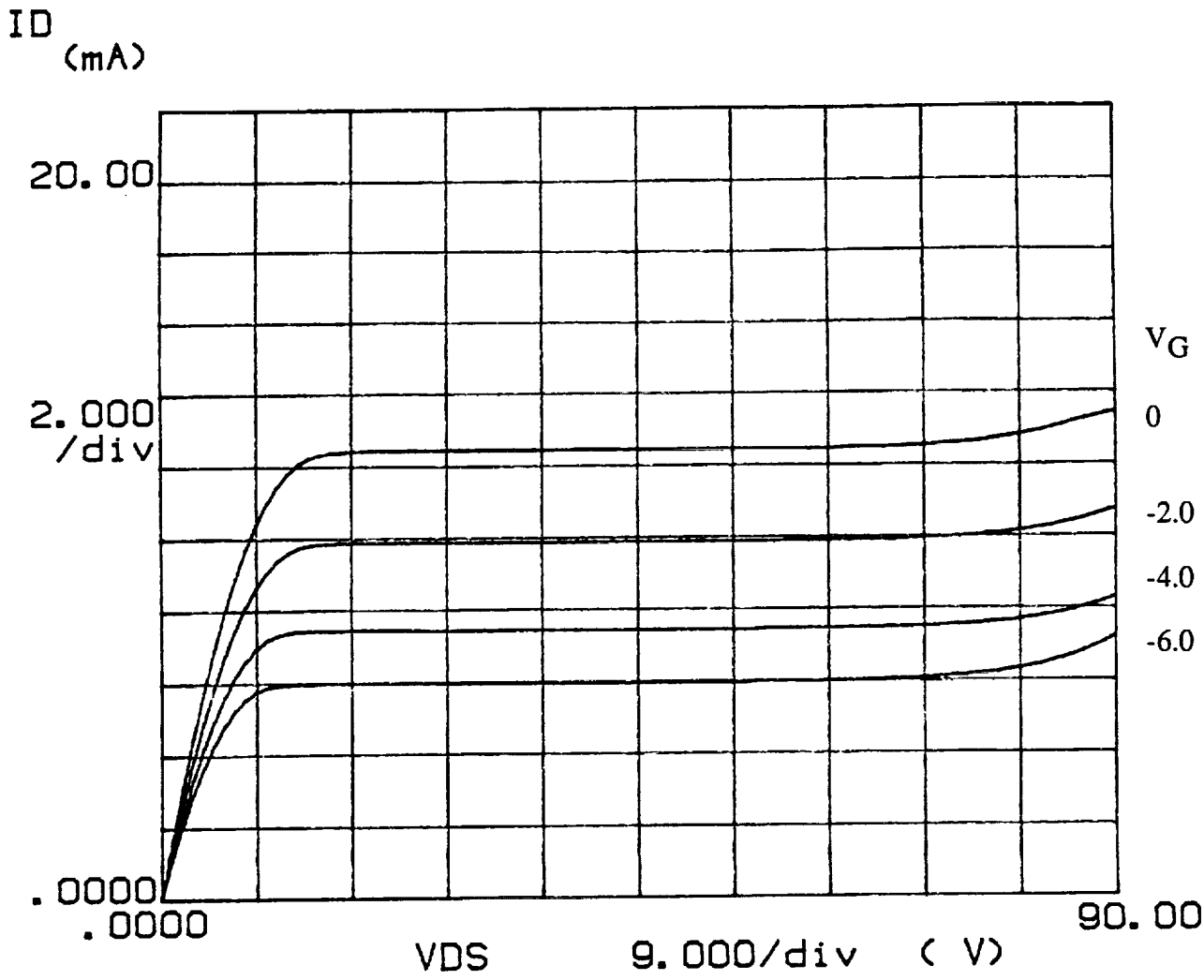

Fig. 11. Drain characteristics of a 20 μm Pt gate MESFET fabricated on 1 μm thick n on 2 μm p film grown on n-type substrate provided by CREE.

6.0 MOS Capacitors on Beta-Silicon Carbide Films

6.1 Process steps

1 Oxide layer of ~600Å in thickness grown at 1200° C in dry oxygen ambient.

2 Poly-silicon layer, 4500Å in thickness, deposited on the grown oxide.

3 Poly-silicon doped with phosphorus oxychloride vapor.

4 Capacitor dots 500 µm in diameter defined using a bright-field mask with positive photoresist.

6 Poly-silicon etched

7 Ring shape contact windows around the poly-silicon dots defined using a pattern-reversal step with a bright-field mask and positive resist.

8 Oxide etched from window area.

9 $TaSi_2$ sputter deposited.

10 Metallization defined by photoresist lift-off in acetone.

11 Sample cleaned in acetone and methanol.

12 $TaSi_2$ contacts annealed for 3 min at a temperature of 900° C at a pressure of ~ 5×10^{-5} torr.

13 Capacitance measurements conducted at a frequency of 1 MHz with a voltage sweep between 0 V and -60 V.

6.2 Characteristics

Inversion occurred at -52 V, and the oxide broke down at -55 V indicating a field-strength of 1×10^{-6} V/ cm. Bias-temperature stressing experiments indicated an absence of mobile charges in the oxide. However, a density of fixed charge of ~ 1×10^{13} /cm^2 in the oxide and a flat-band voltage of ~30 were estimated from the C-V plots.

A polysilicon gate MOS capacitor structure was also fabricated on a substrate that had undergone a triple Al ion implant schedule, at a substrate temperature of 550°C, as follows:

1.9×10^{15} cm^{-2} : 350 keV (twice this dose for 175keV Al^{++}),
1.25×10^{15} cm^{-2} :180 kev and
6.7×10^{14} cm^{-2} :80 keV.

The measured high-frequency capacitance was an order of magnitude smaller than the expected value and independent of applied bias between -30V and +30V.

7.0 Pnpn Diode Fabrication and Characteristics

Initially, β-SiC films on Si substrates were employed for the fabrication of the pnpn diodes. The fabrication steps were identical to those utilized for the implanted junction diodes. These devices exhibited only soft breakdown type forward characteristics. In subsequent attempts, n^+ α- SiC substrates were used for CVD growth of the n^+npnp structure. Layer thicknesses and carrier concentrations were,

n^+	1.4 μm	$n = 2 \times 10^{18}$ cm^{-3}
n	0.7μm	$n = 2 \times 10^{17}$ cm^{-3}
p	2.7μm	$p = 1 \times 10^{17}$ cm^{-3}
n	0.7 μm	$n = 2 \times 10^{17}$ cm^{-3}and
p	2.0μm	$p = 1 \times 10^{17}$ cm^{-3}.

Al^+ was ion implanted into the substrate held at ~550° C (this substrate temperature was employed in all subsequently mentioned implantation steps) at a dose and energy of 7.8 X 10^{14} cm^{-2} and 100keV, respectively, to produce the p^+ contact layer.

Subsequently, mesa active devices were formed by reactive-ion-etching down to the n^+ α- SiC substrate. An Al contact was applied to the p^+ layer; whereas, a Ni ring contact surrounding the mesa was employed for the n^+ α- SiC substrate. Electrical characteristics of these diodes are shown in Fig. 12. A forward breakover voltage of ~ 45 V and a turn-on voltage of ~ 40 V were observed. The high turn-on voltage is suspected to be due a high resistance contributed by the non-optimized structure. The reverse breakdown of these devices were observed at -55 V.

A second batch with an improved structure was fabricated where highly doped p layers were produced by a triple Al ion implantation step. Initially a layer of 1.25 μm in thickness of unintentionally doped n-type was grown. The following triple implant schedule was employed to produce the first p-layer

5.0×10^{15} cm^{-2} : 350 keV (twice this dose for 175keV Al^{++}),
2.5×10^{15} cm^{-2} : 180 kev and
7.0×10^{14} cm^{-2} : 80 keV.

The samples were annealed at a temperature of 1200° C for 30 min in dry oxygen followed by 30min in argon. The oxide layer was etched in BOE and a second layer of SiC of 1.75 μm in thickness was grown by CVD. The second p-layer was produced using the above implantation and anneal schedule. Following a BOE etch, mesa pnpn diodes were defined by RIE etching of SiC, and Ni and Al metal layers were applied to the n^+ and the p regions, respectively.

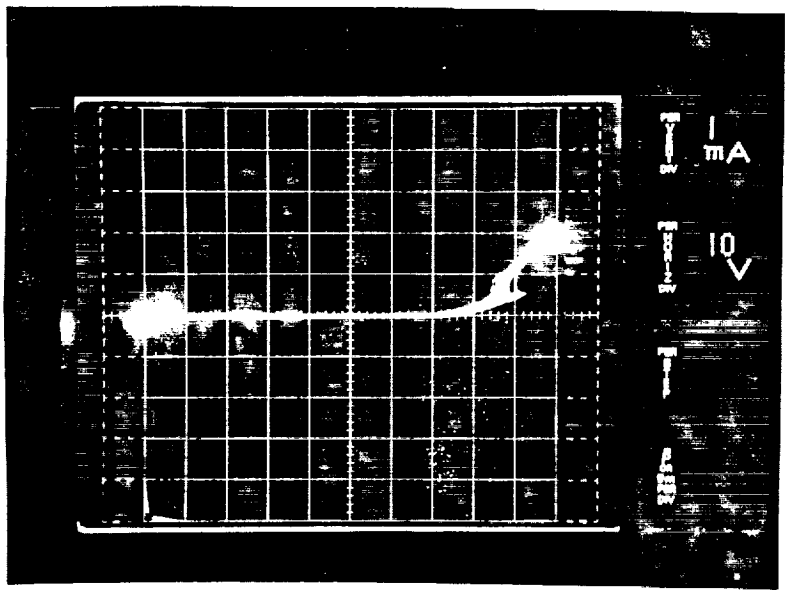

Fig. 12. Pnpn diode characteristics. The p layers were formed during CVD growth. The observed turn-on voltage of ~ 40 V is not a desirable feature for pnpn diodes.

The electrical characteristics of these diodes are shown in Fig. 13. A forward breakover voltage of ~ 25 V and a desirable turn-on voltage of ~ 2 V were observed. Although an improvement in the turn-on voltage was obtained, a forward drop of 20 V was required for a forward current of 100 μA indicating that the device resistance was still too high. The reverse breakdown of these devices was observed at -175 V. In an optimized structure the magnitude of the reverse breakdown and the forward breakover voltages should be about the same.

8.0 Conclusions

A number of basic building blocks, i.e. rectifying and ohmic contacts, implanted junctions, MOS capacitors, pnpn diodes and devices, such as, MESFETs on both α- and β-SiC films have been fabricated and characterized. Gold forms a rectifying contact on β-SiC. Gold contacts degrade at high temperatures, therefore, they are not considered to be suitable as a gate contact in high-temperatures MESFETs. However, it has been possible to utilize Au contact diodes for electrically characterizing SiC films. Preliminary work indicates that sputtered Pt or Pt/Si contacts on β-SiC films are someways superior to Au contacts. Sputtered Pt layers on α-SiC films form excellent rectifying contacts, whereas Ni layers, following anneal at ~1050°C, provide an ohmic contact. It has been demonstrated that ion implantation of Al into substrates held at 550° C can be successfully employed for the fabrication of rectifying junction diodes. Feasibility of fabricating pnpn diodes and platinum gated MESFETs on α-SiC films has also been demonstrated.

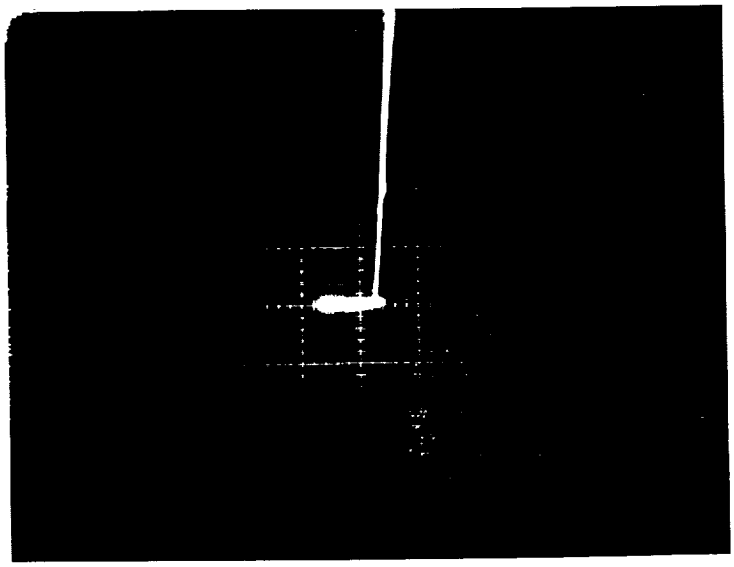

Fig. 13. Pnpn diode characteristics. The p layers were formed by Al ion implantation. Desired turn-on voltage of 2 V was obtained.
Vertical scale : 1div = 50 μA
Horizontal Scale : 1 div = 50 V.

APPENDIX 1

DEEP-LEVEL DOMINATED ELECTRICAL CHARACTERISTICS OF Au CONTACTS ON β–SiC

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ABSTRACT

Current-voltage characteristics of Au contacts formed on β-SiC films grown heteroepitaxially on both nominally (100) oriented and off-axis (100) silicon substrates have been investigated. Logarithmic plots of the I-V characteristics in the forward direction indicate space charge limited current conduction through the active volume of the diodes. The β-SiC films grown on nominally (100) oriented substrates show the presence of two deep levels located approximately between 0.26 eV and 0.38 eV below the conduction band edge. In some films on nominal (100) substrates, the I-V characteristics are also influenced by additional traps which are exponentially distributed in energy with a maximum occurring at the conduction band edge. In contrast, the films deposited on off-axis substrates have only one deep level located at approximately 0.49 eV for the 2° off (100) substrates and 0.57 eV for the 4° off (100) substrates. Previous microstructural analysis revealed that the nature and density of defects in the β-SiC heteroepitaxial films on both nominal and off-axis (100) silicon are similar except that the films on nominal (100) substrates have a high density of antiphase domain boundaries. Therefore, the presence of the shallower deep-level states observed in the β-SiC films grown on nominal (100) substrates is speculated to be due to the electrical activity of antiphase domain boundaries.

INTRODUCTION

Rectifying metal-semiconductor contacts (Schottky-barrier diodes) on SiC, a wide band-gap semiconductor that is emerging as a material for high-temperature [1], high-power and high-frequency devices [2], have been studied by a relatively small number of workers [3]. In all these studies Au was the metal of choice for these contacts. In the present study, values of the ideality factor, *n*, between 1.3 and 3.5 were observed from the apparently linear portion of the semi-logarithmic I-V plots for diodes fabricated in several different β-SiC films. The deviation of *n* from 1.0 in these crystals and the detailed structure of the forward characteristics appear to be caused by a space charge limited current (SCLC) conduction mechanism. Observations of **SCLC conduction in both alpha-and beta-SiC have been reported previously [4,5]**

Considering the potential importance of SiC as an electronic device material, a detailed study of Au/β-SiC contacts on both nominal and off-axis (100) silicon substrates has been conducted and is reported here. A detailed analysis of the fine-structure in the observed I-V characteristics has revealed information pertaining to the deep states present in the material studied. It appears that certain deep-level states which are likely to affect device performance are characteristically associated with given types of crystallographic defects.

THEORETICAL CONSIDERATIONS

Space charge limited current flow in insulators and wide band gap semiconductors has been considered in detail by Lampert and Mark [6]. Representative I-V characteristics obtainable from such materials are shown in Fig. (1). Ideal SCLC conduction is characterized by a square-law dependence on voltage (Fig. 1 (a)). Initially, ohmic behavior is observed if thermally generated free carriers are present (Fig. 1(b)). For traps above the Fermi level, termed "shallow-traps" by Lampert and Mark, a trapped square law behavior is observed at a lower bias (Fig. 1 (c)). When these traps are filled, current rises rapidly to true SCLC square law regime. If deep traps located

below the equilibrium Fermi level are present, ohmic behavior will be observed until all the trap levels are filled. At this point a sharp rise followed by square law behavior will be observed in the I-V curve (Fig. 1 (d)). An *n* value much greater than 1 is obtained if the sharp rise in current is interpreted as an exponential function given by, $I \propto e^{qV/nkT}$.

The "trap-filled-limit" voltage at which the sharp rise in current occurs is designated by V_{TFL}, and is given by [6],

$$V_{TFL} \approx \frac{qp_{to}L^2}{\varepsilon\varepsilon_o} \quad (1)$$

where p_{to} is the hole occupancy of the traps in the active region of the diode (i.e., the concentration of traps not occupied by electrons), L is the thickness of the active region (obtained from the measured zero-bias capacitance), q is the electronic change, ε is the dielectric constant, and ε_o is the permittivity of free space. The effective carrier concentration in the active region, n_o, is given by the relation [6]:

$$\frac{J(2V_{TFL})}{J(V_{TFL})} \approx \frac{p_{to}}{n_o} \quad (2)$$

where J is the current density. In the diodes studied, values of n_o range between 10^9 and 10^{13} cm^{-3}, whereas the bulk carrier concentration in the films is of the order of 10^{17} cm^{-3}. The apparently low effective carrier concentrations arise from carrier-transport through the active volume of the diode that is partially depleted at low biases. The effective carrier concentration determines the position of the quasi-Fermi level. The position of the deep level is taken as being within kT of the quasi-Fermi level [6]. As such, p_{to} is the concentration of the unoccupied states located approximately at the calculated quasi-Fermi level.

Traps distributed in energy may occur due to a high density of defects [7]. Current voltage characteristics, in the presence of traps distributed in energy, may not exhibit all the features of SCLC discussed above. In particular, the sharply rising regime in current may not be evident, although an exponent of greater than one is likely to be observed. This super-linear behavior can be conveniently described by an exponential distribution of traps given by $N(E) = N_o e^{-E/\Delta}$, where N_o is the density of trap states at the conduction band edge, N(E) is the density of trap states at an energy E below the conduction band-edge, and Δ is a thermal energy parameter characterizing the trap distribution [7].

The SCLC is then given by

$$I_{SCLC} = A\, q\, \mu\, N_c \left(\frac{\varepsilon\varepsilon_o}{qN_o\Delta}\right)^{\Delta/kT} \left(\frac{V^{\Delta/kT+1}}{L^{2\Delta/kT+1}}\right) \quad (3)$$

where $\Delta/kT+1$ is equal to m, the observed exponent of the experimental I-V curve (i.e., $I \propto V^m$). A characteristic temperature, such that $\Delta = kT_t$, has been defined [7]. However, the physical significance of temperature T_t is not clear [6].

EXPERIMENTAL

β-SiC films were epitaxially grown on nominal (100) and on off-axis <100> oriented (2-4° toward <011>) silicon substrates by chemical vapor deposition (CVD). Details of the CVD reactor systems and growth procedures employed were previously published [8-10].

These layers were not doped intentionally; however, a net electron concentration of ~$1x10^{17}$ cm^{-3} was measured in these films. To prepare the surface for diode fabrication, the grown films were polished with 0.1 μm diamond paste for 48 hr. The mounting wax residue was removed with hot concentrated H_2SO_4. A final cleaning was carried in a 1:1 mixture of H_2SO_4 : H_2O_2 followed by a 2 min buffered oxide etch. In order to remove the damage caused by the polishing process, an ~1000Å thick oxide layer was thermally grown in a dry oxygen ambient at 1200°C.

The oxide layer was etched and a layer of gold, ~2000Å in thickness, was thermally evaporated onto the samples to form a metal-semiconductor contact. Active diode areas, 100 μm diameter, were delineated by photolithography and gold etching in a $KI:I_2:H_2O$ solution, 4:1:40 by weight. The diodes were separated from the field region by a 100 μm wide annular ring. The structure of these diodes were similar to those reported by Ioannou *et al.* [3]. The infinitely large area of the field-region ensured an adequate 'back contact' with required current handling capability. A measurement of I-V characteristics between the active device and the field region was conducted using an HP 4145A Semiconductor Parameter Analyzer. Current-voltage measurements as a function of temperature between 25°C - 150°C were obtained for the diodes on NCSU 870626/1 (since these diodes did not exhibit ohmic conduction at low biases), in order to establish whether thermionic emission was the prevailing conduction mechanism. This procedure was also expected to yield the barrier height and the modified Richardson's constant [11]. However, at temperatures of 50°C and above, ohmic conduction at low forward biases was observed indicating the non-thermionic character of the contact diodes.

RESULTS

The current-voltage characteristics of the metal-semiconductor contact diodes fabricated in β-SiC on nominal (100) and off-axis (100) silicon substrates are shown in Fig. 2. The linear plots in Fig. 2 (a) show asymmetric (rectification) behavior. The diodes in films deposited on the nominally (100) oriented substrates have higher reverse currents. The semi-logarithmic plots of the measured data are shown in Fig. 2 (b). Values of n range between 1.23 and 3.5. No improvement in the n values was obtained when the measured I-V data was corrected for the effective series resistance of the contact diodes. An effective resistance of 125 Ω was obtained from I-V measurements on $TaSi_2$ metallized representative samples of β-SiC having the same active area as the Au contact diodes. Tantalum silicide forms an ohmic contact on n-type β-SiC with a contact resistance of 2.0×10^{-2} Ω-cm^{-2}[12].

In silicon junction devices at the early stages of the technology, surface recombination and surface channel effects resulted in n values greater than 2 [13]. In the present β-SiC material, studies of MOS devices indicate that the surface is reasonably well-controlled, permitting the fabrication of high-quality MOS transistors in the material [14]. The observed low reverse currents in the off-axis films are considered to be an indication of the absence of any significant surface leakage component. Although the role of the surface in determining the characteristics of the Au-contact diodes is not clear, it appears that under identical conditions of surface preparation and metal deposition the observed effects and differences in the various films studied are bulk-dominated.

The high values of n indicated a mechanism other than thermionic emission dominating current transport in these devices. An ohmic slope at low biases (0.01V-0.1V), as seen in the logarithmic plots of Fig. 2 (c), is a clear indication of non-thermionic behavior. Features in the I-V characteristics which strongly indicate SCLC conduction in the presence of deep-level states became evident at higher biases(1-5V). The diode in films deposited on off-axis substrates also exhibit ohmic behavior at an elevated temperature of 50°C, but not usually at room temperature. The exceptions are discussed later in this section.

In the nominal (100) plot shown in Fig. 2 (c), the transition from an ohmic regime to a sharply rising current regime is an indication of the presence of deep traps. Normally a sharp rise to a true SCLC level is obtained when all the deep traps are filled. From the estimated value of V_{TFL} given by Eqn. (1) (see Fig. 2 (a) and Fig. 3, plot 1), the concentration of unoccupied states, p_{to} is obtained. The effective carrier concentration, n_o, is obtained from Eqn. (2). The approximate location of the deep-level states is at the quasi-Fermi level determined by n_o.

In the diodes fabricated in films on off-axis substrates, the current at low forward biases is independent of bias as shown in Fig. 2 (c). The voltage at which the sharp rise in current occurs is taken as V_{TFL}. A given choice of V_{TFL} determines the value of p_{to}, but the position of the deep-level is primarily determined by the slope of the sharply rising regime in current.

A single discrete deep level is normally observed in the diodes in the off-axis material. In the 2° off-axis material, NASA 816/4, the deep level is located at 0.49 eV and in the 4° off-axis, NCSU 870626/1, 0.57 eV below the conduction band with respective concentrations of unoccupied states of 5.0×10^{15} and 5.2×10^{15} cm^{-3}.

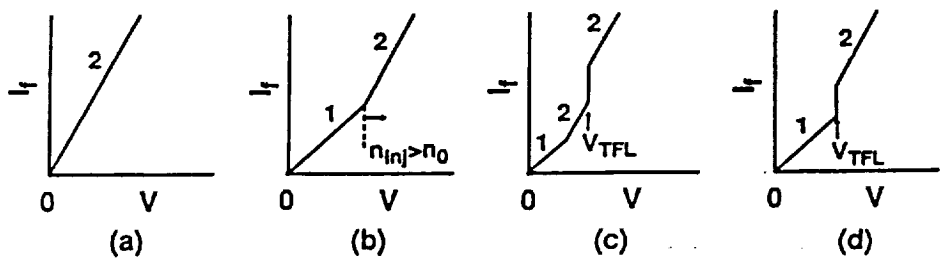
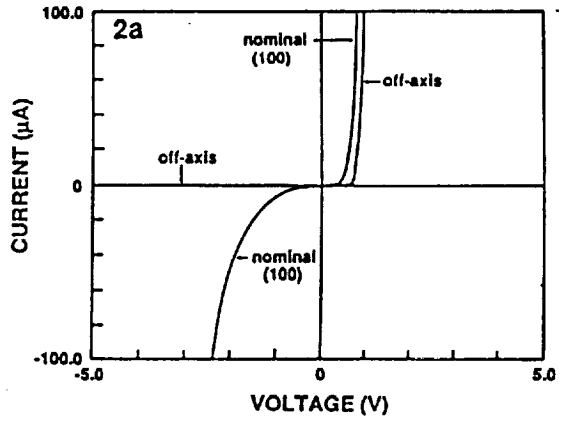
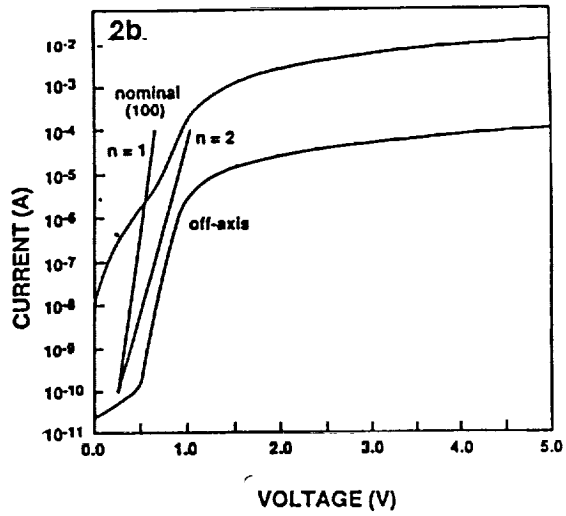


Fig. 1. Logarithmic dependence of current on voltage for: (a) Ideal SCLC conduction in an insulator. (b) Trap-free insulator with thermally generated free carriers. The slope changes from 1 to 2 when the injected carrier density exceeds the free carrier density. (c) An insulator with shallow traps and free carriers. (d) An insulator with deep-traps and thermal carriers.





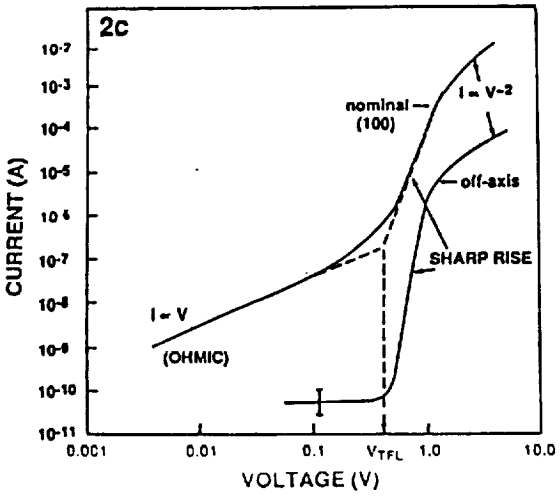


Fig. 2. (a) Linear plots of I-V characteristics for Au/β- SiC diodes on nominally (100) oriented (NASA 816/2) and off-axis <100> oriented (2° toward <011>) (NASA 816/6) silicon substrate. (b) Semilogarithmic plots of the forward characteristics presented in (a). (c) Logarithmic plots of the forward characteristics presented in Fig. 1. (a). Error bar represents maximum noise amplitude at low currents.

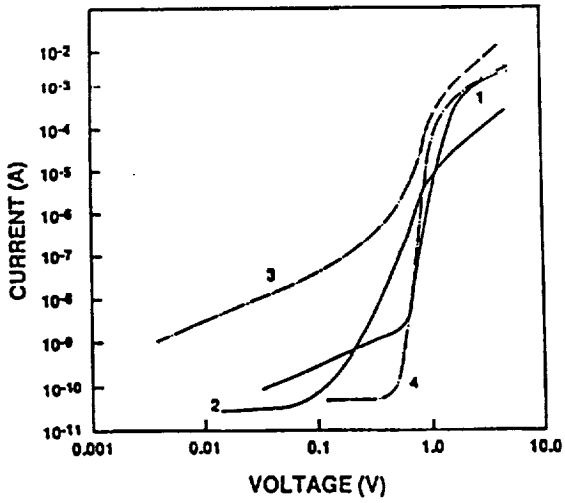


Fig. 3. Logarithmic plots of the forward characteristics of different diodes showing effects of localized nonuniformities in the carrier concentration and deep-level contributions. (1): 4° off-axis (100) Si (NCSU 870715), shows effect of higher carrier concentration than normal. (2): 2° off-axis (100) Si (NASA 721/6), shows effects of two closely located deep-levels. (3) Nominal (100) Si (NASA 816/2). (4) 4° off-axis (100) Si (NCSU 870626/1).

In a number of diodes in films on the off-axis substrates, a change in slope is observed at the end of a sharply rising current regime, as shown in Fig. 3, plot 2. This change in slope is interpreted to be due to the filling of two sets of closely located deep level traps. In NASA 721/6 these traps are 0.33 eV and 0.4 eV below the conduction band with concentration of unoccupied states of 1.2×10^{15} and 2.5×10^{15} cm^{-3}, respectively. A small number of diodes in 8707/5 also showed an ohmic regime at room temperature, as shown in Fig. 3, plot 1. Nonuniformities in defect distribution and carrier concentrations are suspected to be the origin of these observed features. At low forward biases, diodes fabricated in films on nominal (100) substrates conduct a much higher current than those on off-axis substrates. In a number of cases, an ohmic regime is initially observed (NASA 816/2) and the rise in current following V_{TFL} is not very sharp. In this case, $I \propto V^3$. This is considered to be an indication of smearing of the states due to electrical activity of crystallographic defects in the material [14]. However, for the simple analysis using Eqns. (1) and (2) only one discrete level is considered. In NASA 816/2, this level is located at 0.26 eV below the conduction band with a concentration of unoccupied states of 6.6×10^{15} cm^{-3}, whereas in NCSU 870130 a similar level is located 0.32 eV below the conduction band with 3.8×10^{15} cm^{-3} unoccupied states. When the shallower distributed traps are filled, the current rises sharply, and the characteristics are dominated by a deeper level at 0.38 eV in both NASA 816/2 and NCSU 870130 with concentration of unoccupied states as 3.8×10^{15} and 3.0×10^{15} cm^{-3}, respectively. In NCSU 870130, the current initially is proportional to $V^{1.6}$. This super-linear behavior appears to be due to an exponential distribution of traps. A value of N_0 of 3.1×10^{16} cm^{-3} eV^{-1} is obtained with eqn. (3) using the following: $\Delta = (m - 1)kT = 0.0156$ eV, $I = 1 \times 10^{-9}$A, $V = 0.054$V, $A = 7.8 \times 10^{-5}cm^2$, $\mu = 200$ cm^2/V sec, and $N_c = 1.5 \times 10^{19}$ cm^{-3}. The slope of the SCLC part of the I-V characteristics following trap-filling varies from 1.5 to 1.9. It is probable that a resistive component or high-level injection effects degraded the ideal slope of 2.0.

A previous microstructural study established the presence of antiphase domain boundaries (APB's) in the heteroepitaxial β-SiC films deposited on nominal (100) Si substrates. These faceted boundaries also contain a high density of dislocations. These defects are mostly eliminated by depositing β-SiC on off-axis (100) oriented Si substrates [9,15]. The density of defects other than APB's, mainly stacking faults and microtwins, is comparable in heteroepitaxial films grown on both nominal and off-axis substrates. The high density of deep level states distributed in energy below the conduction band is attributed to the electrical activity of the APB related defects. The observed deep-level states located 0.57 eV below the conduction band-edge in films grown on off-axis substrates appear to be native to β-SiC considering its close agreement to the theoretically predicted state associated with isolated Si vacancy at 0.61 eV [16].

CONCLUSIONS

Gold deposited on heteroepitaxial β-SiC films grown both on nominal (100) and off-axis (100) silicon forms rectifying contact diodes. Very low reverse leakage currents are observed in diodes fabricated in films grown on off-axis silicon substrates. Although the I-V and C-V characteristics indicate the presence of a barrier, the I-V characteristics are dominated by bulk effects rather than by thermionic emission over the barrier.

Logarithmic plots of the I-V characteristics in the forward direction indicate space charge limited current conduction through the active volume of the devices. The β-SiC films grown on nominally (100) oriented substrates show the presence of two deep levels located between 0.26 eV and 0.38 eV below the conduction band edge. In some films on nominal (100) substrates, the I-V characteristics are also influenced by some additional traps which are exponentially distributed in energy with a maximum occurring at the conduction band edge.

In contrast, β-SiC films deposited on off-axis substrates have only one deep level located approximately 0.49 eV below the conduction band edge for the 2° off (100) substrates and 0.57 eV for the 4° off (100) substrates. The shallower distributed deep states in the β-SiC on nominal (100) silicon substrates are attributed to the presence of antiphase domain boundaries in these films. The deep-level states located 0.57 eV below the conduction band-edge in films grown on

off-axis substrates appear to be native to β-SiC considering its close agreement to the theoretically predicted state associated with an isolated Si vacancy at 0.61 eV. The shallower discrete levels observed are believed to be related to crystallographic defects other than APBs.

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