N90-21324

COMMON SOURCE CASCODE AMPLIFIERS FOR INTEGRATING IR-FPA APPLICATIONS

James T. Woolaway

Amber Engineering Inc.

Santa Barbara, California

Erick T. Young

Steward Observatory

University of Arizona

Tuscon, Arizona

* Work sponsored in part through NASA contract NAS2-12578.

ABSTRACT

Space based astronomical infrared measurements present stringent performance requirements on the infrared detector arrays and their associated readout circuitry. To evaluate the usefulness of commercial CMOS technology for astronomical readout applications a theoretical and experimental evaluation has been performed on source follower and common-source cascode integrating amplifiers. Theoretical analysis indicate that for conditions where the input amplifier integration capacitance is limited by the detectors capacitance the input referred rms noise electrons of each amplifier should be equivalent. For conditions of input gate limited capacitance the source follower should provide lower noise. Measurements of test circuits containing both source follower and common source cascode circuits showed substantially lower input referred noise for the common-source cascode input circuits. Noise measurements yielded 4.8 input referred rms noise electrons for an 8.5 minute integration. The signal and noise gain of the common-source cascode amplifier appears to offer substantial advantages in acheiving predicted noise levels.

INTRODUCTION

An attempt has been made to correlate the theoretical and experimental noise performance for CMOS source follower and common-source cascode integrating amplifiers operating with temperature and bandwidth consistent with astronomical infrared measurement applications. Several CMOS process technologies were evaluated for low temperature noise performance. Theoretical performance predictions were made using the measured noise performance of each process and models developed for the Source Follower (SF) and Common Source Cascode (CSC) amplifiers. A test circuit was designed and fabricated using an advanced commercial 1.25um CMOS technology that contained both P & N channel amplifiers of the SF and CSC configurations. Measurements of the circuits were performed at Amber Engineering and the University of Arizona. The CSC circuits showed excellent noise performance and agreed well with theory. The SF circuits, however, exhibited much higher noise than was predicted.

PROCESS MEASUREMENTS

Three processes were evaluated for low temperature operability and noise. These were CMOS 3um, 2um, and 1.25um analog processes. Noise was evaluated for the P & N-channel MOSFETs of each process with the MOSFETs in a common source configuration. A HP-3582A spectrum analyzer was used to measure the output noise spectrum of each device. The gain of each circuit was also measured. Input referred noise voltage spectral density curves were obtained by dividing the output noise spectrum by the measured AC transfer function of the circuit.

The input referred noise spectra exhibited a classical behavior with the low frequency behaving as 1/f and the high frequency as thermal white noise. The measured 1/f and thermal noise voltage spectra were numerically fit. In addition to measurements of several processes, devices of differing sizes were measured for each process. For these devices the 1/f noise scaled as the inverse of the square root of the gate area as expected. The 1/f measurement results have been normalized to 1000um^2 gate at 1Hz and are presented in Table 1 below. Thermal noise levels were measured at about 1.5X of what was predicted by sqrt(8/3KT/Gm).

TABLE 1. (CMOS, 77 KELVIN, 1000UM^2, VOLTS/RTHZ)

Device	P-channel	N-channel
Process		
3um	1uV/rtHz	2uV/rtHz
2um	800nV/rt/Hz	1.2uV/rtHz
1.25um	200nv/rtHz	200nv/rtHz

INTEGRATED NOISE

The input referred noise voltage spectral density can be expressed as

$en^2 = en^2(1/f) + en^2(thermal)$

The RMS or integrated noise is then

$$Vn2 = \int_{f1}^{f2} (en(1/f)^2/f)df + \int_{f1}^{f2} en^2(thermal)\, df$$

This reduces to $Vnrms = \{en^2(1/f)[\ln(f2/f1)] + en^2(thermal)[f2-f1]\}^{1/2}$. For the 1.25um CMOS process a $1000um^2$ gate area would measure at about 600nV rms for integrated 1/f for a bandwidth of .01Hz to 100Hz. The 1/f voltage noise spectra measured (0.1Hz to 100Hz) was also integrated directly and was found to agree reasonably well with the theoretical expression above.

SOURCE FOLLOWER AND COMMON SOURCE AMPLIFIER THEORY [1,2]

The principle difference between the CSC and SF circuits is that the CSC circuit has a gain of approximately Rload*GM (20-50V/V) where the SF circuit gain is less then unity, typically .7V/V. Figure 1 shows the schematic diagrams for these circuits. The voltage gain of the SF amplifier is:

$Av = Vout/Vin = Gm1/(Gds1+Gds2+gm1(1+n)$ where $n=Gmbs/Gm1$

which approximately equals $1/(1+n)$ or 0.75 to 0.95 for bulk effect and no bulk effect, respectively. Similarly the voltage gain of the CSC ampfifier is:

$Av = Vout.Vin = -Gm1(Gds2+gm2+gmbs2)/[Gds1Gds2+Gds1Gds3+Gds2Gds3+Gds3(Gm2+Gmbs2)]$

which is approximately $-Gm1/Gds3$ or about -10 to -50. It is important to note the effectiveness of the cascode in reducing the gain to the drain of M1. The gain to M1 or Miller gain is:

$Av(Miller) = Vd(m1)/Vin = -2Gm1/(Gm2+gmbs2)$ or about -2 to -3.

The cascode reduces the Miller gain to from -10 to -50 to -2 to -3. This is significant as the Miller gain multiplies the parasitic capacitance between the gate and drain of the input transistor.

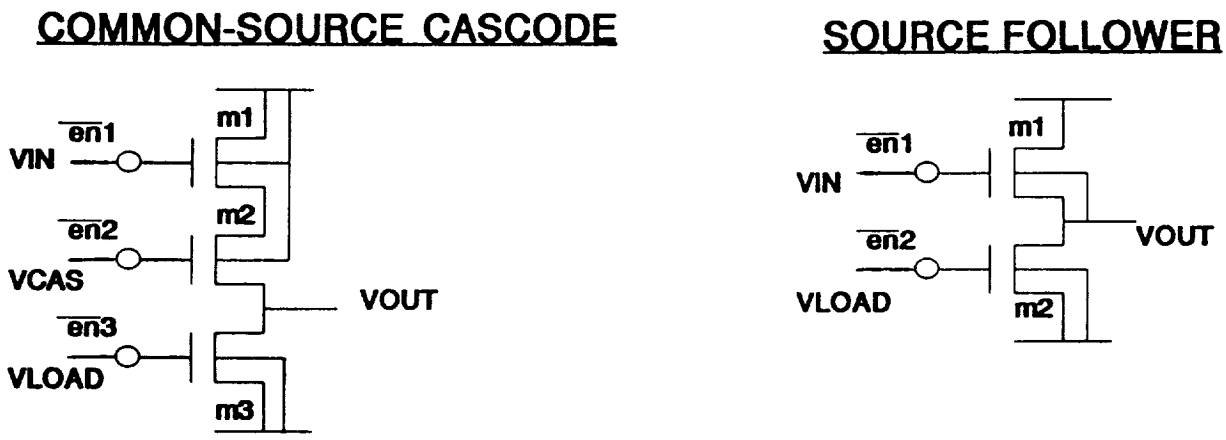


FIGURE 1. COMMON SOURCE CASCODE AND SOURCE FOLLOWER CIRCUIT CONFIGURATIONS

PREDICTED NOISE PERFORMANCE

The measured MOS noise characteristics showed classical behavior with 1/f and thermal noise characteristics. These noise sources appeared as noise voltage sources at the input or gate of the MOSFET. The noise performance of the MOS integrating amplifier can be expressed in terms of the integrators input referred noise voltage and the total integration node capacitance (including detector capacitance and Miller). This relationship is drawn from:

$$Q = nq = C*V = Ctotal*Vn(rms)$$

The input referred rms noise electrons can be expressed as:

$$e\text{-}(rms) = Ctotal*Vn(rms)/q$$

The total capacitance of the integration node is composed of the capacitance of the detector, the detector to input circuit interconnect, the source or drain diffusion to bulk capacitance of the reset transistor, the capacitance of the gate of the input MOSFET, and other similar components. For simplicity this analysis assumes all stray capacitance with the exception of the gate capacitance is lumped into the detector capacitance term.

$$Ctotal = Cgate + Cdetector$$

It is also useful to limit this analysis to the condition where the SF and CSC circuits are operating in saturation. In saturation SF gate capacitance is approximately equal to one minus the SF gain multiplied by the gate to source capacitance (0.1(Cgs) to 0.3(Cgs)) and the CSC configuration gate capacitance is approximately equal to the gate to source capacitance. Where Cgs is Approximately equal to CoxWL (Cox

= [EE0/Tox], and E & E0 are the Dielectric constant for SiO2 Permittivity in a vacuum and Tox is the thickness of the oxide).

Technology	Gate Capacitance
1.25um technology	[1.53ff/um^2]
3.0um technology	[0.6ff/um^2]

The input referred rms noise electrons for the SF and CSC circuits can be expressed as

e-(rms,SF) = (*Cdet*+*COX*WL*0.1)*Vn*(rms)*/q

e-(rms,CSC) = (*Cdet*+*COX*WL)*Vn*(rms)*/q

The input referred noise of the MOSFET is proportional to one over the square root of the gate area. The input referred noise voltage for a MOSFET of arbitrary size can be expressed in terms of the input referred noise of a MOSFET with gate area of 1000umsq:

$En^2(1/f) = en^2(1/f\ 1000umsq)$*sqrt(1000*umsq*/GateArea *squm*)

for 1/f dominated noise performance

$Vn(rms) = [En^2(1/f)*\text{sqrt}(\ln(f2/f1))]^{1/2}$

where En is the 1/f noise voltage per rtHz at 1Hz and f1 and f2 define the sampling band width. Combining we can express the input referred rms noise electrons for the SF and CSC as

$e\text{-}(rms,SF) = (Cdet + COX WL*0.1)(1/q)(en(1/f1000um^2))(\text{sqrt}(1000um^2/WL um^2)^{1/2}(\ln(f2/f1))^{1/2}$

$e\text{-}(rms,CSC) = (Cdet + COX WL)(1/q)(en(1/f1000um^2))(\text{sqrt}(1000um^2/WL um^2)^{1/2}(\ln(f2/f1))^{1/2}$

Figures 2 and 3 show the calculated input referred rms noise electrons of the SF and CSC circuits fabricated in 1.25um CMOS for varying gate area and stepped Cparasitic. These figures are based on calculations using the measurements of gate referred voltage noise and the expression derived above. The Cdet term in Figure 2 is stepped from 0 to 1.0pF by 0.2pf where Figure 3 Cdet is stepped from 0 to 10pF by 2.0pf. These calculations show a low in the rms input referred noise electrons for each value of parasitic capacitance with the minimum moving to larger gate areas with increased Cparasitic. The calculations were based on the following:

f1 = .01Hz
f2 = 100Hz
En*(1/f 1000umsq)* = 1uV/rtHz at 1Hz for 3um technology
En*(1/f 1000umsq)* = 200nV/rtHz at 1Hz for 1.25um technology
Gate Capacitance = 0.69ff/um for 3um technology
Gate Capacitance = 1.53ff/um for 1.25um technology

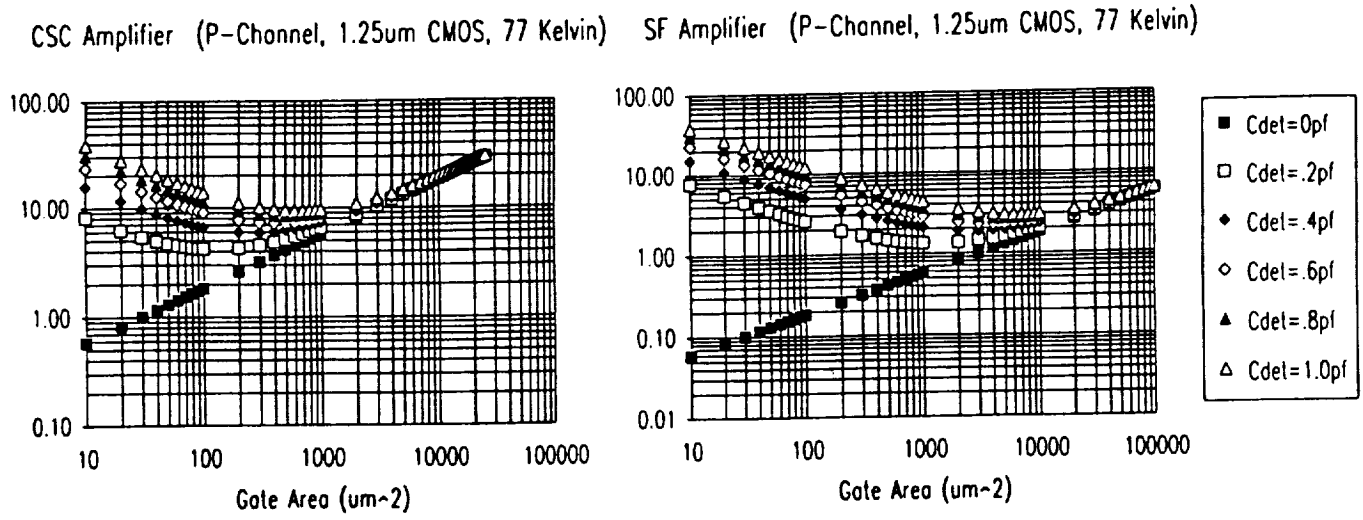


FIGURE 2. COMMON SOURCE CASCODE AND SOURCE FOLLOWER NOISE PREDICTIONS

(RMS E- VS. INPUT CAPACITANCE [0.2PF STEPS] & GATE AREA)

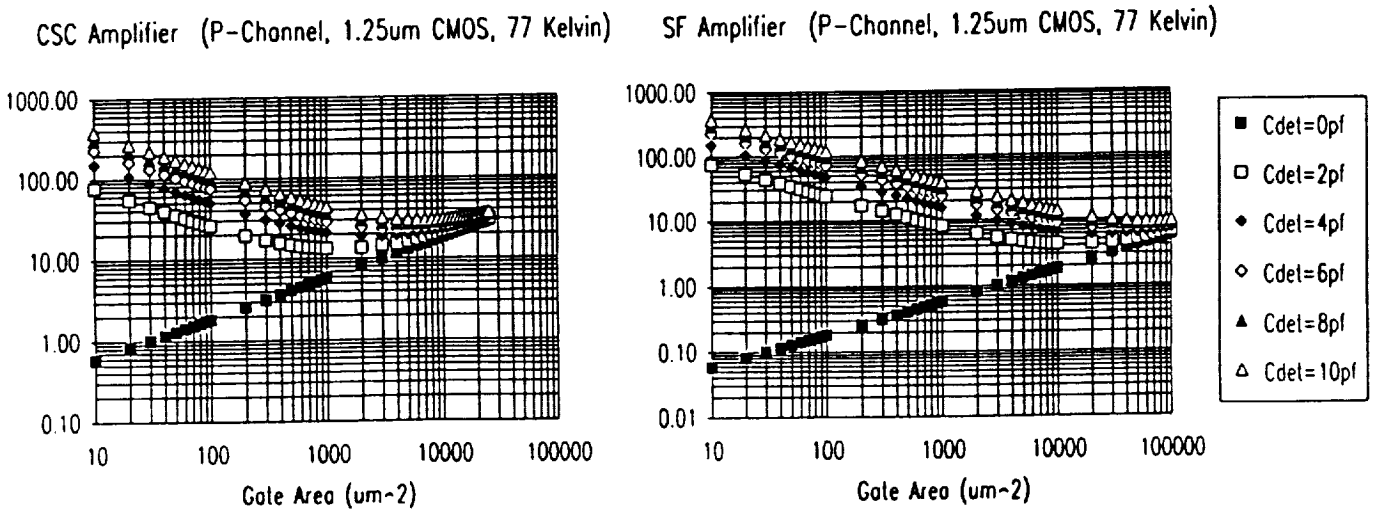


FIGURE 3. COMMON SOURCE CASCODE AND SOURCE FOLLOWER NOISE PREDICTIONS

(RMS E- VS. INPUT CAPACITANCE [2.0PF STEPS] & GATE AREA)

TEST CIRCUIT DESCRIPTION

A test circuit containing four reset integrator circuits was designed and fabricated in 1.25um CMOS. The four versions of the input circuit consist of SF and CSC designs implemented in both P and N type MOSFET's. These circuits are shown in Figure 4.

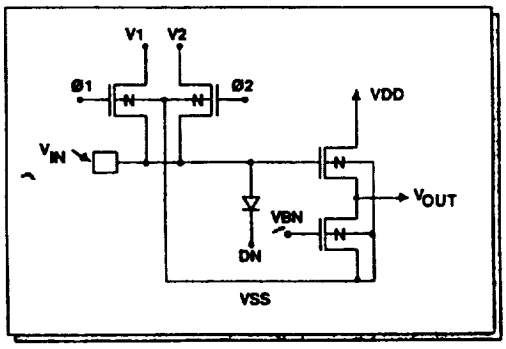
The operation of the reset intergator test circuits is based on the integration of the detector current on a capacitive node. The change in potential on the capacitive node is used to modulate the potential of the gate of the input MOSFET. The MOSFET output voltage is sensed non-destructively to measure the total integrated detector current.

Two means of determining the input node capacitance were incorporated into the design for each circuit. The first was a p/n photo diode connected to the input of each amplifier to allow the optical stimulation of input current. An additional photo diode was provided with direct connection to the test set to provide a reference for the test input current source. The photo diode current would cause a change in the input node potential $I = CdV/dT$. Since the input to output voltage transfer function can be measured directly, the input capacitance can be determined. The input node is also connected to two small switch MOSFET's with gates PHI1 and PHI2. The additional reset MOSFET to the input node of the circuit was provided to allow a switched capacitor resistor measurement of the input node capacitance.

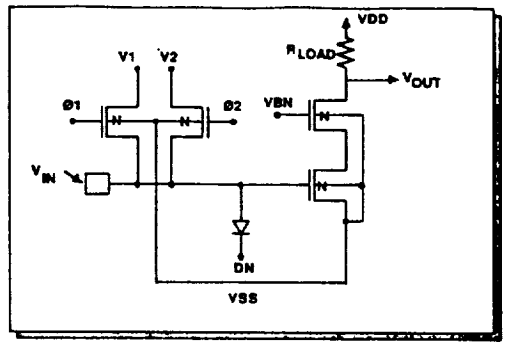
All four circuits are laid out with the input MOSFET W/L at 50/10. The sum of the estimated capacitance of the reversed biased 10 x 10 um test input diode and 85 x 85 um input pad is 250 fF. The input gate capacitance is estimated to be 750 fF. The effective gate capacitance is expected to be lower than this depending upon the circuit operation. For the SF configuration, most of the capacitance is between the gate and source. However, since the source varies in phase with the gate, the effective capacitance is reduced by one minus the SF gain.

With the CSC circuit the MOSFET is in saturation and the depletion region is increased reducing the effective gate capacitance. The gate to drain capacitance is kept low by using the cascode MOSFET which reduces the Miller capacitance between the gate and drain. The total input node capacitance of the CSC amplifier is expected to be somewhat less than the sum of the input pad, diode, and input gate. The SF total input node capacitance is expected to be about half of the above sum or about 500fF.

All four circuit versions have static protection devices on all pads except for the small internal input pads. Diodes to VDD and VSS with resistive input routing on the pads are used for the static protection.



N-channel Source Follower Input Circuit



N-channel Common Source Cascode Input Circuit

FIGURE 4. COMMON SOURCE CASCODE & SOURCE FOLLOWER TEST CIRCUIT

TEST MEASUREMENT RESULTS

Measurements of the test circuits were performed at Amber Engineering and at the Steward Observatory Detector Laboratory at the University of Arizona. Measurements at Amber were performed at 77 Kelvin for a bandwidth of 0.1Hz to 100Hz. Steward Observatory measurements were made at 28 Kelvin with a bandwidth of 620 micro-Hertz to 10 Hertz.

MEASUREMENT TECHNIQUES

Three basic measurements were performed at Amber and the University of Arizona on the reset integrator test circuits. These measurements were transfer function, input node capacitance, and input referred noise spectral density. These measurements were all performed using the measurement techniques described below.

TRANSFER FUNCTION

The voltage transfer function (TF) relates the circuit output voltage to the circuit input voltage. The TF is measured with the test device operating at nominal bias conditions. A 220K ohm resistor was used to load the CSC circuits. The on chip current source was used for the SF circuits. These measurements were performed using the HP4145A Parameter Analyzer to supply the DC and ramped voltages and to measure the output voltages. The AC gain was verified by connecting the input to a sine wave source and then measuring the amplitude response of the circuit output.

CAPACITOR MEASUREMENT

The input node capacitance was measured while the circuit is in operation by using a switch capacitor technique with switches PHI1 and PHI2. The circuit is biased in its dynamic range as in the transfer function measurement with the exception of PHI1, PHI2 and V2. V2 is set to produce a mid-scale output when PHI2 is turned on and PHI1 is turned off. V1 is swept from V2-delta to V2+delta where delta is about .1 volt for the CSC circuits and 1 volt for the SF circuits. As V1 is slowly swept, PHI1 and PHI2 are clocked with non-overlapping 30% duty cycle pulses with a period T. The current (I) from V1 to V2 is measured.

The input node capacitance can be calculated from:

$$I = C (V1-V2) / T$$

The period T was made short enough to produce a measurable current but also must be long enough that the input node capacitance can be fully charged through PHI1 to V1 and discharged through PHI2 to V2. A value of 5 to 100 microseconds is appropriate for the period T.

NOISE MEASUREMENTS

For the noise spectral density measurement the circuit is biased as in the transfer function measurement above with the addition that V1 is biased to produce a mid_scale output(input diode reversed biased). PHI1 is turned off, ending the reset process isolating the input node potential near V1.

Measurements performed at Amber utilized a HP3561A Dynamic Signal Analyzer to measure output noise spectral density in the bandwidth of 0.1Hz to 100Hz. Steward Observatory laboratory measurements were made using a successive differencing apparatus capable of measuring noise over integration times of 20 minutes. In both facilities the measurements were made after the reset process, so the KTC reset noise is correlated during the measurement procedure and dose not contribute to the measurement noise.

The output noise spectral density is then divided by the voltage gain of the input circuit to yield the input referred noise spectral density. The input referred rms voltage noise can be expressed as rms noise electrons by multiplying the noise voltage by the capacitance and dividing by the electronic charge.

MEASURED PERFORMANCE

The results of the gain, capacitance, and noise measurements taken on the reset integrator test circuit are summarized in Table 2 and Table 3.

	Gain	Cap.	Noise	A1/f@1Hz	Predicted	
	v/v	pf	uv rms	e rms	uv/rt(Hz)	e rms
NCS	27.6	0.68	1.6	6.8	0.44	3.6
PCS	26.9	0.66	1.9	7.7	0.44	3.6
PSF	0.84	0.43	14	38	3.0	3.0
NSF	0.75	0.44	n/a	n/a	n/a	n/a

TABLE 2. SUMMARY OF AMBER MEASURED GAIN, CAPACITANCE, AND NOISE RESULTS FROM RESET INTEGRATOR TEST CHIP.

Temp Kelvin(Start)		28.86	28.62	28.62	29.8	
Temp Kelvin(Stop)		28.64	28.62	28.62	29.03	
Bandwidth(f1,f2)		(Noise data in rms e-)				Predicted
40mHz	10Hz	5.4	5.2	5.4	5.2	2.9
20mHz	10Hz	4.4	4.7	5.1	6.1	3.0
10mHz	10Hz	4.0	5.1	4.8	9.2	3.1
5mHz	10Hz	4.8	4.3	4.8	16.2	3.3
2.5mHz	10Hz	5.4	5.1	5.7	29.8	3.5
1.2mHz	10Hz	10.0	5.8	4.8	55.7	3.6
620uHz	10Hz	n/a	n/a	n/a	89.6	3.7

TABLE 3. SUMMARY OF STEWARD OBSERVATORY TEST RESULTS.

The SF circuits tested at Amber measured about 30 to 40 rms e-. Steward Observatory measurements were similarly above 25 rms e-.

The data in Tables 2 and 3 show a potential advantage that the CSC circuit has over the SF circuits for noise performance. Here the voltage gain in the front end of the CSC circuits elevates both the signal and the noise voltages to levels 20 to 30 times that of the SF circuits. This may allow the input cell and signal path to be less susceptible to interface electronics and post chip noise sources and more importantly it may reduce the noise sensitivity of the input circuit to the switching and multiplexing electronics on chip.

1X32 ELEMENT COMMON SOURCE DEVELOPMENT FOR SIRTF

An array of 32 CSC input amplifiers is in development for the SIRTF high capacitance long wave length detectors. Figure 5 shows the layout for a single channel of the 1 x 32 readout. The performance perditions for this array are about 60 and 30 rms electrons for 2um and 1.25um CMOS technologies for a 10pF total input capacitance and a bandwidth of 0.1Hz to 100Hz.

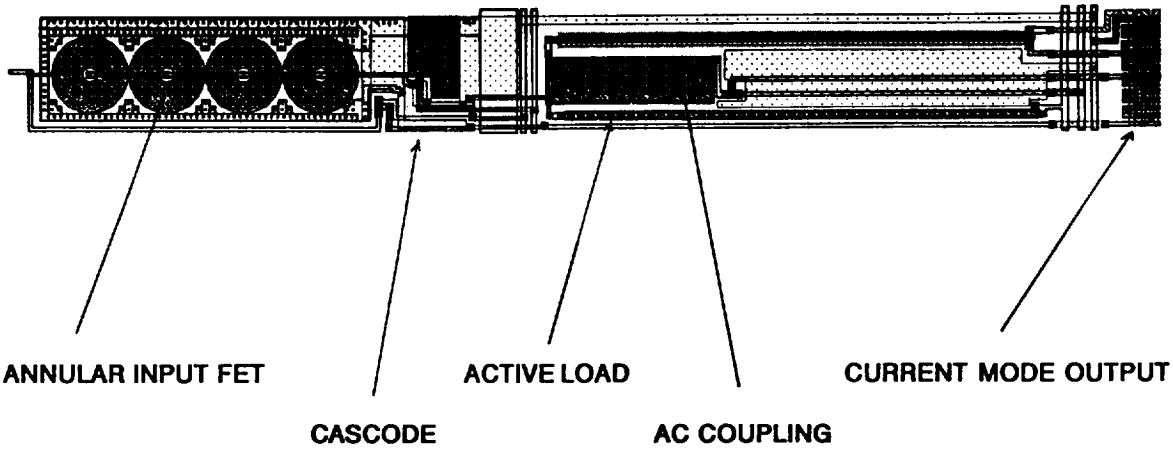


FIGURE 5. SINGLE CHANNEL COMMON SOURCE CASCODE AMPLIFIER CELL FOR 1 X 32 SIRTF HIGH CAPACITANCE DETECTOR ARRAY

SUMMARY

Measurement and theoretical performance perditions based on CMOS process performance measurements agreed extremely well for the CSC input amplifiers. The SF configuration, however, showed much higher noise than predicted. Both input circuit configurations should provide excellent noise performance for low detector and input stray capacitance focal plane arrays.

In the case where the input capacitance is dominated by the detector capacitance, input referred noise performance for the CSC and SF circuits should be identical. The SF should achieve low noise for gate capacitance limited conditions. This was not seen in our measurements of the SF test circuit.

For the bandwidth discussed of .01Hz to 100Hz with a total parasitic detector and stray capacitance at 0.5pF input referred RMS noise electrons should be around 27e- and 8e- for 3um and 1.25um CMOS technology. The availability of CMOS processes is abundant with competitive commercial sources. Processing is relatively low cost and yields are high. Readout processing capabilities and input cell sizes and power requirements should be compatible with large starring arrays for formats to greater then 128x128 elements. The size limitations will be imposed by hybridization and detector yield and not readout fabrication.

The key to realizing this performance will be in the multiplexer architecture and the careful shielding of on and off chip noise sources from the input cell and signal path.

ACKNOWLEDGEMENTS

We acknowledge the important contributions of Chris Fletcher for the layout of the SF and CSC test circuit, Glenn Kincaid for layout of the 1 x 32 CSC array for SIRTF, John Blackwell for noise and test circuit performance testing, and Dr. William Parrish for technical discussions. Work sponsored in part through NASA contract NAS2-12578 through a University of Arizona subcontract.

REFERENCES

1. P. Gray and R. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 1984

2. P. Allen and D. Holberg, "CMOS Analog Circuit Design", Holt Rinehart and Winston Inc., 1987