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HgCdTe 256x256 MWIR FPA

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Abstract

We have developed a HgCdTe 256x256 focal plane array (FPA) which operates in the 1-5 μm band. This is presently the largest demonstrated HgCdTe FPA. The detector material is HgCdTe on sapphire (PACE-1 technology) which has a low thermal expansion mismatch with silicon. The multiplexer is a CMOS FET-switch device processed through a commercial silicon foundry. The multiplexer input is direct injection and the charge capacity is about 2×10^7 electrons. The kTC limited read noise is 400 electrons. We have demonstrated high background imaging using the device. The broadband quantum efficiency is measured to be 59%. Dark currents less than 0.1 pA have been measured at 77K for detectors processed on PACE-1 material with 4.9 μm cutoff. The dark currents decrease as the temperature is lowered and we are presently studying the T<77K characteristics. The interconnect yield is >95%. The devices are available for astronomical applications.

Material

The detector array material is HgCdTe on sapphire called PACE-1 (Producible Alternative to CdTe for Epitaxy). A layer of CdTe is deposited onto the sapphire first using vapor phase epitaxy. The HgCdTe is grown by liquid phase epitaxy. The sapphire substrate is strong, durable and has large area (2 inch diameter wafer) which is crucial for large arrays such as a 256x256. The sapphire is transparent up to 5.5 μm and this technology is used for the 1.0-5.5 μm band. For longer wavelengths (8-12 μm) we are developing HgCdTe on GaAs (PACE-2) technology.

Detector Array

The photovoltaic detectors are planar structures formed by ion implantation. After passivation indium columns are deposited for hybridization to the multiplexer. The detector unit cell size is 40 μm x 40 μm. Typically over 90% fill factor is obtained with less than 2% crosstalk.

We have characterized the detectors at 77K. The R_oA is typically 10^6 to 10^7 Ω-cm^2 and the dark current is less than 0.1 pA for 100 mV reverse bias. The dark currents decrease further as the temperature is lowered. George Rieke, University of Arizona,

measured 30-60 e-/s at 30-35K for detectors with similar cutoff but larger area. These detectors have not been optimized for low temperature (<77K) operation; with further work the dark current can be reduced to lower levels.

Multiplexer

The multiplexer has a CMOS FET-switch architecture and is processed at a commercial silicon foundry. A schematic is shown in Figure 1. The input is direct injection and the charge is integrated on a capacitor. The charge capacity is about $2x10^7$ electrons and the kTC limited read noise is 400 electrons. The dynamic range is about 50,000. The integration time can be varied from 0.5 to 99.5% of frame time. Three clocks and four bias voltages are needed to operate the device.

Focal Plane Array

The FPA is fabricated by mating the detector array and the multiplexer through the indium columns (Figure 2). Interconnect yields of above 95% were obtained and 99% yields similar to the 128x128 FPAs are possible. A concern is the reliability of large area hybrid structures. We have thermally cycled 256x256 test structures (more than 100 times) and MWIR FPAs (more than 20 times) between room temperature and 77K with no mechanical or electrical degradation. The excellent reliability is a result of the PACE-1 material having low thermal expansion mismatch with silicon. A photo of the 256x256 FPA mounted on a 68 pin chip carrier is shown in Figure 3.

Initial characterization tests show that the mean broadband (no filters) quantum efficiency is 59% at 77K (Figure 4). Higher quantum efficiencies (>70%) are possible as evidenced from 128x128 FPA results. At short wavelengths (1 μm), >50% quantum efficiency is observed. We are presently continuing the characterization of the FPA.

Summary

We have developed a HgCdTe 256x256 focal plane array (FPA) which operates in the 1-5 μm band. The detector material is HgCdTe on sapphire (PACE-1 technology) and the multiplexer is a CMOS FET-switch device. The FPA charge capacity is about $2x10^7$ electrons with a read noise of 400 electrons. The mean broadband quantum efficiency is measured to be 59%. Dark currents less than 0.1 pA have been measured at 77K. The dark current can be further lowered by decreasing the temperature of operation. These devices are available for astronomical applications.

Acknowledgments

256 X 256 MULTIPLEXER
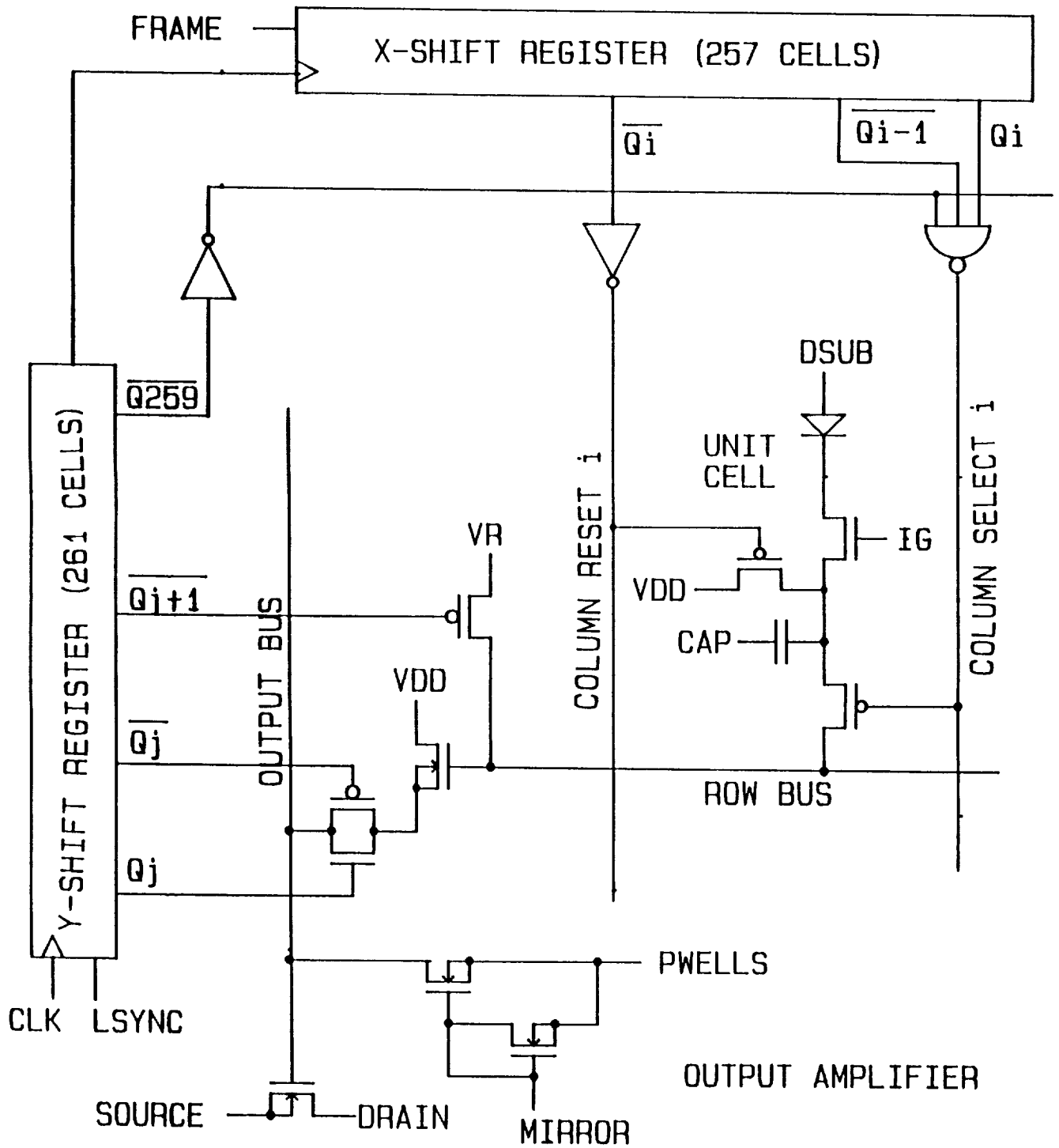
FIGURE 1.   256x256 CMOS Multiplexer Schematic

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PACE-1 HYBRID FOCAL PLANE ARRAY

SC40003A

SWIR/MWIR
INFRARED
RADIATION

DETECTOR
ARRAY

Si PROCESSOR

SAPPHIRE
SUBSTRATE

HgCdTe EPITAXIAL LAYER

INDIUM BUMP

Si SIGNAL PROCESSOR

HgCdTe DETECTOR ARRAY
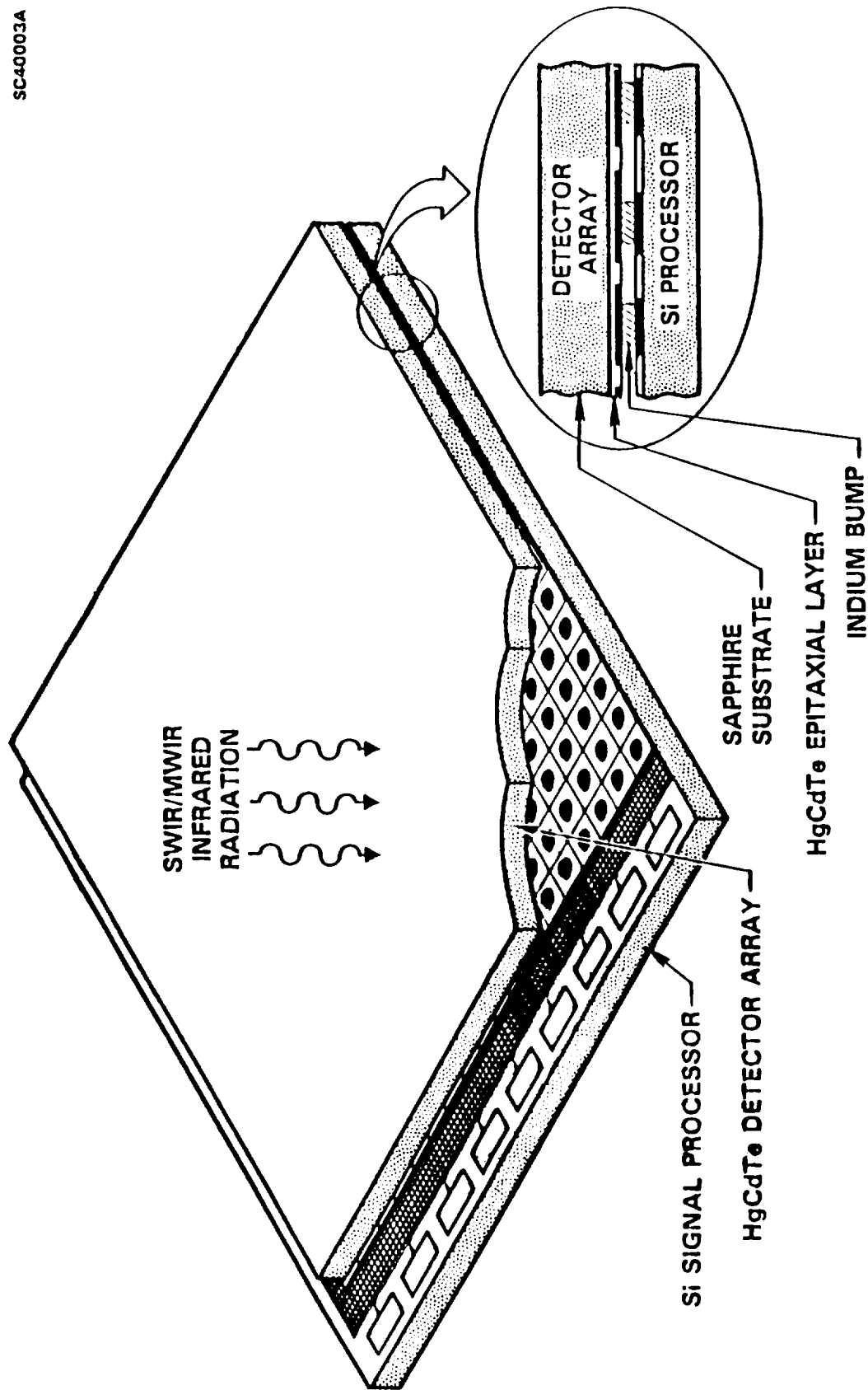
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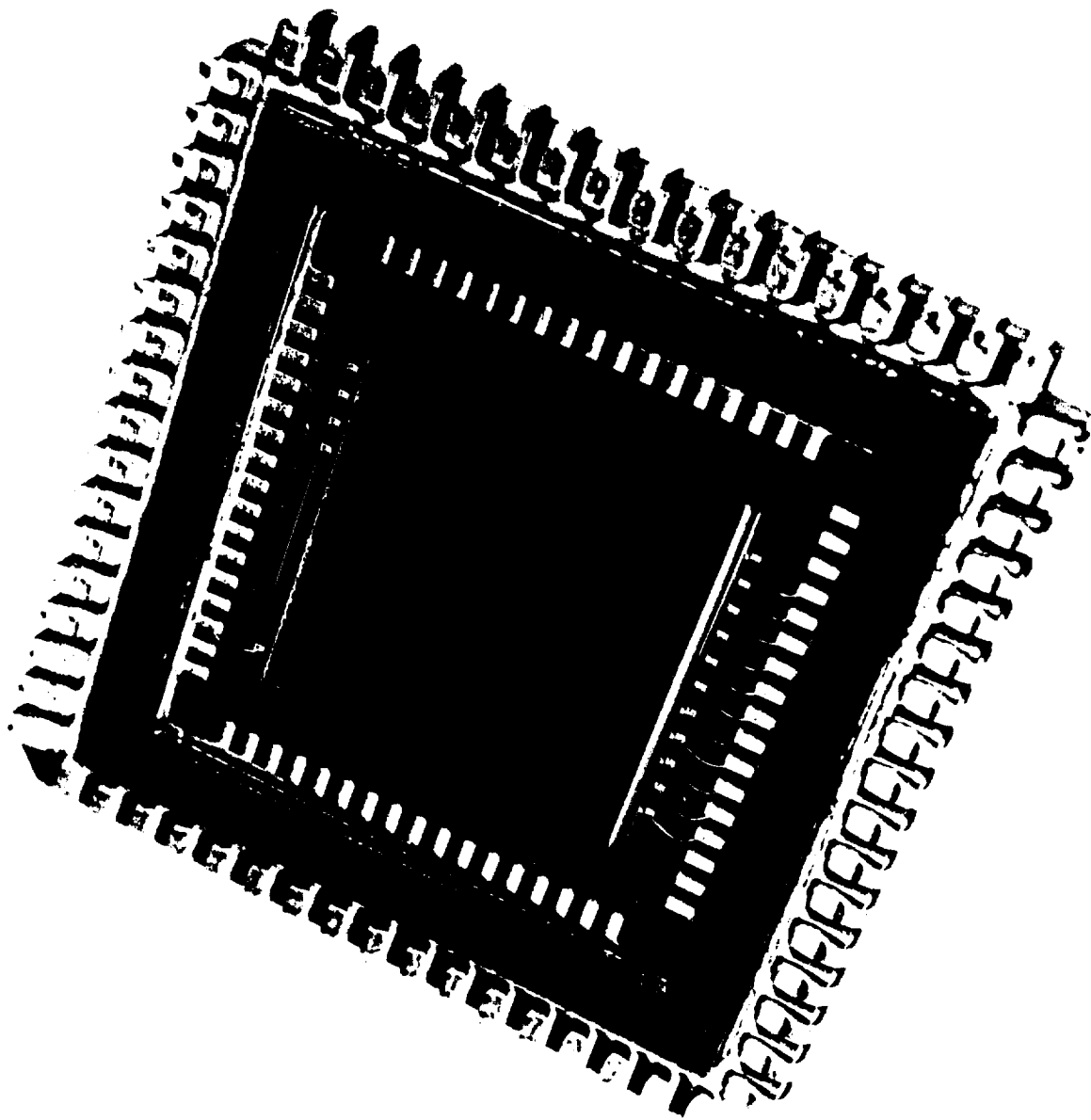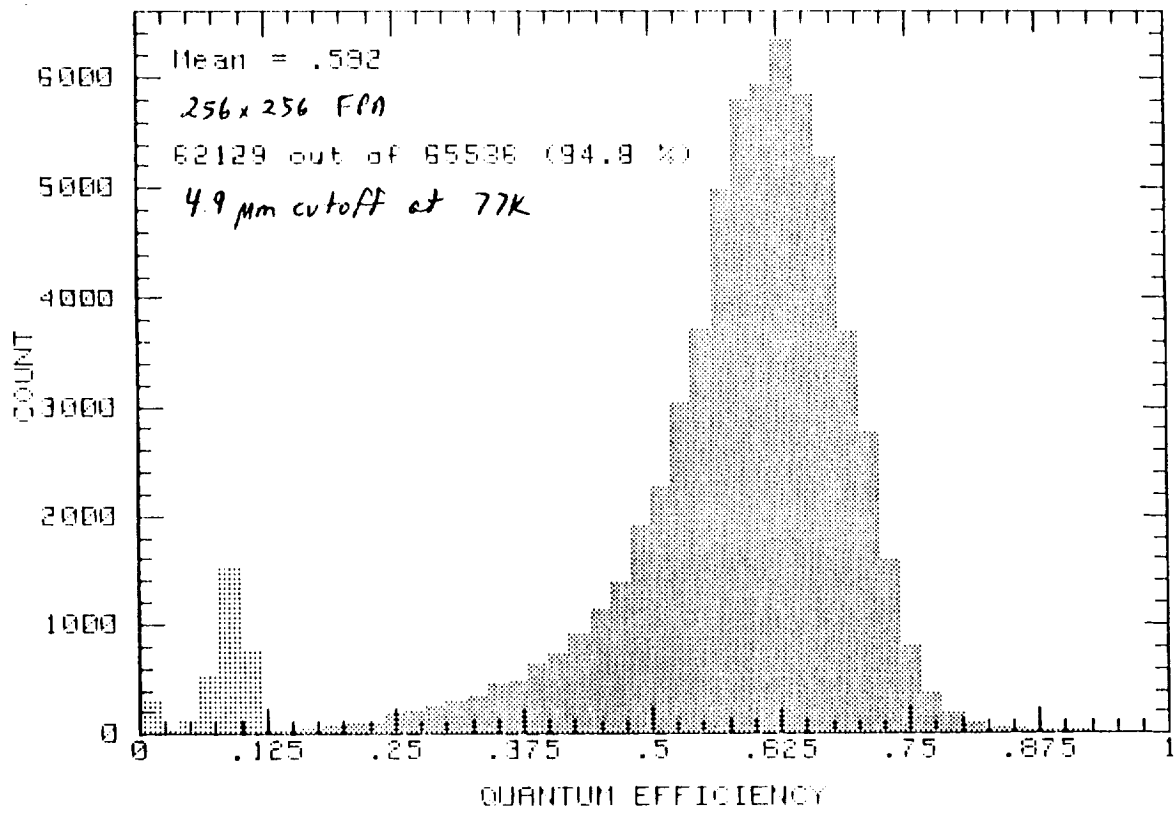FIGURE 2. Hybrid Focal Plane Array Cross Section

FIGURE 3. 256x256 FPA

FIGURE 4. Quantum Efficiency of 256x256 FPA

HIGH SPEED, LOW READ NOISE ELECTRONICS
FOR ASTRONOMY DETECTOR ARRAYS

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Abstract

The third generation electronics system of the Berkeley infrared camera has been built with improved frame rate, size, manufacturability, and real-time data processing power. The flexibility to easily operate a variety of detectors and the vast improvement in speed was achieved by using Motorola DSP56001 Digital Signal Processors[1,2] (DSP) to serve as controllers and processing elements throughout the system. The new data acquisition system has one DSP per analog channel, making the system scalable to match the sensor being used. Each channel can run up to 1 MHz sampling rate (A/D limited) using 20% of the DSP's 10-30 MIPS bandwidth for interrupt driven data acquisition, leaving 80% for background processes. The A/D is presently a 1 MHz 12 bit unit. The conversion resolution is enhanced by a pattern subtraction system allowing the removal of the first order signal and digitization of the amplified residual.

The analog board is dynamically configurable and is capable of performing self diagnostics and calibration. A DSP56001 is also used in the timing generator, which outputs patterns at a rate up to 10MHz and has a fine timing adjustment of 2 nsec using programmable delays. The computer system hardware and software are layered, supporting real-time interrupt response down to the microsecond level. The system is is the prototype for the electronics for the 1-5 μm and 8-24 μm cameras being designed for the Keck Ten Meter Telescope.

Introduction

High speed electronics is required for the high photon fluxes encountered when observing at wavelengths longward of 2.5 μm. Low read noise is required at shorter wavelengths or
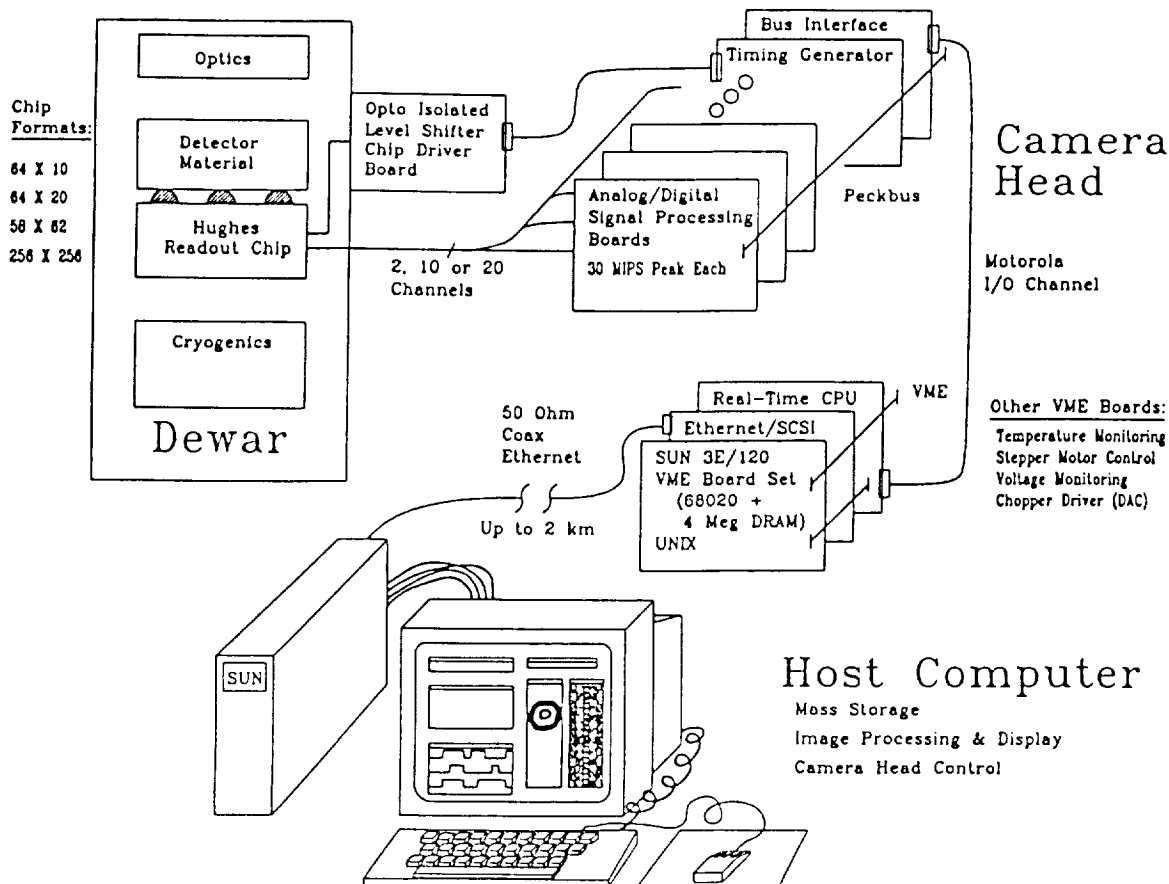

Fig 1 System Block Diagram

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narrow bandwidths, where the charge and the statistical variation in the charge collected in a pixel are small. The old Berkeley infrared camera[3,4,5] operated at 10 μsec/pixel/channel peak rate, forcing the use of narrow bandwidths. In the new system, the pixel read time has been decreased to 1 μsec, allowing observations over the full 8 to 13 μm atmospheric window.

The new system's speed is achieved by incorporating high speed, highly integrated single chip computing elements on every analog amplifier chain. The Motorola DSP56001 was chosen for this task.

The camera system, Figure 1, is based on a four level hierarchy. The components are: a Sun workstation in the control room, a Sun 3E/120 VME card set on the camera head running Unix, a Parity Inc. 68020 single board computer in the VME rack running Magic/L[6], and a bank of DSP56001s in the analog rack running optimized hand coded assembly routines. UNIX gives us the powerful development environment and transparent access to the camera head over Ethernet. The camera control, data acquisition, and DSP monitor software are written in Magic/L, which is an interactive language developed by Loki Engineering Inc. that looks like C or Pascal but works like Forth allowing spontaneous code creation and use. It is most useful for hardware debugging and user interface environments. The DSP assembly code was developed using the Motorola development package and our look-alike debugger running on the targets. The software system breaks new ground in the layering of the application by putting the vast majority of the code on a single host processor and only the core of the application on the front end DSPs.

The use of commercial VME cards and the use of VME sized Eurocards for the timing generator and analog boards allowed for a compact package as shown in Figure 2.

Low Noise on a Mixed Analog and Digital Board

The amplifier board block diagram is shown in Figure 3. It is a highly configurable pulse amplification system with support for diagnostics and self calibration. A feature of the system is variable bandwidth in the analog chain. As the gain is increased and integration time increased for low signal level conditions, the bandwidth of the analog channel is decreased to reduce the noise bandwidth of the system. In the low gain (=5) setting, full scale pulse settling time to 12 bits is 100 nsec from input to A/D. The
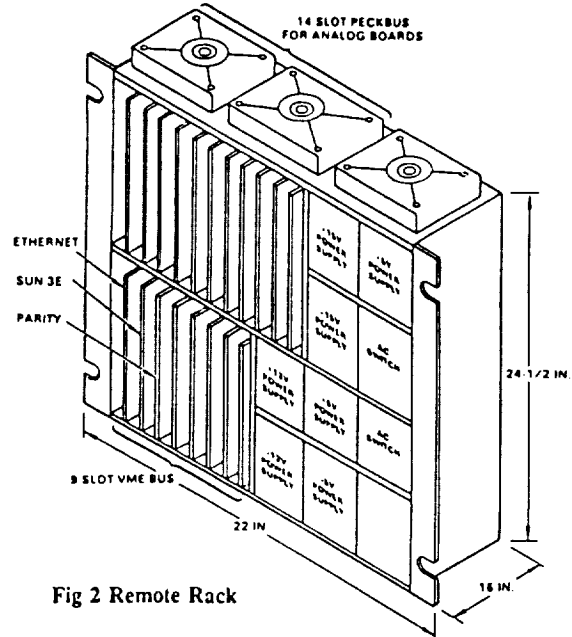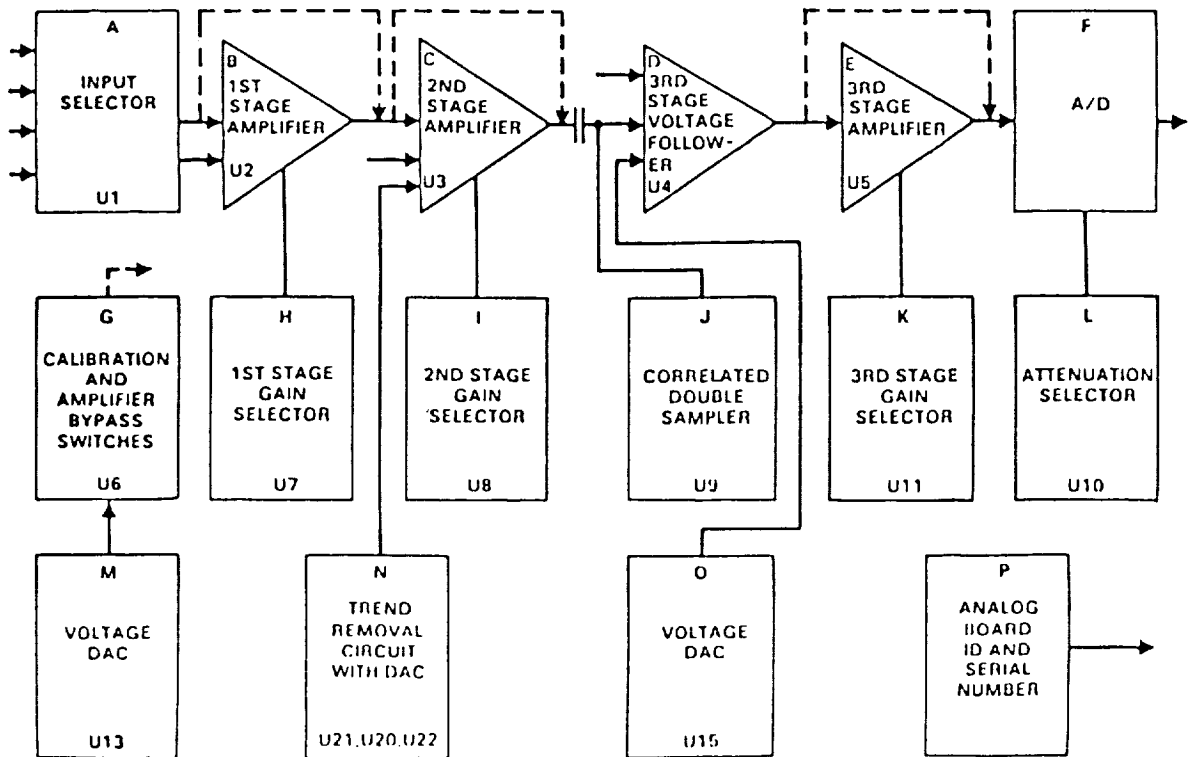
Fig 2 Remote Rack

Fig 3 Analog Block Diagram

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amplifiers used are the OEI AH0013 JFET preamp and the Harris 5195 high speed fast settling opamp. The system also incorporates a fixed pattern subtraction circuit to remove the first order pattern from the chip, allowing use of higher gains into the A/D and therefore higher resolution. Correlated double sampling is used to eliminate the 1/f noise (DC instability) inherent in the readout MOSFETS as shown in the timing diagram in Figure 4.

In Figure 1, the bus interface logic represented by block "P" was a dozen ICs on the prototype board. In the production run, these ICs were replaced by three CMOS programmable logic devices (PLD) and the DSP56001, using less space on the board and eliminating the separate digital board. The PLDs were the XL78C800[7] from EXEL, an extremely flexible 800 gate equivalent electrically erasable application specific integrated circuit (ERASIC).

All timing and digital clocks are generated from a central 20 MHz clock on the timing generator board. The timing signals are transmitted differentially over the backplane using high speed parts (75ALS194/5). The fine adjustment on the timing signals is in 2 nsec increments so that the noise critical sampling time can be moved to a quiet period between digital transitions. This feature should allow the system to approach the noise performance of the previous generation Berkeley camera electronics which had 20 μvolts rms noise. Low noise measurements on the new system are yet to be completed.

Coadder

The system has a DSP on each of the 20 analog channels that coadds in 700 nsec with interrupt signals, or 200 nsec in bursts with an input FIFO. The old camera had a coadder external to the analog box, requiring 5 μsec to coadd ten pixels. The DSP and PLDs also implement the bus interface logic, reducing the complexity of the analog board.

Timing Generator

The timing generator uses a DSP56001, is situated in the analog rack, and is the source of the clock and timing for all camera functions. The DSP56001 enables the timing generator to be built with a small number of chips. Because its characteristics are determined by software it can be programmed for a variety of observing modes, and it is functionally open-ended to support lab testing.

DSP Operation

16 bit DSPs have been available for many years. Motorola's DSP56001, which became available in 1987, has a 24 bit word size and 56 bit accumulators, which allows processing real data without roundoff. As shown in Figure 5, the chip is massively parallel and incorporates peripheral chip functions making it very easy to use. The Host Port and the Host Command facility made hardware and software design simple. The
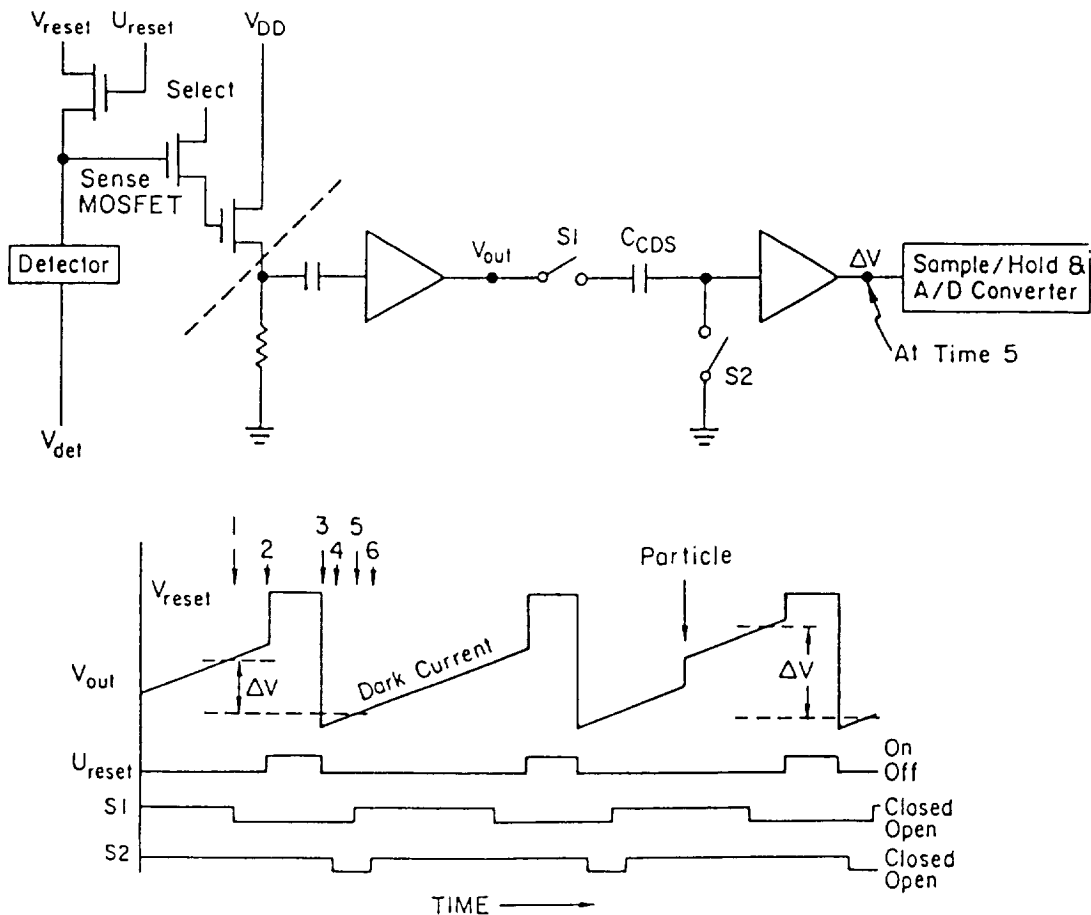

Fig 4 Correlated Double Sampling

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DSP host port is interfaced to the Peckbus[8], a minimal bus using CMOS levels that is trivial to interface to and works with extender cards. The bus consists of 16 data bits, 16 board select lines, 8 address lines for on card selection, and read, write and acknowledge handshake lines. The signals are on the a and c rows of the 96 pin DIN connector, leaving the unbused b row for user definition. A controller card resides in slot one translating the Motorola I/O Channel signals from the Parity CPU board to Peckbus signals.

DSP56001 Characteristics

The DSP56001[2] is a self contained computer on a chip, with program controller, math unit, program and data memories, and peripherals typically associated with computers, and a selection of bootstrap modes[1] The chip executes instructions at a 10 MHz rate, but the instruction fields can contain up to three instructions, giving a peak rate of 30 MIPS at 20 MHz clock. 27 MHz parts are now available, and we have run the 20 MHz parts at up to 40 MHz in the lab with a special clock generator. Tests have been done at Lincoln Labs on radiation hardness. The clock rate was run up to see where the parts stopped, then the parts were radiated and tested again. The test part died between 100krad and 200krad, and ran at 32 MHz up to that point. The chip has a 5 Mbit synchronous serial link, a UART, and a host interface port. The host interface port looks like a set of 8 byte wide registers (50 nsec access time) and can be very simply interfaced into any computer system.

DSP Software

The most unusual aspect of the host port is the host interrupt facility. The host can invoke one of the 32 interrupt service routines by writing the vector number to a register in the host interface. Using 8 of these vectors, we built a complete monitor and development system, supporting memory dump and load, program execution control, and machine state dump.

Monitor

The monitor in the target DSP consists of 16 lines of code:
```
;      MONITOR SERVICE ROUTINES:  300 nsec @ 20 MHz
;      {address,vector}
;      All functions require that r7 be set (via SETr7 call).

; SETr7 {24,12} Transfer the address value to r7
        movep           x:HRX,r7
        nop
; XPEEK {28,14} Read a 24-bit value from X memory
        movep           x:(r7)+,x:HTX
        nop
; XPOKE {2a,15} Write a 24-bit value to X memory
        movep           x:HRX,x:(r7)+
        nop
; YPEEK {2c,16} Read a 24-bit value from Y memory
        movep           y:(r7)+,x:HTX
        nop
; YPOKE {2e,17} Write a 24-bit value to Y memory
```
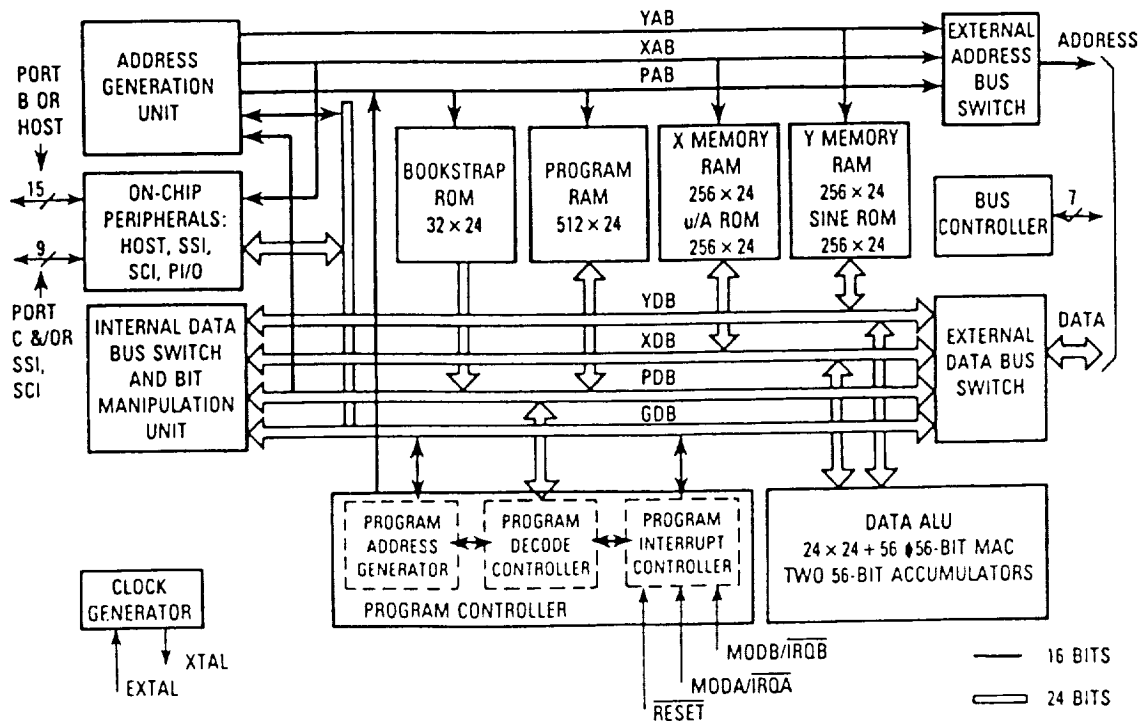

Fig 5 DSP 56001 Block Diagram

```
            movep              x:HRX,y:(r7)+
            nop
; PPEEK (30,18) Read a 24-bit value from program memory
            movep              p:(r7)+,x:HTX
            nop
; PPOKE (32,19) Write a 24-bit value to program memory
            movep              x:HRX,p:(r7)+
            nop
; SOFT  ( 6, 3) Code is PPOKEd here for dynamic expansion
            nop
            nop
```

The host computer is used to implement all the higher level code including initialization, data transfer, non time critical operations, and a full development system, monitor and debugger. The functions we implemented were made to duplicate the functions available in Motorola's DSP Development Software package. Using three windows on a workstation, code can be assembled and executed in the simulator, added to the target hardware and experimented with, and added to the source code. This development system allows loading of object files into the simulator and the target from the same load file generated by the Motorola assembler.

Timing Generator Code

An example of application code is the timing generator:
```
; outer loop to address all (aalen=64) rows of the array
AATOP   do      #aalen,AAEND
; inner loop: output 12 bits of CDS pattern at 10MHz
            rep     #cdslen
            move                 x:(r1)+,b    b,y:(r4)
; does:                          x(i+1) -> b  & x(i) -> latch

; strobe 24 bits of AAPM and CDSPM
            move                 x:(r0)+,a    a,y:(r5)
AAEND

; Frame time code goes here
            rep     #framewait
            nop

            jmp     AATOP
            end
```

Data Acquisition - Coadd Code

An example of interrupt service routines for data acquisition are the coadd short interrupt service routines. These routines are transferred into the low memory vector location at frame time by a frame interrupt routine that counts frames. Each of these routines executes in 200 nsec after a 500 nsec synchronization delay in the DSP. No instruction execution cycles are lost in the process.
```
;               first frame
MOVEX   movep    y:$ffc1,x:(r4)+ ; A/D -> X data buffer
            nop

;               frames 2 to n-1
ADDX    tfr      b,a     x:(r2)+,b       y:(r6),y1
            add      y1,b    a,x:(r4)+

;               last frame: results in y buffer for readout
ADDXY   tfr      b,a     x:(r2)+,b       y:(r6),y1
            add      y1,b    a,y:(r4)+
```

Conclusion

We took a big risk on redesigning the camera's entire digital system based on DSPs. The success of this experiment shows that there is a new generation of programmable logic to bring to bear on difficult design problems. Hardware designs can be greatly simplified and made more flexible. It is yet to be seen wheather or not the necessary software tools also appear to support these chips in general use. We have made initial steps in developing these tools, but they are far from what is needed to make these parts as easy to use as the hardware they replace. The power, simplicity and tremendous flexibility do come at a price for now.

References

1. *56-Bit General Purpose Digital Signal Processor*, document DSP56001/D, Motorola, 1988.

2. *MOTOROLA DSP56000 DIGITAL SIGNAL PROCESSOR USER'S MANUAL*, document DSP56000UM/AD, Motorola, 1986.

3. John F. Arens, J. Garrett Jernigan, Michael C. Peck, Carl A. Dobson, Erik Kilk, John Lacy, and Stephen D. Gaalema, "10 Micrometer Infrared Camera," *Applied Optics*, vol. 26, 1987.

4. J.F. Arens, G.M. Lamb and M.C. Peck, "Infrared Camera for 10 Micron Astronomy," *Optical Engineering*, vol. 22, pp. 267-268, 1983.

5. John F. Arens, Gerald M. Lamb and Michael C. Peck, "Infrared Camera for 10 Micron Astronomy," *Proceedings SPIE*, vol. 280, no. Infrared Astronomy, April, 1981.

6. Arnold Epstein, David M. Jordan and Jeffrey D. Morris, *Magic/L User's Manual*, Loki Engineering, Inc., Cambridge, MA, March 1987.

7. *ERASIC XL78C800, Multi-Level E² PLDs*, EXEL Microelectronics, Inc., San Jose, CA.

8. Peter C. Abrams, William T. Marchant, Michael C. Peck, Carl A. Dobson, and Roger F. Malina, "Real-Time Data Acquisition for the Extreme Ultraviolet Explorer Science Instruments," *Proc. IEEE 1987*, Astronomy Department & Space Sciences Laboratory, University of California, Berkeley.

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