A Fast Lightstripe Rangefinding System with Smart VLSI Sensor

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Introduction

The focus of our research is to build a compact, high performance lightstripe rangefinder using a VLSI *smart* photosensor array.

Rangefinding, the measurement of the three-dimensional profile of an object or scene, is a critical component for many robotic applications, and therefore many techniques have been developed [2]. Of these, lightstripe rangefinding is one of the most widely used and reliable techniques available.

Though practical, the speed of sampling range data by the conventional light stripe technique is severely limited. A conventional light stripe rangefinder operates in a *step-and-repeat* manner. A stripe source is projected on an object, a video image is acquired, range data is extracted from the image, the stripe is stepped, and the process repeats. Range acquisition is limited by the time needed to grab the video images, increasing linearly with the desired horizontal resolution. During the acquisition of a range image, the objects in the scene being scanned must be stationary. Thus, the long scene sampling time of step-and-repeat rangefinders limits their application.

The fast range sensor we propose to build is based on the modification of this basic lightstripe ranging technique in a manner described by Sato [6] and Kida [3]. As will be seen, this technique does not require a sampling of images at various stripe positions to build a range map. Rather, an entire range image is acquired in parallel while the stripe source is swept continuously across the scene. Total time to acquire the range image data is independent of the range map resolution.

Our target rangefinding system will acquire 1,000 100×100 point range images per second with 0.5% range accuracy. It will be compact and rugged enough to be mounted on the end effector of a robot arm to aid in object manipulation and assembly tasks.

Integrated *Smart* Sensing

The search for an efficient implementation of the parallel algorithm leads one to the use of *smart* sensors. A smart sensor has cells which provide processing at the point of sensing. Our range sensor uses smart cells to independently acquire data for range map points in parallel. When a scan has completed, the collected data can be read sequentially from the sensor. The slight increase in cell functionality from sensing-only to sensing-and-storage makes a high performance rangefinder based on the parallel algorithm realizable.

Advances in VLSI technology make smart sensors possible and hold the promise for further integration of computation and sensing. The key to a VLSI implementation of the lightstripe sensor chip is the ability to integrate photoreceptors, analog circuitry, and digital logic on a single CMOS chip. Examples of this class of chip exist and include commercial *CCD* camera chips, the *Xerox Optical Mouse* [4], Mead's *Artificial Retina* [7], and an *Optical Position Encoder* done at the CSEM in Switzerland [1].

Parallel Rangefinder System Overview

Algorithm

Figure 1 shows the principle on which a lightstripe rangefinder operates. The scene is illuminated with a vertical plane of light. The light is intercepted by an object surface in the path of the beam and, when seen by a video camera placed left of the light source, appears as a stripe which follows the surface contour of objects in the scene.
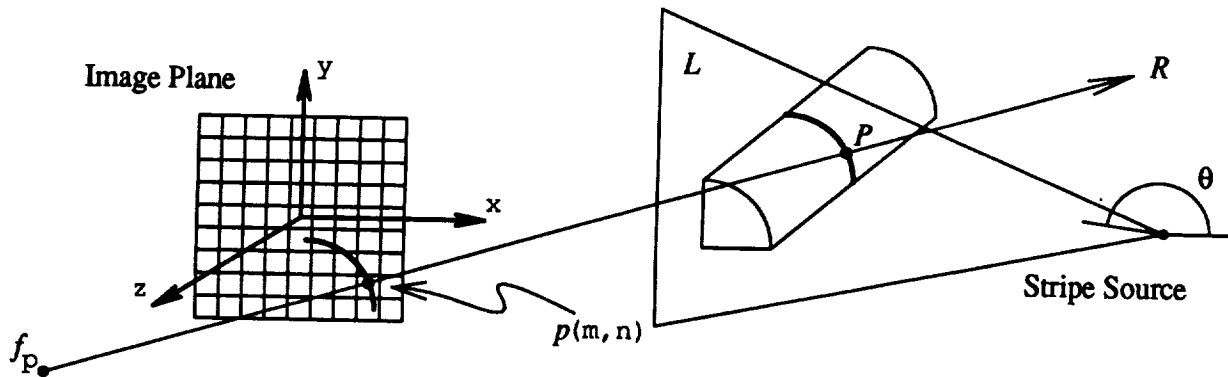

Figure 1: Lightstripe Rangefinder Geometry

Range data along the contour can be calculated easily using the principle of triangulation. In figure 1, the equation of the plane of light L is known because the projection angle θ is controlled. The line of sight R for each point p on the image of the stripe can be also determined by tracing a line from the image focal point f_p through p. The intersection of the ray R with the plane L uniquely determines the three-dimensional position of P on the surface corresponding to p. Range data of the whole scene is collected via a *step-and-repeat* procedure, that is, iterating the process of fixing the stripe on the scene, taking a picture, and processing the resultant image until the entire scene has been scanned.

Though practical, the speed of sampling range data by the conventional light stripe technique is severely limited. Assume that a video camera image has N rows. Since from one image at each step we can obtain up to N data points, the maximum speed of sampling is $S_{max} = \frac{N}{T_f}$ where T_f is the time required to acquire and process an image frame. Typically, N ranges between 256 and 512 samples and T_f ranges between one-thirtieth and one-tenth of a second. Thus, sampling speeds of camera based systems are limited to $S_{max} \approx 2.5K \sim 15K\ samples/second$.

In the parallel rangefinding technique, the video camera is replaced by a two-dimensional array of smart photosensitive cells. In addition, range data is not acquired in a step-and-repeat manner. Instead, the plane of light is swept across the scene at a constant angular velocity once from left to right.
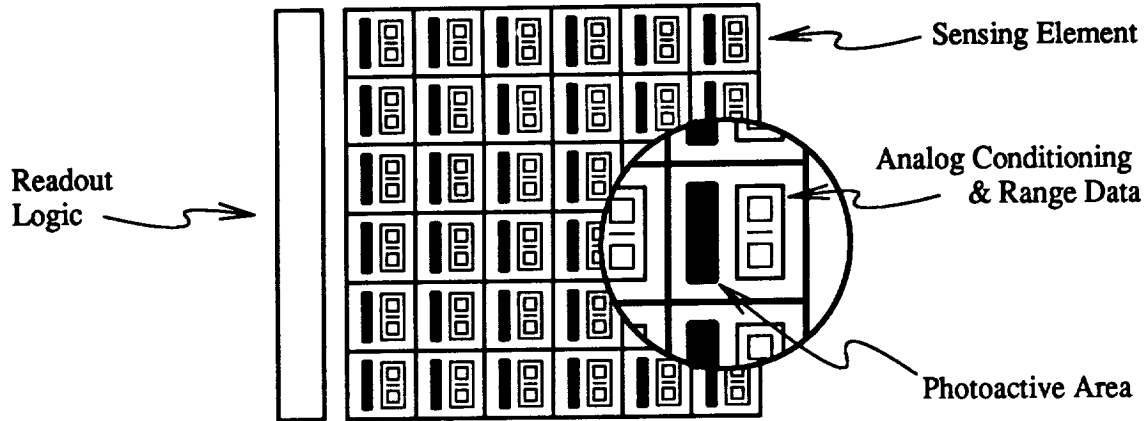
Figure 2: 2D Array of *Smart* Photosensors

The array of photosensitive cells, shown in figure 2, is smart for the following reason. Each has circuitry that can remember the *time* at which it observed the peak incident light intensity during a sweep of the stripe L. Observe that each cell predefines a unique line of sight R and that the information t_{cell} recorded by each cell defines a particular orientation of the stripe $L(t_{cell})$. Recalling the geometry in figure 1, one sees that this information is sufficient to calculate the three-dimensional position of the imaged object point P, again using triangulation. The data gathered during *one* pass of the stripe in an $M \times M$ array of these smart sensing elements is sufficient to calculate the $M \times M$ range map of an imaged scene.

For an $M \times M$ array of these cells, the sweep time T_s of the lightstripe and M determine the sampling speed. The sweep time T_s will be limited by photoreceptor sensitivity and M by integration technology. We are predicting values of T_s on the order of one to ten milliseconds, and values of M ranging between 40 and 100. The rates at which the smart sensor array generates range data will be

$$S_{max}^{Smart} = \frac{M^2}{T_s} \approx 0.2M \sim 10M \, samples/second.$$

This is a speedup of several orders of magnitude over that of a conventional camera-based system.

System Implementation Issues

The hardware necessary to construct a rangefinding system based on the parallel technique is comparable to that found in a conventional rangefinder. One needs a photosensitive array, stripe generation hardware, and system interface circuitry.

Functionally, each element of the smart photosensitive array converts light energy into an analog voltage, determines the time at which the voltage peaks, and remembers the time at which the peak occurred. The implementation of this functional specification requires that photoreceptor and signal conditioning circuitry be integrated into a unique hybrid sensor cell. The sensing element design must consider tradeoffs in cell size, power dissipation, bandwidth, sensitivity, and accuracy.

Special care must be taken with the photodiode amplification stages. Photocurrents induced by incident light from the stripe are on the order of a nanoamp and must be amplified to reasonable voltage levels. In addition, the high rate of range map acquisition supported by our system implies high bandwidth

photodiode signals. A 100×100 element sensor gathering 1,000 range images per second requires an amplifier that can provide gain out to $100KHz$. On the other hand, we know that the frequency content of signals generated by a continuously moving stripe will be found above the base scanning frequency. Thus, the low pass nature of amplified photocurrents should be combined with a high pass filter stage to yield an amplifier with an overall bandpass frequency response. The cells that result will be most sensitive to frequencies generated by the image of a moving stripe. The amount of interference caused by ambient light and signal conditioning circuitry $1/f$ noise will be reduced.

The stripe generation hardware consists of a coherent light source, stripe optics, and sweep mechanics. It must project a continuously moving stripe whose geometry with respect to the sensor is known as a function of time. A *start-of-scan* (SOS) detector and its conditioning electronics must also be included in the stripe generation assembly. The SOS indication defines a reference point in time relative to which range data will be measured and recorded by the sensing elements.

The system interface circuitry bridges the gap between range sensor and host processor. Range image acquisition must be coordinated between the sensor and the stripe generation hardware. Sensing element data must be acquired and accurately converted into a form usable by the host. Finally, the system interface must provide a high bandwidth path to the host for acquired range data.

Photodiode Based Test System

Implementation

We have designed and built a prototype rangefinding system based on the parallel algorithm. Essential components in this system included stripe generation hardware, range sensor, range sensor optics, and host interface. This implementation is similar in spirit to systems built by others [6] [3] and served as groundwork for our VLSI sensor based system.
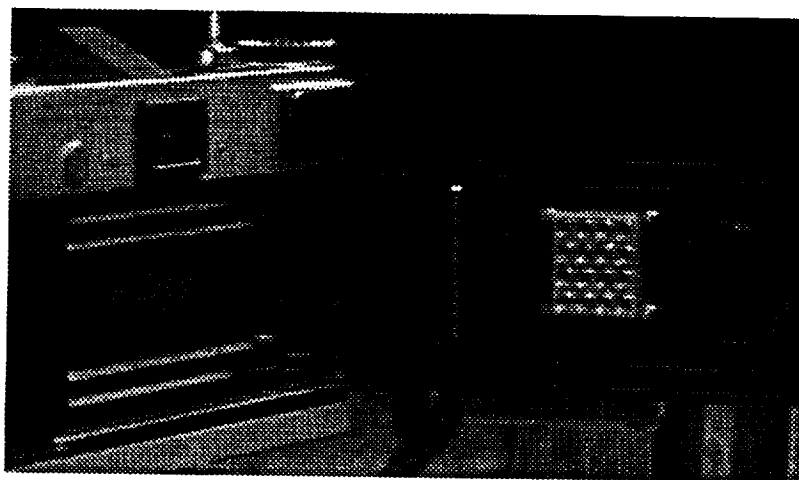

Figure 3: 4×4 Photodiode Array Mounted in a 35mm Camera

The sensor in our evaluation system has been constructed using a discrete 4×4 array of photodiodes as the sensing device as seen in figure 3. The photodiodes are mounted in a 35mm SLR camera body which provided a convenient mechanism for incorporating focusing optics and for sighting the rangefinder.

Photodiodes were chosen for the sensing elements because they possess bandwidth sufficient to meet our sweep rate specifications.
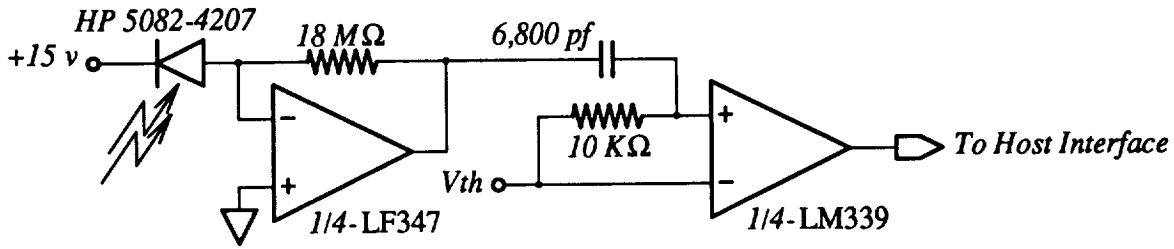

Figure 4: Photodiode Signal Conditioning Circuitry

Analog signal conditioning circuitry for each of the discrete photodiodes was designed to provide a digital transition when the reflection of the stripe passed through a diode's field of view. It consisted of a high gain transimpedance amplifier and simple thresholding stage as shown in figure 4.

The design of the photocurrent amplifier was crucial. For purposes of small signal bandwidth analysis, reversed biased photodiodes can be modeled as the parallel combination of a current source of a few nanoamps, a resistance, and a capacitance. Though the internal capacitance is moderate, on the order of a few picofarads, the internal resistance is ten gigaohms or more. The parallel combination of these creates an undesirable pole at a frequency of a few hertz which tends to low pass filter any output signal. The photocurrent amplification circuitry must provide a large photocurrent to voltage gain while presenting a small impedance to the diode. The amplifier shown in figure 4 provides $18M\Omega$ of photocurrent amplification and employs negative feedback to servo the photodiode anode to a constant voltage, increasing available bandwidth.

Amplified photodiode signals were high pass filtered before reaching the comparator. This was done to make the comparator threshold level independent of photodiode dark current and ambient light levels and to remove low frequency circuit noise.

The digital output from the comparator in each cell was passed directly to the host interface. This is practical when a sensor of only 16 elements is involved, but would not be practical for sensor densities much above 10×10. On the host interface, the 16 comparator outputs were sampled into a local dual-ported memory. Host access to the data was provided via a memory-mapped VME interface.

The stripe in this discrete implementation was generated using a $5mW$ helium-neon (HeNe) laser and half-cylindrical lens. Sweeping of the stripe was accomplished using a mirror mounted on a galvonometer. Use of a galvonometer to sweep the stripe meant that scans alternated in direction between left-to-right and right-to-left. The galvonometer was driven with a $500Hz$ triangle wave in order to generate our target 1,000 sweeps per second.

Two additional photodiodes were used to provide *start-of-scan* (SOS) and *end-of-scan* (EOS) indications necessary for determining the time origin, direction, and duration of a sweep. Conditioning circuitry used for these scan detectors is similar to that used by the sensing elements. The digital output from these detectors is used by host interface hardware to initialize the sample memory address counter and determine the direction of stripe scan.

Results

The photodiode based rangefinding system hardware was able to generate and record over 1,000 4×4 range images each second. System software, running on a SUN 3/160 workstation, slowed the rate of processed image data to about 100 frames a second. Range data, encoded in the time from a scan origin to when a sensing element sees the flash, was continuously displayed on the monitor of the host workstation.

VLSI Range Sensor Based System

System Overview

From a speed and sensitivity standpoint, our discrete photodiode based system is a successful implementation of the parallel rangefinding algorithm. However, a 4×4 array does not provide enough range points to be useful. As one considers building larger and larger arrays out of discrete photodiodes, implementation problems quickly become apparent. The cost of wiring individual photodiodes to interface circuitry becomes prohibitive for arrays much larger than 10×10. Support circuitry must be built out of off-the-shelf analog and digital IC components for each sensing element. Schemes which time multiplex wires from the photodiodes and sensing element conditioning electronics are not practical because one cannot predict when a given cell will see the stripe.

A VLSI implementation of the range sensor shows the greatest promise for increasing the range image density of the system. The essential thing that VLSI provides is the ability to integrate the sensor, conditioning circuitry, and range memory into a single smart cell. Wiring costs from sensor to amplifier to memory circuitry are virtually eliminated. Time multiplexed readout of range data is practical once data for a scan has been recorded within the sensor cells. Thus, the range map resolution of a VLSI based sensor is not limited by the number of connections which can be made to the sensing elements.

Range Sensor IC Interface

The range chip provides data in the form of two time multiplexed *analog* outputs. The first transfers sensed stripe arrival time values from the chip. The second provides the intensity seen at a cell when the incident stripe intensity was at a maximum. This intensity output will give a rough idea of scene reflectance and will be useful in determining the level of confidence one can attach to the corresponding time sample. Storage of chip data as analog values might at first seem to be inherently noisier than storing acquired data digitally. Justification for this decision is outlined in the description of the sensor chip.

The system interface will control the range image acquisition process, drive the sensor chip, retrieve raw range data, and make this data available to the host over a high bandwidth path. Two analog-to-digital converters will be necessary. The first will be used to convert the analog time values, the second to convert the maximum sensing element intensity values. These analog-to-digital converters will need to have a $2\,MHz$ conversion rate and better than ten bits of accuracy. Stripe sweep control circuitry will generate the analog time ramp. The period of the ramp will be phased locked to index pulses generated by the SOS detector.

IC Based Rangefinder Stripe Generation

HeNe laser tubes are not well suited for use in a compact rangefinding system. We plan to construct an infrared (IR) laser diode based stripe source. Silicon photodiodes have good sensitivity to light in the near infrared[1] area of the spectrum, in the range wavelengths emitted by typical IR laser diodes. A good match of spectral characteristics between stripe source and photodiode based detector will aid in stripe detection. A cylindrical lens will serve to fan the collimated beam into a stripe.

In order to sweep a 60° field of view in one millisecond, the stripe will have to rotate at 10,000 *RPM*. A multifaceted mirror attached to the shaft of a motor spinning at 5,000 *RPM* is one candidate for sweeping the stripe. The stripe sweep hardware and range sensor will be assembled as one unit to insure an accurate and steady baseline for range calculations.

The Sensor Chip

A block diagram of our sensor chip, showing sensing element layout, can be seen in figure 2. Photodiode areas are arranged in vertical stripes which are to be aligned in the direction of the imaged light stripe. Sensing element support circuitry is sandwiched between the photodiodes. As will be described, the design of sensing elements on the IC differs from the design of sensing elements in the discrete photodiode implementation in several important ways.

Sensor chips and test structures are being fabricated in a 2.0 μ CMOS[2] P-well double-metal, double-poly process. Fabrication is provided through the MOSIS [5] system. Global chip busses required for power and ground runs, timestamp input, and multiplexed data readout can easily be realized with this two layer metal process. Total sensing element area is projected to be 200 μ×200 μ. We expect to be able to integrate a 40×40 cell sensor in a roughly one square centimeter die. In order to keep chip power dissipation to a few watts, cell current is budgeted at around 200 *μamps*.

If our sensor chip design is to be successful, attention must be paid to the following issues:
- design of the integrated photoreceptors,
- photocurrent amplification bandwidth and noise floor,
- representation of the global timestamp signal on the chip,
- data storage capability, and
- design of the sensor chip interface.

Refer to the block diagram for one sensing element, shown in figure 5, as we discuss the manner in which these issues are addressed in our sensing element design.

Integrated Photodiodes as Sensing Devices

The photodiodes are critical to the sensitivity and bandwidth of the sensor cells. Current output at a given incident light intensity is directly proportional to the photodiode area. The more area devoted to photodiode structures the better the optical sensitivity of the sensing elements will be. Our photodiodes are 20,000 μ² in area, one half the total area budgeted for a cell.

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[1] Near infrared includes wavelengths between 700 *nm* and 1,000 *nm*. IR laser diodes emit light at wavelengths ranging between 820 *nm* and 880 *nm*.

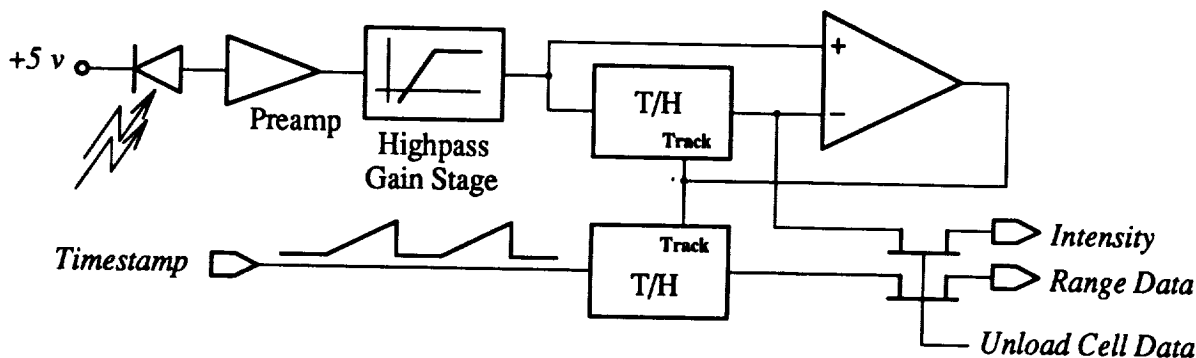[2] A *micron* (μ) is 10^{-6} *meters*.

Figure 5: Sensing Element Circuitry

In a CMOS process, maximum sensitivity photodiodes are build using the well-substrate junction [1]. This vertical photodiode structure is constructed using the n-type substrate as the cathode and the p-type well as the anode. An additional p^+ implant is driven into the well to reduce the surface resistivity of the anode to which contact is made. Finally, the photodiode structures are surrounded with guard rings to minimize the chance of photocurrent induced latchup. Only the anode of the photodiode is accessible for reversed biased operation. The cathode of the diode will be at the substrate voltage.

Photocurrent Amplification

A candidate photocurrent preamplifier is based on one developed for use in an optical position encoder [1]. This amplifier is logarithmic in that its output voltage is proportional to the log of the induced photocurrent. A negative feedback loop consisting of a p-channel FET common source amplifier and common base lateral NPN transistor servos the photodiode anode to a constant voltage. This reduces the effective capacitance of the photodiode by a factor equal to the loop gain and thus extends operational bandwidth. The lateral bipolar transistor used in this circuit is fabricated in a P-well area into which a p^+ base contact has been implanted. A small area of n^+ diffusion, which becomes the emitter, is surrounded by a ring of n^+ diffusion to form the collector. A parasitic vertical NPN structure is also formed by the substrate, the P-well base, and the emitter. The parasitic lowers the α of the lateral device but does not adversely affect its operation as a common base stage.

The output of the transimpedance amplifier feeds a second stage of amplification through a high pass filter. As was the case in the discrete photodiode implementation of this sensor, the high pass section nulls out the effects of dark current and ambient light. In addition, $1/f$ noise inherent in MOSFET based amplifiers is also filtered out. The low pass nature of the photodiode combined with the high pass filter of the second gain stage yields an overall bandpass transfer characteristic for the photodiode amplifier stages. Thus, sensing elements on the chip will be most sensitive to those frequencies generated by the image of the stripe moving across the sensor.

Representing Time as an Analog Voltage

Representing time as an analog voltage has several advantages over the digital equivalent of latching the value of a continuously running counter. The analog only scheme avoids noise problems associated with mixing sensitive analog circuits with digital logic within the cell. A digital timestamp bussed over an entire chip, combined with transients associated with the latching of timestamp values by sensing elements, are sources of noise with the potential to corrupt the measurement of small levels of

photocurrent. Photodiode anode points are high impedance nodes and will be susceptible to noise coupling from other chip circuitry.

The chip area needed for timestamp broadcast and latching will be smaller for the analog scheme when compared with the circuit area required by the digital scheme. An analog timestamp can be broadcast over the entire chip on a single wire and the circuitry to record an analog time value consists of a holding capacitor and a switch. The eight bits of digital time necessary for 0.5% resolution would have to be broadcast over a bus and each sensing element would need an eight bit latch.

Raw Range Data Storage with Track-and-Hold Circuitry

The system analog timestamp voltage is switched on to the holding capacitor in a track-and-hold (T/H) circuit until incident intensity has peaked. A second T/H follows the sensed light intensity until the point when its held voltage exceeds the input voltage. At that time, the comparator stage changes state, disabling the T/H circuits and recording a range time value.

In addition to the structures that can be built using a standard P-well CMOS process, the double-poly process we are using provides high quality linear capacitors. These capacitors exhibit good matching across a die and are needed by sensing elements on the range sensor IC to store analog voltages. The matching of these capacitors across the sensor chip will in large part determine the variance in voltage reported by individual sensors for given time values. At capacitive densities of $0.5ff/\mu^2$, a $1pf$ T/H capacitor will be 45μ on a side.

Host Interface Considerations

Charge accumulated in the sensing elements on the holding capacitors is passed out of the chip on a bus and integrated to produce a voltage. Both the range data and maximum intensity values will be read from the sensor in this way. We plan to offload sensing element range data in raster fashion, much like a CCD camera chip. For the initial 1,600 element sensor, we can spend $500ns$ on each cell if range acquisition time and offloading time are to remain comparable. Future versions could certainly take advantage of multiple data pathways to reduce the time necessary to dump stored range data. Data could also be pipelined with range acquisition if two sets of T/H circuitry were built into each cell. Initially we have decided not to do this for two reasons. First, cell area would grow mainly due to the size of the two additional T/H capacitors needed. Second, time multiplexing of the on chip busses is essentially a digital process which has the same noise pitfalls as any other digital circuitry on the chip. By separating acquisition and offloading phases, we can insure that no digital switching will be occurring while range measurements are taking place.

Future Work

Our decision to represent range data on the sensor chip as an analog voltage will enable us to apply analog signal processing techniques for on chip computation. Simple computations can be done with analog circuitry in less area than possible with corresponding digital computations. For example, switched capacitor technology can reduce the circuitry needed to compute a weighted average to a few capacitors and transistors. We hope to explore these possibilities further.

We also plan to explore the use of layered or *three-dimensional* (3D) VLSI to assist in increasing sensor

density. A 3D VLSI process is an ideal one for building a dense parallel range sensor. Photosensitive elements can cover the surface of the chip without gaps in a 3D process, maximizing sensitivity and range image density.

The research leading to the development of our lightstripe chip has great potential for advancing smart sensor technology in general. The sensor will need to acquire, amplify, and process information derived from a weak incident power source. We will need to incorporate ideas from a variety of disciplines to achieve this goal. In addition, decisions on the kinds of signal processing operations to be performed on the sensor itself must be made. A *smarter* chip has the potential to operate on its data directly, saving the considerable time and bandwidth spent shuffling data between sensors and processing in a typical system.

References

[1]   P. Aubert and H. Oguey.
      An Application Specific Integrated Circuit (ASIC) with CMOS-Compatible Light Sensors for an
         Optical Position Encoder.
      In *IEEE 1987 Custom Integrated Circuits Conference*, pages 712-716. IEEE, May, 1987.

[2]   P.J. Besl.
      Range Imaging Sensors.
      Research Publication GMR-6090, General Motors Research Laboratories, March, 1988.

[3]   T. Kida, K. Sato, and S. Inokuchi.
      Realtime Range Imaging Sensor.
      In *Proceedings 5th Sensing Forum*, pages 91-95. April, 1988.
      In Japanese.

[4]   R.F. Lyon.
      The Optical Mouse, and an Architectural Methodology for Smart Digital Sensors.
      Technical Report VLSI-81-1, Xerox Palo Alto Research Center, August, 1981.

[5]   G. Lewicki, et. al.
      MOSIS User's Manual
      USC Information Sciences Institute, 4676 Admiralty Way, Marina Del Rey, CA 90292-6695,
         1988.

[6]   Y. Sato, K. Araki, and S. Parthasarathy.
      High Speed Rangefinder.
      SPIE , 1987.

[7]   M.A. Sivilotti, M.A. Mahowald, and C.A. Mead.
      Real-Time Visual Computations Using Analog CMOS Processing Arrays.
      In P. Losleben (editor), *Advanced Research in VLSI -- Proceedings of the 1987 Stanford
         Conference*, pages 295-312. The MIT Press, 1987.