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OLYMPUS PROPAGATION STUDIES
IN THE U.S.
Receiver Development and the
Data Acquisition System

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Abstract - Virginia Tech has developed two types of receivers to monitor the OLYMPUS beacons, as well as a custom data acquisition system to store and display propagation data. Each of the receiver designs uses new hybrid analog/digital techniques. The data acquisition system uses a stand alone processor to collect and format the data for display and subsequent processing.

1. Introduction

The launch of the OLYMPUS satellite with its coherent beacons offers new opportunities to study propagation effects at 12.5, 20 and 30 GHz. At Virginia Tech, the satellite is at 14 degrees in elevation, which allows us to measure low elevation angle effects. However, to make these measurements, a very accurate and stable measurement system is required.

Virginia Tech has constructed a complex receiving system which monitors the OLYMPUS beacons and all parameters associated with propagation research. In our current configuration, we have developed a receiver which frequency locks to the less fade susceptible 12.5 GHz beacon. Since all beacons on the satellite are driven from a single master oscillator, drift in the 12.5 GHz beacon implies corresponding drifts in the 20 and 30 GHz beacons. The receivers for our 20 and 30 GHz systems derive their frequency locking information from the 12.5 GHz system. This widens the dynamic range of the receivers and allows our receivers to maintain lock in severe fade conditions.

In addition to monitoring the beacons, we also monitor the sky noise with radiometers at each frequency. The radiometer output is used to set the clear air level for each beacon measurement. We also measure the rain rate with several tipping bucket rain gauges placed along the propagation path. In the future, we hope to provide radar coverage of rain events. System temperature is continuously monitored at 22 points in the receiving system in an effort to obtain precise calibration of the receivers. Lastly,

wind speed and direction are monitored by the data acquisition system to keep a log of meteorological data.

In this paper, the details of the two receiver prototypes are first presented. An overview of the data acquisition system is then presented.

2. Receiver Development

Virginia Tech, with help from JPL personnel, has developed two receiving systems for use with OLYMPUS. Both systems input an IF of 70 MHz. The first system downconverts the IF to 10 kHz and then digitizes the signal to obtain the I and Q outputs. The second system downconverts the 70 MHz to 10 MHz, digitizes the 10 MHz IF, and then uses Fast Fourier Transform (FFT) techniques to obtain the I and Q outputs.

2.1 Hybrid Analog/Digital Receiver

Our 12.5 GHz receiving system is shown in Figure 1. The incoming microwave beacon signal is first converted to 1120 MHz and then to 70 MHz. Our microwave LO is controlled by the Frequency Locked Loop (FLL). The 70 MHz signal is then converted to 10 kHz. To reduce the possibility of false lock, the 69.98 MHz image is suppressed in an image cancelling mixer. The 10 kHz signal is passed through a limiter which removes amplitude variations to prevent the loop gain from varying with signal level. The output of the limiter is bandpass filtered and then input to the frequency detector. The loop dynamics are set by the loop filter that follows the frequency detector.

The frequency detector mixes the incoming 10 kHz IF signal with quadrature 10 kHz reference signals. The mixing products are low pass filtered and the result is the quadrature of the frequency difference between the reference and the IF signal. These quadratures are delayed in an R-C network and then cross multiplied. The filtered output is then used to control the VCXO so that the IF output to the A/D converter is always 10 kHz.

IQ detection is accomplished by multiplying the signal with quadratures of its carrier frequency using a sampling process. The I and Q samples are separated by demultiplexing and low pass filtering to produce the detected output.

As shown in Figure 1, our IQ detection system consists of a 12 bit analog to digital convertor (ADC), a programmable timer, an 80286 microprocessor, memory and a clock generation circuit. A 200 Hz wide, 10 kHz filter is placed before the A/D to ensure that the IF signal is sufficiently bandlimited. The ADC converts the input signal to a digital form and the microprocessor performs a digital low pass filter on the data. After performing the filtering operation, the microprocessor outputs the measured I and Q values

to a data acquisition and display system. Coordination of the sampling and filtering as well as handshaking to the data acquisition system is accomplished by the microprocessor.

The low pass filter used is a finite impulse response (FIR) filter which implements a Kaiser window 1116 points long. The Kaiser window forms a digital 3 Hz low pass filter to ensure that the detected signal is sufficiently bandlimited for the desired 10 Hz output rate. Although the detector was programmed to produce output at 10 Hz, the hardware design is flexible enough to implement other algorithms at varying sampling rates.

The software of the digital detector implements two low pass digital filters on the incoming IF data, one each for I and Q. The use of integer mathematics allows the system to operate without the complexity and cost of a math co-processor chip.

During normal operation, the hardware continuously collects I and Q data from the ADC and stores them in two buffers. These buffers are somewhat larger than the size of a complete filter set to allow samples to be collected while the processor concurrently performs a filter calculation.

2.2 Digital Receiver

Our digital receiver design is shown in Figure 2. In our design, the 10 MHz IF is sampled at 8 MHz to yield the I, Q, -I, -Q sample stream. The resulting samples are then decimated and sign corrected to yield a complex sample stream of 500 kHz. These data are stored in a dual ported random access memory (RAM) as the real and imaginary inputs for a complex FFT.

Once 1024 samples have been received, the DSP processor (TRW TMC 2310) retrieves the samples and applies a Hamming window to the data. These data are then input to a 1024 point complex FFT and the results are stored in the dual ported RAM. The DSP, which is controlled by an INTEL EPLD, then computes the power in each frequency bin by summing the squares of the real and imaginary components. At this point, the frequency "resolution" of each bin is $500 \text{ kHz}/1024 = 488 \text{ Hz}$.

As the power associated with each bin is computed, (i.e. $I^2 + Q^2$) a simple comparator circuit compares the power of each bin until the bin with the greatest power is located. This bin is assumed to contain the carrier signal.

The contents of the single FFT bin corresponding to the bin with the largest energy is then stored in a second bank of dual ported RAM. Thus, one pair of IQ samples which correspond to the carrier power is stored for each of the first stage FFTs. When 1024 of these samples accumulate, a second FFT is performed. In a manner similar to the first FFT, a Hamming window is applied to the data and these data are again input to a 1024 pt FFT. The output of

this FFT is then stored in the second set of dual ported RAMs. At this point, the frequency "resolution" per bin is 488 Hz/1024 or 0.477 Hz.

After the second FFT is performed, the frequency components are squared and summed to determine the magnitude (squared) in each bin. The bins are then sorted to find the bin with the largest power. The I and Q components of that bin form the I and Q outputs for the beacon. The frequency of the carrier is then computed using an Intel 8085 processor and displayed along with the power on an LCD display.

The frequency information from the second FFT output is used to adjust the 48.45 MHz VCXO. This keeps the beacon signal within the bandwidth of one 488 Hz wide bin from the first FFT. Although the output of the second FFT is updated at approximately 500 Hz, the VCXO is only corrected at a 0.1 Hz rate to avoid instability. A flowchart of the FFT processing is shown in Figure 3. Figure 4 shows a block diagram of the FFT processing hardware.

The current version of the digital receiver is undergoing test and we expect to have a production version operational by 15 June 1990.

3. Data Acquisition System

The major components of the data acquisition system (DAS) are shown in Figure 5. The DAS is comprised of two units: the control rack and the personal computer.

The control rack is a standard 19" chassis unit whose function is to collect all data, format the data and transmit the data to the personal computer. In its minimum configuration, it is comprised of an electrical backplane, a power supply, a central processing card, 2 IQ detection cards, a radiometer card, a digital input card and one temperature card. The control rack is built around a standard (STD) bus electrical backplane.

Using a standard backplane allows the experimenter to easily modify the collection system by adding or removing boards as needed. The control card, which contains a stand alone 80286 system, was designed to sample the IQ outputs of the IQ card, the radiometer card outputs, the digital input card and the temperature outputs. The sampling rate is variable, however, we will be sampling at 10 Hz.

The IQ detection card performs the IF sampling and low pass filtering for two receivers. In our configuration, the 12.5 and 20 GHz IF signals are input to one IQ detection card, the 30 GHz and 20 GHz diversity IF signals are input to another. To keep the IQ detection synchronized, one common 40 kHz clock source is used for all IQ sampling cards as well as to set the system-wide 10 Hz sampling interval.

The radiometer card receives one output from each of the four radiometers. This output is a square wave whose frequency corresponds to the noise power in each radiometer band. The radiometer card converts these signals to digital noise values and provides them to the central processing card when polled every second.

The temperature card receives separate analog signals which represent the temperature at 22 locations in the experiment system. One temperature value is sampled in sequence at each 0.1 second interval.

4. Acknowledgements

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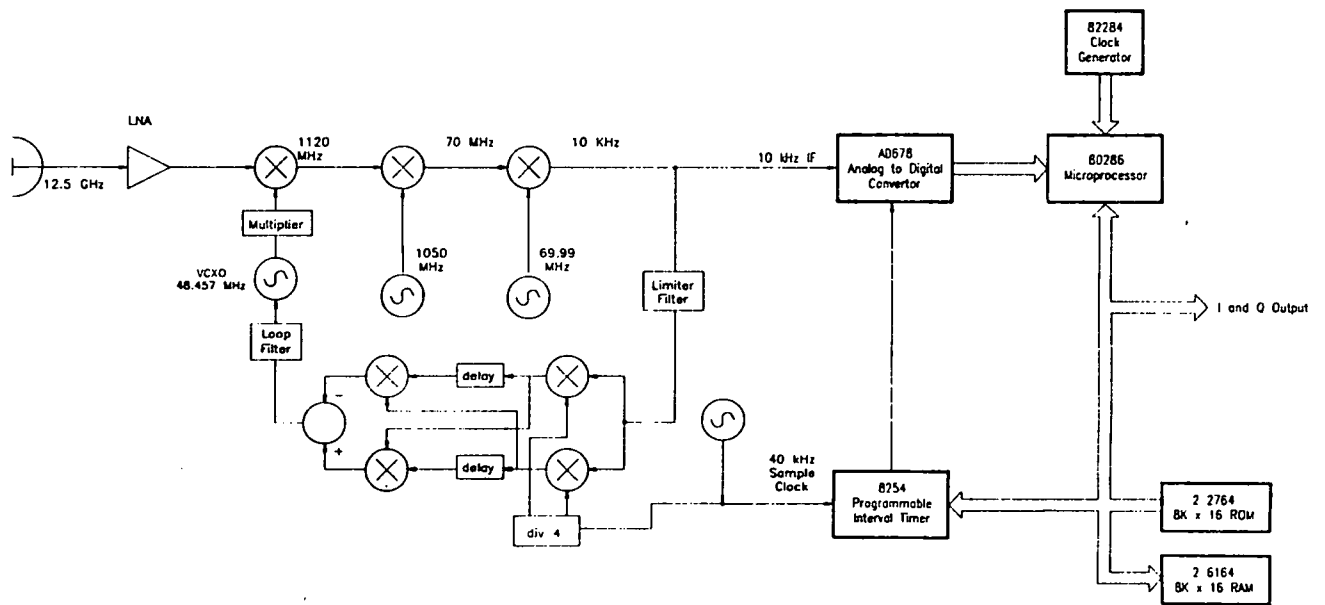


Figure 1. Block diagram of the hybrid analog/digital receiver

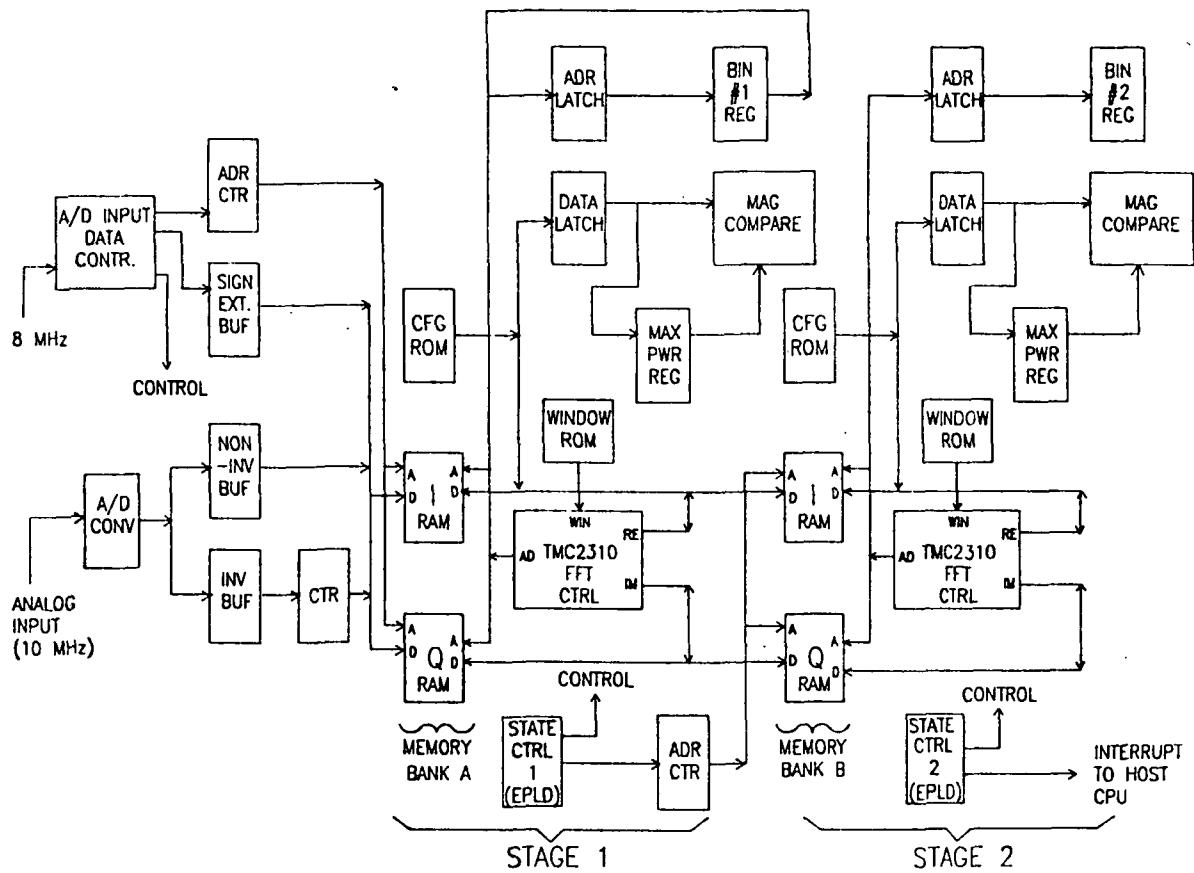


Figure 2. Block diagram of the digital receiver

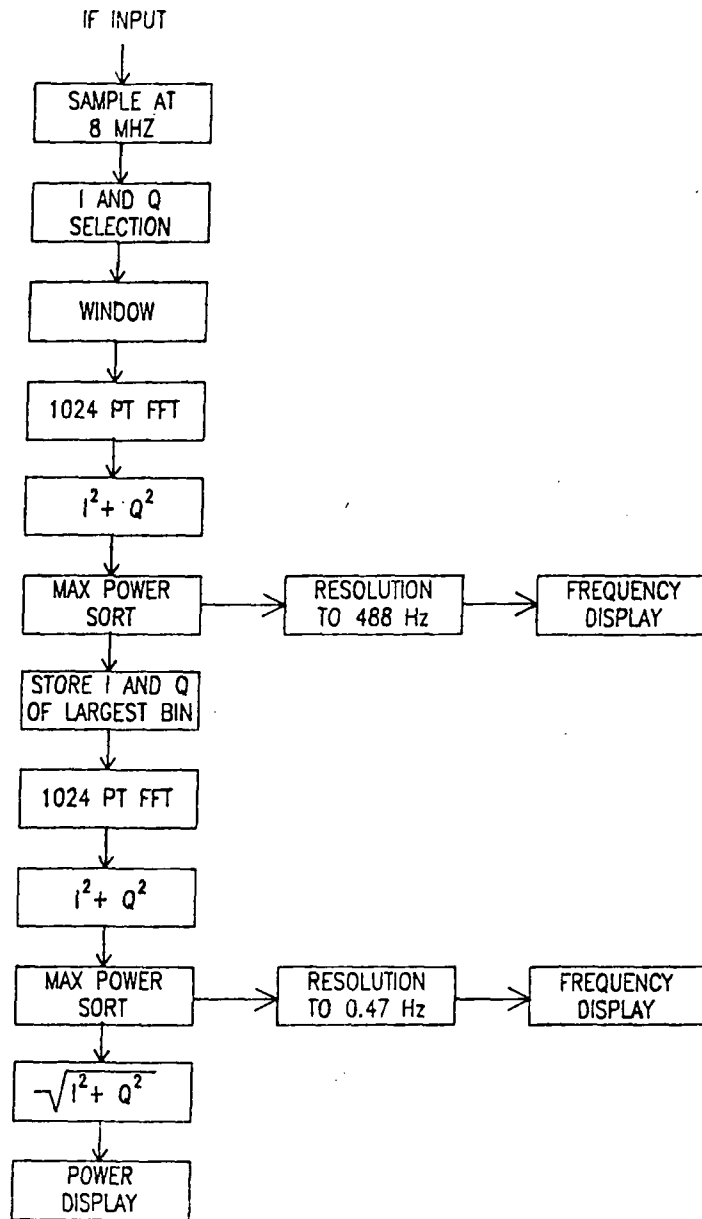


Figure 3. Flowchart of FFT processing

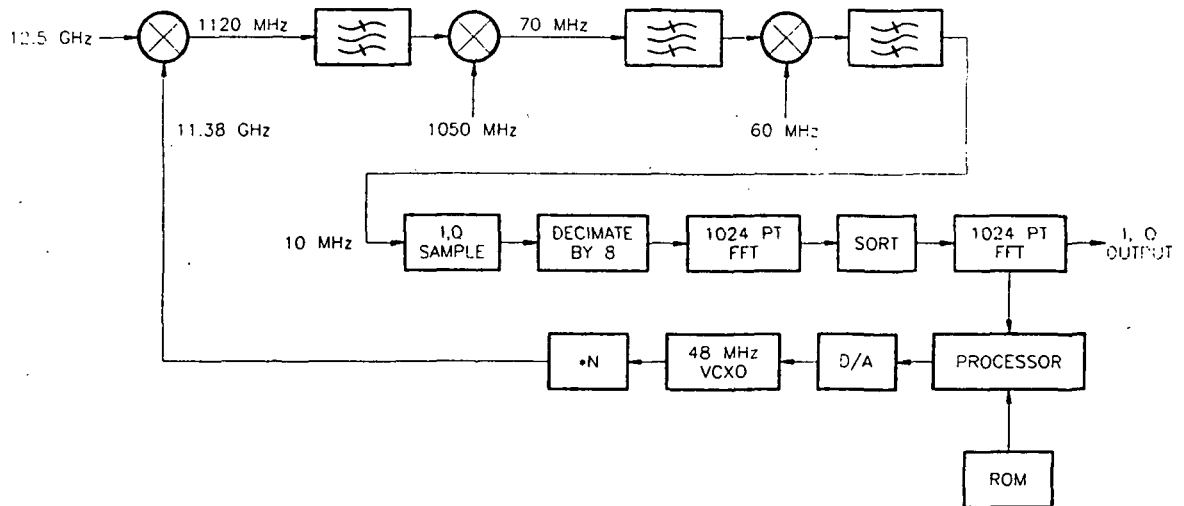


Figure 4. Hardware block diagram

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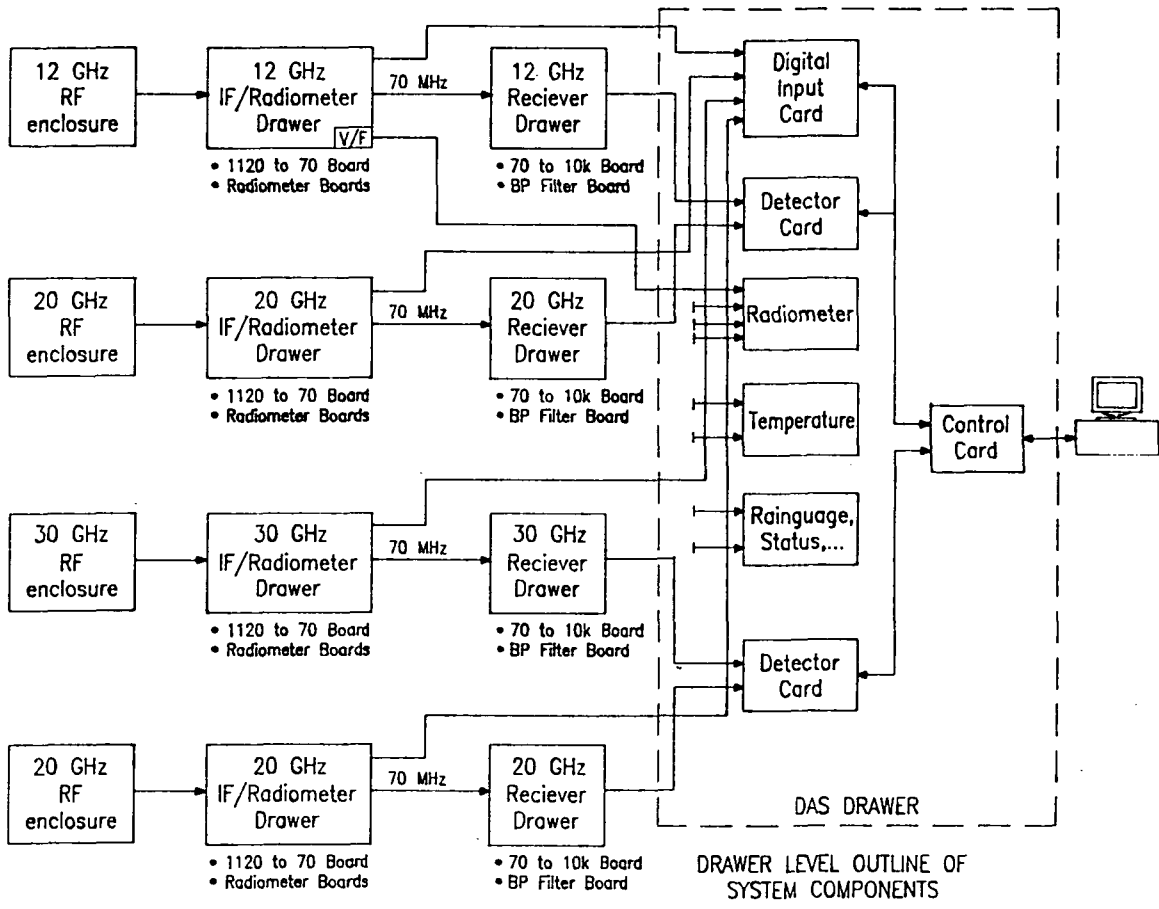
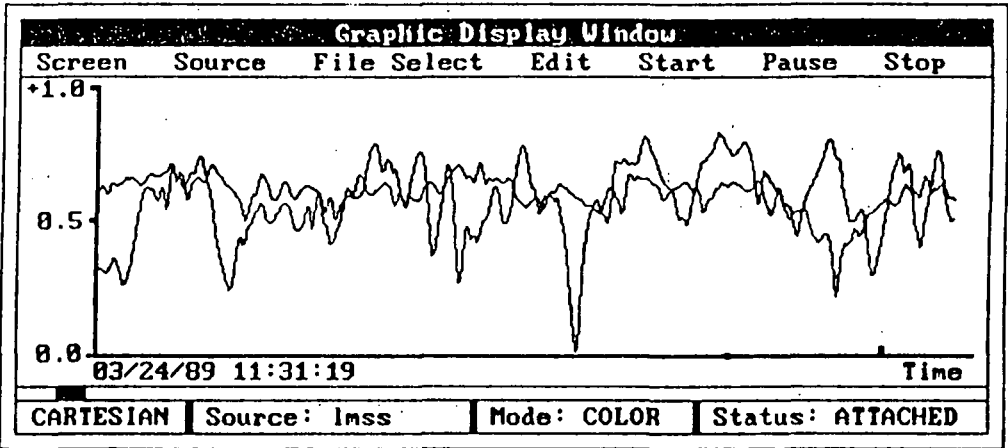


Figure 5. Overview of Data Acquisition System

System Clock
Time 12:42:33 Date 04/28/89



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Figure 6. DAS Software Display