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Digital Frequency Synthesizer for Radar Astronomy

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August 15, 1990

NASA

National Aeronautics and
Space Administration

Jet Propulsion Laboratory
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Pasadena, California

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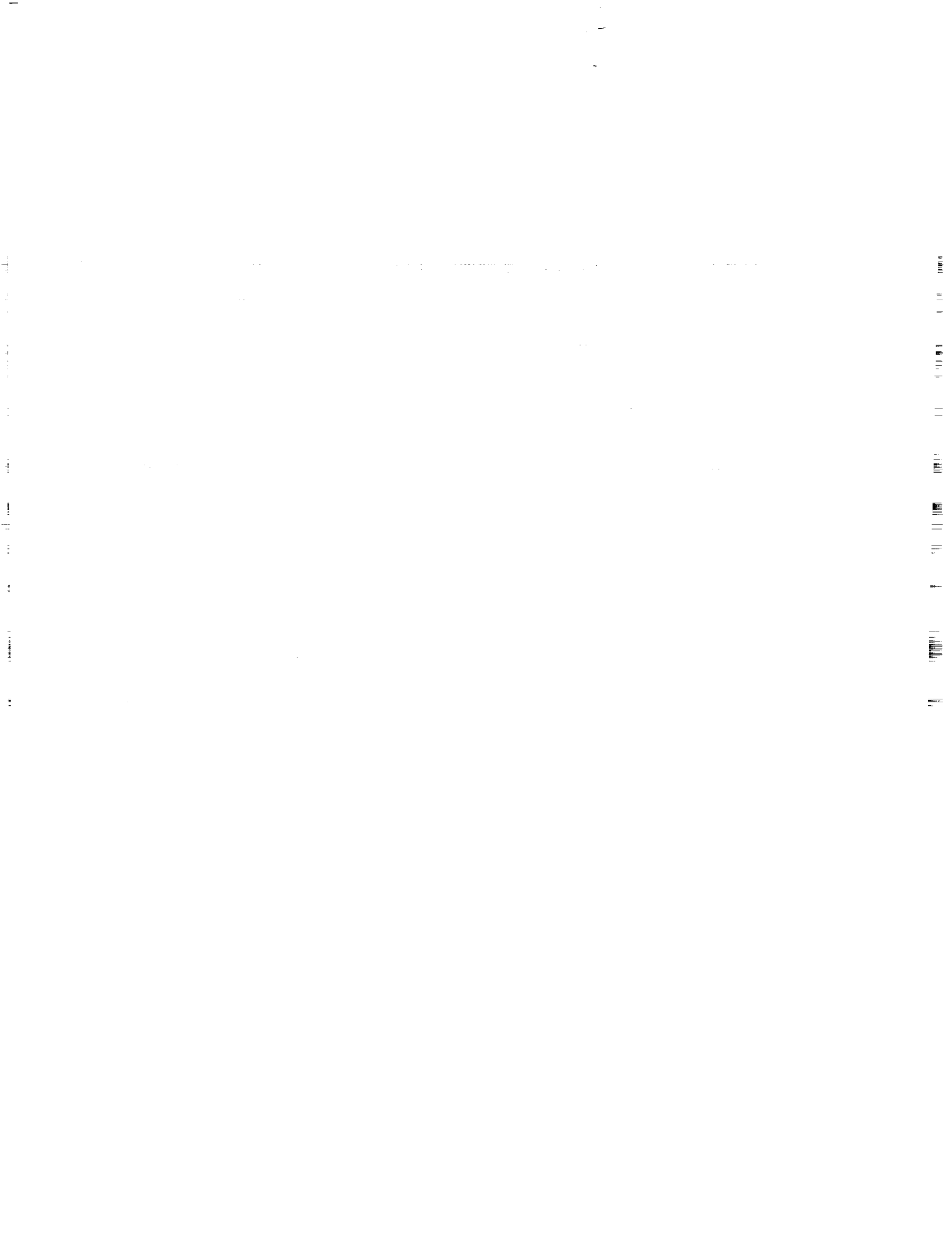
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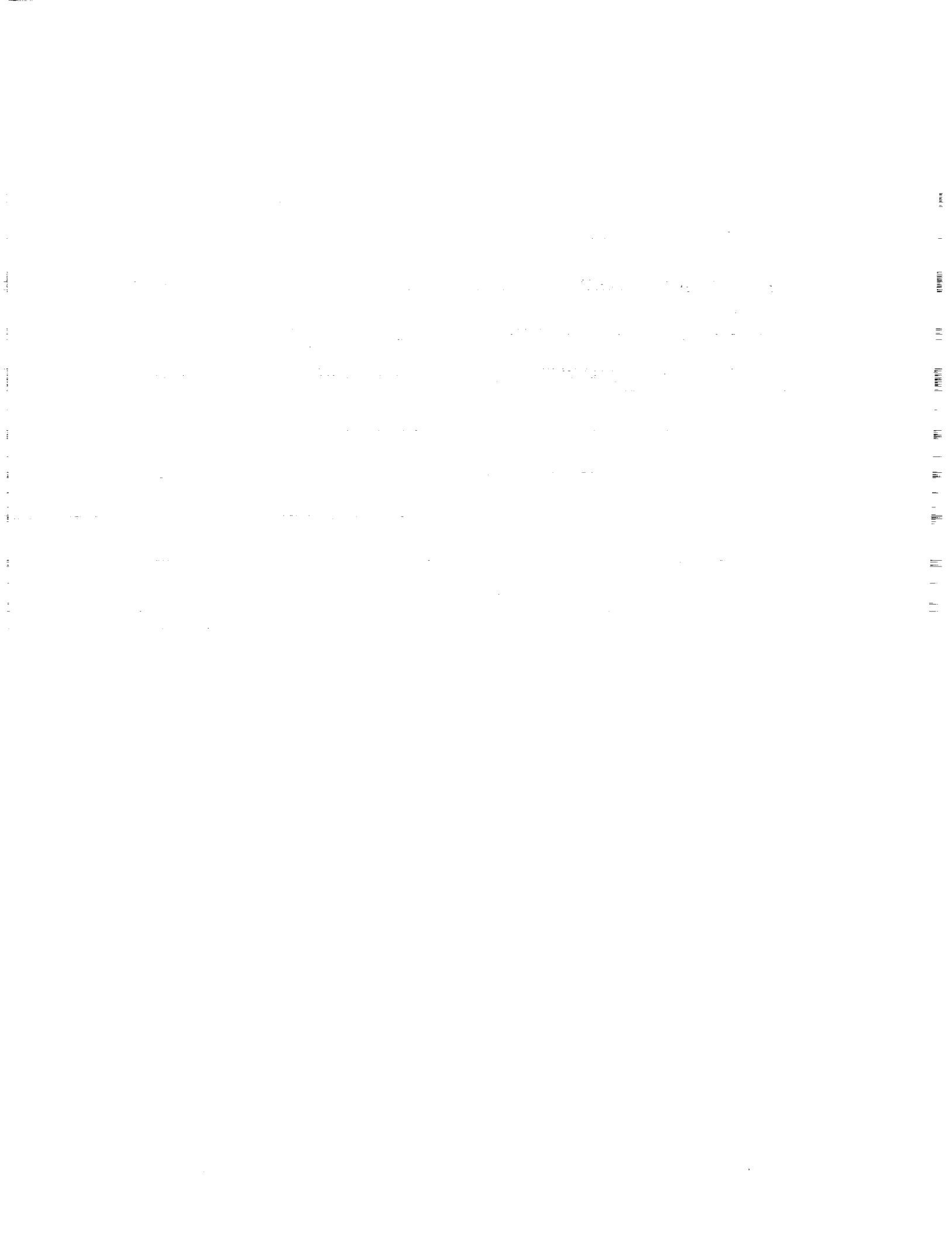
Abstract- The digital frequency synthesizer (DFS) is an integral part of the programmable local oscillator (PLO) which is being developed for the NASA's Deep Space Network (DSN) and radar astronomy. In this report, the theory of operation and the design of the DFS are discussed, and the design parameters in application for the Goldstone Solar System Radar (GSSR) are specified. The spectral purity of the DFS is evaluated by analytically evaluating the output spectrum of the DFS. A novel architecture is proposed for the design of the DFS with a frequency resolution of $1/2^{48}$ of the clock frequency ($0.35 \mu\text{Hz}$ at 100 MHz), a phase resolution of 0.0056 degrees (16 bits), and a frequency spur attenuation of -96 dBc .

DFS for Radar Astronomy



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I. Introduction

This report describes the theory and the design of a digital frequency synthesizer (DFS) used in the programmable local oscillator (PLO) for applications in the NASA's Deep Space Network (DSN) and the Goldstone Solar System Radar (GSSR) [2,3,4]. The DFS provides a low cost solution for frequency synthesis with the following features:

- Controllable frequency and phase with extremely high resolution
- Long term stability in the output frequency
- Low phase noise and high spectral purity
- Phase continuous frequency adjustment

In Figure (1), the overall configuration of the X-band exciter proposed in [1] is shown. This exciter is used for transmission of a coherent X-band signal from the DSN station, to a distant solar system planet. The reflected signal from the planet is used for generating radar images of the planet [2,3].

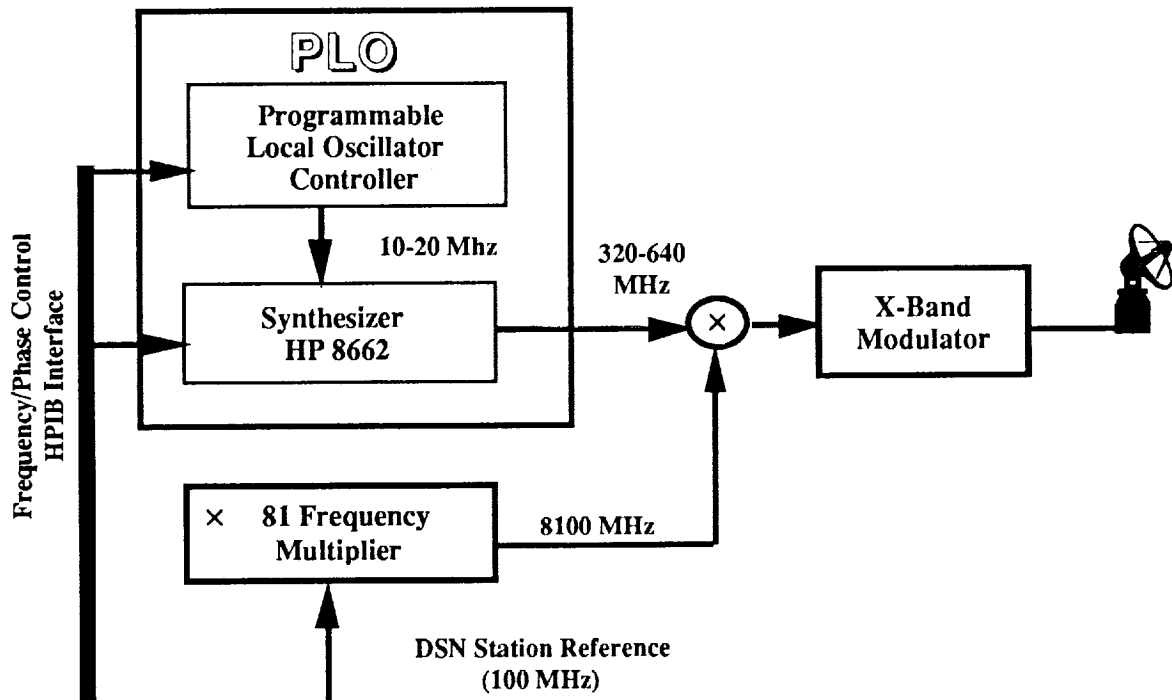


Figure (1). X-Band Exciter for the Goldstone Solar System Radar Transmitter

The design of the exciter is based around using a high-resolution PLO with controllable phase and frequency. The output of the PLO is ideally a single carrier with a frequency range of 10-20 MHz. This signal is used as a reference by an HP-86621 synthesizer; the output of the synthesizer is up-converted with an ultra-stable maser clock provided by the station. This signal is then modulated and transmitted in the X-band.

The main focus of this work is the design and analysis of the PLO shown in Figure (1). In Figure (2), the block diagram of the PLO is depicted. The PLO is composed of a DFS and digital-to-analog conversion module, and is controlled by a host via an HP¹ Interface Bus (HPIB).

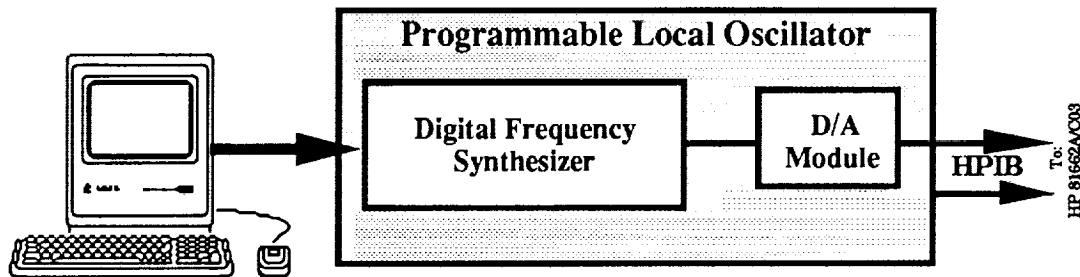


Figure (2). Programmable Local Oscillator Block Diagram

The PLO controller software controls both the frequency and the phase from the PLO, via the HPIB. Other control functions of the host via the HPIB are described in more detail in [4].

I.1 Organization of This Report

In sections II through IV, the design and analysis of the DFS are covered. In section V, the design requirement in application for GSSR is outlined. In section VI, it is shown that none of the off-the-shelf DFS modules available in the commercial market satisfy our design requirement. In section VII, an architecture for the DFS is proposed that satisfies our requirement.

II. Digital Frequency Synthesizer

With the advent of high-speed digital signal processing hardware, today frequency synthesis for intermediate frequencies (IF) can be achieved in the digital domain. A DFS uses a single reference frequency to generate a range of output frequencies. In general, an ideal frequency synthesizer would generate a single sinusoid at a desired output frequency denoted as $S(t) = \text{Sin}(2\pi F_o t)$. The underlying theoretical model of the DFS is shown in Figure (3).

¹ HP™ is the trademark of the Hewlett-Packard Co.

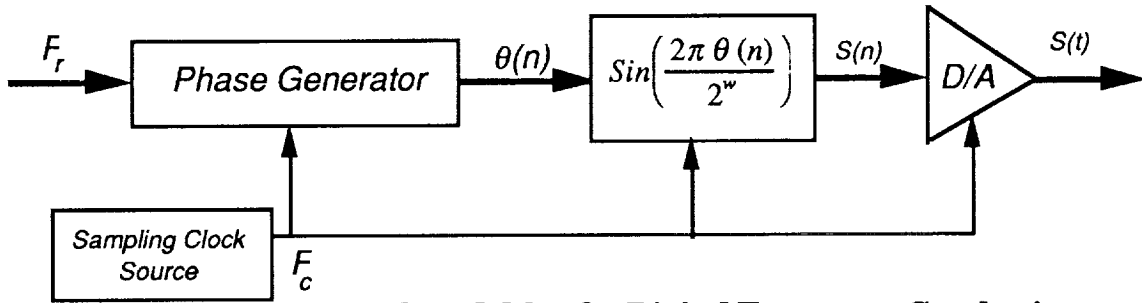


Figure (3). Theoretical Model for the Digital Frequency Synthesizer

The phase and frequency of the output sine wave are controlled by the frequency control word, denoted as F_r . This value is used by the phase generator to compute the phase sequence $\theta(n)$; this sequence is then mapped around the quantized unit circle with each clock pulse, which occurs at frequency F_c . The granularity of the phase space depends upon the number of quantization intervals around the unit circle, and is taken to be equal to 2^W in Figure (3). Ideally, the sequence $S(n)$ is the sampled values of $S(t)$ at the discrete sampling points nT , where each sample is taken at the rate of $T=1/F_c$, i.e., $S(n)=\text{Sin}(2\pi F_0 nT)$. In the next section, the relation among F_c , F_0 and F_r is clarified.

III. Theory of Operation

The implementation of the DFS shown in Figure (4) was first introduced in [8]. This approach employs a binary accumulator for the phase generator, and a look-up table for converting $\theta(n)$ to $S(n)$.

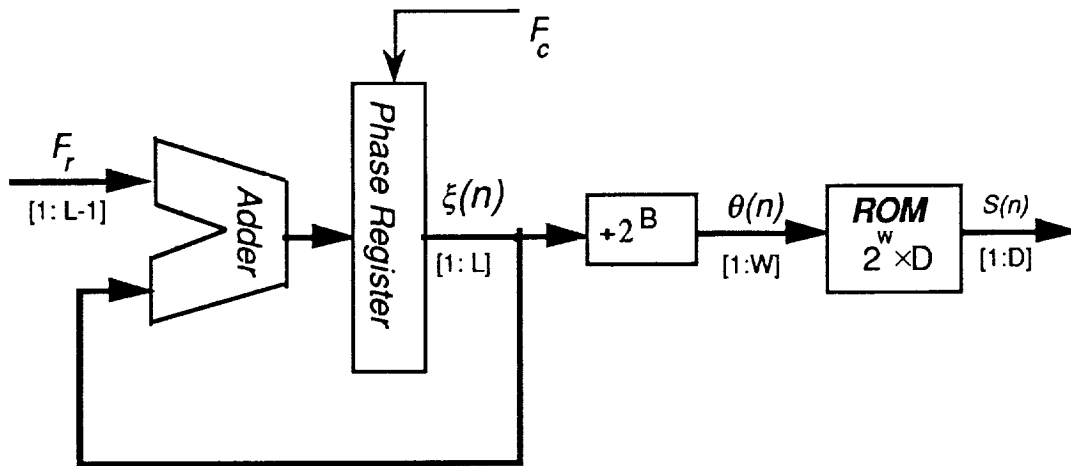


Figure (4). Implementation Model for DFS

The theory of operation for this model is as follows: an L -bit binary adder is incremented using modulo 2^L addition by the frequency control word: F_r , and the accumulated result is stored in the phase register as $\xi(n)$. The sequence $\xi(n)$ is truncated from L -bit to W -bit to produce $\theta(n)$, which is used to address a look-up table stored in a read-only memory (ROM) to output the desired output samples $S(n)$. In order to provide sufficient resolution in

most applications, the binary accumulator size must be in excess of 20 bits long. It is practically impossible to use a ROM with a depth of 2^{20} for converting the phase sequence $\xi(n)$ to the sine samples. Hence, it becomes necessary to truncate the output of the phase generator by B -bit to a practical range $W=L-B$. The truncation $\xi(n)$ to $\theta(n)$, is equivalent to a modulo- $2^{(L-B)}$ division (or shift), as shown in Figure (4). The truncated phase sequence $\theta(n)$ is used as an address to the $2^W \times D$ -bit-wide ROM which maps $\theta(n)$ into the desired sequence $S(n)$.

The output frequency of the DFS, denoted as F_o is related to F_c , and F_r by considering the recursion relation for the phase sequence $\xi(n)$, which is $\xi(n+1) = (\xi(n) + F_r)$ modulo- 2^L . The rate of change in each unit time for $\xi(n)$ is

$$\frac{\Delta \xi(n)}{\Delta t} = F_r F_c \quad (1)$$

In case of infinite precision in the ROM and no phase quantization with $\theta(n) = \xi(n)$, the output is $S(n) = \text{Sin}(2\pi F_o n T)$, where the output frequency F_o for the sine function is

$$F_o = \frac{\omega_o}{2\pi} = \frac{\Delta \xi(n)}{2^L} = \frac{F_r F_c}{2^L} \quad (2)$$

Note that F_r is an integer valued variable, and F_o is a real valued variable, thus for a given fixed clock frequency and accumulator length L , the frequency control word is $F_r = \lfloor 2^L F_o / F_c \rfloor$, where $\lfloor x \rfloor$ denotes the floor of x .

From the sampling theorem, it is well known that the maximum frequency of a sampled sinusoid is bounded by $F_c/2$. Hence, we have

$$F_o^{\text{Max}} = \frac{F_c}{2} \Rightarrow \text{from (1)} \quad 1 \leq F_r \leq 2^{L-1} \quad (3)$$

From equation (3), it is concluded that it is possible to generate $2^{(L-1)}$ possible output frequencies with a frequency resolution of $F_c/2^L$.

To explore the spectrum of this sequence consider the sequence $\xi(n)$ which is periodic. The period here is defined as the smallest integer N such that $\xi(n) = \xi(n+N)$. This period is $N = 2^L / \text{gcd}(F_r, 2^L)$, where $\text{gcd}(\alpha, \beta)$ denotes the greatest common divisor of integers α and β . Thus, N will be equal to the period of the output sine wave if and only if $F_r = \text{gcd}(F_r, 2^L)$, or equivalently F_r is purely a power of two. Since $\xi(n)$ is periodic with period N , it can be represented by a Fourier series composed of N -harmonics with the first fundamental frequency at $F_r/2^L$. We refer to these $N-1$ harmonics

(excluding the first fundamental frequency) as "*frequency spurs*", which form the induced interference with the desired output signal.

In case $W < L$, the truncated phase sequence $\theta(n) = [\xi(n)/2^{(L-W)}]$, where $[x/y]$ denotes taking the integer part of the division of x by y , has the same period N as $\xi(n)$. Therefore, the sequence $\theta(n)$ can also be represented by a discrete spectrum of a periodic sequence consisting of N spectral lines. Furthermore, if F_r and 2^L are mutually prime (i.e., F_r is odd), the number of spectral lines is exactly 2^L , which in practice is a very large number.

The size of the arithmetic field used to compute the phase sequence $\theta(n)$ directly impacts the frequency spur characteristics of the DFS. When using the binary field to compute this sequence, the DFS's output sine wave consists of $N = 2^L / \text{gcd}(F_r, 2^L)$ harmonics with the first fundamental frequency at $F_c F_r / 2^L$, and the number of possible output frequencies is also always restricted to be powers of two, if binary number representation is used for representing $\theta(n)$. It should be noted that this restriction can be avoided by using other arithmetic fields such as the decimal field, or alternatively other forms of number representation such as binary coded decimals (BCD).

III.1 Output of DFS Due to Phase Truncation

For simplicity assume without loss of generality that $F_c = 1$. When the phase sequence $\xi(n)$ is truncated to W -bit, let $L = W + B$, then the the output sequence is

$$S(n) = \text{Sin} \left(2\pi \frac{\left[\frac{\xi(n)}{2^B} \right]}{2^W} \right) \quad (4)$$

The integer part of the ratio in the numerator of (4) can be written as

$$\frac{\xi(n)}{2^B} = \left[\frac{\xi(n)}{2^B} \right] + \varepsilon(n) \quad (5)$$

where $\varepsilon(n)$ is an error sequence corresponding to the remainder of the expression in (5), and its value is always bounded by one. Using equation (5) in (4), the output sequence can be expanded as

$$\begin{aligned}
\text{Sin}\left(2\pi\left[\frac{\xi(n)}{2^B}\right]\right) &= \text{Sin}\left(\frac{2\pi}{2^W}\frac{\xi(n)}{2^B} + \frac{2\pi}{2^W}\varepsilon(n)\right) \\
&= \text{Sin}\left(\frac{2\pi}{2^L}\xi(n)\right)\text{Cos}\left(\frac{2\pi}{2^W}\varepsilon(n)\right) + \text{Cos}\left(\frac{2\pi}{2^L}\xi(n)\right)\text{Sin}\left(\frac{2\pi}{2^W}\varepsilon(n)\right) \quad (6)
\end{aligned}$$

Under reasonable circumstances, $2^L \gg 1$, the magnitude of the sequence $\varepsilon(n)$ is small so that $\text{Sin}(2\pi\varepsilon(n)/2^W)$ will be small compared to $\text{Sin}(2\pi\xi(n)/2^L)$ and $\text{Cos}(2\pi\varepsilon(n)/2^W)$ is close to 1. Hence, we can make a first order approximation to the output sequence $S(n)$, denoted as $S_1(n)$ to be

$$S_1(n) = \text{Sin}\left(\frac{2\pi\xi(n)}{2^L}\right) \quad (7)$$

which is the desired output sequence. To estimate the frequency and the size of the largest spur which is denoted by $\psi(n)$, we look at the next approximation, and note that

$$\begin{aligned}
&\text{Sin}\left(\frac{2\pi}{2^W}\left[\frac{\xi(n)}{2^B}\right]\right) - \text{Sin}\left(\frac{2\pi\xi(n)}{2^L}\right) = \\
&= \text{Sin}\left(\frac{2\pi}{2^L}\xi(n)\right)\left[\text{Cos}\left(\frac{2\pi}{2^W}\varepsilon(n)\right) - 1\right] + \text{Cos}\left(\frac{2\pi}{2^L}\xi(n)\right)\text{Sin}\left(\frac{2\pi}{2^W}\varepsilon(n)\right) \\
&= -2\text{Sin}\left(\frac{2\pi}{2^L}\xi(n)\right)\text{Sin}^2\left(\frac{\pi}{2^W}\varepsilon(n)\right) + \text{Cos}\left(\frac{2\pi}{2^L}\xi(n)\right)\text{Sin}\left(\frac{2\pi}{2^W}\varepsilon(n)\right) \quad (8)
\end{aligned}$$

Since $\varepsilon(n)$ is small, $\text{Sin}^2(\pi\varepsilon(n)/2^W) \ll \text{Sin}(2\pi\varepsilon(n)/2^W)$ for n such $\text{Sin}(2\pi\xi(n)/2^L) \leq \text{Cos}(2\pi\xi(n)/2^L)$, the size of the largest spur, by approximating the second term in (8), and bounding the magnitude of this term as follows

$$\left|\text{Cos}\left(\frac{2\pi}{2^L}\xi(n)\right)\right|\left|\text{Sin}\left(\frac{2\pi}{2^W}\varepsilon(n)\right)\right| \leq \frac{2\pi\varepsilon(n)}{2^W} < \frac{\pi}{2^{W-1}} \quad (9)$$

The first inequality is valid since $2^{-W}\varepsilon(n)$ is small, and the second inequality is due to the fact that $\varepsilon(n)$ is always bounded by one. These approximations are not valid for certain frequency ranges, and therefore it becomes necessary to analytically evaluate the output spectrum of DFS.

III.2 Output Spectrum of DFS

To analyze the spectral purity of the DFS, it is desirable to derive an analytical expression for the size of the spurs as a function of frequency. In reference [5], the authors attempt to drive an analytical expression for the output of DFS, however, their approach has a number of flaws [6].

It is shown in Appendix A that the ratio of the power of the output frequency to the power of the largest spur denoted as ρ is

$$\rho_{dB} = 20 \text{Log}_{10} (2^W) \quad (10)$$

This equation is shown to be valid only for odd values of F_r , and the location of the largest spurs are m such that $m/F_r = +1 + 2^w$, and $m/F_r = -1 + 2^w$. As it will become evident later, the requirement of F_r being odd is not restrictive, since a small modification in the architecture of DFS could assure this condition without any impact on the performance, resolution or the spectral purity.

IV. Simulation Results

In cases when L is a small number (<16) it is possible to obtain the output spectrum of DFS by simulation. The DFS shown in Figure (4), was simulated on Mathematica®¹ [9], which is equipped with Fourier transform routines. The output of this program is shown in Figure (5) for the parameters are $L=12$, $F_c=1$ and $W=5$. This example was chosen to verify the result against those of reference [5], which was obtained directly from the output hardware of a DFS.

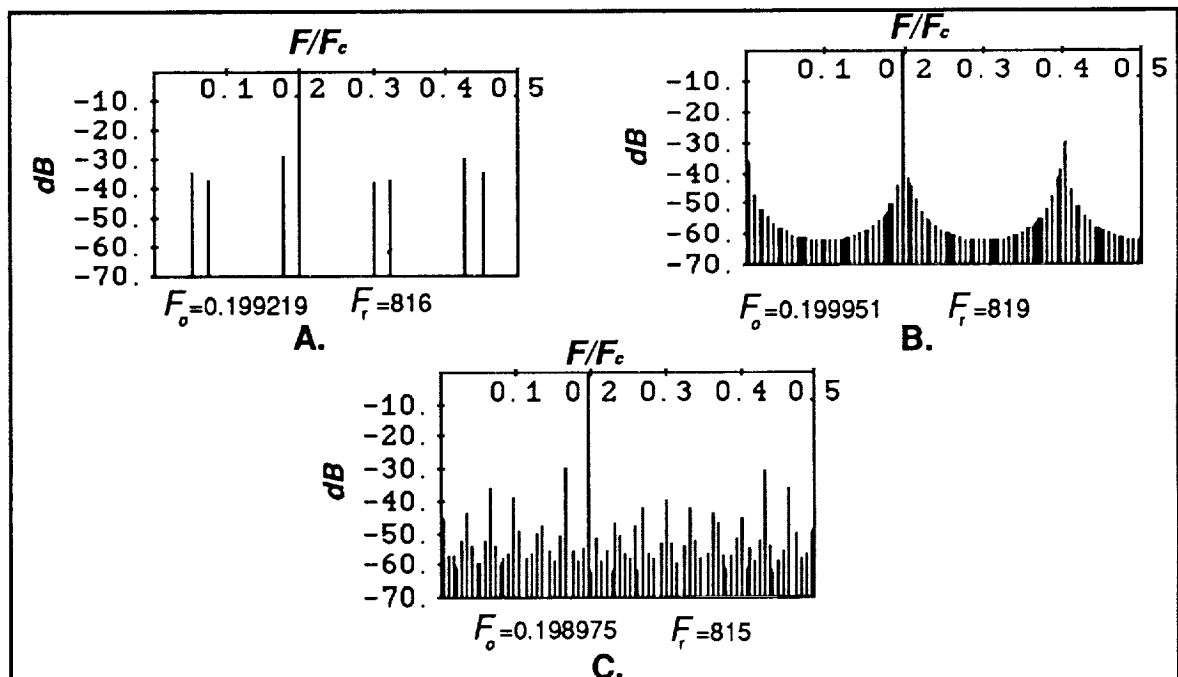


Figure (5). Discrete Fourier Transform Computed From Simulation

¹ Mathematica® is a trademark of Wolfram Research Inc.

IV. 1 Effects of Windowing

The output sequence from the DFS is periodic with period N . When simulating the DFS, it is not practical to generate and store the whole sequence of length N , since the range of values for N in our case of study in some cases is in excess of 2^{32} . Furthermore it is not feasible to compute the discrete Fourier series for very large N . Thus, it becomes essential to window the output sequence $S(n)$ to a practical range.

Let $S^-(n)$ denote the windowed sequence, i.e.,

$$\bar{S}(n) = \sum_i S(i)w(n-i) \quad (11)$$

Consider a window of length M , that is

$$w(n) = \begin{cases} \neq 0, & \frac{-M}{2} \leq n \leq \frac{M}{2} \\ 0, & \text{Otherwise.} \end{cases} \quad (12)$$

Let $\Phi(\omega) = \mathcal{F}(S(n))$ and $\bar{\Phi}(\omega) = \mathcal{F}(S^-(n))$ each respectively represent the Fourier transforms of $S(n)$ and $S^-(n)$, where $\mathcal{F}(\cdot)$ denotes the discrete Fourier transform operator. Since $\Phi(\omega)$ is periodic with period N , it can be written as

$$\Phi(\omega) = \sum_{k=-\frac{N-1}{2}}^{\frac{N-1}{2}} \alpha_k \delta(\omega - \frac{2\pi k}{N}) \quad (13)$$

Here $\delta(\cdot)$ denotes the delta-Dirac function, and the Fourier series coefficient α_k is

$$\alpha_k = \sum_{n=-\frac{N-1}{2}}^{\frac{N-1}{2}} S(n) e^{j\frac{2\pi nk}{N}} \quad (14)$$

The Fourier transform of the windowed sequence can be evaluated as $\bar{\Phi}(\omega) = \Phi(\omega) \otimes W(\omega)$, where \otimes denotes the convolution operation, which is

$$\bar{\Phi}(\omega) = \int_{-\pi}^{\pi} \sum_k W(\omega - \gamma) \alpha_k \delta(\gamma - \omega_k) d\gamma \quad (15)$$

By changing the order of summation and integration in (15) and evaluating the output spectrum at each point $\omega_i = 2\pi i/M$, with $i = -M/2, (M+1)/2, \dots, 0, \dots, (M-1)/2, M/2$ (15) becomes

$$\bar{\Phi}(\omega) = \sum_{k=-\frac{(N-1)}{2}}^{\frac{N-1}{2}} \alpha_k W\left(\omega - \frac{2\pi k}{N}\right) \Bigg|_{\omega = \frac{2\pi}{M}} \quad (16)$$

$\bar{\Phi}(\omega)$ in (16) is a distorted version of $\Phi(\omega)$ due to the spectral leakage caused by windowing. To illustrate the effect of spectral leakage consider the Fourier transform of a rectangular window of length M which is $W(\omega) = \text{Sin}(\omega M/2) / \text{Sin}(\omega/2)$ [10]. The amplitude spectrum of $W(\omega)$ is shown in Figure (6.a). The zero crossing of this function is at $2\pi/M$. It is evident from equation (16) that the output spectrum is the superposition of the original spectrum and the basis function $\text{Sin}(\omega M/2) / \text{Sin}(\omega/2)$ as shown in Figure (6.a) shifted at each point $2\pi i/M$, with $i = -M/2, -(M+1)/2, \dots, 0, \dots, (M-1)/2, M/2$, as shown in Figure (6.b).

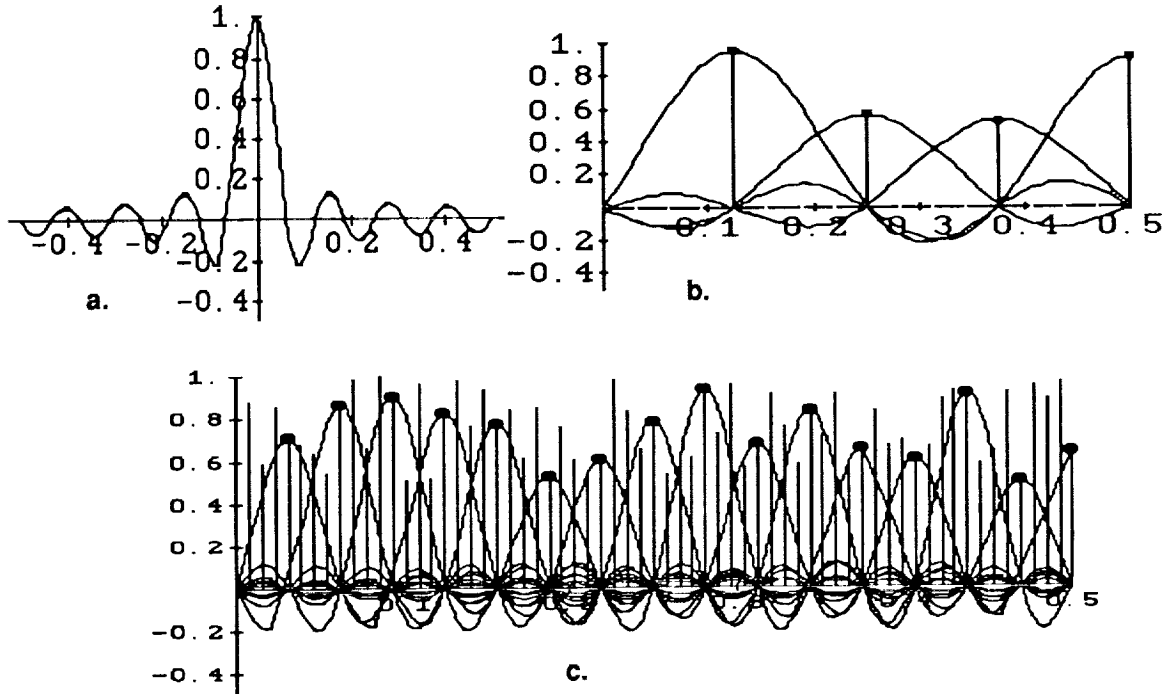


Figure (6). Fourier Transform of the a. Window b. Basis Function c. $\bar{\Phi}(\omega)$

In Figure (6.c), the sampled spectrum is shown for every 4-th impulse. At each discrete point spaced at $2\pi/M$, the original spectrum is superimposed with all the other $(M-1)$ sidelobes. In Figure (7.a and b), the distorted version of the output spectrum is shown for the example of Figure (5), where $N=2048$, and $M=256$.

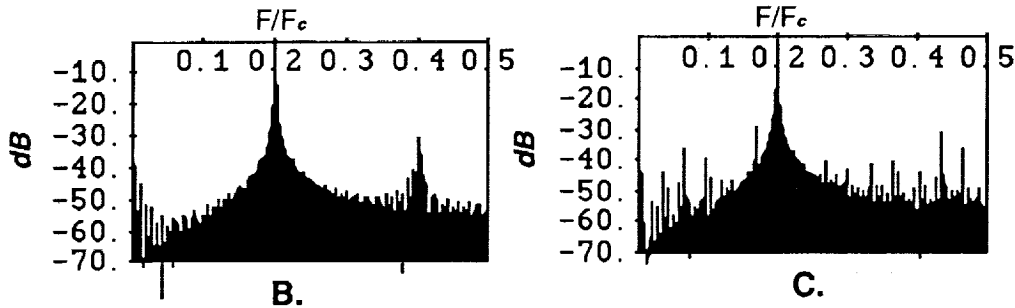


Figure (7). Effect of Windowing on the Output Spectrum for cases B. and C. of Figure (5).

The spectral leakage causes a bias in the amplitude and the location of the harmonics. To reduce this effect, the window should exhibit low-amplitude sidelobes far from the central lobe, and the transition of to the low sidelobes should be very rapid. Hence, a design criterion to suppress the leakage is the peak sidelobe level, relative to the main lobe. For the rectangular window shown in Figure (6.a), the highest sidelobe level for the rectangular window is -13 dB. To assess the spectral purity of the DFS in our application, it is necessary for the highest sidelobe level to be around -96 dB. A class of windows known as the Kaiser-Bessel window exhibit this desired level of sidelobe attenuation. This window is defined by

$$w(n) = \frac{I_0 \left[\pi \alpha \sqrt{1 - \left(\frac{n}{M/2} \right)^2} \right]}{I_0(\pi \alpha)}, \quad 0 \leq n \leq \frac{M}{2}, \quad (17)$$

where, $I_0(x) = \sum_{k=0}^{\infty} \frac{x^{2k}}{(2k!)^2}$.

The parameter $\pi \alpha$ is half of the time bandwidth product, and with $\alpha=4.0$ the highest side-lobe level is -97 dB. In Figure (8) both the window sequence and its amplitude spectrum are shown when $\alpha=4.0$.

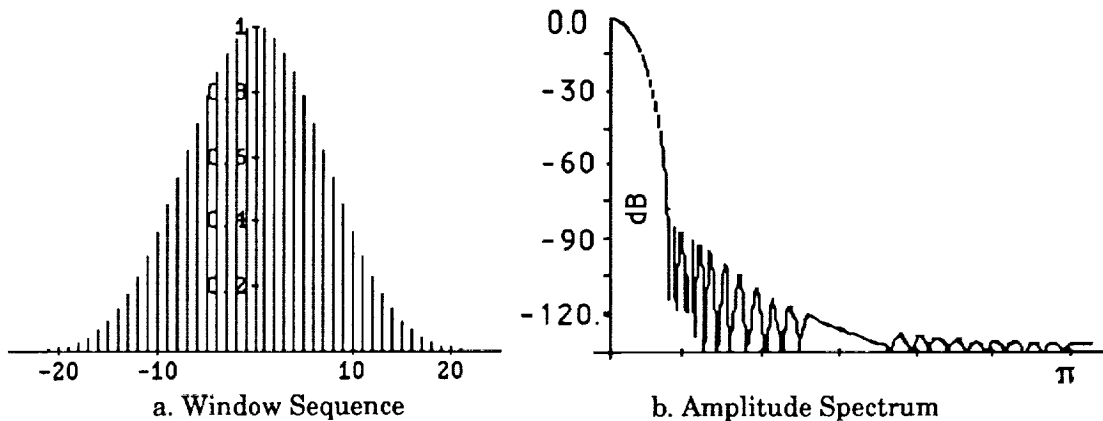


Figure (8). Kaiser-Bessel Window $\alpha=4.0$

V. DFS Requirement for Our Case of Study

The design requirement for the DFS is summarized in Table [1].

<u>Design Requirements</u>	
Output Frequency	10-20 MHz
Frequency Resolution	1 μ Hz
Settling Time Maximum	5 msec
Spectral Purity	-70 dB/c
Dynamic Range	-72 dB
Spectral Continuity	Phase continuous
Phase Resolution	0.2 $^\circ$
Phase Stability	1 $^\circ$ /24 hours

Table [1]. Design Requirement for GSSR

This requirement is extracted from references [1,4], where the advanced exciter is described and the advantages of this requirement for the DSN and radar astronomy are discussed.

VI. Evaluation of Off-the Shelf DFS Modules

At the time when this study was undertaken the two fastest DFS modules available off-the-shelf were Qualcomm¹ Q2334- and Sciteq²VDS-30000. However, it works out that neither one of these products satisfies our design requirements as it is described below.

Qualcomm Q2334:

This single chip also has two problems:

- It only provides a frequency resolution of $1/2^{32} \times 30 \times 10^6 = 7\text{mHz}$, which is not sufficient for our application.
- The maximum clock frequency is 30 MHz, which is not sufficient for our application.

Sciteq VDS-3000:

This module provides the required frequency resolution with (from equation(2)) $1/2^{48} \times 64 \times 10^6 = 0.2\mu\text{Hz}$ which is sufficient for our application. However, there are two problems with this module:

- The phase resolution is only 1.4 $^\circ$ ($360/2^8$), which is not sufficient for our application.

¹ Qualcomm[®] is a registered trademark for Qualcomm Corp.

² Scitec[®] is a registered trademark of Scitec Corp.

•The dynamic range of the output is only 8 bits, which is also not sufficient for our application.

However, the phase resolution which is $360/2^{16} = 0.00549316^\circ$ and the dynamic range, which is 12 bits, are appropriate for our application.

VII.DFS Implementation

In this section, an architecture is given that satisfies our design requirement, and it is also well suited for VLSI implementation. This architecture employs standard off-the-shelf Bipolar ECL (Emitter Coupled Logic) components for implementing the DFS model shown in Figure (4). The proposed architecture has the features and specifications shown in Table [2]:

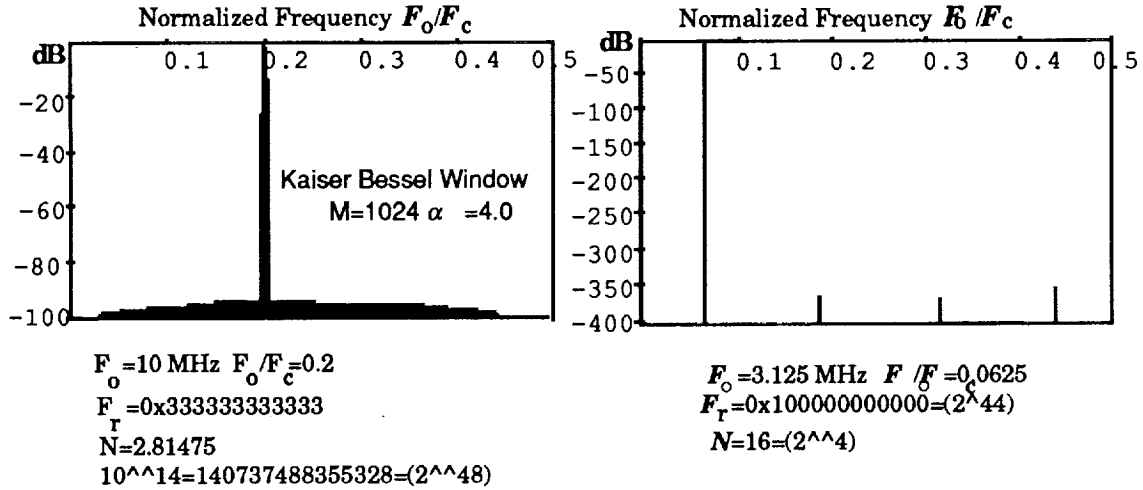
Design Features	
Output Frequency	0-50 MHz
Frequency Resolution	0.35 μ Hz at 100 MHz Sampling Rate
Spectral Purity	-96 dB/c Worst Case
Dynamic Range	Min -72dB Max -96dB
Spectral Continuity	Phase continuous
Phase Resolution	0.0056 $^\circ$
Hardware Requirement	
Accumulator Length	48 bits
Sin (.) Look-up Table Resolution	16 bits
Maximum Clock Frequency	110 MHz
Output Resolution	12/16 bit

Table [2]. Design Features and Hardware Requirements

The resulting architecture not only satisfies our design requirement, it is also the fastest DFS with highest resolution ever built, thus providing an effective approach well into the next century.

VII.1 Spectral Purity

In this section the Kaiser-Bessel window outlined in Section IV.1 is employed to simulate the output spectrum of the DFS. In Figure (9), the simulated spectrums for our design parameters ($F_c=50$ MHz, $L=48$, $W=16$, $M=1024$) for two different frequencies are shown. In Figure (9.b), the output frequency was chosen so the period of the output sequence is 2^4 .



$$F_c = 50 \text{ MHz} \quad L = 48 \quad W = 16 \quad B = 32 \quad \text{Resolution} = 0.177636 \text{ } \mu\text{Hz}$$

Figure (9). Output Spectrum for Our Case of Study

As before, we conclude that the spectral purity of the DFS is dependent on the frequency control word F_r . From this simulation and equation (12), it is concluded that the spurs are well below our design requirement of -96 dBc .

VII.2 DFS Architecture

Our proposed architecture for the DFS is shown in Figure (10). The design methodology is a fully synchronous sequentially pipelined architecture, synchronized with the system clock. The main difference between this architecture and the original model shown in Figure (4) lies in the manner in which the $\text{Sin}(\cdot)$ component of the phase accumulator is computed. The phase generator is a standard 48 bit binary accumulator. Frequency control is provided by loading a 48 bit value computed from equation (2). Phase control is achieved by preloading the upper 16 bit of the 48 bit internal register of the accumulator. Once the device is enabled the content of the internal register is continuously incremented by the value of the frequency control register. The most significant word (16 bits) of the internal register denoted by the index i is used to address the look-up table which output is $\text{Sin}(i2\pi/2^{16})$.

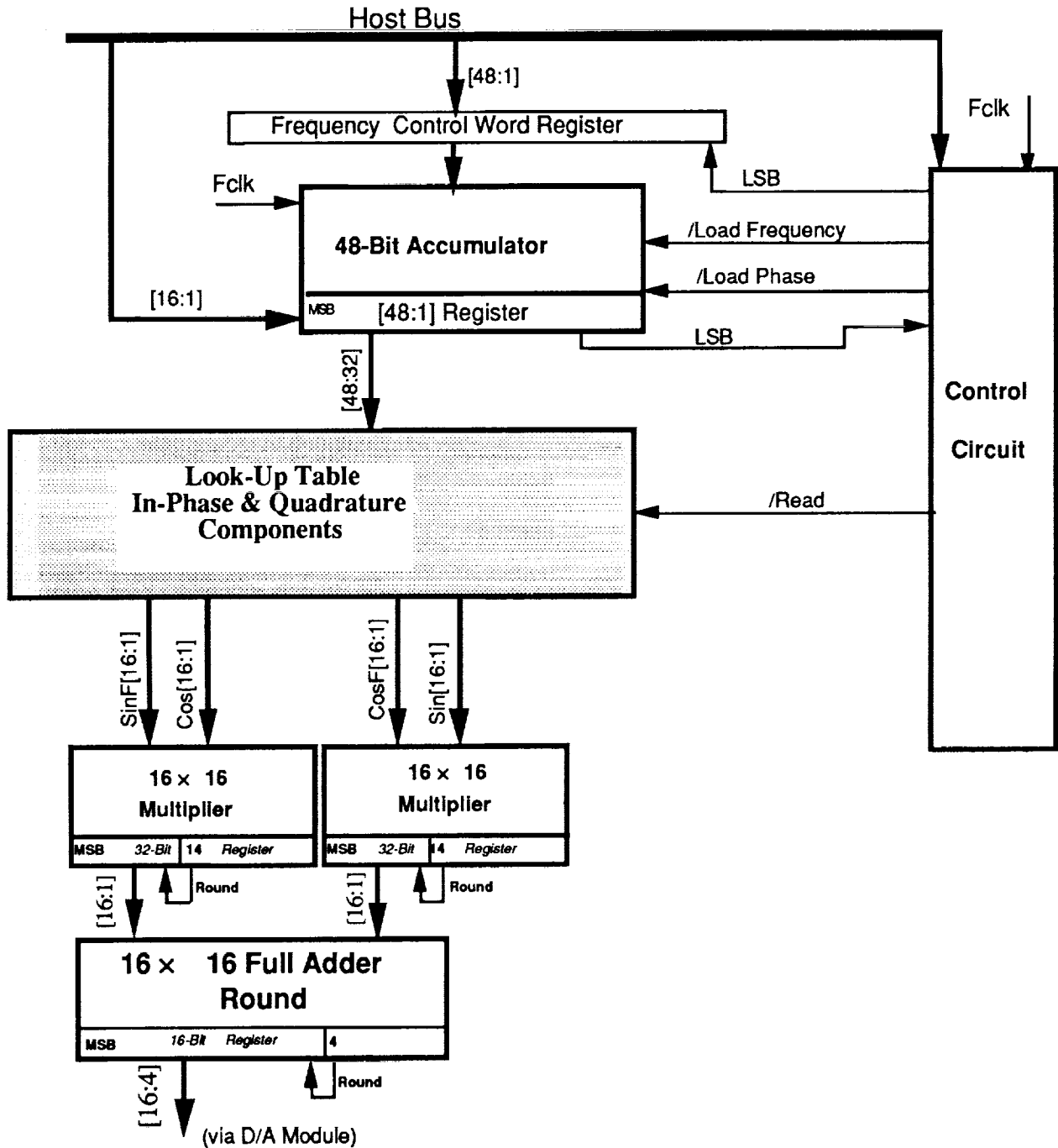


Figure (10). DFS Architecture

One of the fundamental difficulties in designing the DFS is the depth of the look-up table to generate the sine samples of the phase sequence. A simple method to reduce the table size is to decompose the output of the phase generator in binary representation, where

$$\theta = 2^{15} d_{15} + 2^{14} d_{14} + \dots + 2^1 d_1 + d_0 \quad \text{where, } d_i \in \{0,1\} \forall_i \quad (18)$$

Define α and β in terms of θ as

$$\begin{aligned}\alpha &= 2^{15}d_{15} + 2^{14}d_{14} + 2^{13}d_{13} + 2^{12}d_{12} + 2^{11}d_{11} + 2^{10}d_{10} + 2^9d_9 + 2^8d_8 \\ \beta &= 2^7d_7 + 2^6d_6 + 2^5d_5 + 2^4d_4 + 2^3d_3 + 2^2d_2 + 2d_1 + d_0\end{aligned}\quad (19)$$

Using this decomposition we have

$$\begin{aligned}\sin(\theta) &= \sin\left(\frac{\alpha + \beta}{2^{16}}2\pi\right) = \sin\left(\left(\frac{2^7d_{15} + \dots + d_8}{2^8} + \frac{2^7d_7 + \dots + d_0}{2^{16}}\right)2\pi\right) = \\ &\sin\left(\frac{2^7d_{15} + \dots + d_8}{2^8}2\pi\right)\cos\left(\frac{2^7d_7 + \dots + d_0}{2^{16}}2\pi\right) + \cos\left(\frac{2^7d_{15} + \dots + d_8}{2^8}2\pi\right)\sin\left(\frac{2^7d_7 + \dots + d_0}{2^{16}}2\pi\right)\end{aligned}\quad (20)$$

The computation of $\sin(i2\pi/2^{16})$ is now reduced to two look-up tables with a depth of 256 points (as opposed to 65536 points), with an additional complexity of two multiplications and an addition. Equation (20) is essentially equivalent to quantizing the unit circle into two levels. The first level is coarse quantization with a quantization interval of $2\pi/256$ as shown by 'x'-mark in Figure (11), and the second level is fine quantization with a quantization interval of $2\pi/65536$. In Figure (11), the fine quantization intervals are shown by solid lines. In the block diagram of Figure (10), the in-phase and quadrature components of the fine quantization points are denoted as SinF and CosF correspondingly, and simply as Sin and Cos for the coarse quantization points.

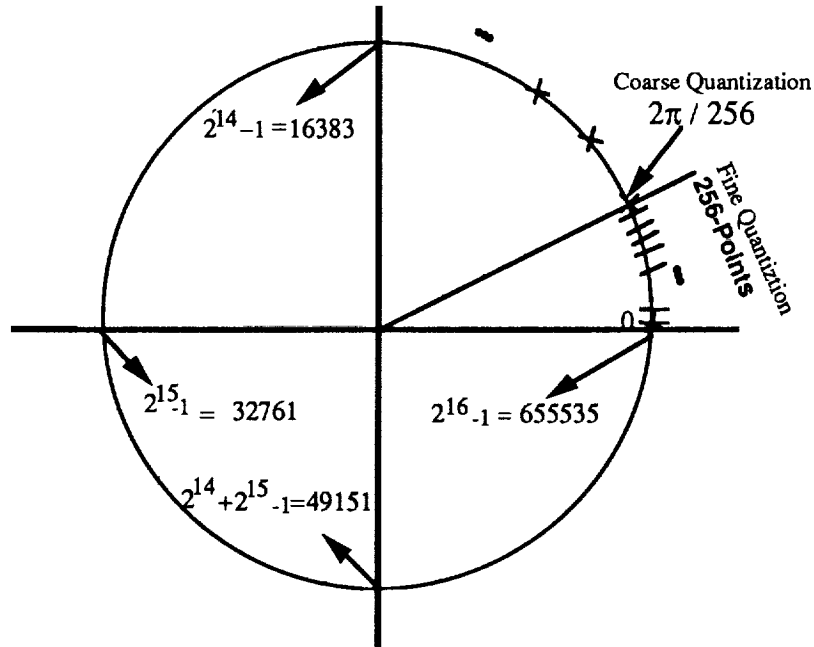


Figure (11). Quantized Unit Circle into Fine and Coarse Angles

To compute equation (20), it is necessary to perform two multiplication and a single addition, organized as a sequential pipeline. This is done by multiplying one component from each set of fine and coarse angles, as shown in Figure (11), resulting into a 32-bit value in which the higher 16-bit values for in-phase and quadrature (I&Q) components are added to yield the desired result. The multiplication operation is performed using a standard off-the-shelf multiplier, with the rounding feature enabled at the 15th-bit. The rounding from the least significant bit is also performed at the last stage as a part of the full adder.

To assure the spectral purity of the DFS expressed in terms of ρ in equation (12), the following minor modification to the control word register can be made to force the accumulator to always make odd frequency steps.

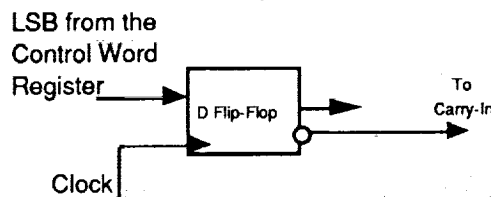


Figure (12). Modification to the Content of Phase Generator to Force F_r to Become Odd

This modification amounts to using the least significant bit of the phase accumulator, as if the word length of the accumulator is $L+1$ and the least significant bit is always set to one. This logic circuit essentially doubles the frequency resolution of the phase accumulator by adding an extra bit to its word length, and forcing the input frequency control word F_r to be used internally as if it is an odd number. This is performed without any compromise to the frequency resolution of the DFS. The input to the carry-in of the 48-bit accumulator is toggled from one to zero when the least significant bit of the phase accumulator is one, and is toggled from zero to one when the least significant bit of the phase accumulator is zero. This operation is effectively equivalent to alternately flipping the carry-in to the accumulator in each clock cycle. It is pointed out in reference [5] that this circuitry improves the spectral purity of the DFS 4 dB; however, their suggestions are based on some flawed results [6]. Our motivation to use this modification is based on our analysis on the spectral purity discussed in section III.

This completes our discussion of the overall architecture of the DFS. In the next section, we outline the detail design of the look-up table to generate the in-phase and quadrature components.

VII.2.a Design of the Look-Up Table

The look-up table is composed of the I&Q components of the fine and coarse quantization intervals. The coarse quantization intervals span the whole unit circle, hence it is only necessary to store a single quadrant for the

coarse I&Q values and adjust the sign prior to computing (20). The I&Q values for the fine quantization angles are small and, for 16-bit fixed point presentation of these values, the in-phase component is between 1 and 0.99969, thereby requiring only 4 bits of resolution. The quadrature component is bounded between 0.0 and 0.0246, thus requiring only 10 bits of resolution. The architecture shown in Figure (13) for the look-up table takes advantage of these observations.

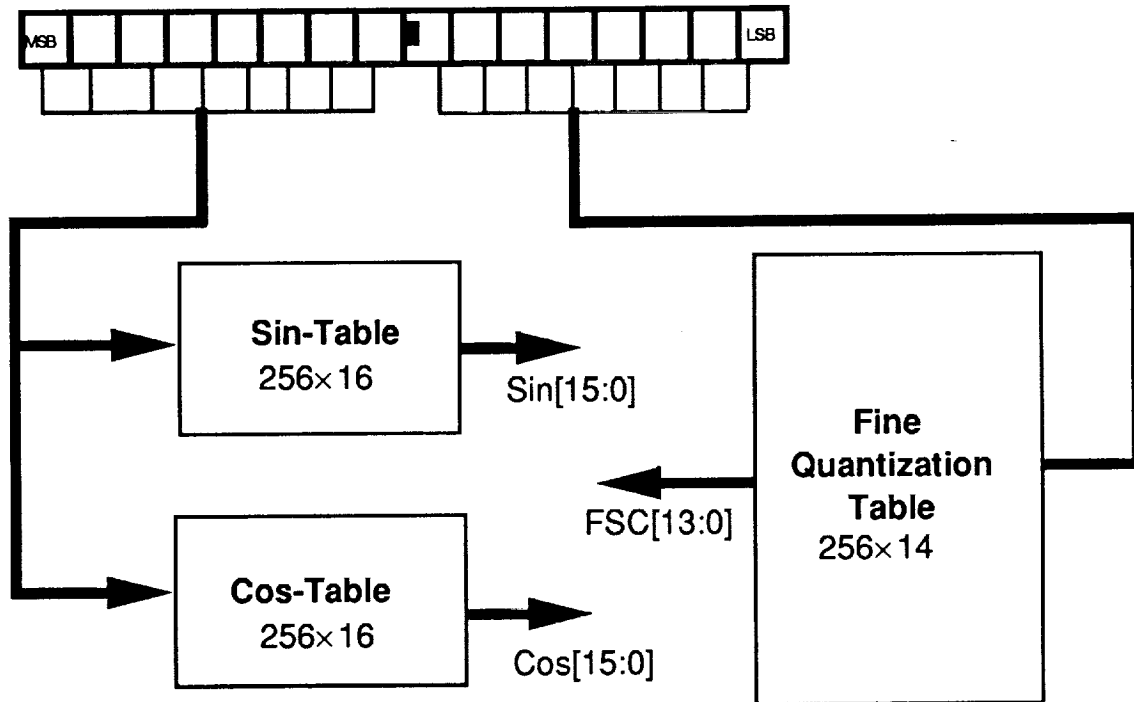


Figure (13). In-Phase & Quadrature Component Look-up Table

In Figure (13), the 16-bit output of the phase generator is split into three parts; the least significant byte is used to output the I&Q components of the fine quantization angles denoted by a single bus name FSC[.] of a width of 14 bits which is in a packed format with 4-bit in-phase and 10-bit quadrature component. The upper 6-bit is used to address the I&Q components of the coarse angles (Sin[], and Cos[]) with 16-bit resolution corresponding to each component.

The format of each output from the look-up table, which forms the input to the multiplier accumulator for computing (20), is shown in Figure (14).

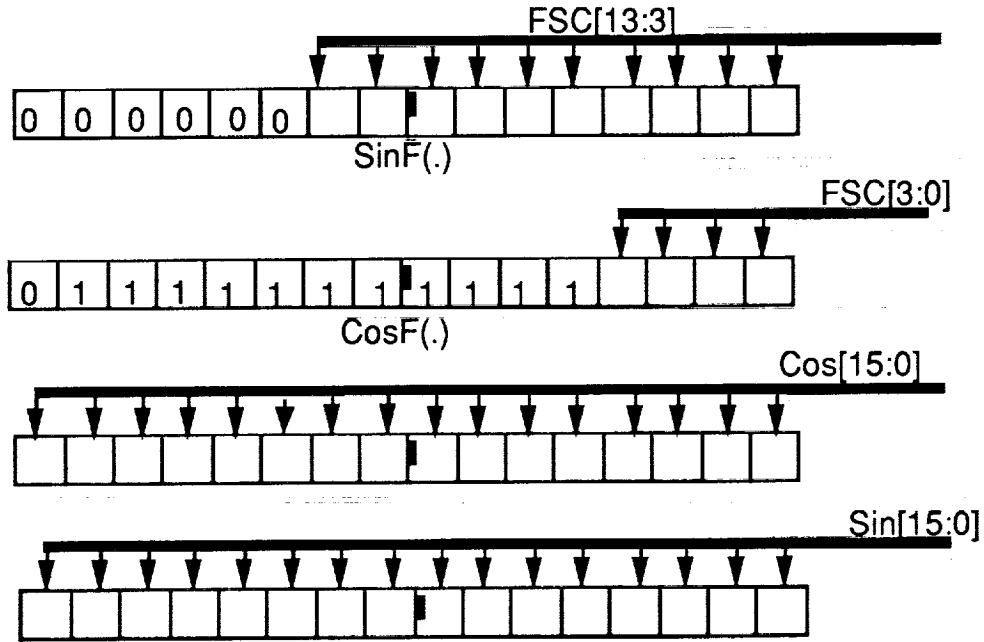


Figure (14). Coarse and Fine I&Q Format

The format of all the numbers in the look-up table is in two's complement format. However for the coarse angles, a scaling factor of $(2^{11}-1)/211$ must be used to scale all the I&Q values. This is due to the fact the D/A module uses offset binary format, and given that this scaling is performed in the look-up table, then converting the output sequence from the two's complement format to offset binary format amounts to inverting the sign of the most significant bit of the results.

VII.2.b DFS Address Map

For control operation of the DFS, the following registers are mapped into the address space of the controlling host. In Table [3], it is assumed that a fixed base address for the DFS is used, which is decoded from the host bus, i.e., the addresses are the offsets from the base address and are shown in the left-hand column. The second column in Table [3] describes the function of accessing each address space, and the last column indicates whether the address space is readable (R) or writable (W).

Add	Function	Purpose	R/W
0x1	Fo -Reg	48 bit Frequency Control Register	W
0x2	Phase Reg	16-bit Phase Accumulator	R/W
0x3	Out-Reg	Output Register 16-Bit	R
0x4	Reset	Software Reset to zeroize all Regs	W
0x5	Freeze	Disable Clock	W
0x6	Go	Enable Clock	W
0x6	Enable	Device Enable	W

Table [3]. DFS Address Map

The first three addresses essentially provide the means to control the frequency and the phase of the DFS. The last four addresses initiate a control function that can be performed under software control from the host. The purpose of a software reset is for initialization of the DFS, and the freeze and go functions are provided so the DFS can be stopped and go anytime during its operation, while maintaining phase and frequency continuity. This feature is useful in application of radar astronomy or spread spectrum communication. The device enable is provided for software control of the device from the host.

VIII. Conclusion

In the first part of this report, a DFS module which forms the main building block for the PLO was analyzed and designed. The spectral purity of the DFS was studied using both analytical and simulation methods. An architecture for the DFS was outlined which is also well suited for VLSI fabrication. This architecture provides a frequency resolution of $1/2^{48}$ of the clock frequency (0.35 μ Hz at 100 MHz), a phase resolution of 0.0056 degrees (16 bits), and a frequency spur attenuation of -96 dBc (16-bit output frequency).

Appendix A. Derivation of Output Spectrum of DFS

Consider the function

$$S(n) = \text{Sin} \left(2\pi \frac{\left[\frac{(nF)_{2^L}}{2^B} \right]}{2^W} \right) \quad (\text{A.1})$$

where $(nF)_{2^L}$ means we take the representative modulo 2^L of nF among the numbers $(0, 1, \dots, 2^L - 1)$.

Case 1:

Let $F=1$, and consider the function $\phi(n) = [n2^L / 2^B]$. The values of $\phi(n)$ are

$$\begin{array}{ll} n < 2^B & \phi(n) = 0 \\ 2^B \leq n < 2 \cdot 2^B & \phi(n) = 1 \\ \vdots & \vdots \\ k \cdot 2^B \leq n < (k+1)2^B & \phi(n) = k. \end{array}$$

So the function $\phi(n)$ takes values $0, 1, 2, \dots, 2^W - 1$. The Fourier transform of $S(n)$ is

$$\hat{S}(m) = \sum_{n=0}^{2^L-1} e^{2\pi jmn/2^L} S(n) \quad (\text{A.2})$$

Substituting from (A.1) for $S(n)$ we obtain

$$\hat{S}(m) = \sum_{k=0}^{2^W-1} \left(\sum_{n=k2^B}^{(k+1)2^B-1} e^{2\pi jmn/2^L} \right) \text{Sin} \left(\frac{2\pi k}{2^W} \right) \quad (\text{A.3})$$

Using the identity

$$\left(\sum_{n=k2^B}^{(k+1)2^B-1} e^{2\pi jmn/2^L} \right) = e^{2\pi jmk/2^W} \frac{1 - e^{2\pi jm/2^W}}{1 - e^{2\pi jm/2^L}} \quad (\text{A.4})$$

we obtain

$$\hat{S}(m) = \frac{1 - e^{2\pi jm/2^W}}{1 - e^{2\pi jm/2^L}} \sum_{k=0}^{2^W-1} e^{2\pi jmk/2^W} \text{Sin} \left(\frac{2\pi k}{2^W} \right) \quad (\text{A.5})$$

Now

$$\begin{aligned} \sum_{k=0}^{2^W-1} e^{2\pi jmk/2^W} \text{Sin}\left(\frac{2\pi k}{2^W}\right) &= \sum_{k=0}^{2^W-1} \text{Cos}\left(\frac{2\pi mk}{2^W}\right) \text{Sin}\left(\frac{2\pi k}{2^W}\right) \\ +j \sum_{k=0}^{2^W-1} \text{Sin}\left(\frac{2\pi mk}{2^W}\right) \text{Sin}\left(\frac{2\pi k}{2^W}\right) & \end{aligned} \quad (\text{A.5})$$

Using the two trigonometric identities

$$\begin{aligned} 2 \text{Cos}A \text{Sin}B &= \text{Sin}(B+A) - \text{Sin}(B-A), \\ 2 \text{Sin}A \text{Sin}B &= \text{Cos}(A-B) - \text{Cos}(A+B), \end{aligned}$$

we rewrite (A.5) in the form

$$\begin{aligned} 2 \sum_{k=0}^{2^W-1} \text{Cos}\left(\frac{2\pi mk}{2^W}\right) \text{Sin}\left(\frac{2\pi k}{2^W}\right) &= \sum_{k=0}^{2^W-1} \text{Sin}\left(\frac{2\pi(m+1)k}{2^W}\right) + \sum_{k=0}^{2^W-1} \text{Sin}\left(\frac{2\pi(m-1)k}{2^W}\right) \\ 2 \sum_{k=0}^{2^W-1} \text{Sin}\left(\frac{2\pi mk}{2^W}\right) \text{Sin}\left(\frac{2\pi k}{2^W}\right) &= \sum_{k=0}^{2^W-1} \text{Cos}\left(\frac{2\pi(m-1)k}{2^W}\right) - \sum_{k=0}^{2^W-1} \text{Cos}\left(\frac{2\pi(m+1)k}{2^W}\right) \end{aligned} \quad (\text{A.6})$$

It follows that if $m \neq \pm 1 \text{ Mod } 2^W$, then

$$\hat{S}(m) = 0 \quad (\text{A.7})$$

If $m = 1 \text{ Mod } 2^W$, then

$$\hat{S}(m) = 2^{W-1} j \frac{1 - e^{2\pi j/2^W}}{1 - e^{2\pi jm/2^L}} \quad (\text{A.8})$$

If $m = -1 \text{ Mod } 2^W$, then

$$\hat{S}(m) = -2^{W-1} j \frac{1 - e^{-2\pi j/2^W}}{1 - e^{-2\pi jm/2^L}} \quad (\text{A.9})$$

Q.E.D

Case II:

F and 2 are relatively prime. The numbers $(nF)_{2^L}$ are the permutation of the numbers $\{0,1,2,\dots,2^L-1\}$ induced by multiplication by F Modulo 2^L . Let us write $S_F(n)$ for $S(n)$ to emphasize the dependence on F . Then $S_F(n)=S_1(Fn)$. Consequently,

$$\begin{aligned}\hat{S}_F(m) &= \sum_{n=0}^{2^L-1} e^{2\pi jmn/2^L} S_F(n) = \sum_{n=0}^{2^L-1} e^{2\pi jmn/2^L} S_1(n) \\ &= \hat{S}_1(mF^{-1}) \quad (\text{A.10})\end{aligned}$$

This settles the case $\text{g.c.d}(2,F)=1$.

Let us obtain approximations to the largest and the second largest values for $|S_F^\wedge(m)|$. Clearly the largest value of $|S_1^\wedge(m)|$ occurs for $m=\pm 1$. For such values of m we have the approximation

$$\frac{1 - e^{-2\pi j/2^W}}{1 - e^{2\pi j/2^L}} \approx \frac{\frac{2\pi}{2^W}}{\frac{2\pi}{2^L}} = 2^B \quad (\text{A.11})$$

so that

$$|\hat{S}_1(\pm 1)| \approx 2^{L-1} \quad (\text{A.12})$$

The second largest value of $|S_1^\wedge(m)|$ occurs for $m=\pm 1+2^W$. Here we obtain approximations

$$\begin{aligned}\frac{1 - e^{-2\pi j/2^W}}{1 - e^{2\pi j(\pm 1+2^W)/2^L}} &\approx \frac{\frac{2\pi}{2^W}}{\frac{2\pi(\pm 1+2^W)}{2^L}} = \frac{2^B}{\pm 1+2^W} \approx 2^{B-W} \quad \text{therefore} \\ |S_1(\pm 1+2^W)| &\approx 2^{B-1} \quad (\text{A.13})\end{aligned}$$

When F is relatively prime to 2, i.e., $\text{g.c.d}(F,2)=1$, from (A.9), we have $S_F^\wedge(m)=S_1^\wedge(mF^{-1})$, hence the largest value of $|S_F^\wedge(m)|$ occurs for $m=\pm F$ Modulo 2^L

$$|\hat{S}_F(\pm F)| \approx 2^{L-1} \quad (\text{A.14})$$

Similarly, the second largest value of $|S_F^\wedge(m)|$ occurs for $m=F(\pm 1+2^W)$,

$$|\hat{S}_F(F(\pm 1 + 2^W))| \approx 2^{B-1} \quad (\text{A.15})$$

Thus, the ratio ρ of the power of the output frequency to the power of the largest spur which is obtained by dividing (A.14) by (A.15), and when expressed in dB is

$$\rho = 20 \text{ Log}_{10} (2^W) \quad (\text{A.16})$$

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16. Abstract The digital frequency synthesizer (DFS) is an integral part of the programmable local oscillator (PLO) which is being developed for the NASA's Deep Space Network (DSN) and radar astronomy. In this report, the theory of operation and the design of the DFS are discussed, and the design parameters in application for the Goldstone Solar System Radar (GSSR) are specified. The spectral purity of the DFS is evaluated by analytically evaluating the output spectrum of the DFS. A novel architecture is proposed for the design of the DFS with a frequency resolution of $1/2^{48}$ of the clock frequency (0.35 microHz at 100 MHz), a phase resolution of 0.0056 degrees (16 bits), and a frequency spur attenuation of -96 dBc.					
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