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Digital Test Signal Generation: An Accurate SNR Calibration Approach for the DSN

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A new method of generating analog test signals with accurate signal-to-noise ratios (SNRs) is described. High accuracy will be obtained by simultaneous generation of digital noise and signal spectra at a given baseband or bandpass-limited bandwidth. The digital synthesis will provide a test signal embedded in noise with the statistical properties of a stationary random process. Accuracy will only be dependent on test integration time with a limit imposed by the system quantization noise (expected to be 0.02 dB). Setability will be approximately 0.1 dB. The first digital SNR generator to provide baseband test signals is being built and will be available in early 1991.

I. Introduction

Spacecraft link performance optimization has always been a requirement for the missions supported by the Deep Space Network (DSN). This optimization relies on accurate predictions for the degradations (and losses) encountered in the different modulation and detection processes in use in the telecommunications link. Mathematical models for these processes are usually available beforehand, to be later verified by tests run at the Telecommunications Development Laboratory (TDL), the Compatibility Test Area, and sometimes at the DSN stations.

Figure 1 represents the Signal Processing Center (SPC) portion of a typical DSN communications link. The parameters of interest to be considered are:

$$\text{Carrier SNR} = P_C/N_0 \tag{1}$$

$$\text{Symbol SNR} = ST_S/N_0 \tag{2}$$

$$\text{Bit SNR} = ST_b/N_0 \tag{3}$$

with

P_C = the portion of received power in the residual carrier

S = the portion of received power in the modulation sidebands

T_S = the symbol period

T_b = the bit period

N_0 = the noise spectral density

Note that the above parameters, to be referred to generically as SNR, may also be considered as the residual

carrier power, energy per symbol, and energy-per-bit to spectral-noise-density ratios, respectively.

Calibration of telemetry system losses and SNR degradation[1] has traditionally been performed with the well-known Y-factor method [1]. Different error sources come into play depending on whether the calibration is performed in the carrier or in the modulated part of the transmitted spectrum. In [1], these error sources have been identified and quantified with a final worst-case error of ± 0.45 dB. Reported accuracy of the manual method varies from 0.3 dB at the TDL to 1 dB at the DSN stations.

To improve the accuracy and to automate the measurement process, a method has been developed to digitally synthesize the precision test signal. The signal-to-noise ratios obtained are then independent of gain variations, and full knowledge and control of waveshapes and the modulation index can be achieved. As shown in Fig. 2, calibration of the degradation and losses of the different processes are performed as in the traditional Y-factor method. Calibrated SNR and bit-error rate (BER) of signals input to the device under test are compared to the observed SNR and BER of the signals the device outputs. The advantage of the digital SNR generator (DSG) approach is that the SNR-generation process is truly stationary. Therefore, long integration times can be used to obtain the accuracy and precision needed. Details of this approach will be described in the following paragraphs.

II. DSG Description

The DSG, as shown in Fig. 2, will generate test signals at baseband (BB). The design allows the generation of an intermediate frequency (IF) to be upconverted, as a future option, to the desired radio frequency band. Note that the baseband spectrum may correspond to coded or uncoded data. Figure 3 is a flowchart describing programmable capabilities of the DSG. It also shows the basic software functions for the baseband spectrum generation mode. These basic functions will also be common to all the other modes. For coded data, the DSG will accept the encoded symbols from some external encoder, e.g., the Test Support Assembly (TSA) in the SPC environment as shown in Fig. 4.

Figure 4 also shows the other DSG components: a SNR generator box (SGB) being built by the Radio Frequency and Microwave Subsystems Section (Section 333), a personal computer (PC) or workstation, and a synthesizer—the latter two being off-the-shelf. The SGB generates the different signal spectra, including IF, dual subcarrier, or quadrature phase-shift key (QPSK). The monitor and control, as well as other signal-processing programs, will reside in the PC or workstation. Commands will be transmitted to the SNR generator box CPU (SGB-CPU), which in turn will configure the special high-speed hardware needed to generate the output calibrated signals. A programmable frequency synthesizer will generate the variable system clock needed by the high-speed hardware. When the DSG is installed in the DSN-SPC environment, an external interface to the TSA may be used, providing the added capability of coded data, simulated Doppler, and other spacecraft-unique parameters which are already available in the TSA.

Figure 5 shows in block diagram form the main functions assigned to each board residing in a Multibus-I chassis in the SGB. Three channels with identical hardware (pattern generator, filter, and attenuator) will be used to generate two baseband-filtered data channels (channels 1 and 2) of subcarrier binary phase-shift keyed data (BPSK) and one channel of lowpass-filtered noise (noise channel) to be subsequently added to produce an analog output

$$S_T(t) = d_1(t)\text{Sin}\, w_{sc1}t + d_2(t)\text{Sin}\, w_{sc2}t + N_{BB}(t) \quad (4)$$

where

$w_{sc1,2}$ = the first or second subcarrier frequency, rad/sec

$d_{1,2}$ = the first or second baseband-filtered data process

N_{BB} = the baseband-filtered noise process

Sin x = sign[sin(x)] or sin(x)

Single channel generation will be attained by elimination of one of the data channels from Eq. (4).

In case of residual carrier generation, channel 1 will generate the carrier, channel 2 will generate the modulation, and the noise channel will generate the bandpass-filtered noise.

Therefore, the filtered output of the DSG in this configuration will be

$$S_T(t) = \cos\Theta(t)\sin w_c t + m(t)\sin\Theta(t)\cos w_c t + N_{BP}(t) \quad (5)$$

where

[1] *Deep Space Network Flight Project Interface Design Handbook*, JPL 810-5, Rev. D (internal document), Jet Propulsion Laboratory, Pasadena, California.

w_c = the carrier frequency, rad/sec

Θ = the modulation index

N_{BP} = the bandpass-filtered noise process

$m(t)$ = the modulation signal

If QPSK signal generation is desired, channel 1 will generate the bandpass-filtered in-phase component, channel 2 will generate the bandpass-filtered quadrature component, and the noise channel will generate the required bandpass-filtered noise. The filtered analog output of the DSG will therefore be

$$S_T(t) = d_I(t)\sin w_c t + d_Q(t)\cos w_c t + N_{BP}t \quad (6)$$

A concise description of the DSG's different functions follows. Refer to Fig. 5 for architectural details.

A. Pattern Generation

The pattern generator, when configured to generate noise, will accept data bytes (from the SGB-CPU through the Multibus-I interface) to be mapped into a random-access memory (RAM). After the RAM has been loaded, it will be sequentially read by a random-address generator whose output will represent the RAM's address to be accessed. This random-address generator will be a pseudonoise (PN) code generator with inherent uniform output distribution and a very long period (longer than 24 hours). The distribution function of the data bytes mapped into the RAM in conjunction with the uniform distribution function of the addresses with which this RAM is read will determine the distribution function of the noise generator output. Usually the distribution function mapped into the RAM will be a Gaussian or normal distribution quantized to B bits from the corresponding analog probability function

$$f(x;u,s) = 1/(s\sqrt{2\pi})e^{-1/2[(x-u)/s]^2} \quad (7)$$

with $u = 0$ for unbiased noise and s = standard deviation.

The discrete probability function will therefore be

$$P_d(x_d;u,s) = 1/2\{\mathrm{erf}[(x_d + 0.5 - u)/(\sqrt{2}s)] - \mathrm{erf}[(x_d - 0.5 - u)/(\sqrt{2}s)]\} \quad (8)$$

for $x_d \in \{-(L-2),\ldots,-1,0,1,2,\ldots,(L-2)\}$,

$$P_d(x_d;u,s) = 1/2\{1 + \mathrm{erf}[(x_d + 0.5 - u)/\sqrt{2}/s]\} \quad (9)$$

for $x_d = -L - 1$, and

$$P_d(x_d;u,s) = 1/2\{1 + \mathrm{erf}[(x_d - 0.5 - u)/\sqrt{2}/s]\} \quad (10)$$

for $x_d = L - 1$, where the subscript d denotes discrete. In addition, for B = number of bits including sign

$$L = 2^{(B-1)} \quad (11)$$

$$s < L/3 \quad (12)$$

From [2],

$$1 + \mathrm{erf}[(x-u)/(s\sqrt{2})] = 1/(s\sqrt{2\pi})\int_{-\infty}^{x} e^{-1/2[(t-u)/s]^2}dt \quad (13)$$

and

$$\mathrm{erf}(-x) = -\mathrm{erf}(x) \quad (14)$$

In the present breadboard design

$$B = 8, \quad L = 128, \quad s < 43, \quad \text{and} \quad u = 0 \quad (15)$$

and the output noise sequence, $N_0(n)$, will be normally distributed with statistical parameters defined by the mapping itself and mainly dependent on the uniformity of the random-address generator and not on its autocorrelation function.

The pattern generator may also be programmed to generate a subcarrier frequency and a data pattern. In both cases, special waveforms or encoded (convolutional, Reed-Solomon, etc.) data sequences may also be mapped into either RAM. The possibility of generating very long random data sequences is also available by reading the data RAM with the random address generator, as in the case of generating random noise. The normal configuration will be the sequential reading of the data mapped into the RAM. The time sequences derived by the sequential reading of both data RAM, $d(n)$, and subcarrier RAM, $Sc(n)$, are multiplied at the system clock rate (T_{sys}) to obtain a BPSK modulation sequence

$$D(n) = d(n)Sc(n) \quad (16)$$

It was considered that a data pattern of 65,536 bits would be the maximum length ever to be required; therefore, the RAMs implemented will be 64K RAMs.

B. Digital Filtering and Attenuation

The main purpose of this digital filter and attenuator circuitry will be to provide a user-defined lowpass filter when generating a baseband spectrum, or a bandpass filter when generating an IF spectrum. Noise and data will be independently filtered by two digital filters. These filters may have, if desired, the same frequency response, in which case the output difference equation [3] will be for the data path:

$$D_f(n) = h(0)D(n) + h(1)D(n-1) + \cdots + h(N-1)D(n-N+1) \quad (17)$$

and for the noise path

$$N_{0f}(n) = h(0)N_{0f}(n) + h(1)N_{0f}(n-1) + \cdots + h(N-1)N_{0f}(n-N+1) \quad (18)$$

with $h(n)$ = finite impulse response (FIR).

A 63-tap FIR filter ($N = 63$) will be implemented. The user may define the filtering process independently for each noise or data path by simply modifying the coefficients $h(n)$. Filter coefficients' definition will be attained by DSP software residing on the workstation or PC (refer to Fig. 4). After independent filtering, the noise and data outputs are properly scaled (attenuated) and added to generate the desired symbol SNR on the output sequence

$$S_T(n) = A_D D_f(n) + A_N N_{0f}(n) \quad (19)$$

with $A_D \leq 1$ for the signal path attenuator factor and $A_N \leq 1$ for the noise path attenuator factor. Note that, due to this independent filtering and individual attenuation, the filtered data spectrum will be known. This precise knowledge provides the basis for optimum subcarrier and data demodulation processes [4] to be performed later on the statistics function. The DSG SNR output, or equivalently the SNR input, to the demodulator under test will, thus, be continuously monitored by this optimum process.

C. Digital-to-Analog Conversion

The DSG will provide a digital output for baseband synchronous testing and, through the digital-to-analog conversion function, an analog output for a more general asynchronous type of testing. Therefore, the input sequence Eq. (19) containing the subcarrier, data, and noise at the system clock rate is converted to the analog representation in Eqs. (4), (5), or (6) by a digital-to-analog converter (DAC). This DAC is the element dictating the number of bits to be used in the DSG design. Bandwidth requirements limited to 12 the number of bits to be used at the time of design definition and will be the quantization used in the prototype demonstration. The DAC analog output spectrum will be rich in harmonics that have to be attenuated by an output analog filter. The amplitude, and more important, the phase characteristics of this filter have to be very well controlled in the design in order to conserve the input spectrum characteristics. The effect on SNR of several Butterworth filters with numbers of poles ranging from three to nine were simulated with the conclusion that in the worst case, to obtain less than 0.1-dB output SNR degradations, a three-pole Butterworth filter should be used.

D. Statistics Monitor

The DSG will be used to calibrate SNR measurements and losses on other signal processes; therefore, several statistical measurements have been implemented through the statistics' monitor function. The same statistical measurements will be implemented in the digital output, as well as in the analog output. Note that the digital output time sequence Eq. (19) is directly brought to the statistics board where an optimum subcarrier and data demodulation is performed by digital multiplication of this time series by an exact replica of the data spectrum embedded in that output

$$S(n) = S_T(n)A_D D_f(n) \quad (20)$$

where the delay of the digital hardware has been arbitrarily set to zero due to its precise knowledge.

The result of that multiplication is accumulated in the symbol integrator and dump for exactly a symbol period (T_S), related to the system clock period (T_{sys}) by the relationship

$$T_S = I_S T_{sys} \quad (21)$$

where I_S is an integer.

Therefore the ith symbol integrated value will be

$$S_i = \sum_{n=(i-1)I_S+1}^{iI_S} S(n)$$

$$= \sum_{n=(i-1)I_S+1}^{iI_S} [A_D{}^2 D_f{}^2(n) + A_D A_N N_{0f}(n) D_f(n)] \tag{22}$$

Note that all statistics are performed in this integrated symbol output, S_i. Thus, the mean value of the detected symbols will be calculated on the SGB-CPU from results of the symbol value accumulator obtained for a fixed number of symbol periods (K) completing approximately one second of elapsed time

$$\overline{S} = 1/K \sum_{i=1}^{K} S_i \tag{23}$$

Simultaneously, the squared value of the detected symbol is also accumulated in the symbol squared accumulator for the same number (K) of symbols

$$\overline{S}^2 = 1/K \sum_{i=1}^{K} S_i{}^2 \tag{24}$$

From these two values the symbol SNR evaluation immediately follows (in decibels)

$$SNR_M = 10 \log_{10} \left\{ \overline{S} / \left[2\left(\overline{S^2} - \overline{S}^2 \right) \right] \right\} \tag{25}$$

The last measurement made in this output is the symbol error count in the symbol error accumulator. This measurement is arrived at by just counting the output negative events in the same period of time ($KT_{sys}I_S$).

$$SER = 1/K \sum_{i}^{K+i} \text{neg}[S_i] \tag{26}$$

with

$$\text{neg}[S_i] = 1 \text{ if } S_i < 0$$
$$\text{neg}[S_i] = 0 \text{ if } S_i > 0 \tag{27}$$

In order to characterize the hardware performance, a histogram accumulator will be implemented, thereby providing a straightforward method to confirm the actual probability density function of the filtered or unfiltered noise from Eq. (18). Statistics on data and subcarrier waveforms can be performed and will be used as a hardware-software performance verification self test.

To calibrate the analog output SNR, the first function to be performed is the digital conversion of the analog output. In the case of baseband or IF testing, the analog-to-digital conversion is performed directly on the DSG analog output through a 12-bit analog-to-digital convertor. In the case of higher frequency spectra, a downconversion will precede the analog-to-digital conversion, as shown previously in Fig. 2. In both cases, the delay introduced by the analog circuitry, T, has to be accounted for. This delay (T) will not necessarily be an integer number of system clock cycles (k), but rather will have also a fractional part (τ)

$$T = kT_{sys} + \tau$$

Therefore, after removing the integral part of system clock cycles, kT_{sys}, Eq. (22) will now be

$$S_i = \sum_{n=(i-1)I_S+1}^{iI_S} S(n)$$

$$= \sum_{n=(i-1)I_S+1}^{iI_S} [A_D{}^2 D_f(n) D_f(n+\tau)$$

$$+ A_D A_N N_{0f}(n) D_f(n+\tau)] \tag{28}$$

To account for this unknown fractional delay, τ, a delay line of 2-nsec steps will be implemented. SNR degradation due to these quantization steps will be (in decibels)

$$\Delta SNR = 20 \log_{10}(1 - 2\tau/T_S) \tag{29}$$

with τ = delay quantization and T_S = symbol period. In any case, this degradation will be calibrated through the autocorrelation function Eq. (28) obtained with 2-nsec quantized steps.

III. Error Analysis

Whenever practical, the error contributions to the SNR generation were evaluated by analysis or computer simulation (A). If impractical, an engineering judgment approach (EJ) was taken. The expected errors on the setability and the actual measurement of the DSG output SNR are summarized in Tables 1 and 2. The total error contribution will be verified when the design is completed. Individual errors will also be measured whenever possible.

The errors to be encountered when a given SNR is desired in the analog output, assuming a memoryless DSG,

have been summarized in Table 1. Note that subsequent SNR settings may be known with the accuracy deduced in Table 2 when the operator takes advantage of the accuracy provided by the SNR monitor (the operator has now provided memory to the process).

The digital output monitoring error will be mainly produced by the deviation from a perfect uniform distribution of the PN generator addressing the Gaussian noise RAM and the quantization noise of the digital process. Both have been quantified in Table 1 for one-second integration times with an evaluated error of 0.01 dB for the nonuniformity of the random-address generator. This error will diminish as the integration time is increased, with a limit imposed by the quantization noise (0.002 dB). Therefore, the accuracy of the digital SNR measurement will only be dependent on the integration time used to obtain that measurement, or equivalently on the number of samples used in the computation with a lower limit imposed by the quantization noise of the digital process—in the present case 0.002 dB. Confidence intervals can be found if the cumulative distribution function of the SNR measurement is known. It has been shown [5] that the distribution function of the SNR measurement, Eq. (25), is a noncentral F-distribution. The cumulative distribution of this function may be approximated by the standard normal distribution function as follows:

$$F(SNR_M) = P(x) = 1/\sqrt{2\pi} \int_{-\infty}^{x} e^{-1/2t^2}\, dt \qquad (30)$$

with

$$x = (n_1 - n_2)/(d_1 + d_2)^{1/2} \qquad (31)$$

$$n_1 = [(N-1)SNR_M/(1 + N\ SNR_T)]^{1/3} \times \{1 - 2/[9(N-1)]\} \qquad (32)$$

$$n_2 = 1 - \left\{(2 + 4N\ SNR_T)/[9(1 + N\ SNR_T)^2]\right\} \qquad (33)$$

$$d_1 = (2 + 4N\ SNR_T)/[9(1 + N\ SNR_T)^2] \qquad (34)$$

$$d_2 = 2/[9(N-1)][(N-1)SNR_M/(1+N\ SNR_T)]^{2/3} \qquad (35)$$

and

N = the number of samples in the measurement

SNR_T = the true SNR

SNR_M = the measured SNR

Figure 6 is a plot of Eq. (30). It gives the cumulative probability distribution of measuring the SNR (SNR_M) within 0.1 dB of the true SNR (SNR_T) as a function of the number of samples used in the measurement. SNR_T has been used as the parameter.

Table 2 summarizes the error budget for the SNR measurement on the analog output.

IV. Capabilities

Table 3 summarizes the capabilities of the present breadboard design. When the DSG is configured to generate a baseband spectrum, it will be able to provide two data channels with or without subcarrier, or two biphase data channels in a total baseband bandwidth of 10 MHz (dc to 10 MHz). If the DSG is configured to generate a bandpass spectrum it will be able to provide a residual carrier up to 5 MHz with one data channel with or without subcarrier, or one QPSK or one offset QPSK (OQPSK) data channel, or two data channels (carrier suppressed) in a total bandpass bandwidth of ±5 MHz.

The frequency generation on the DSG is related to the system clock rate (f_{sys}) in use. The subcarrier frequency (f_{Sc}) or intermediate frequency (IF) will be generated with a variable frequency resolution ranging from $f_{sys}/2^{17}$ for the highest frequencies (5 MHz) to $f_{sys}/2^{32}$ for the lowest (100 Hz). The data period (T_S) will be related to the system clock period (T_{sys}) by

$$T_{sys} = T_S/I_S \qquad (36)$$

with

$$2^1 \leq I_S \leq 2^{24} \qquad (37)$$

and

T_{sys} = system clock period = $1/f_{sys}$

T_S = symbol period

$2\ \text{MHz} < (1/T_{sys} = f_{sys}) < 20\ \text{MHz}$

An external DSG mode is provided. In this mode, the data waveform (or the subcarrier biphase modulated by the data) is externally generated and sampled at the system clock rate f_{sys}. In general, the frequencies involved will not be coherently related. Note that the mean frequency derived from this, in general, asynchronous sampling process will still correspond to the data rate (or subcarrier and data) required. Because of knowledge of the asynchronous sampled data spectrum, the DSG SNR-monitoring process will provide an optimum demodulation independent of the sampling process. This will not generally be the case of the demodulation process under test when the symbol clock is synchronous with the incoming symbol or with the mean symbol rate. In this case, the synchronous detection will expect symbols with exactly the same period and not the jittery ones being provided. The worst-case degradation of such a process will be quantified as follows.

Assume that a periodic signal (f_{Sc}) is sampled at a fixed sampling rate (f_{sys}). The resulting frequency spectrum is composed of spectral lines (f_H) related to the sampling frequency by

$$f_H = \mid nf_{Sc} - mf_{sys} \mid \tag{38}$$

with $\underline{n}$ and $\underline{m}$ integers.

Assuming, for simplicity, that the sampled periodic signal (f_{Sc}) is a square wave, the useful spectral lines in a subsequent symbol synchronous demodulation process will only be those corresponding to the odd harmonics of the corresponding Fourier series with corresponding total power

$$P_{Sq} = \sum_{i}^{\infty} [2A/(i\pi)]^2 \tag{39}$$

for ($i = 1, 3, 5, \ldots$). The remaining alias harmonics given by Eq. (38) may, in the most general sense, be treated as unwanted noise in the subsequent symbol synchronous demodulation process. Given a Nyquist bandwidth, if the useful square-wave signal power is

$$P_{SqN} = \sum_{i}^{N} [2A/(i\pi)]^2 \tag{40}$$

for ($i = 1, 3, 5, \ldots, N$) with

$$Nf_{Sc} \leq 1/2f_{sys} \tag{41}$$

and the total available power is P_T, then the available SNR on the square wave (or subcarrier SNR) is defined as

$$SNR_{SqN} = 10 \log_{10}[P_{SqN}/(P_T - P_{SqN})] \tag{42}$$

The above process was computer simulated for 20 equally spaced subcarrier frequencies (0.0977 MHz to 4.7363 MHz) and a system clock of $f_{sys} = 20$ MHz. Results are shown in Fig. 7. Note that discontinuities will exist due to the changing number of odd harmonics in the ideal rectangular Nyquist filter.

Other discontinuities will exist at subcarrier frequencies (f_{Sc}) corresponding to an exact even submultiple (2, 4, 6,...) of the system clock rate (f_{sys}). In this case, the sampling process becomes synchronous and the available SNR becomes infinity (∞) at those particular frequencies. This synchronous mode will have to be used for calibrations of data rates higher than 2 MS/sec (1-MHz square wave). All the required operations in the external mode will be transparent to the DSG operator and will be automatically software-controlled.

V. Conclusions

A digital synthesis method to generate bandlimited test signals with precise signal-to-noise ratios has been described and the expected errors have been quantified. Design of appropriate hardware and software to demonstrate the performance of this method has been initiated. The DSG is expected to replace the presently used Y-factor method with improvements on testing time, accuracy, stability, and repeatability.

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Table 1. Setability error budget (worst case)

Error	dB	Source
RAM (64K, 8-bit) resolution	0.04	A
PN generator uniformity	0.01	EJ
Quantization noise	0.002	A
DAC nonlinearities	0.01	A
DAC frequency response	0.01	A
System clock phase jitter	0.02	EJ
Analog filter	0.1	A
Amplifiers	0.01	EJ
Total error on SNR setting (root sum square, rss)	0.11	

Note: Evaluated by: (A) analysis or computer simulation
(EJ) engineering judgment

Table 2. Analog output monitoring error budget

Error	dB	Source
Quantization noise	0.002	A
System clock phase jitter	0.02	EJ
ADC quantization noise	0.002	A
ADC nonlinearities	0.01	A
Waveform distortion	0.01	A
Total error on SNR monitor (rss)	0.02	

Note: Evaluated by: (A) analysis or computer simulation
(EJ) engineering judgment

Table 3. Summary of DSG capabilities

Function	Capability
System clock	2 to 20 MHz
Analog power output	7 dBm (50 ohms)
Noise density distribution	Gaussian
Noise bandwidth	0.1 to 10 MHz
Noise autocorrelation period	> 24 hr
Baseband external input	TSA compatible
Symbol SNR	
Setability	0.1 dB
Accuracy and stability	±0.05 dB
Range	−6 to 20 dB
Data types	Nonreturn to zero; biphase; QPSK; OQPSK
Data rates	4 S/sec to 6.6 MS/sec
Modulation types	Phase-shift keyed
Data pattern	2048 and 16,384 PN code
Data transition density	10; 30; 50; 70; and 100%
Frame synchronization word	Up to 64 bits
Frame length	Up to 65,536 bits
Subcarrier or IF frequencies	100 Hz to 5 MHz

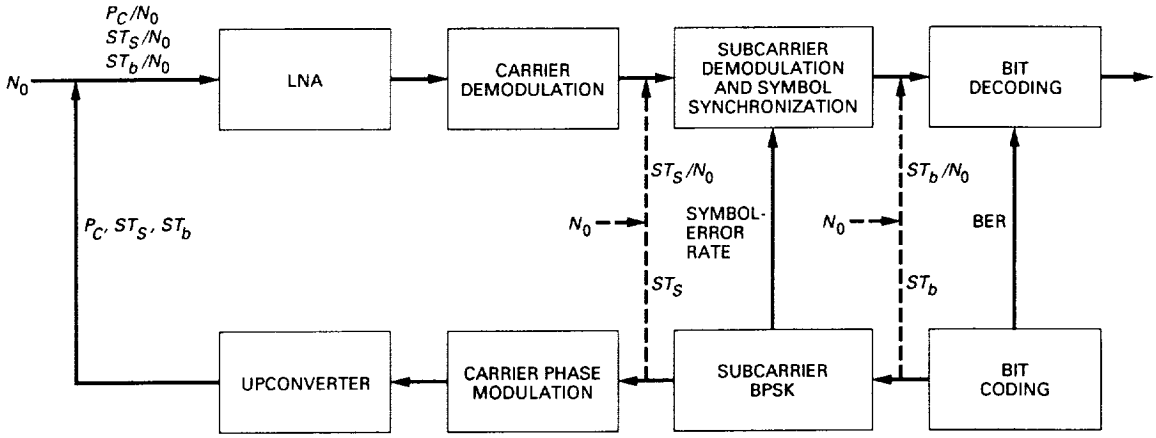

Fig. 1. The SPC portion of a typical DSN communications link.

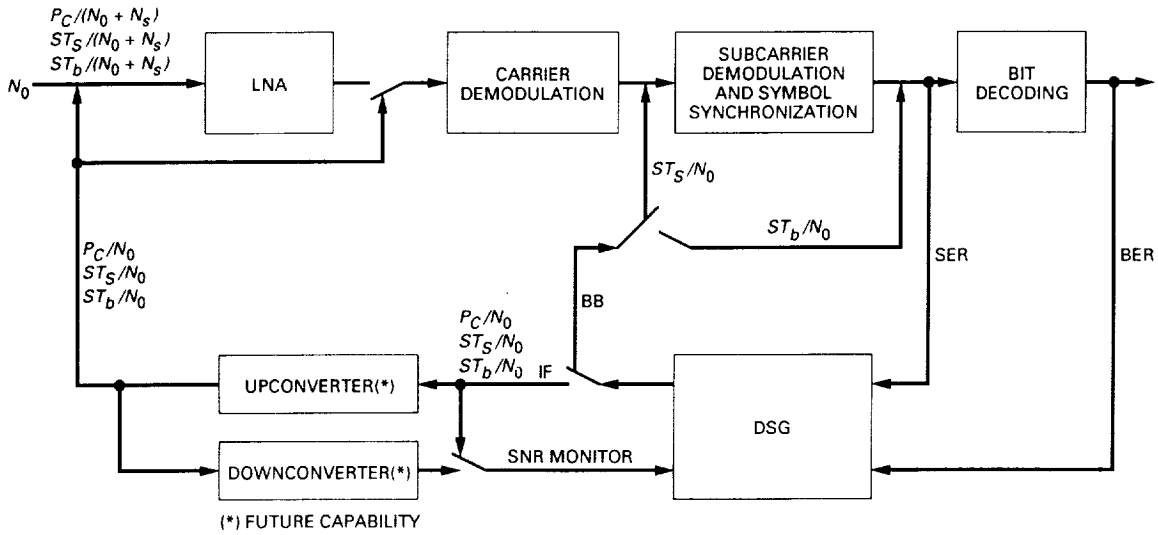

Fig. 2. Calibration of SPC system degradation and losses.

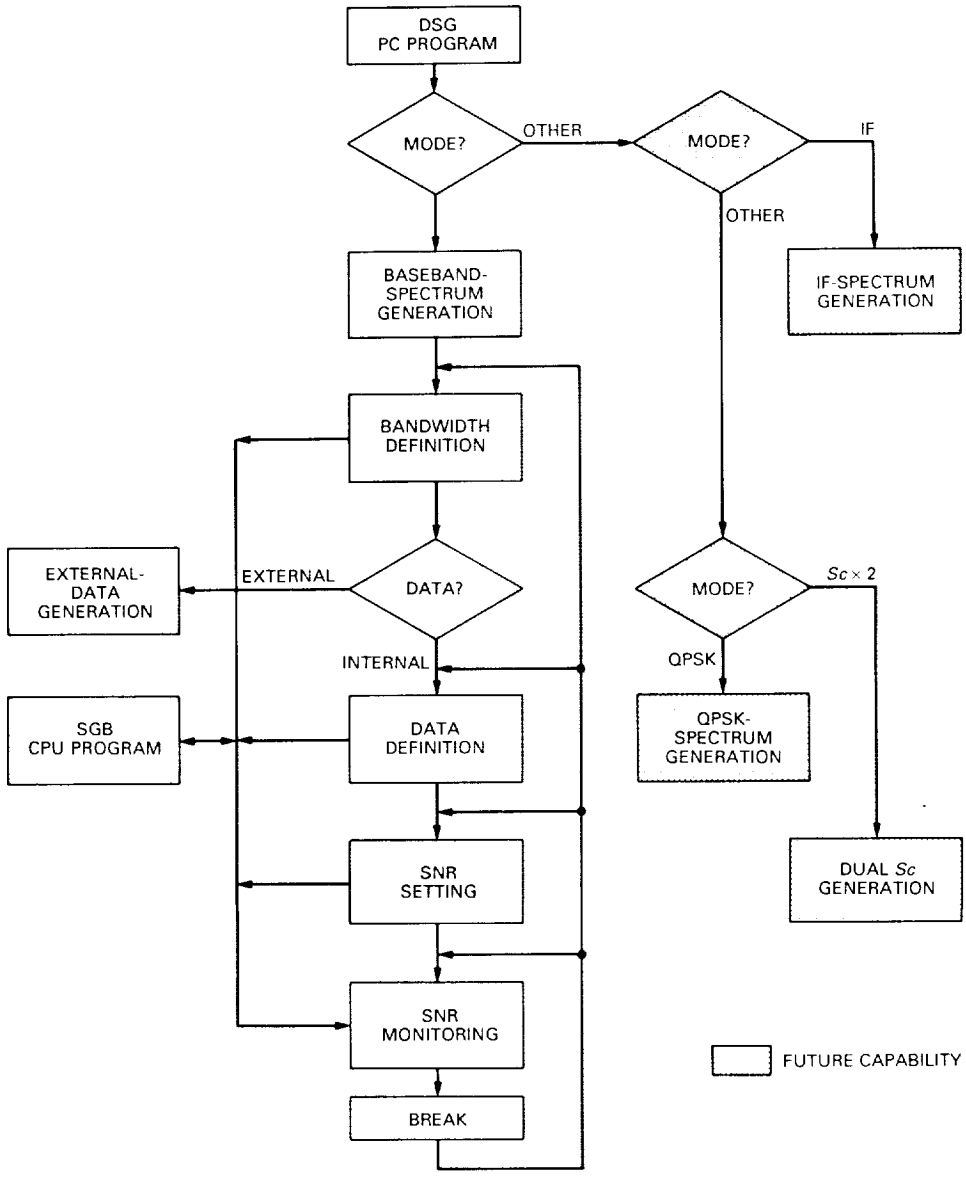

Fig. 3. Programmable capabilities of the DSG.

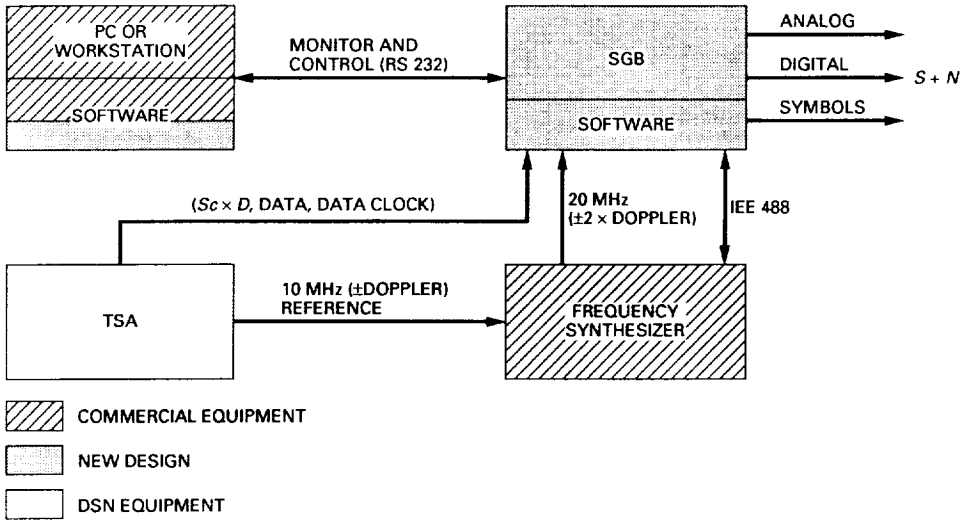

Fig. 4. The DSG external interfaces in the SPC environment.

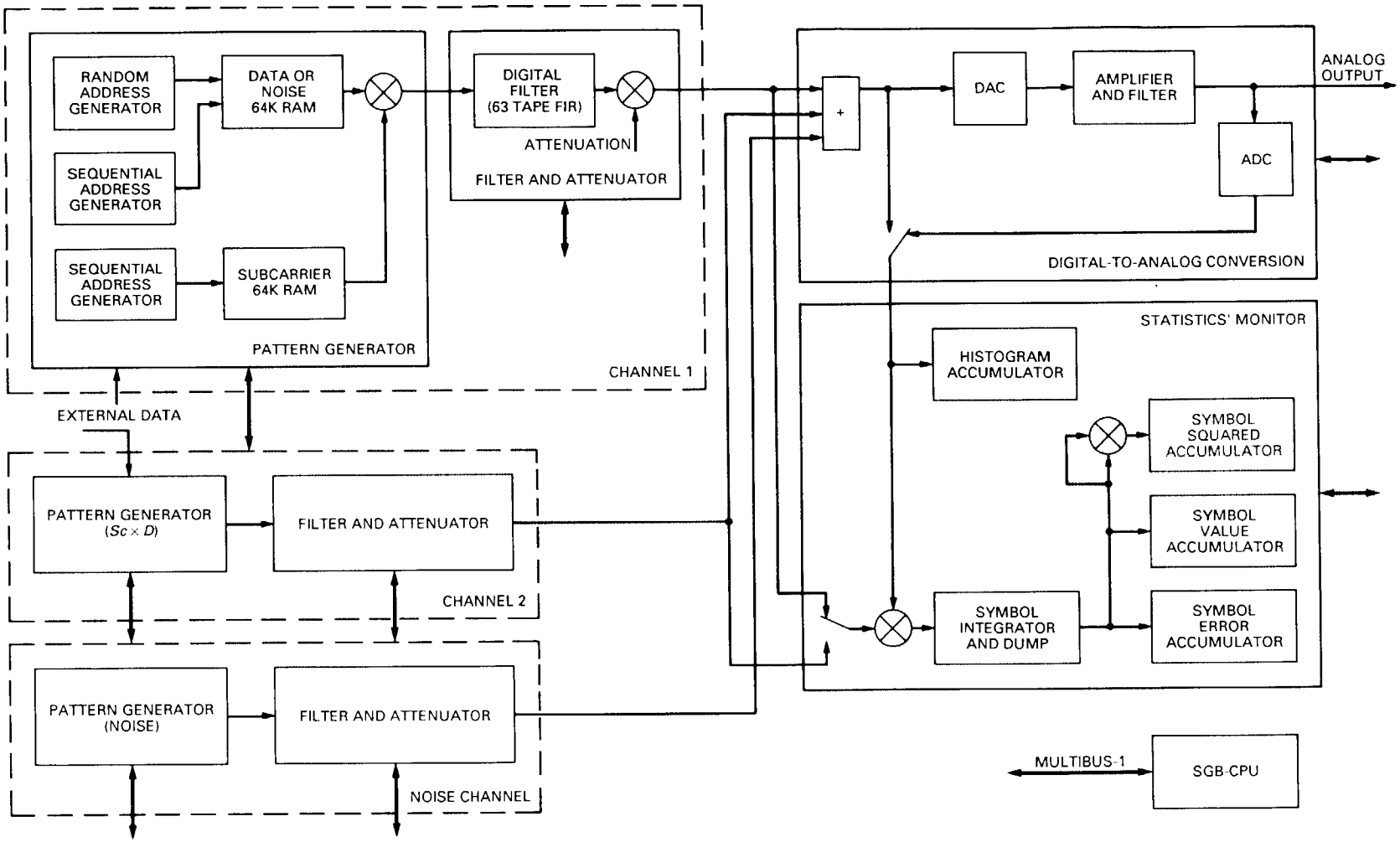

Fig. 5. SNR generator box.

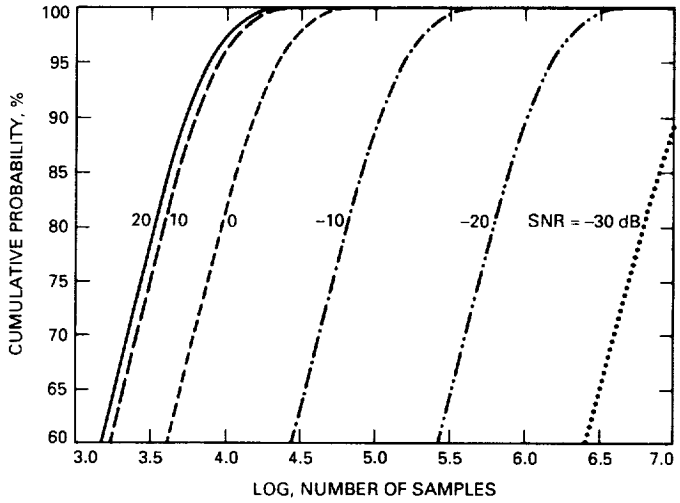

Fig. 6. Cumulative probability (of measured SNR being within 0.1 dB of true SNR) versus total number of samples.

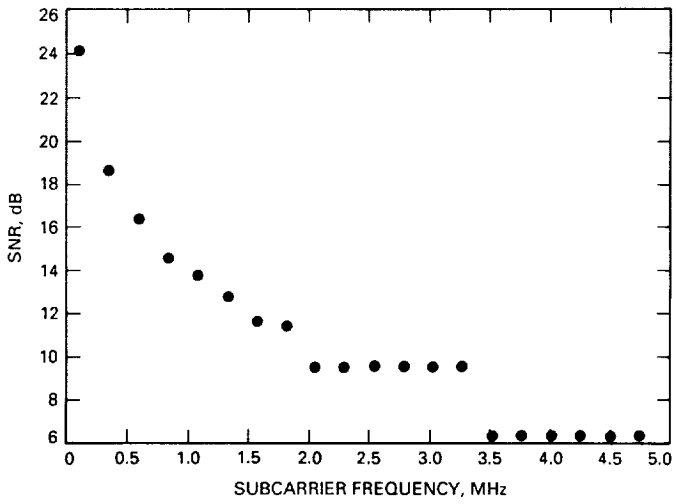

Fig. 7. Upper limit of subcarrier SNR (due to asynchronous sampling) versus subcarrier frequency.

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