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Progress Toward the Development of Dual Junction GaAs/Ge Solar Cells

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Introduction

Space photovoltaic cell technology has seen substantial improvements to cell efficiency, size, and weight and cost reduction since the first cells were flown in the early '60s.

Improvements to material and process technology together with a better understanding of device physics has resulted in planar space silicon solar cell efficiencies of up to approximately 15% AM0 in sizes up to 8 cm × 8 cm. Although terrestrial solar cell designs have shown substantially higher conversion efficiencies at beginning of life (BOL) [ref. 1,2] the susceptibility of these designs to radiation damage has made them unsuitable for space use at this time. It is generally accepted therefore that current silicon efficiencies of 15% represent the plateau in space silicon cell technology until more advanced qualified designs evolve.

In contrast, GaAs and related III-V material based solar cells are in their infancy of development and offer substantial increases in efficiency and radiation hardness compared to silicon. Single junction GaAs cell efficiencies of 18.5% have already been demonstrated in production [ref. 3] and efficiencies up to 32% have been reported on prototype two junction cells [refs. 4-6].

A significant impediment to the widespread use of GaAs cells is the cost and fragility of the wafer. Although 5 mil GaAs cells up to 2 cm × 4 cm have been demonstrated [ref. 3], the manufacture of larger area, thinner GaAs/GaAs cells is virtually impossible given their poor mechanical strength. Both Si and Ge have been considered as alternative substrates on which to grow GaAs layers. The problems associated with the GaAs/Si system, while not unsolvable, are formidable, and large area solar cells based on this system are somewhat distant in the future. Ge on the other hand is well suited for GaAs epitaxy both in terms of thermal expansion coefficient and lattice match and Spectrolab has been actively developing this cell for several years. Furthermore, with appropriately focussed development on 4 inch diameter Ge wafer growth and high volume MOCVD reactor systems it will become possible to manufacture cells up to 8 cm x 8 cm in size with thicknesses down to 3 mils thus providing the aerospace industry with a "plug in" high power replacement technology for many silicon solar arrays.

Cell Construction

The cross-section of the GaAs cell is shown in Figure 1. It consists of an N^+ GaAs buffer (2.0 microns),N-GaAs base (3.0 microns), P-GaAs emitter (0.4-0.5 microns) and a P-$Al_{0.87}Ga_{0.13}As$ window (0.05-0.1 microns). An P^+ GaAs cap separates the front contact from the window allowing very low contact resistance to be achieved while at the same time preventing the diffusion of metal into the sensitive junction region during interconnect attachment. Contact to the cap is made using a stable Ti/Pd/Ag metallization, proven to be stable at 300°C for 500 hours. Further addition of diffusion barriers to the metallization system also shows promise of increasing thermal stability to 550°C or more. The thin window also allows high efficiency, both by minimizing the absorption of short wavelengths and by improving the optical performance of the antireflection (AR) coating. This is important at short wavelengths where optical interference effects in the window are high.

Modeling of GaAs/Ge Cell Performance

Spectrolab has developed computer codes to predict the performance of GaAs/Ge cells. These models determine the cell characteristics as a function of optical coupling into the cell and material parameters for each layer such as thickness of each region, minority carrier diffusion length, diffusion coefficient, doping concentration and recombination velocity.

Our model assumes that the top GaAs cell is electrically joined to a bottom Ge cell by an N^+ GaAs/P^+ Ge tunnel junction. This junction may be formed by the diffusion of Ga into the Ge and out-diffusion of Ge into the GaAs during growth. A full description of this cell and the model is given elsewhere [refs. 7,8].

Our analysis performed to date shows that in order to achieve high efficiencies in the dual junction configuration it is important that certain boundary conditions are met. These are:

1. A low recombination velocity at the Ge back surface.
2. A low recombination velocity at the Ge emitter surface.
3. A thin Ge emitter.
4. Good optical coupling of infra red wavelengths into the Ge cell.

5. Long diffusion length in the Ge bulk.

6. A highly reflecting back contact to the Ge cell.

Each of these boundary conditions results from the need to maximize the current generation in the Ge cell since current matching between the GaAs and Ge cells is required in order to achieve monolithic (i.e. two terminal) device performance. The problem is further exacerbated by the weakly absorbing nature of Ge beyond 1.4 microns wavelength and the thinness of the substrate (typically 4 mils).

Effect of Ge Wafer Diffusion Length on Cell Performance

The importance of material quality on Ge cell performance is shown in Figure 2 where we have plotted the internal Q.E. as a function of Ge base diffusion length. The calculated short circuit current generation in both the GaAs and Ge cells is also shown in the figure. Current generation in the GaAs cell at wavelengths below 0.35 microns is assumed to be negligible since the cell will ultimately be covered by a filter which is either absorbing below 0.35 microns wavelength (e.g. cerium oxide doped borosilicate glass) or is coated with a UV rejecting filter. Other parameters used in the calculation are shown in Table 1. The value for Ge emitter diffusion length was obtained from data on experimental discrete Ge cells recently made at Spectrolab. A base diffusion length of 80 microns was also measured on these cells. The GaAs cell parameters are those known to give good agreement between experiment and theory for high efficiency MOCVD and LPE homojunction cells. The window and emitter thickness of 0.05 and 0.5 microns respectively are chosen to give the highest efficiency and best radiation hardness and are well established. The thin window thickness of 500 Å also forms a fourth component of the multilayer a.r. coating described later.

In Table 2 we also show the computed effect of Ge base diffusion length on cell efficiency. Other parameters used were again those shown in Table 1. Provided good quality GaAs layers may be grown on the Ge substrate, the model conservatively predicts an AM0 conversion efficiency of 20.29% for the GaAs cell with a short circuit current density of 32.57 mA cm^{-2}. In order to achieve equal current generation in the Ge cell, good quality base material is obviously required. For a base diffusion length of 100 microns the Ge short circuit current density is 31.57 mA cm^{-2} indicating that current matching is indeed possible. The Ge cell efficiency is then 4.12% giving a total GaAs/Ge cell efficiency of approximately 24.3%.

Back Surface Reflector/Back Surface Field

The use of a BSR and BSF is also important in maximizing current generation in the Ge cell. In Figure 3 we show the computed reflectance, (based on literature values of the optical constants) from the interface between various metals and Ge. It is clear that the reflectance for the Ge/Ti interface is only 17% whereas it is greater than 95% for Al or Au making the use of the latter desirable as a back contacting material. In Figure 4 we also show the corresponding effect of these various back contacting metals on the Ge cell internal Q.E. We note a substantial improvement in QE at long wavelengths due to the use of Al or Au as a BSR. The effect of a BSF in the Ge cell is also shown. If an 80 micron Ge base diffusion length is assumed and other parameters shown in Table 1 are used we calculate a Ge short circuit current density of 31.04 mA cm^{-2} for an Al BSR/BSF contact, 30.36 mA cm^{-2} for a Ti/BSF contact and 29.35 mA cm^{-2} for the case of a Ti contact with no BSF. The use of an Al (or Au) BSR *and* BSF is therefore clearly desirable.

Experimental Performance Data

GaAs/Ge dual junction cells, 2 cm × 2 cm in size have been fabricated on 8 mil thick polished Ge substrates. No attempt was made to improve the boundary conditions such as incorporating a BSF or BSR, optimizing the Ge emitter or enhancing the red performance of the AR coating. Measurements were made under an XT10 solar simulator at 28°C. An average efficiency of 18.7% was measured. A full description of the cells is given elsewhere [ref. 9].

In order to evaluate the performance of the GaAs and Ge cell components we measured the temperature coefficient of efficiency of several cells. Typical data on a 19.1% (28°C) cell is shown in Figures 5 and 6. Our computer model predicts that the Ge cell efficiency falls to zero at approximately 120°C due to the extremely high first diode saturation current. Hence extrapolation of the high temperature portion of the curve predicts a 28°C GaAs AM0 cell efficiency of 16.6% and a Ge AM0 cell efficiency of 2.5%. Improvements to GaAs cell efficiency will be made by improvements to GaAs MOCVD growth quality while the Ge cell may be improved by the use of a BSF/BSR and by better IR optical coupling as mentioned earlier.

In Figure 6 we also show the temperature coefficient of open circuit voltage of the same cell. At lower temperatures the temperature coefficient is equal to -3.94 mV/°C due to the series connection of both GaAs and Ge cells. At higher temperatures the coefficient of -2.33 mV/°C approaches that of GaAs for reasons previously mentioned. Both temperature coefficients of voltage and power are in broad agreement with our model.

Improved A.R. Coating Design

Most GaAs/Ge cells reported to date have utilized a dual antireflection coating of TiO_2/Al_2O_3 optimized for GaAs homojunction cells. In Figure 7 we show the measured reflectance from such a cell. A passive thermal absorptance of 0.88 was measured. This is high compared to GaAs alone due to the absorbing nature of the Ge substrate out to 1.85 microns. It is also evident that the DAR coating does not provide a good bandpass filter at long wavelengths for high Ge cell performance in a dual junction configuration.

In contrast we also show in Figure 7 the effect of a third layer of MgF_2 in the optical stack to form a triple layer AR (TAR) coating. There is a significant reduction in red reflectance beyond 0.87 microns wavelength, thus allowing more light to reach the Ge cell.

In order to evaluate the efficacy of this third coating on cell performance under "true" AM0 illumination, two GaAs/Ge cells were flown on the NASA LeRC Lear jet. This technique has proven to be extremely valuable in providing rapid access to "true" AM0 measurements and has shown good correlation with high altitude balloon and shuttle flight data.

In Figures 8 and 9 we show data on a DAR and TAR coated cell as measured on the Lear jet flight at approximately AM0.22. Since it was the purpose to make relative measurements between AR coatings rather than obtain absolute data, no corrections for ozone, Earth-Sun distance or air mass were made. The kink seen on the DAR coated cell is caused by current starvation in the Ge cell causing it to become reverse biased as the GaAs/Ge cell approaches short circuit conditions. Similar effects have been observed by others [ref. 7]. In contrast the cell with the TAR has a substantially improved fill factor due to increased Ge cell current generation although further improvements to achieve current matching are obviously needed.

We have continued to identify superior a.r. coatings to ensure that the increase in Ge cell performance still persists after glassing, since MgF_2 becomes ineffective when an adhesive of refractive index n=1.43 is applied.

In Figure 10 we show the computed normal reflectance from the filtered optical stack comprising the 0.05 μm AlGaAs window plus an additional proprietary three layer a.r. coating. An adhesive of n=1.43 was assumed to cover the cell. The tolerance on the thicknesses of the individual layers of this stack is high making it a viable production coating. In addition all of the materials are space qualified. This a.r. coating will shortly be used on experimental GaAs/Ge cells and should minimize reflection losses from GaAs in the IR region.

Conclusions

Large area GaAs/Ge cells offer substantial promise for increasing the power output from existing silicon solar array designs and for providing an enabling technology for missions hitherto impossible using silicon. Single junction GaAs/Ge cells offer substantial advantages in both size, weight, and cost compared to GaAs cells but the efficiency is limited to approximately 19.5%-20% AM0. The thermal absorptance of GaAs/Ge cells is also worse than GaAs/GaAs cells (0.88 vs 0.81 typ.) due to the absorption in the Ge substrate.

On the other hand dual junction GaAs/Ge cells offer efficiencies up to ultimately 24% AM0 in sizes up to 8 cm × 8 cm but there are still technological issues remaining to achieve current matching in the GaAs and Ge cells. This can be achieved through tuned AR coatings, improved quality of the GaAs growth, improved quality Ge wafers and the use of a BSF/BSR in the Ge cell.

Although the temperature coefficients of efficiency and voltage are higher for dual junction GaAs/Ge cells it has been shown elsewhere [ref. 9] that for typical 28°C cell efficiencies of 22% (dual junction) vs 18.5% (single junction) there is a positive power trade-off up to temperatures as high as 120°C. Due to the potential ease of fabrication of GaAs/Ge dual junction cells there is likely to be only a small cost differential compared to single junction cells.

Acknowledgements

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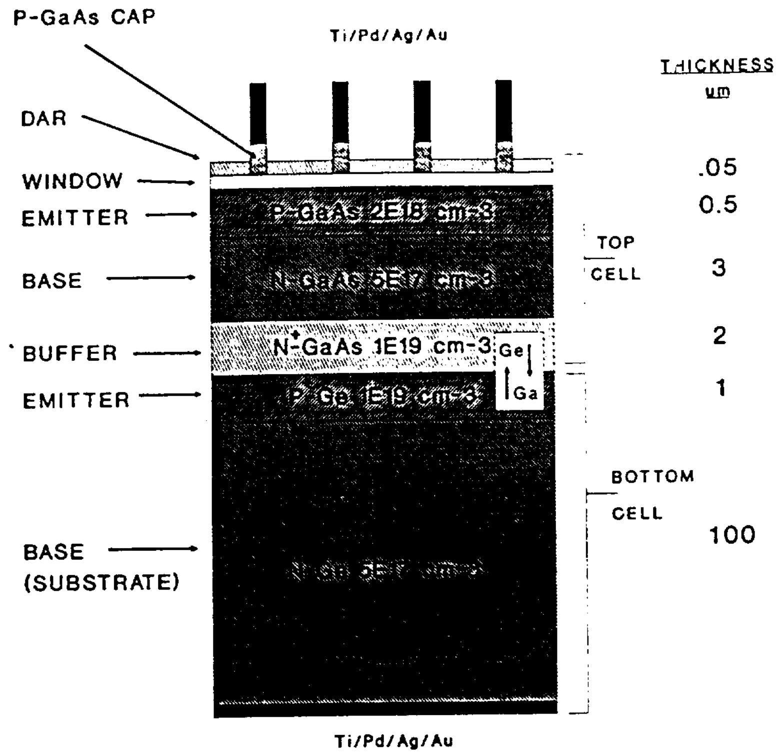

Figure 1 CROSS SECTION OF GaAs/Ge CELL

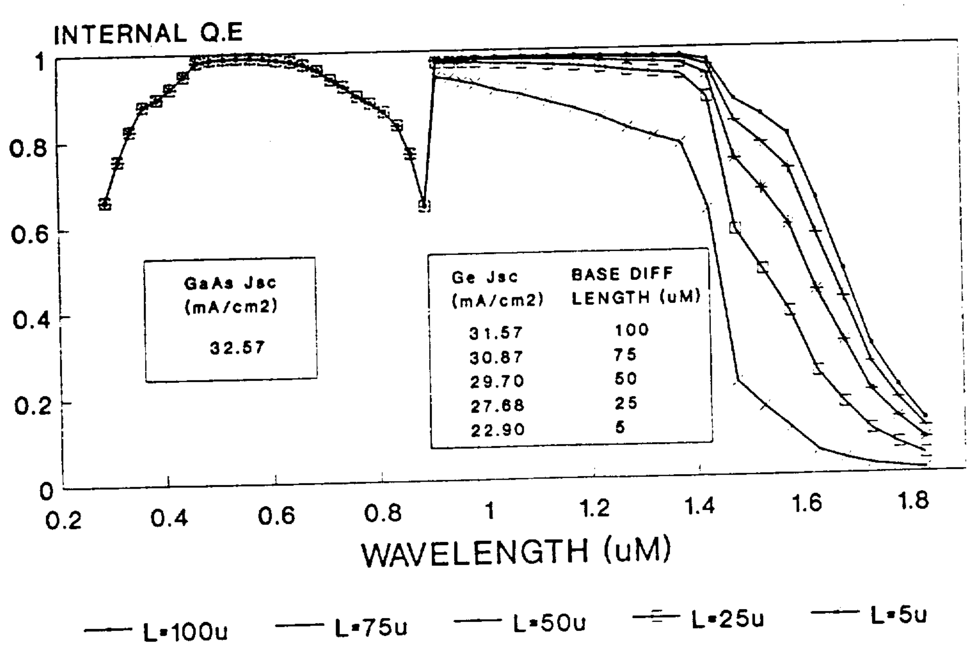

Figure 2 EFFECT OF Ge BASE DIFFUSION LENGTH ON INTERNAL Q.E.

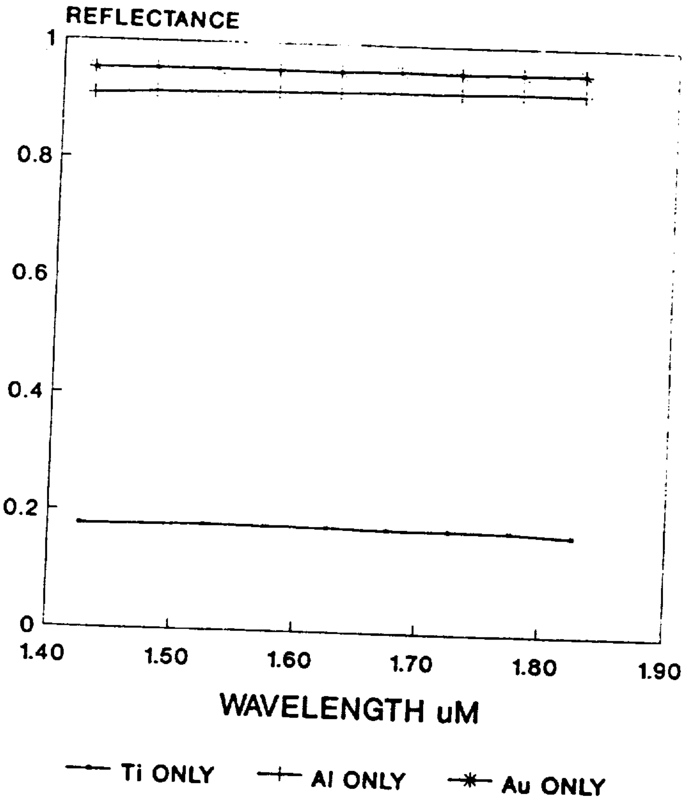

Figure 3 COMPUTED REFLECTANCE FROM THE INTERFACE BETWEEN Ge AND Ti, Al AND Au

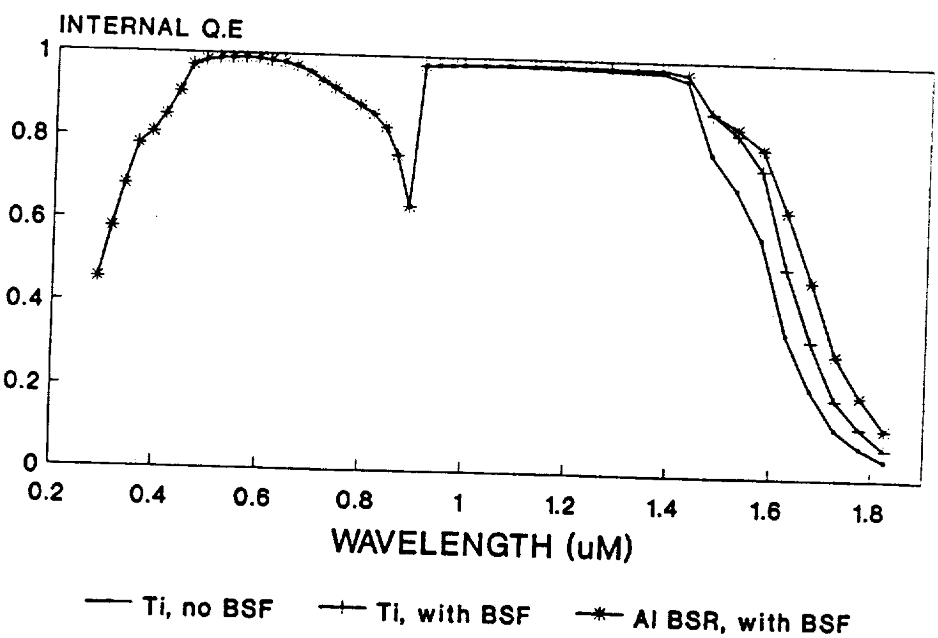

Figure 4 EFFECT OF VARIOUS BACK METALLIZATIONS AND BACK SURFACE FIELD ON INTERNAL Q.E.

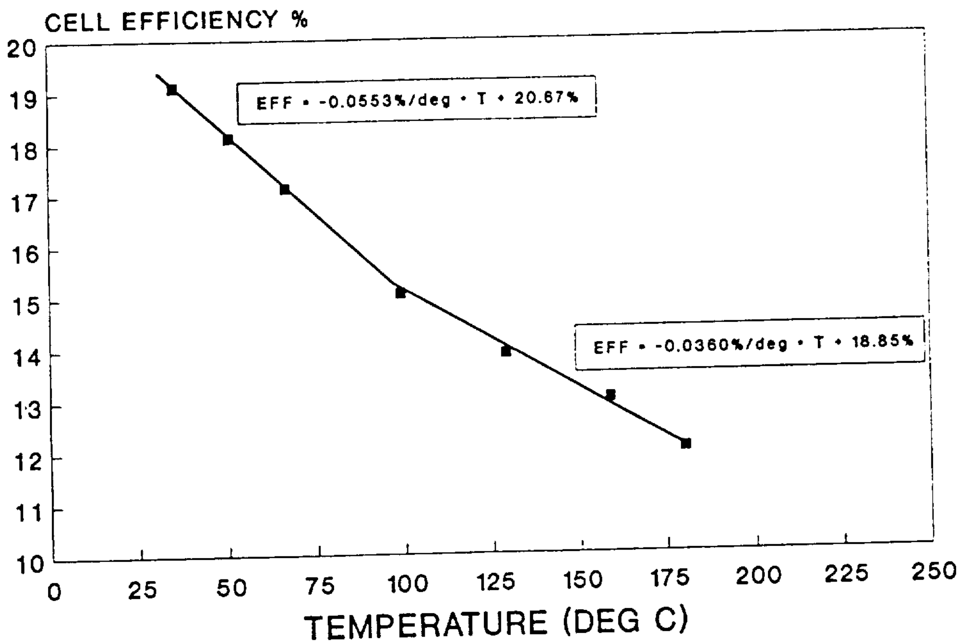

Figure 5 EXPERIMENTALLY MEASURED TEMPERATURE COEFFICIENT OF EFFICIENCY OF DUAL JUNCTION GaA/Ge CELL

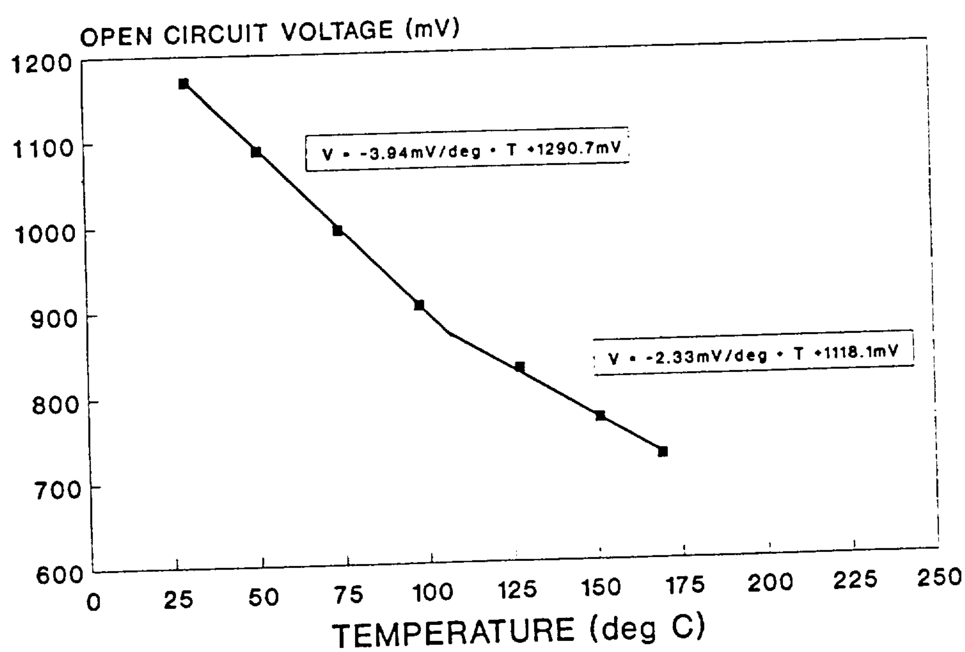

Figure 6 EXPERIMENTALLY MEASURED TEMPERATURE COEFFICIENT OF OPEN CIRCUIT VOLTAGE OF DUAL JUNCTION GaAs/Ge CELL

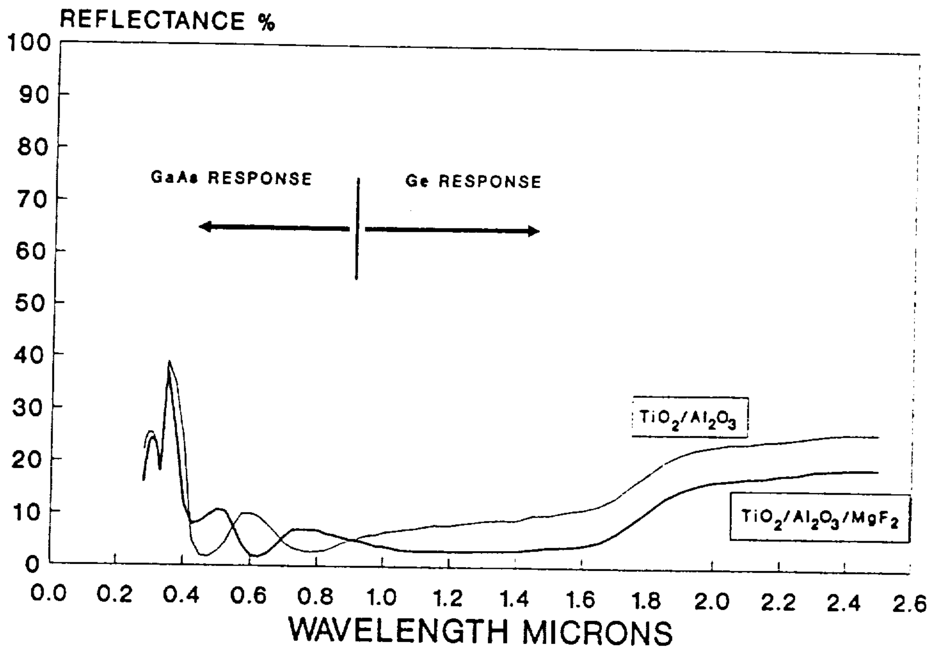

Figure 7 EXPERIMENTLALY MEASURED REFLECTANCE FROM DUAL JUNCTION CELLS WITH TiO_2/Al_2O_3 AND $TiO_2/Al_2O_3/MgF_2$ A.R. COATING

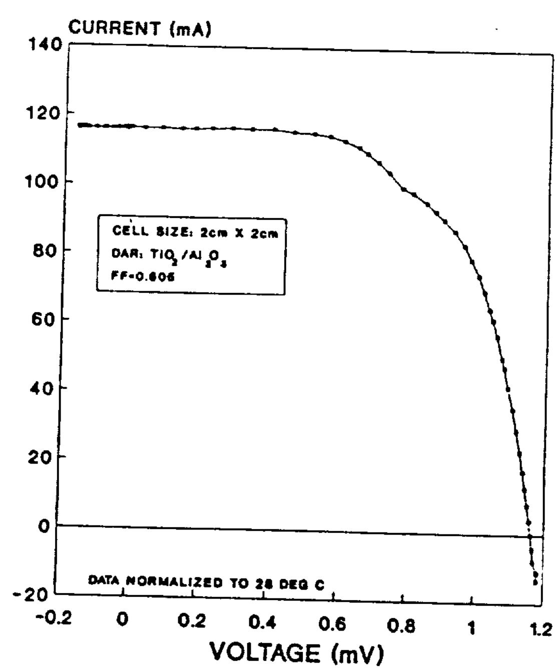

Figure 8 MEASURED AM0.22 I-V CURVE OF GaAs/Ge CELL WITH TiO_2/Al_2O_3 DUAL A.R. COATING. (COURTESY OF NASA LeRC)

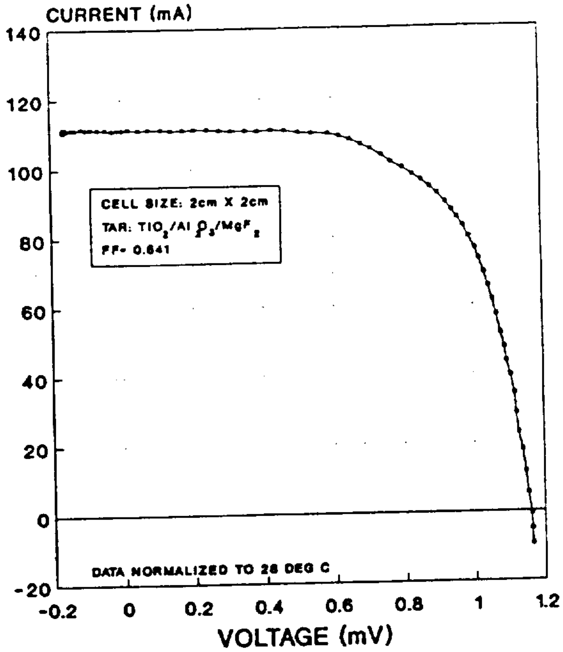

Figure 9 MEASURED AM0.22 I-V CURVE OF GaAs/Ge CELL WITH $TiO_2/Al_2O_3/MgF_2$ TRIPLE LAYER A.R. COATING (COURTESY OF NASA LeRC)

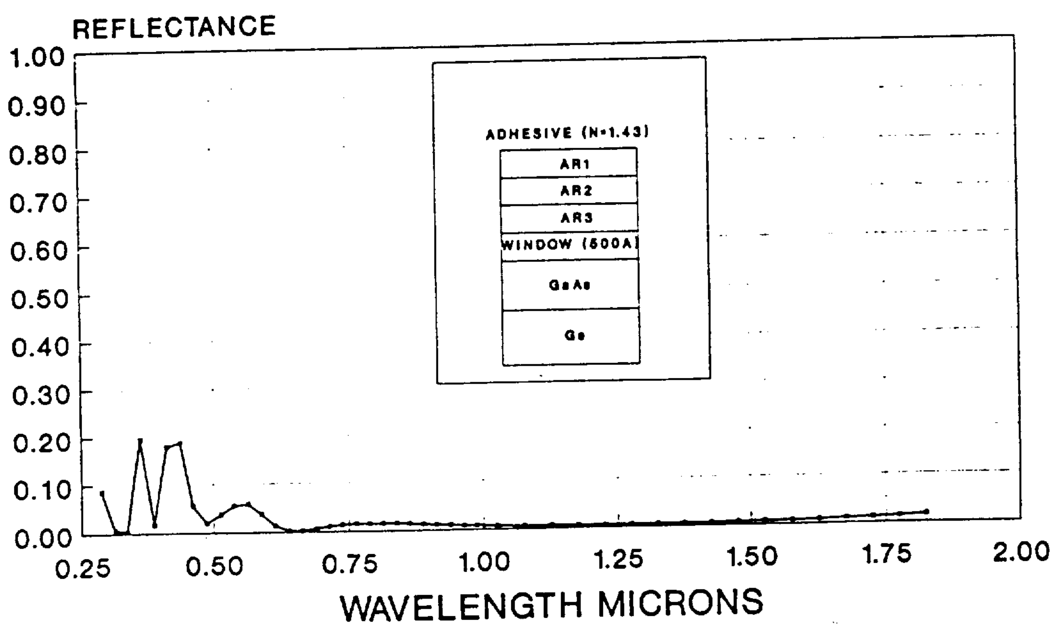

Figure 10 CALCULATED REFLECTANCE OF FILTERED OPTIMIZED GaAs/Ge CELL WITH TRIPLE LAYER A.R. COATING

GaAs CELL PARAMETERS

WINDOW THICKNESS uM	0.05
WINDOW DIFF LENGTH uM	0.2
WINDOW DIFF COEFFT cm2/S	0.27
WINDOW SURFACE REC VELOCITY cm/S	1000000
WINDOW DOPING CM-3	1.0E+18
EMITTER THICKNESS uM	0.5
EMITTER DIFF LENGTH uM	5
EMITTER DIFF COEFFT cm2/S	90
EMITTER INTERFACE REC VELOCITY cm/S	10000
EMITTER DOPING CM-3	2.0E+18
BASE WIDTH uM	3
BASE DIFF LENGTH uM	2
BASE DIFF COEFFT cm2/S	5
BACK SURFACE REC VELY cm/S	100
BASE DOPING CM-3	2.0E+17
SERIES RESISTANCE OHMS	0.2
SHUNT RESISTANCE OHMS	10000
GRID OBSCURATION %	5
TEMP DEG C	28
NO OF SUNS CONC	1

Ge CELL PARAMETERS

EMITTER THICKNESS uM	0.2
EMITTER DIFF LENGTH uM	1
EMITTER DIFF COEFFT cm2/S	24
EMITTER SURFACE REC VELOCITY cm/S	10000
EMITTER DOPING CM-3	1.0E+19
BASE WIDTH uM	100
BASE DIFF LENGTH uM	80
BASE DIFF COEFFT cm2/S	15
BACK SURFACE REC VELY cm/S	100
BASE DOPING CM-3	5.0E+17
SERIES RESISTANCE OHMS	0.2
SHUNT RESISTANCE OHMS	10000

Table 1 GaAs AND Ge CELL PARAMETERS USED IN CALCULATIONS

	GaAs CELL	Ge CELL				
		L=100μ	L=75μ	L=50μ	L=25μ	
Voc (V)	1.023	0.269	0.264	0.255	0.237	0.179
Jsc ($mAcm^{-2}$)	32.57	31.57	30.87	29.7	27.68	22.9
FF	0.821	0.655	0.646	0.630	0.597	0.500
Pmax ($mWcm^{-2}$)	27.37	5.57	5.27	4.78	3.93	2.05
Effy (%)	20.23	4.12	3.89	3.53	2.90	1.52

Table 2 EFFICIENCY PREDICTIONS FOR GaAs/Ge CELL WITH Ge BASE DIFFUSION LENGTH AS A VARIABLE