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REWRITEABLE OPTICAL DISK RECORDER DEVELOPMENT

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ABSTRACT

A NASA program to develop a high performance (high rate, high capacity) rewriteable optical disk recorder for spaceflight applications is presented. An expandable, adaptable system concept is proposed based on disk Drive modules and a modular Controller. Drive performance goals are 10 gigabyte capacity, 300 megabits/second transfer rate, 10^{-12} corrected bit error rate, and 150 millisecond access time. The design for an expandable Controller is presented. System goals are up to 160 gigabyte capacity at up to 1.8 gigabits per second rate with concurrent I/O, asynchronous data transfer, and 2 to 5 year operating life in orbit. Technology developments, design concepts, current status, and future plans are presented.

INTRODUCTION

High performance mass storage systems are crucial to future NASA programs such as the Earth Observing System (EOS) polar orbiting platforms. The complexity and capabilities of space information systems continue to grow. The volume of data generated by orbiting scientific instruments is projected to increase by orders of magnitude over the next decade. Requirements for onboard storage with capacities on the order of one terabit (10^{12} bits) and data rates in excess of one gigabit per second are anticipated. Ground-based mass storage needs such as data downlink buffers, temporary archives, and data processing, particularly by supercomputers and image processing workstations, are also growing.

To meet these needs, the Spaceflight Optical Disk Recorder (SODR) program was initiated. This program is sponsored by the NASA Office of Aeronautics and Exploration Technology and managed by NASA's Langley Research Center. The objective of the SODR program is to develop and demonstrate the technology and subsystem elements which form the basis for versatile, expandable mass storage systems for space flight applications. The approach is to produce a stackable, high performance (300 megabit per second, 10 gigabyte) rewriteable optical disk Drive and a modular system Controller. The system goals are 160 gigabyte (1.28×10^{12}) capacity and 1.2 gigabit (150 megabyte) per second data rate. The Drive and system concept and corresponding functional architecture are shown in Figure 1. This paper will discuss the concept, plans, status, and applications (including ground-based) of the SODR development program.

BACKGROUND

There are three basic types of optical disks. Read only disks, such as CD ROM, are reproduced from a laser written master and cannot be altered. This has become a popular medium for data distribution. Write-once-read-many (WORM) disks allow the user to permanently write information on the disk. These are used primarily for archival applications or when an audit trail is desirable. Both 5.25 (130 mm) and 12 inch (300 mm) write-once commercial products have been on the market for several years, with OEM vendors providing complete (jukebox) systems. Erasable or rewriteable disks allow the user to write, read, erase, and rewrite information. Rewriteable optical Drives, using 5.25 inch disks, are now commercially available. A wide range of information on optical data storage can be found in the SPIE Proceedings.[1,2]

Ruggedized small drives are being developed for the Government. A 5.25 inch write-once Drive is being qualified for a Shuttle experiment by NASA's Lewis Research Center. A 5.25 inch rewriteable disk Drive has been developed and demonstrated in fighter aircraft by the Air Force and is being considered by NASA Langley for aircraft instrumentation programs.[3] This same design has been modified for space flight and Drives are being tested for incorporation into Shuttle experiments by NASA's Goddard Space Flight Center and NASA Lewis.

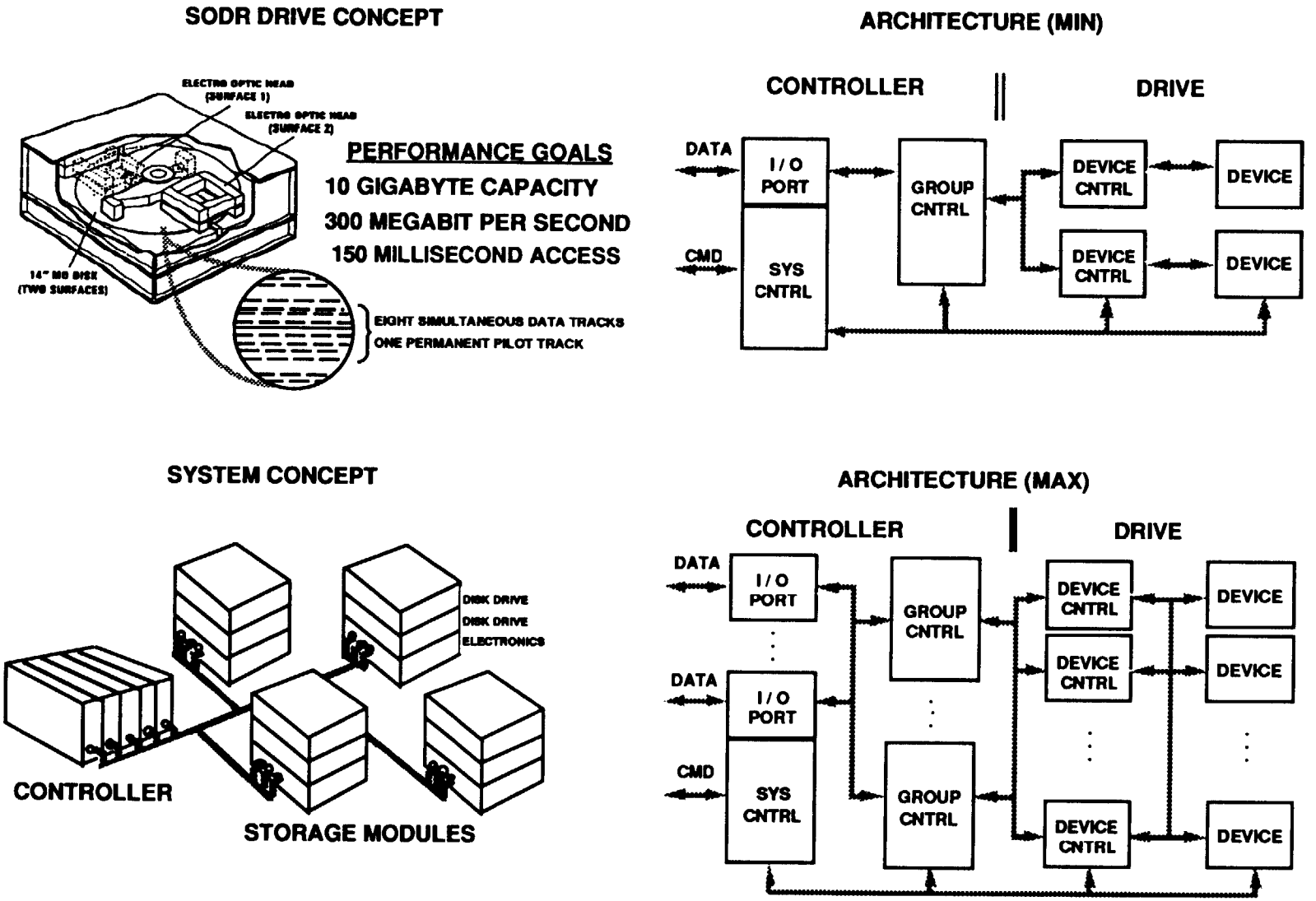


Figure 1. The SODR 14-inch disk Drive and configurable, expandable mass storage system concept. Modular approach based on stackable Drive and modular Controller.

To address high performance needs, the Government has been actively developing 14 inch (350 mm) systems. Two high capacity write-once "jukebox" systems were developed and delivered to NASA's Marshall Space Flight Center and the Air Force. The Air Force is funding the development of a 14 inch rewriteable disk Drive using two simultaneous laser tracks for transport aircraft applications. A consortium of Government agencies, including NASA, sponsored applied research in eight-track rewriteable optical disk storage technology based on a concept known as the Optical Disk Buffer which culminated in a demonstration in July of 1988. Extension of these developments to meet high performance space flight mass storage needs is the challenge being addressed by the SODR program.

DRIVE TECHNOLOGY

The SODR Drive development is based on magneto-optic (MO) rewriteable optical disk technology. The active media is a magnetic material made from rare earth and transition metal compounds. This is the most popular and mature rewriteable media.[4] The phases of the magneto-optic recording process are shown in Figure 2. The media is initialized to a common magnetic orientation that the inherent magnetic forces retain even in the presence of a strong external field. To write a mark, a focused laser spot is used to heat the media to the Curie point where the external field causes the magnetic orientation to be reversed. The laser is then used as a polarized light source to read the disk. The polarization angle of the reflected light is rotated corresponding to the magnetic orientation due to the Kerr effect. This rotation is detected, indicating the presence of a written mark. To erase the disk, the external field is returned to the original orientation and the laser is used to reheat the media and return the disk to its initial state.

Technology development for the SODR program has been focused on three fundamental areas: ruggedized 14 inch dual-sided MO media; independently addressable nine-element solid state laser diode arrays (used to provide eight parallel data tracks); and demonstration of a multi-track electro-optic (EO) head, with its electronic and mechanical subsystems.[5,6,7,8] Current media studies are focused on optimization of MO performance and the suitability of glass substrates for harsh environments. Tests include vibration, thermal cycling, radiation, and outgassing. A blank glass disk has survived 62 grms random vibration. Preliminary results continue to demonstrate that glass is the preferred substrate over aluminum. The laser development effort is focused on operating life and yield improvements. This includes fine tuning of the structure and process refinement and conversion to MOCVD crystal growth. Techniques to stabilize the lasing frequency, which can shift due to optical feedback and aging, are being studied.

As a proof of concept, a Technology Demonstration Unit (TDU) was produced. The TDU is composed of a multi-track EO head with 9-element diode laser array and a single-sided MO disk. Write, read, and erase of eight parallel data tracks, using a separate laser element for focus and tracking, was demonstrated in early 1990.[11] Figure 3 is a polarizing microscope photograph of actual recorded information (marks) from a MO 14 inch aluminum substrate disk. The effective data rate is 133 Mbps per second. The focused laser spot size is 0.7 microns and the minimum recorded feature length is 0.8 microns; this results in a capacity of 5 gigabytes on a side.

DESIGN CONCEPT

NASA's investigation of spaceflight applications led to the modular building block system concept shown in Figure 1. The system is made up of multiple Drive units, with their supporting electronics, and a modular Controller. This concept supports a variety of mass storage applications and forms the basis for an expandable system that can be configured for specific applications (capacity and I/O rate). This modular architecture also permits efficient hardware and software development, starting with single modules and isolates internal Drive interfaces from those likely to change, specifically the user interface.

The top level functional architecture is also shown in Figure 1. It is a hierarchical structure, starting with the device as the lowest level and expanding upwards to the system control function. The device performs the basic storage functions: reading, writing, and erasing of information. The device control supports device specific and data processing functions like data formatting, EDAC, and data encoding/decoding. The group control connects devices (through device control) to ports. It provides port related functions such as

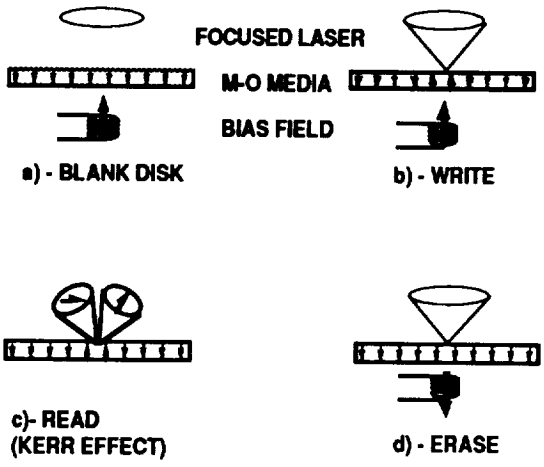


Figure 2. Magneto-optic process: a) initialized media unaltered by external field; b) laser heats media to Curie temperature where external field reverses orientation; c) change in polarization angle of reflected laser light indicates written mark; d) media erased by rewtiring to initial orientation.

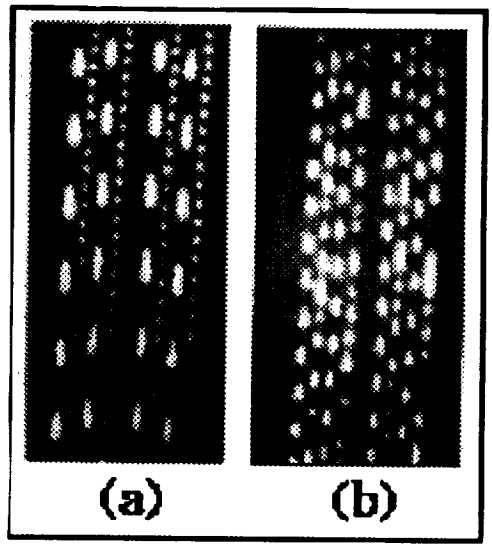
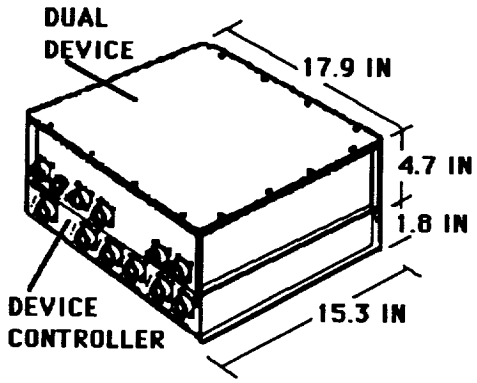


Figure 3. Polarizing microscope photograph of marks written on 14 inch MO disk by Technology Demonstration Unit; a) Alternating 1.875 and 7.5 megahertz square wave; b) Alternating 3.75 megahertz square wave and pseudo random data at 133 megabit per second. Minimum feature is .8 micron. Track spacing is 1.4 micron.



PHYSICAL CHARACTERISTICS

	DUAL DEVICE	DEVICE CONTRL
SIZE:	3/4 FT	1/4 FT
WEIGHT:	45 LBS	15 LBS
POWER:		
WRITE 150	50W	50W
WRITE 300	70W	100W
READ 150	75W	50W
READ 300	130W	100W
ERASE 300	70W	0W

ANGULAR MOMENTUM: 1 FT-LB

Figure 4. Projected flight Drive packaging with projected size, weight, and power. A Drive contains two devices and separate Device Controller.

rate buffering and multiple device synchronization. The system control provides the overall control, command processing, and interface to a single user or network.

The basic functions have been partitioned into a Drive, composed of the logical device and device control functions, and the Controller, composed of the logical group control and system control functions. Ideally, a set of generic control functions and a Controller to Drive interface can be defined which will be suitable for all applications. The detailed functional partitioning of control and system level functions continues. A system model is being developed to support system design and investigate functional issues such as file management, erasure algorithims, resource allocation, and data throughput.[9] This model will be used to validate an expanded multiple Drive system before it is built.

Drive

The SODR disk Drive unit, shown in Figure 1, is similar to a magnetic or Winchester disk Drive. It contains, as a minimum, the media and its supporting mechanisms. These include the optical heads, rotating disks, photodetectors, and the support subsystems (mechanical, optical, and electronic) needed to read or write information on the media. The SODR Drive contains a single disk with independent multi-track heads accessing each surface. Within the SODR system architecture, the Drive is logically equivalent to two devices. The projected physical package for the Drive and supporting electronics package, which represents the Device Controller, and its associated parameters are given in Table 1 and Figure 4.

The design is based on well known split-head, differential detection MO concepts. In a split-head system the laser and associated collection optics are mounted on a fixed, thermally controlled base plate and only the final objective lens assembly moves. Differential detection means the reflected beam is split into its polarized components and directed to separate detectors whose outputs are compared differentially. Supporting subsystems include the spindle and linear translator servos, which position the head, the data modulator/encoder which converts digital data into analog signals to drive the laser, and the demodulator/decoder used to convert detector system analog signals into digital data.

Controller

The Controller provides overall system control and the necessary interface between the user and the storage devices. It is responsible for command processing, multiple Drive synchronization, data buffering, file management, logical to physical mapping, fault processing, system self test, status reporting, and user data connection via high speed data ports. As shown in Figure 1, the System Controller will provide command and control operations, and the Group Controller with the Data I/O Ports will provide high speed data processing. The Drive provides data encoding and EDAC. The command and data interfaces are separated to achieve the desired reconfigurability and data throughput. The SODR Controller provides variable data transfer rates, simultaneous input and output through separate data ports, and dynamic reconfiguration.

CONTROLLER SUBSYSTEMS

The modular design approach has been followed within the Controller by further partitioning into subsystems and modules as shown in Figure 5. Each of these subsystems will be developed separately for the breadboard controller using commercially available technology; eventually they will be packaged as one system element for the flight SODR Controller.

A Group Controller internal circuit module is referred to as a slice and consists of the hardware necessary to implement the complete data path circuit for an eight bit parallel increment of data. The slice concept is consistent with the current design of the storage Device which will record the data on the disk surface in an eight bit parallel format. Each slice can be processed and transferred at a 150 Mbps rate. Data rate capabilities can be expanded by adding one slice for each 150 Mbps increment of the required data rate.

The Data Ports provide modularly expandable user interfaces. To achieve the rate requirements, the proposed ANSI High-Performance Parallel Interface (HPPI) standard was selected to be used for the User

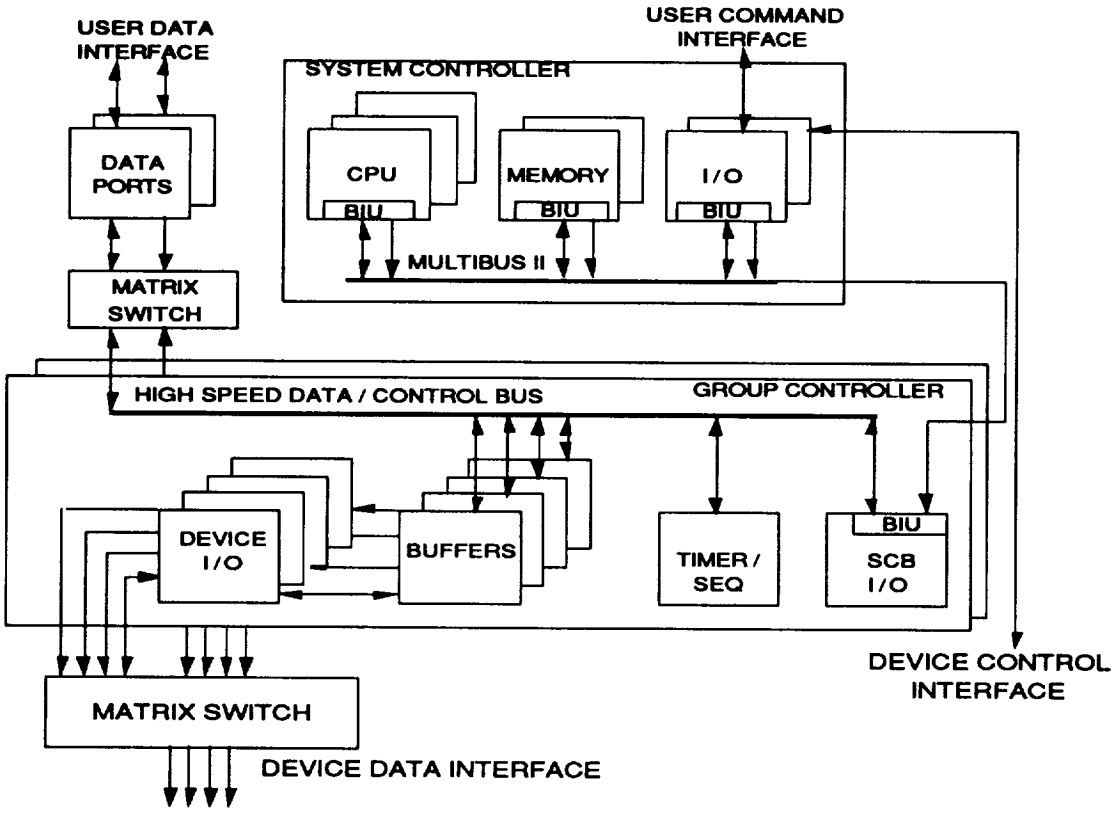


Figure 5. SODR Controller block diagram. Modular design approach which supports multiple Drives, multiple ports and byte wide expansion in data transfer.

interface Data Port. It will be implemented in eight bit parallel modules that correspond to a Controller slice for Drive compatibility and expansion.

The Matrix Switch provides the capability to quickly switch the data transfer path from one subsystem to another. This supports dynamic reconfiguration of the system according to user rate and capacity requests and supports graceful degradation by removing failed components from the data path. It also provides the capability to place unused drives on standby for reduced power consumption. The capabilities provided by the Matrix Switch are primarily for the requirements of flight versions of the controller. Ground-based systems could use direct connections for variations in system configurations.

System Controller

The System Controller decodes user commands and maintains control of the rest of the SODR system. The breadboard version will be composed of triply redundant CPU cards, memory cards, user command port cards, and the Multibus II message passing bus as shown in Figure 5. The CPU is the Harris RTX 2000. This processor was chosen for the high speed achieved by its RISC architecture, low power, ease of interfacing and programming, and availability as a standard cell in the Harris HCMOS process.

For the breadboard, the Multibus II standard has been selected as the primary system control bus. It provides operating flexibility and supports simple implementation of maximum system configuration. The Multibus II provides clearly specified electrical and mechanical systems, protocols for message passing, shared memory access, and support for unsolicited messages (i.e. virtual interrupts), and uses a parallel bus for fast data throughput. Also, it allows concurrent operations, permits convenient implementation of system fault tolerance, and is being considered by other projects for space flight use.

The primary functions of the System Controller software are to maximize data throughput, recover from failures, and maintain data file directories. This software does not directly handle the high speed data being transferred across the data port. It acts as a traffic cop for the data by decoding user commands, coordinating resources, and issuing sub-commands to the various hardware elements at its disposal.

A goal for the software design is to exploit the multiprocessor architecture to provide maximum fault tolerance and throughput. This will be accomplished by developing a data directed programming kernel that executes on each CPU. The scheduling of tasks is coordinated with the other active CPUs and results in a dynamic allocation of tasks to CPUs. Dynamic allocation of tasks enables load balancing of CPU resources and automatic recovery from CPU failures. A task is initiated on an idle CPU when the kernel detects that the appropriate arcs are pending for that task and broadcasts this data to each CPU by an unsolicited message. Message handlers on the other CPUs decode the message and start a timer so a recovery routine can be executed if the task is not finished by a specific amount of time. Tasks broadcast new arc data over the message passing system so all CPUs can update their arc and task definition tables.

Group Controller

The primary function of the Group Controller is data processing, synchronization, and buffering necessary to transfer high speed data between the user and the storage modules. Other functions performed by the Group Controller include System Controller data transfer, self test, and data interface control.

A block diagram of the functional concept for the Group Controller is shown in Figure 5. The Controller is divided into components according to functional requirements. The Buffer provides memory management, configuration control, and dual port RAM storage for data rate synchronization. The high speed Sequencer provides timing, address control, and data routing. The Data Port provides the user high speed data interface. The Device I/O provides the data interface between the buffer and the storage modules. The System Controller I/O provides command and system data transfer between the Group Controller and the System Controller. The High Speed Data Bus provides the interface for high speed data between the Buffer and the Data Port, and the interface for system data and control between all the components of the Group Controller.

One of the areas critical to the success of the Controller is the transfer of high speed data across backplanes and interface cables. Current commercial backplane interface standards have typical bandwidths around 10-16 MHz. Transfer rates are limited by IC propagation data delays, backplane clock skews, and multiple card loading. Backplane transmission line characteristics must be considered to minimize undesirable reflections. Analysis of the Futurebus indicates a best case transfer rate of 23.8 Mbps for synchronous and asynchronous systems. Due to the limitations of these commercial standards, a custom interface design is required for the Group Controller High Speed Data Bus. This custom interface is expected to achieve slightly better performance than the Futurebus standard by implementing the interface with minor variations from the standard. These changes include limiting the card loads to six and bus lengths to six inches and, if necessary, using ECL instead of ASTTL logic for the data latches. Fiber optic technology will also be considered for the design of the flight version of the Controller.

Interface Ports

The Controller will contain interface ports, as shown in Figures 1 and 4, to provide control and data to the User. The ports are separated into User Command and User Data segments to achieve desired reconfigurability and throughput. An SODR system may contain one or more data ports with slightly different configurations based on the number of slices needed to meet specific applications. The User Data Interface must be easily adaptable to variable maximum data rates; each slice in the User Data Interface will transfer data to and from the user at rates of up to 150 Mbps. The User Command Interface will provide transfer of all commands and status needed by the user to control the data recording operations.

The current User Data Interface design is based on the HPPI standard. Although this standard has not been finalized, available specifications clearly indicate that the basic HPPI concepts are ideally suited for this interface. The 200 Mbps transfer rate for each eight bit segment in the HPPI cable provides a comfortable margin above the system requirements of 150 Mbps for each slice. Design time will be minimized by taking advantage of the specifications and signal protocol within the standard. Also, future commercial HPPI hardware could be adapted to later versions of SODR.

The User Data Interface for the breadboard system will be implemented with currently available technology. The primary functions will be provided by high speed PLD chips and FIFOs, as well as standard high speed logic chips. These designs will be readily adaptable to take advantage of future developments in VLSI and ASIC technologies when the flight version is built.

Current plans for the User Command Interface include the use of standard interfaces such as the RS232, RS422, or Mil-Std-1553. The selected interface plugs directly into the System Controller MultiBus II backplane and minimizes the complexities of changing interfaces to meet different user needs.

Drive Interfaces

The actual design of the Device Data and Device Control interfaces has not been started, but the concept and approach have been fully developed. The eight bit parallel slice concept will be maintained at the Device Data interface. Data transfer across this interface will be slightly over 150 Mbps/slice to allow the transfer of both the original data and the associated overhead while maintaining a 150 Mbps delivery rate of the original data. If possible, the Device Control interface will be selected from available standard interfaces that provide the necessary device and data transfer control. The final selection of this interface will depend primarily on the final design details of the SODR Controller and the Storage Drive unit that is being developed separately.

DEVELOPMENT PLANS

The SODR Drive development has been divided into three phases. The first phase includes preliminary design of the flight Drive; detailed design, fabrication, and test of a Brassboard Disk Drive; integration and test with a Government fmished breadboard Controller; and verification of both the technology and design by a flight experiment as a Space Shuttle HitchHiker payload. Phase one will address developmental issues associated with the fundamental storage mechanisms specifically focused on spaceflight applications. Some of the issues to be addressed are bearings, bit error rate improvement by EDAC incorporation, flight optics design, flight packaging, and reliability.

The second phase includes design, fabrication, and test of a ground-based, fully functional Engineering Disk Drive (EDD) providing complete 16 track data processing electronics. The EDD will be integrated with a Government furnished Controller to produce a minimum system. This will be installed into a data systems test bed at a NASA facility for demonstration of simultaneous input and output of processed (corrected) data at 150 megabits per second or 300 megabits per second unidirectional data transfer. This unit is most likely to have potential commercial ground-based applications.

The final phase is design, fabrication, and test of a Prototype Disk Drive (PDD). This will include complete VLSI development and environmental testing. The PDD is to be integrated with a Government furnished flight qualified Controller and the EDD to provide a complete two disk system for demonstration and test. At the completion of phase three, a flight qualified Drive should be available for integration with a flight experiment.

SYSTEM APPLICATIONS

The random access capability of a disk memory makes many spaceflight applications possible, in addition to those classically served by tape recorders. Applications range from communications link buffer or temporary storage (much like a magnetic tape recorder) to single instrument or multi-user mass storage

subsystem (random access file storage). Random access storage enables data selection for quick-look or priority downlink. It allows onboard data processing or data compression. Operational telemetry data could be stored and analyzed onboard, or a subset transmitted and additional data transmitted as required. A multi-port system with rate buffering enables dynamic experiment operations. The inherent ability to play data back in a first-in-first-out mode increases the efficiency of ground-based data processing over the current tape approach that uses reversed playback to extend tape and magnetic head life.

The EOS polar orbiting platforms have been selected as candidate users in order to focus the program. The SODR has applications to many future programs, such as shuttle payloads, Space Station Freedom, Mars Rover, and other polar and geostationary orbiting platforms. The unmanned EOS has been identified as a system that could greatly benefit from the new technology and is a suitable target in terms of physical and operational environment. It is also on a schedule consistent with proposed SODR development.

Unfortunately, high performance random access storage represents a new system technology for spaceflight. Today's data systems are designed around magnetic tape recorders, a "proven" technology meeting past and present system needs (maybe not future needs). System designers and users are biased in their thinking by the constraints of sequential access storage. Until the optical disk is demonstrated to be a proven spaceflight technology, their thinking will probably remain constrained. The full random access potential of an optical disk system may not be achieved in the initial applications. As the potential advantages of rewriteable optical disk recorders are recognized, total system concepts and design requirements are expected to change.

Flight Environment

The space environment imposes unique operational and physical requirements when compared to ground-based or even airborne optical disk applications. Weight, volume, and power are always critical in space, but reliability, self-test capability, commanded or autonomous reconfiguration, and modular packaging are also important. Fortunately, EOS only requires operation on orbit which is a relatively benign mechanical environment. However, launch survival remains a major challenge. Other factors such as operation in a vacuum, zero gravity, subatomic and electromagnetic radiation, and angular momentum or gyroscopic effects associated with the large spinning disks must also be considered.

The SODR architecture and design addresses many of these problem areas. Redundancy, built-in test, and automatic reconfiguration to map out failed elements are planned to provide the graceful degradation needed for extended missions. A packaging concept based on counter rotating disks is proposed to minimize instability caused by angular momentum. To reduce outgassing effects caused by operation in a vacuum, SODR will use materials that do not dissipate or redeposit on optical surfaces. Special lubricants and sealed or magnetic bearings are under consideration for moving parts. Heat transfer problems apply to both the Drive and the Controller. The heat must be removed through the housing by conduction or radiation and the thermal expansion of materials can drive the design of optical systems. This highlights the importance of low power components such as CMOS and VLSI electronics and efficient solid-state lasers.

Ground-based

Although the current NASA program is focused on spaceflight, there are comparable ground-based applications that could benefit from an SODR like system.[10,11] The scheduling algorithms developed to handle the separate read, write, and erase cycles to support prioritized and/or shared data access by flight experiments are equally applicable to ground use. Ground configurations can be more elaborate because the typical flight constraints of power, weight, and volume need not be met. One use is as a rate buffer to provide initial storage of telemetry data prior to dissemination to slower speed distribution networks or facilities. As a supercomputer peripheral, a high performance optical disk system would enable more efficient use of these highly capable machines. Since the HPPI interface selected for SODR data transfer is under design and review by representatives from the leading computer manufacturers in the country, it is expected that SODR can be readily matched to one of these powerful CPUs. SODR can also perform in an

archival fashion and provide effective management of large continuously updated data bases. These applications are also being considered in the current program and are viewed as potential spinoffs.

CONCLUSIONS

High performance rewriteable optical disk memory with random access capability is an enabling spaceflight technology. Utilization of multiple data tracks, multiple disks, and an expandable Controller offers both high data rate and high capacity storage. The technologies have been demonstrated and the plans are in place for a versatile spaceflight mass storage system to become a reality. The spin-off potential for ground based applications is great.

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