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# INTEGRATED VERTICAL BLOCH LINE (VBL) MEMORY

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## ABSTRACT

Vertical Bloch Line (VBL) Memory is a recently conceived, integrated, solid-state, block-access, VLSI memory which offers the potential of 1 Gbit/cm$^2$ areal storage density, data rates of hundreds of megabits per second, and submillisecond average access times simultaneously at relatively low mass, volume, and power values when compared to alternative technologies. VBLs are micromagnetic structures within magnetic domain walls which can be manipulated using magnetic fields from integrated conductors. The presence or absence of VBL pairs are used to store binary information. At present, efforts are being directed at developing a single-chip memory using 25 Mbit/cm$^2$ technology in magnetic garnet material which integrates, at a single operating point, the writing, storage, reading, and amplification functions needed in a memory. This paper describes the current design architecture, functional elements, and supercomputer simulation results which are used to assist the design process.

## INTRODUCTION

Vertical Bloch Line (VBL) Memory[1, 2, 3] is a solid-state, radiation-hard, nonvolatile, block access, magnetic VLSI memory. Research and development efforts for this novel memory are being pursued in the United States, Europe, and Japan. Table 1 shows the potential storage density that is achievable with VBL memory. The densities are a function of stripe width and line feature width, which are defined respectively by the magnetic garnet material and the lithographic process.

In a VBL memory, information is stored using VBL pairs in magnetic stripe domains in garnets. The presence or absence of a Vertical Bloch Line pair in a bit-cell location defines a binary "1"and "0," respectively. Input to the chip is performed by converting currents into magnetic bubbles and then into VBL pairs. Output sensing is performed by converting VBL pairs into magnetic bubbles and sensing magnetic bubbles magnetoresistively.

## PRESENT DEVICE DESIGN

### Fabrication

The present design uses the magnet garnet, $(BiYGdHoCa)_3(FeGeSi)_5O_{12}$, as the storage medium. The thickness, stripe width, collapse field, saturation magnetization, and anisotropy field of the film is approximately 2.4 $\mu$ m, 2.4 $\mu$ m, 230 Oe, 450 Oe, and 1800 Oe, respectively. The film is grown epitaxially on a non-magnetic gadolinium-gallium-garnet (GGG) substrate. These films are transparent but also have a large Faraday rotation, so that magnetic stripes, magnetic bubbles, and, under certain conditions, VBLs can be observed magneto-optically with polarized light using the Faraday effect in a polarized light microscope.

The magnetic garnet has perpendicular magnetic anisotropy so that the magnetization lies perpendicular to the film plane, with the bulk of the film magnetized in one direction, and the stripes magnetized in the opposite direction. A magnetic domain wall is the boundary between the stripe's magnetization and the magnetization of the rest of the film. A twist of magnetization in the domain wall in the plane of the film is a VBL, and two such twists form a VBL pair. If the chirality, or sense of rotation, of the VBLs in the wall is the same, the VBL pair is stable, with a size calculated to be much less than 1 $\mu$ m. The VBL pair is bound together energetically by VBL demagnetizing field energy and magnetic exchange energy.

The present device is divided into four main functional areas. First, the VBL storage area is designed to confine and stabilize stripe domains. Second, read/write gates are needed to convert VBLs to bubbles and vice versa. Third, a major line is needed for propagating bubbles which are used for input and output. Fourth, the output detector is needed for generating the output signal voltage. A sample architecture for a VBL chip is shown schematically in Figure 1.

The present device is built with ten mask layers as shown in Figure 2. Three metal mask layers are used for providing the contact pads and conductors which control the strip generator, read/write gates, bubble generator, and major line. $SiO_2$ and photoresist are used for insulating metal layers, and a window mask is used to open vias and contacts when needed between metal layers. Two ion implantation mask steps, using 150 keV Ne+ ions at a dosage of $4 \times 10^{15}$ ions/cm$^2$, are used so that, after etching, grooves which are 0.2 $\mu$ m and 0.4 $\mu$ m thick are created. These grooves create stable locations in the garnet film for VBL stripe domains. An additional ion implantation mask layer is used in the major line to inhibit VBL formation in the input/output bubbles. A permalloy ($Ni_{0.8}Fe_{0.2}$) mask deposition is used to develop a magnetoresistive sensor which senses magnetic bubbles at the output and produces output voltages. A cobalt-alloy (i.e., CoPt) mask deposition is used for creating bit cells for VBL pairs along the walls of stripe domains. In test chips, a 5 nm thick Cr mirror layer is used to assist in stripe, bubble, and VBL observations using the magneto-optic Faraday effect during testing.

Supercomputer simulations[4, 5] which compute the effect of magnetic fields on magnetic domains, such as with stripe grooving, the major line, and the major line expander, are used heavily to assist in device design. VBL chip layouts are performed on an HP workstation and IBM PC/AT computers. Layouts are converted into fabrication masks using CIF and GDS II formats.

Stripe and Bit Stabilization

Data in the form of VBL pairs are stored in the domain walls of array of strip domains as depicted in Figure 3. The stripes are physically located in grooved regions in the garnet, as shown schematically in Figure 1 and in the design layout in Figure 4. The grooving allows selecting the bias field so that stripes are stable when the other chips functions, including the major line, are operating. The demagnetizing field produced by the bias field at the edge of grooved regions also serves to hold the stripe end and produce a stabilizing, effective edge-affinity magnetic field. Results from a supercomputer simulation of the formation of stable stripes in grooved garnet are shown in Figure 5. The computations were performed at 1 nsec time steps, and the computed stripe domain shape is shown at 40 nsec intervals.

Bit stabilization is used to stabilize VBL pairs along the stripe, as shown in Figures 1, 3, and 4. A periodic potential is placed along the stripe by an array of CoPt bars. For the CoPt, the saturation magnetization, coercivity, geometry, and spacing from the garnet are chosen to provide a sufficient field of approximately 5 Oe at the VBL stripe. This field value is currently considered to be enough to provide fields which create potential wells for the VBL pairs without disrupting the VBL pairs and moving stripes away from their groove-stabilized positions. The computed bit stabilization field profile at the end of an array with a 2 $\mu$ m bit period is shown in Figure 6. The distance between the CoPt and the garnet film is a parameter in the plot. The periodicity in the field profile is clearly evident.

Propagation of the VBL pairs, around the bit cells and to the read/write gates, can be achieved in two ways. First, a vertical pulse field can be applied which presses, or rocks, the stripe against the groove wall which gyrotropically causes VBL pairs to propagate down the stripe. Second, an in-plane field can be applied which directly causes VBL pairs to advance along the stripes' walls.

Read/Write Gates

Read/write Gates are used to convert VBL pairs in stripes into bubbles during the read process, and to convert bubbles into VBL pairs during the write process. It is necessary to read and write both "1's"and "0's"correctly. Nondestructive readback is achieved by using a current in conductors to bring the end of a

stripe out of its groove into the read/write gate and into the presence of another conductor. If no VBL pair is present at the end of the stripe, the sense of the magnetization direction in the stripe wall causes the stripe to be difficult to chop with the field from a conductor because of the effect of exchange energy. The stripe is then returned to its stable position in the grooving. However, if a VBL pair is present, one VBL would be brought into the read/write gate while the other VBL would remain in the grooving. Hence, the chirality of the strip walls would be in the same direction which would readily allow the stripe to be chopped. The chopped portion of the stripe becomes a bubble, which is them propagated to the output for sensing, while the stripe returns to the grooved region. The chopping process recreates a VBL pair in the stripe which leaves the initial information intact.

Writing is achieved by bringing a bubble from the nucleator and major line to the desired read/write gate. If a bubble is present,m when the stripe is subjected to a field to bring it into the read/write gate, the stripe does not get drawn into the read/write gate because of magnetostatic repulsion between the bubble and the end of the stripe. Therefore, no writing to the stripe occurs. But if a bubble is not present, the stripe is brought rapidly into the read/write gate which inserts a VBL pair into the stripe, and the stripe is then allowed to relax into the grooving.

Major Line and Output Detector

The major line consists of a bubble nucleator for converting input signal currents into bubbles, a track for propagating bubbles from the nucleator to the read/write gates and from the read/write gates toward the output, an output detector for converting the demagnetizing field from bubbles into output voltages, and an expander which is used to stretch a bubble to a desired length to provide a satisfactory signal-to-noise ratio at the output.

A hairpin conductor is used for the nucleator. When a current is applied, such a conductor produces a magnetic field which is concentrated at the center of the hairpin. This field is used to generate bubbles which are used to transmit binary information to the VBL stripes via the read/write gates.

The propagation track in the major line consists of two levels of conductors. Each conductor is a sepentine arrangement of hairpin conductors which provide local magnetic field variations which form "waves"of stable positions for the bubbles down the track. The conductors are physically phase shifted by $90^0$ to effect propagation. The principle of operation of the major line is shown in Figure 7. The layout of the major line track, along with the bubble nucleator and two read/write gates and grooves, is shown in Figure 4.

The output detector consists of a rectangular strip of permalloy, which is magnetoresistive. When the fringing magnetic field from a magnetic bubble affects the sensor, the sensor's resistance changes. When a reference current is issued to the sensor, the presence or absence of a bubble induces two different voltage levels which define binary "1's"and "0's." If it were necessary to maximize common-mode rejection from stray magnetic fields, two magnetoresistive sensors, including the actual sensor and a dummy sensor, can be used which allow signals to be measured differentially. Signals from the magnetoresistive sensor are increased if longer elements with greater electrical resistance are used. Bubbles can be stretched in length, to provide additional magnetic fields for the lengthened sensor, by widening the bubble track as the bubble approaches the sensor. The combined output sensor and expanding major line are shown in Figure 8, in which only one propagation metal layer in the major line is shown for clarity. Shown in Figure 9 is a supercomputer simulation, shown at 40 nsec intervals after being computed at 1 nsec intervals, of a bubble being stretched and then unstretched as it passes through the expander and detector.

## EXPERIMENTALRESULTS

Sample experimental results of chip functions from past designs are now presented.[6,7] These data were taken on test chips using a 4.76 $\mu$ m thick $(BiYSmLu)_3(FeGa)_5O_{12}$ garnet film with a saturation

magnetization of 200 Oe, zero-field stripe width of 4.67 $\mu$ m, characteristic length of 0.61 $\mu$ m, domain wall mobility of 350 cm/sec/Oe, anisotropy field of 1350 Oe, coercivity of 1.1 Oe, and collapse field of 100 Oe.

Figures 10 and 11, respectively, show stabilized stripes in grooves near read/write gates at the end of a groove, and near the center of the stripe groove near the stripe nucleator. The stripes are observed, with polarized light using the magneto-optic Faraday effect, as white strips against a darker background. The dark bars running perpendicular to the stripes are the cobalt bit-stabilization bars as described in Figures 1, 3, and 4.

Figure 12 shows nucleated bubbles, as white spots, in the major line as they propagate down the track. Bubbles and stretched bubbles in the expander portion of the major line near the output detector are shown as white sports and strips, respectively, in Figure 13.

## CONCLUSION

VLSI designs, simulation results, and experimental results have been presented which describe current work on the storage and input/output functions for solid state, high density, nonvolatile, radiation hard, block access Vertical Bloch Line (VBL) Memory. Such a memory offers the potential of achieving 1 Gbit/cm$^2$. Three metallizations are used along with three ion implantation steps, one permalloy magnetoresistive sensor deposition, and one CoPt bit-stabilization deposition. Previous and current experimental results and supercomputer simulations indicate that individual storage, read/write gate, and input/output functions are feasible. Present work is aimed at integrating all necessary memory functions on a single chip to achieve simultaneous operation, a unique operating point, and a fully-functional single chip memory.

## ACKNOWLEDGEMENTS

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5. N. Hayashi and K. Abe. "Computer Simulation of Magnetic Bubble Domain Wall Motion," Japanese Journal of Applied Physics, Vol. 15, No. 9, pp. 1683-1694, September, 1976.

6. J. C. Wu, et al. "Major Line Operation in Vertical Bloch Line Memory," Paper FP-10, Accepted for Presentation, 1990 Magnetism and Magnetic Materials Conference, San Diego, CA, October, 1990.

7. J. C. Wu, et al. "Stripe Stabilization in Vertical Bloch Line Memory," Paper FP-9, Accepted for Presentation, 1990 Magnetism and Magnetic Materials Conference, San Diego, CA, October, 1990.

| | $L_f$ = 1 μm | $L_f$ = 0.5 μm | $L_f$ = 0.1 μm |
|---|---|---|---|
| $S_w$ = 5 μm: | 10 Mbits/cm² | 20 Mbits/cm² | 100 Mbits/cm² |
| $S_w$ = 2 μm: | 25 Mbits/cm² | 50 Mbits/cm² | 250 Mbits/cm² |
| $S_w$ = 1 μm: | 50 Mbits/cm² | 100 Mbits/cm² | 500 Mbits/cm² |
| $S_w$ = 0.5 μm: | 100 Mbits/cm² | 200 Mbits/cm² | 1000 Mbits/cm² |
| $S_w$ = 0.25 μm: | 200 Mbits/cm² | 400 Mbits/cm² | 2000 Mbits/cm² |

Table 1: VBL Storage Density as a Function of Stripe Width, $S_w$, and Line Feature Size, $L_f$. Storage density is inversely proportional to $2S_wL_f$.

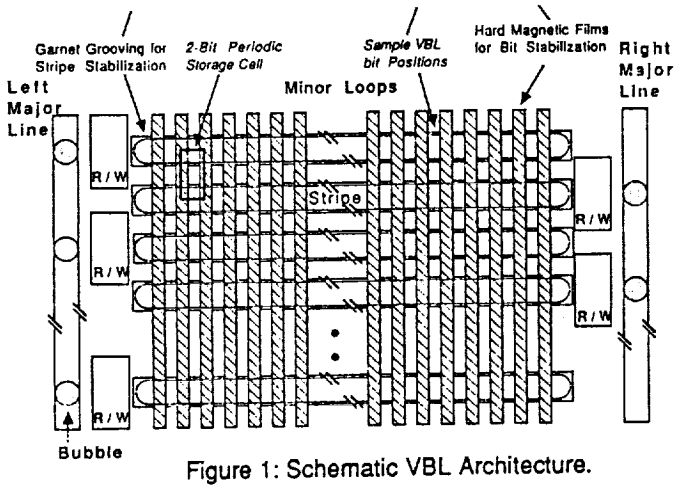



Figure 1: Schematic VBL Architecture.

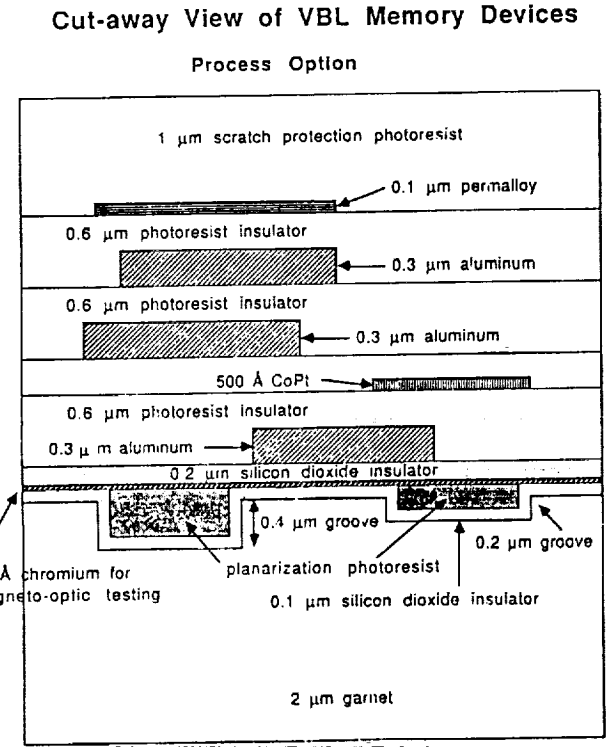



Figure 2: Cross-Section of the Current VBL Fabrication Process.

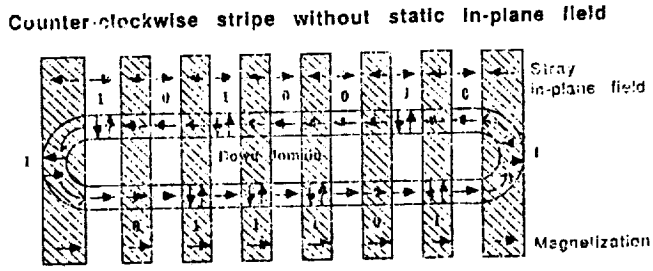



Figure 3: Schematic of VBL Stripe Storage Structure.

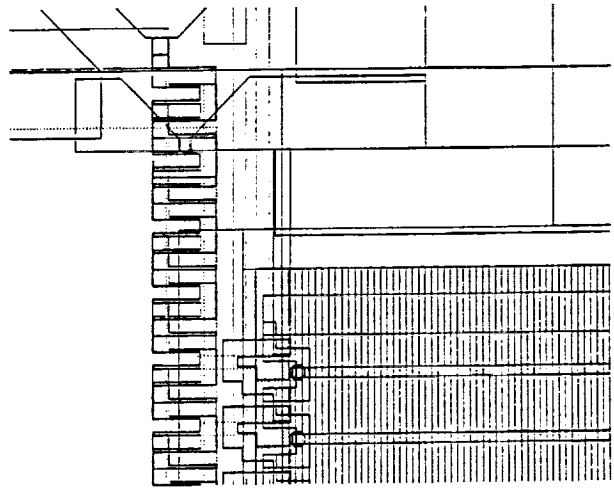


Figure 4: Layout of VBL Chip Nucleator, Dual-Conductor Major Line, and T Read/Write gates and Two Stripe Grooves.

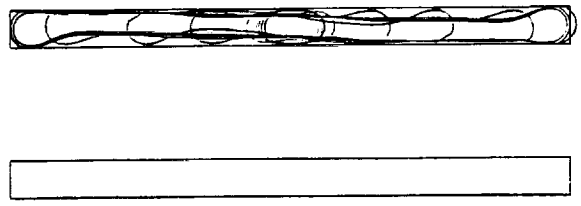


Figure 5: Supercomputer Time-Evolution Simulation Results of Stable Stripe Formation in a Grooved Garnet.

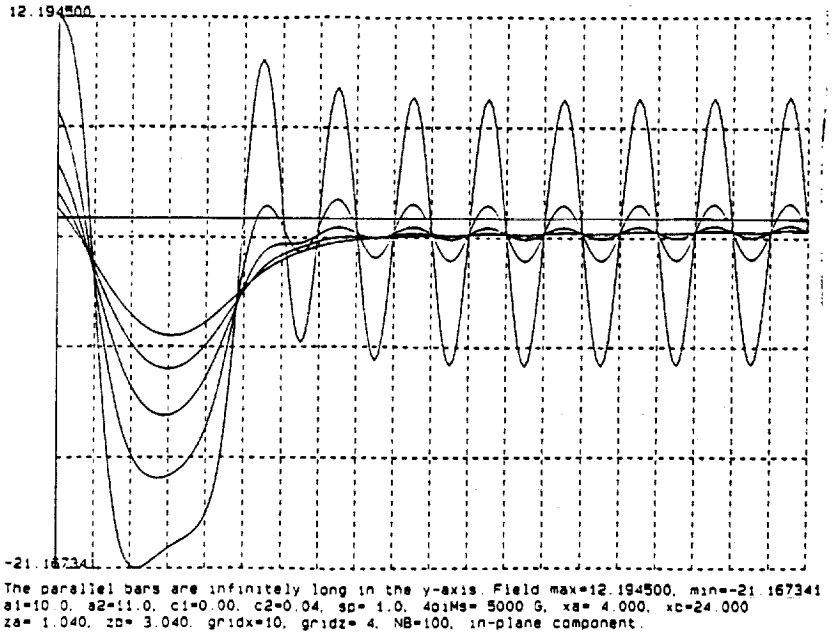
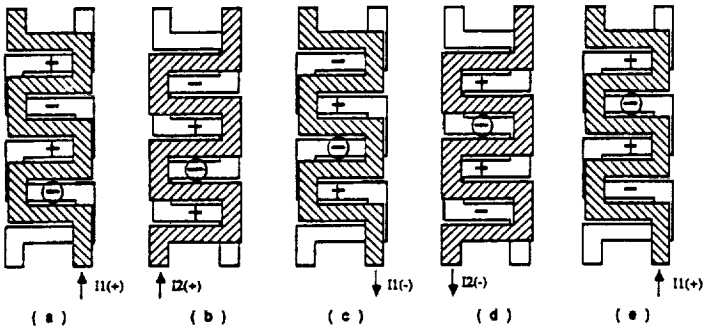



Figure 6: Computed Periodic Magnetic Field Profile of VBL Bit-Stabilization Wells.

**Propagation of Bubbles Using Current**




A current in a zig-zag conductor, as shown in (a), produces an alternating magnetic field pattern which attracts or repels bubbles in sites along the conductor. By staggering two conductor patterns as shown, and alternating the current sent to each conductor, a track is defined which can propagate bubbles. Due to the low inductance of the conductor sheet, such a propagator can be operated at a very high frequency.

Figure 2.4.1.: Principle of Bubble Propagation in a Dual-Conductor Major Line.

Figure 7: Principle of Bubble Propagation in a Dual-Conductor Major Line.

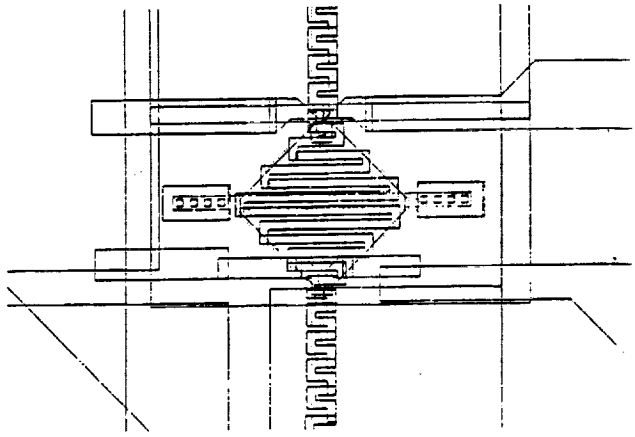


Figure 8: Layout of VBL Expander and Output Detector.

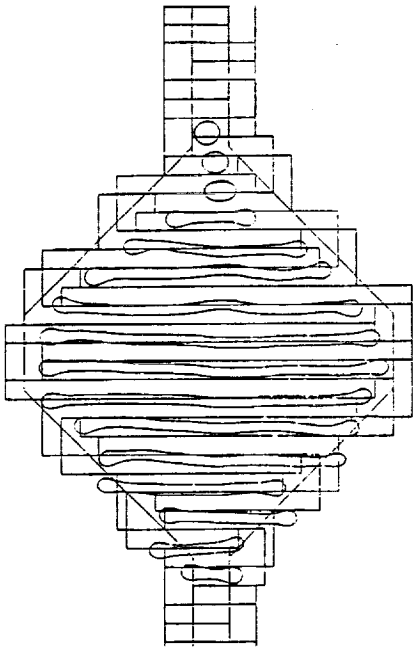


Figure 9: Supercomputer Time-Evolution Simulation of an Expanding Bubble in the Major Line Expander and Output Detector.

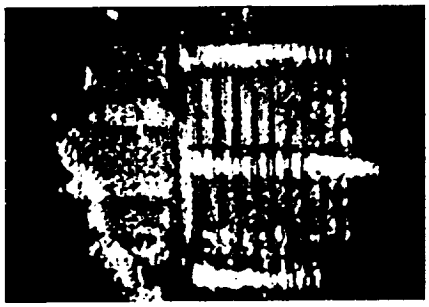


Figure 10: Photograph of Stable Stripes Near the Read/Write Gate end in a VBL Test Chip.

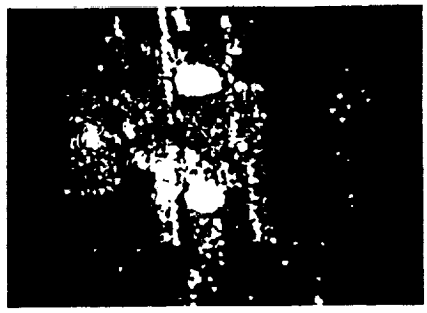


Figure 12: Major Line Under Operation Near the Center of the Major Track.

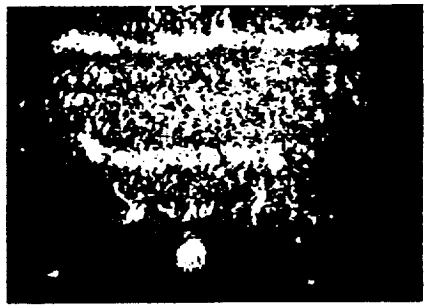


Figure 13: Major Line and the Major Line Expander Under Operation.

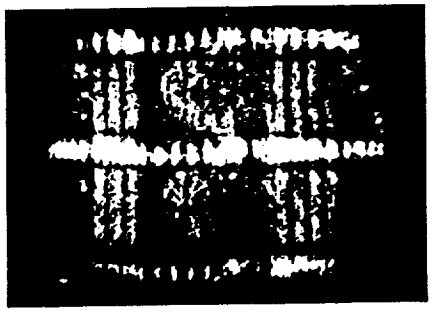


Figure 11: Photograph of Stable Stripes at the Stripe's Center, Near the Stripe Nucleator in a VBL Test Chip.

## SESSION C - ENVIRONMENTAL TECHNOLOGY

**Wednesday November 28, 1990**

- **Physical/Chemical Closed-Loop Water Recycling**
- **Water Quality Analyzer**
- **New Research On Bioregenerative Air/Water Purification Systems**
- **Environmental And Facilities Management System (EMFS)**
- **The Land Analysis System**
- **Potential Commercial Use Of EOS Remote Sensing Products**