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SPACE PLATFORM POWER SYSTEM HARDWARE TESTBED

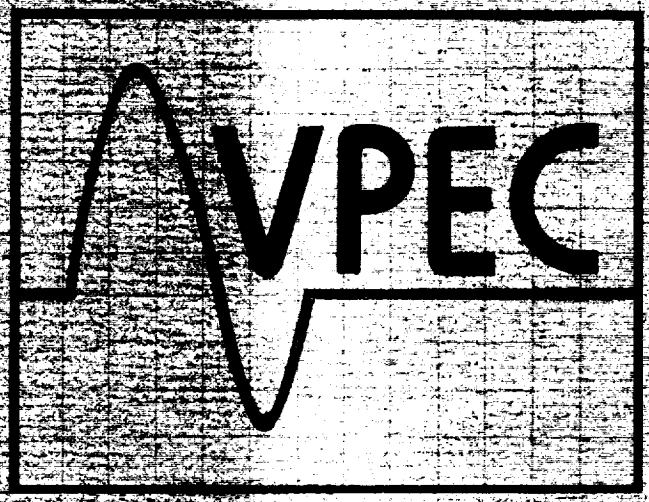
FINAL REPORT

PREPARED FOR

NASA GODDARD SPACE FLIGHT CENTER
GREENBELT, MD
Contract No. NAG 5-1232

PREPARED BY

D. Sable, A. Patil, T. Sizemore, S. Deuty
J. Noon, B.H. Cho, and F.C. Lee



June 21, 1991

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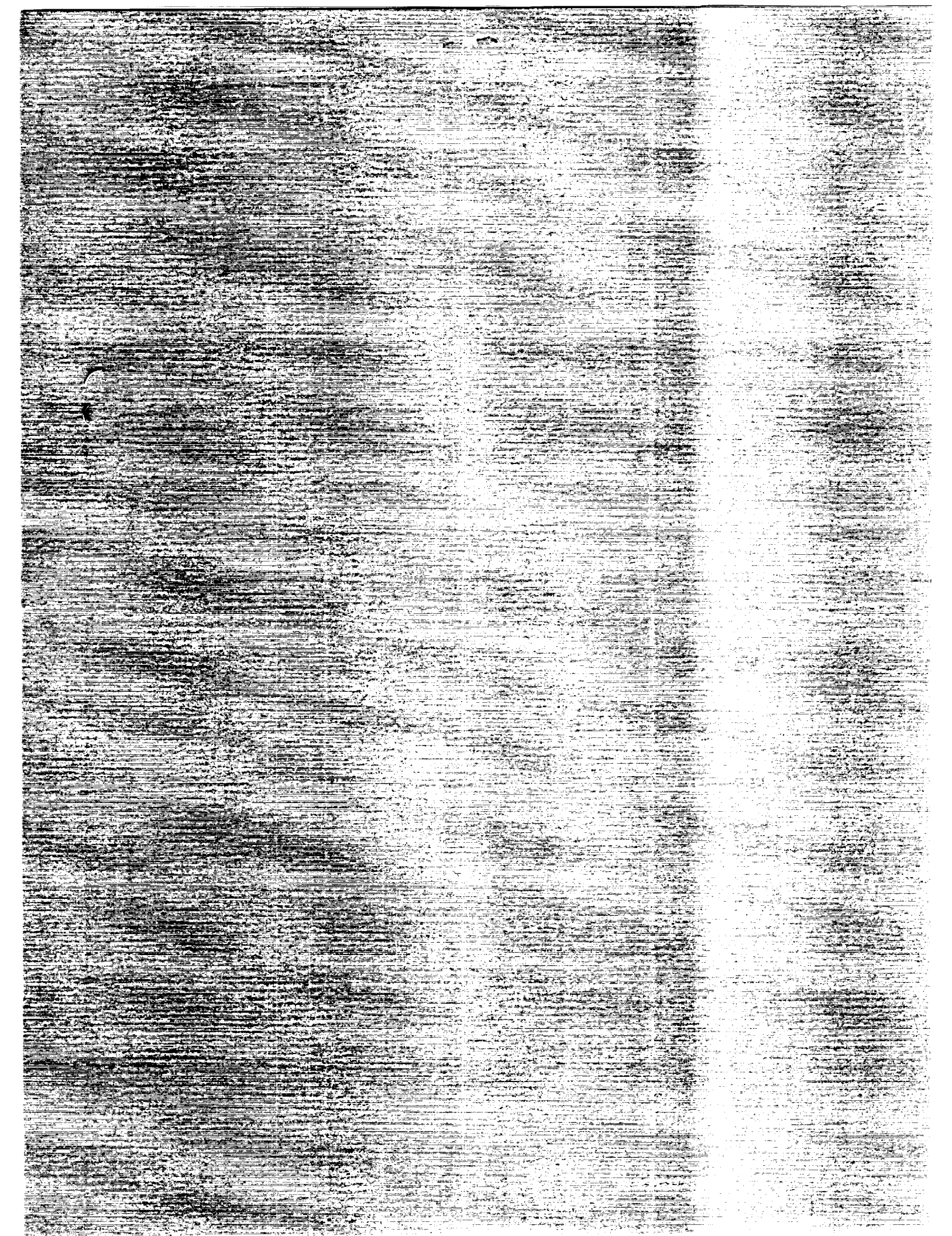

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SPACE PLATFORM POWER SYSTEM HARDWARE TESTBED - FINAL REPORT

1.0 INTRODUCTION

This final report covers work performed under NASA contract NAG 5-1232 from September 1990 to April 1991 on the design, development, and test of a power system suitable for use in the NASA Space Platform. The scope of the work includes the design of a multi-module, multi-phase boost regulator and a voltage-fed, push-pull autotransformer converter for the battery discharger. A buck converter was designed for the charge regulator. Also included is the associated mode control electronics for the charger and discharger, as well as continued development of a comprehensive modelling and simulation tool for the system.

Chapter 2 discusses the design of multi-module boost converter for use as a battery discharger. Chapter 3 discusses an alternative battery discharger design using a voltage-fed, push-pull autotransformer converter and has been submitted by Scott Deuty as his Masters' Thesis. Chapter 4 discusses the design of the charge regulator using a simple buck converter. Chapter 5 discusses the design of the mode controller and effects of locating the bus filter capacitor bank 20 feet away from the power ORU. Chapter 6 includes a brief discussion of some alternative topologies for battery charging and discharging. Chapter 7 describes the power system modelling.

2.0 MULTI-MODULE BOOST CONVERTER DESIGN

A four module, multi-phase boost converter, shown in Fig. 2-1, was analyzed [1] as a candidate topology for the Space Platform battery discharger. Nonlinear design optimization techniques were employed in order to determine the optimum switching frequency of a 95%, 96%, and 97% efficient design. The results of the analysis indicated that a 97% efficient design operating a 45 kHz was feasible with moderate component sizes. This chapter shall detail the design and test of a four module, multi-phase boost converter for the Space Platform battery discharger. Included is a discussion of the magnetics design, the output filter design, the pulse-width-modulator (PWM) design, the protection circuitry, the control loop, and the theoretical and experimental results.

2.1 Magnetics Design

The original analysis called for a METGLAS 2605S-C material gapped cut C-core with foil windings to be employed for the boost inductor. This was selected for its high saturation flux density, low loss, and high window utilization factor. Two cut cores were designed for the application. After experiencing higher than expected losses, two Molypermalloy Powder (MPP) torroid cores were designed and tested. All cores were designed with the aid of a data-base driven electronic spreadsheet. Included is a discussion of the different inductor designs and their test results.

2.1.1 METGLAS Material

Fig. 2-2 shows a representation of a cut-core design with foil windings. Two foil lengths are insulated with kapton tape and wound around separate bobbins. A short piece of wire is soldered to connect the two foil forms. A fiberglass material is placed into both bobbins to

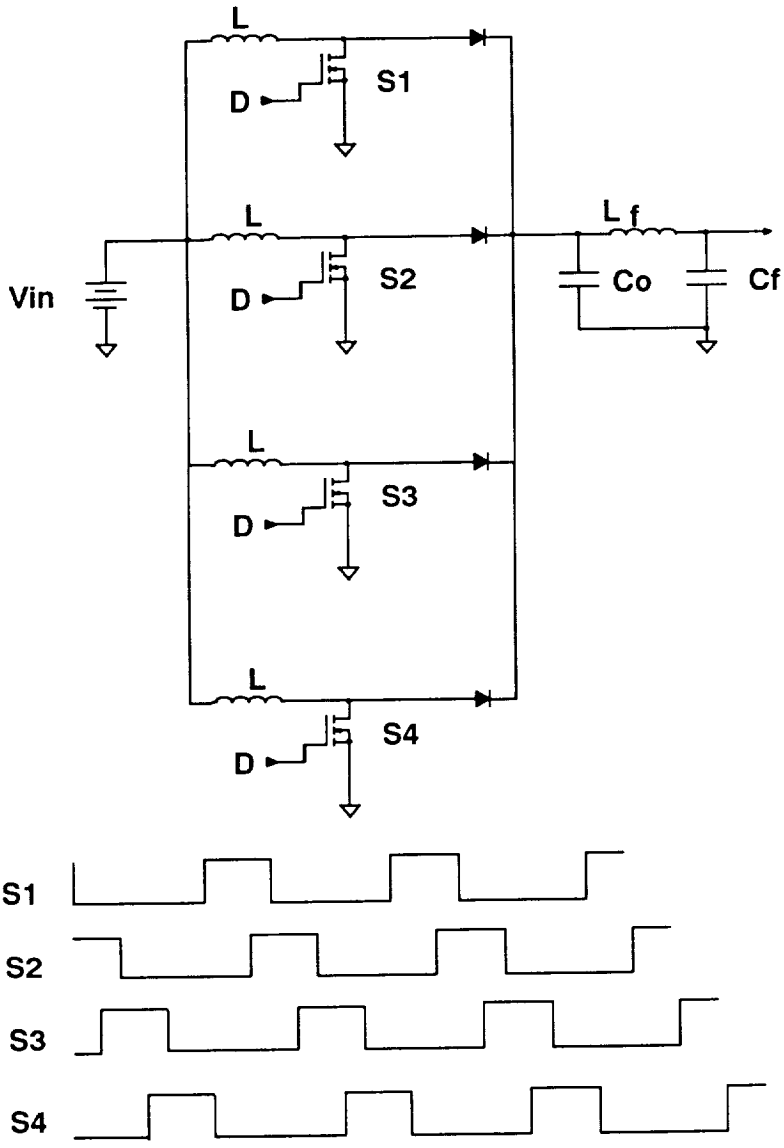


FIG. 2-1 FOUR MODULE, MULTI-PHASE BOOST CONVERTER

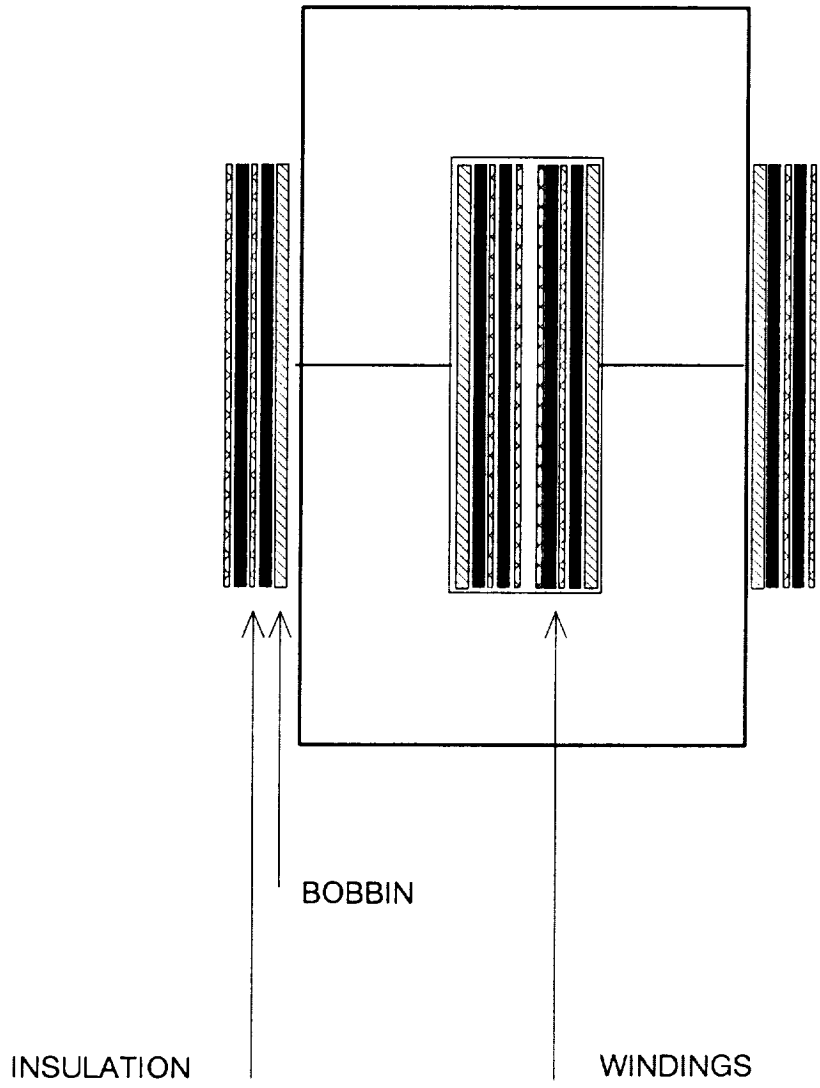


FIG. 2-2 CUT-CORE INDUCTOR WITH FOIL WINDINGS

serve as the air gap. The two halves of the cut-core are placed into the bobbins with the gap sandwiched in between.

One way to for design a cut-core inductor having an inductance, L, a peak current, I_{pk}, and an RMS current, I_{rms}, is to calculate the power handling capability as the window area, cross sectional area product given below:

$$W_a A_c = \frac{I_{rms} I_{pk} L}{0.75 K_u B_{max} J} \quad (m^4) \tag{2.1}$$

The window utilization, K_u, for a foil-wound cut-core can be very high, sometimes over 45%. The constant 0.75 comes from the stack factor of METGLAS material. The saturation flux density, B_{max}, of the METGLAS material is 1.4 Tesla. The current density, J, can vary between 3×10^6 to 3×10^7 A/m^2 and involves a trade-off between efficiency and weight. Based on the results of the optimization study, a low current density of about 3×10^6 A/m^2 is optimum. Once a core is selected having the necessary power handling capability, the number of turns, N, is designed to fill the window area. The air gap length, l_g, is then designed to yield the proper inductance. This is given by (air gap length in mils):

$$l_g = \frac{0.4\pi N^2 (A_c \times 0.75) \times 0.1}{L \times 2.54} \tag{2.2}$$

Inductor core loss for METGLAS material is a function of the core volume, CV_L, the AC flux, B_{ac}, and the switching frequency, F_s. It is estimated from the manufacturers data sheets as:

$$P_{fe} = 3.42 \times 10^{-4} CV_L B_{ac}^{\ 2.04} F_s^{\ 2.23} \tag{2.3}$$

One further significant loss mechanism is eddy current loss induced in the plane of the laminations by the fringing flux around the air gap. Very little information has been published about gap loss, yet it is a significant component of the inductor loss. Using silicon steel cut cores at 60 Hz and 400 Hz, Lee and Stephens [2] offered the following empirical formula for gap loss:

$$P_{gap} = .039 \times l_g F_s C_{wid} B_{ac}{}^2 \tag{2.4}$$

where C_{wid} is the width of the core in the plane of the laminations. This formula was found to be highly useful in determining the gap loss of METGLAS cut-cores in the frequency range of 40 kHz to 100 kHz.

The chosen inductance value was the subject of extensive optimization. Power supply designers will often select an inductance that maintains continuous inductor current at the minimum load condition. This avoids large changes in the converter dynamic characteristics when crossing the boundary between continuous and discontinuous modes. This was not a design criteria for the four module boost converter. Since the converter must operate down to no load, even an infinite inductance cannot maintain continuous inductor current. The four module boost inductors were designed to optimize efficiency and weight only.

A smaller inductance will obviously yield a lighter weight inductor. However, the smaller the inductance value, the higher the AC flux in the inductor resulting in higher core loss and gap loss. A inductance value of approximately 270 μH was selected as a compromise between size and efficiency. This brings the boost converter into discontinuous inductor current mode at a power level of 300 W, one sixth of the peak power. This is a very close to a conventional design.

Specifications called for a design able to regulate 1800 W down to an input voltage of 53 V. This requires an inductor with a saturating current greater than 12 A.

The cut-core design used an MC1490-1b core with 45 turns of 7 mil by 1.1 inch foil. A 20 mil airgap yielded a 250 μH inductor saturating a 15 A. The total weight for the four inductors is 780 grams.

The inductor gap loss led to higher than expected total losses for the cut-core inductors. This prompted the design of an alternative inductor.

2.1.2 MPP Material

Molypermalloy Powder (MPP) cores contain a distributed airgap within a torroid geometry. MPP cores have less than half the saturating flux density of the METGLAS material. Also, the torroidal shape cannot yield as high a window utilization factor. Obtaining the same inductance and saturating current as a METGLAS cut-core will result in an MPP core with larger size and weight. MPP cores, however, have lower core loss and do not have a gap loss. The lower permeability MPP cores have very low losses. Ironically, to obtain lower effective permeability with the cut-cores requires a larger air gap and thus higher losses. Thus a smaller inductance can be used to obtain the same efficiency with an MPP core as with a METGLAS core.

An inductance of 75 μH was selected for the MPP core. This brought the converter into discontinuous mode at power levels below 1200 W which is two thirds of the peak power level. This is much higher than a conventional design. Two 75 μH, MPP inductors were designed. The first used a 55083, 60 μ, core with 31 turns of #12 AWG wire. The total weight of the four inductors was 590 grams. The second used a 55550, 26 μ, core with 52 turns of #16 AWG wire. This has a total weight of 308 grams.

Fig. 2-3 shows a comparison of the four module boost experimental efficiency with the different inductor designs. Both designs with the MPP cores exceed 97% efficiency over the load range from 300 W to 1800 W. The cut-core design drops in efficiency at lighter loads due to the higher eddy current losses. Both MPP core designs have a lighter weight than the cut-core design.

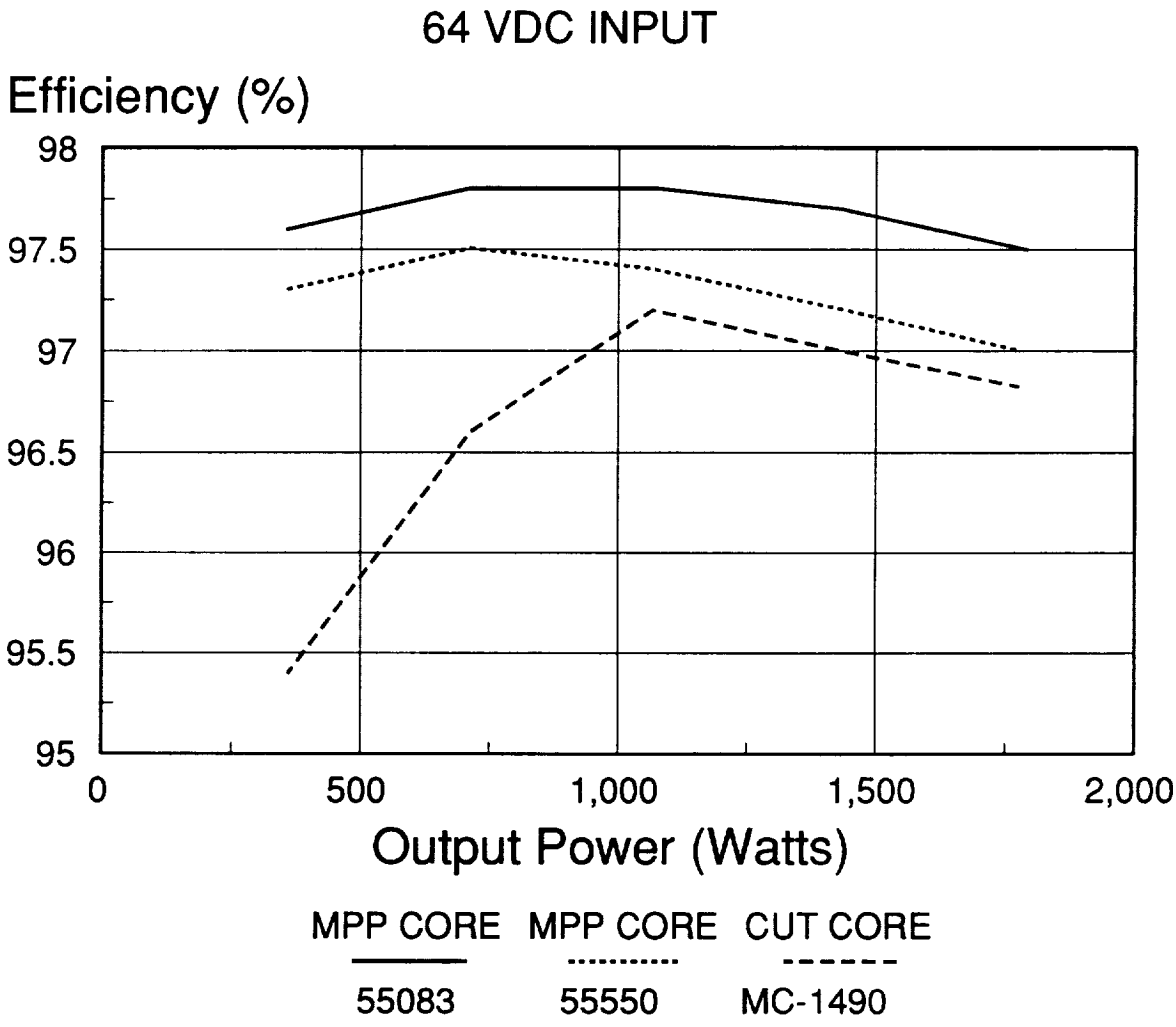


FIG. 2-3 COMPARISON OF FOUR MODULE BOOST EFFICIENCY WITH DIFFERENT INDUCTOR CORES

The final design selected was the 55550 core. It was felt that the lighter weight was worth the small drop in efficiency from the 55083 core.

2.2 OUTPUT FILTER DESIGN

Fig. 2-4 shows the four module boost power stage. The four modules feed into a common first stage capacitor and secondary filter. The bus capacitor serves as the second stage capacitor. If the modules are not multiphased, the RMS current in the first stage capacitor is given by:

$$I_{Corms} = \frac{I_o}{(1-D)}\sqrt{D(1-D)} \tag{2.5}$$

A substantial reduction in the RMS ripple current in the first stage capacitor is achieved by phasing the modules by 90 degrees. Then the RMS ripple current in the output capacitor is given by:

$$I_{Corms} = \frac{I_o}{(1-D)}\sqrt{D(1/4-D)} \quad 0 \le D \le 0.25 \tag{2.6}$$

$$= \frac{I_o}{(1-D)}\sqrt{-D^2+3/4D-1/8} \quad 0.25 \le D \le 0.5 \tag{2.7}$$

$$= \frac{I_o}{(1-D)}\sqrt{-D^2+5/4D-3/8} \quad 0.5 \le D \le 0.75 \tag{2.8}$$

Fig. 2-5 compares the ripple current in the output capacitor for an 1800 W, 120 V boost converter where the input voltage varies between 60 V and 90 V. With multiphasing, the peak

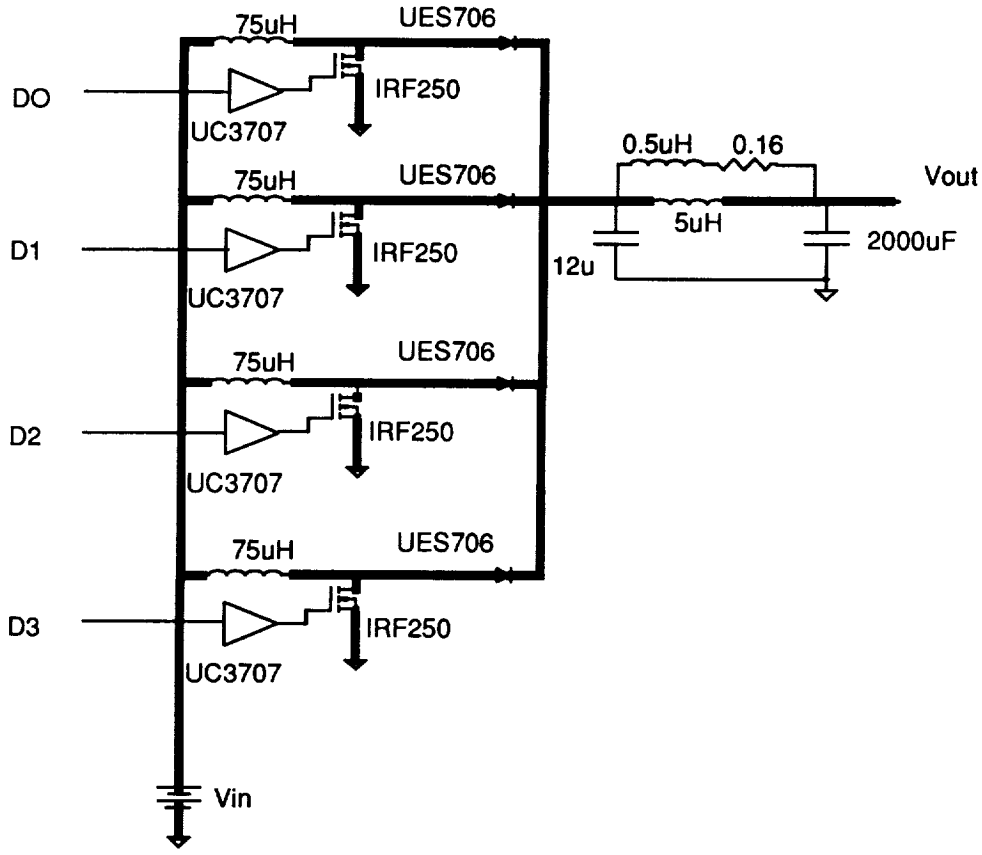


FIG. 2-4 MULTI-MODULE BOOST POWER STAGE

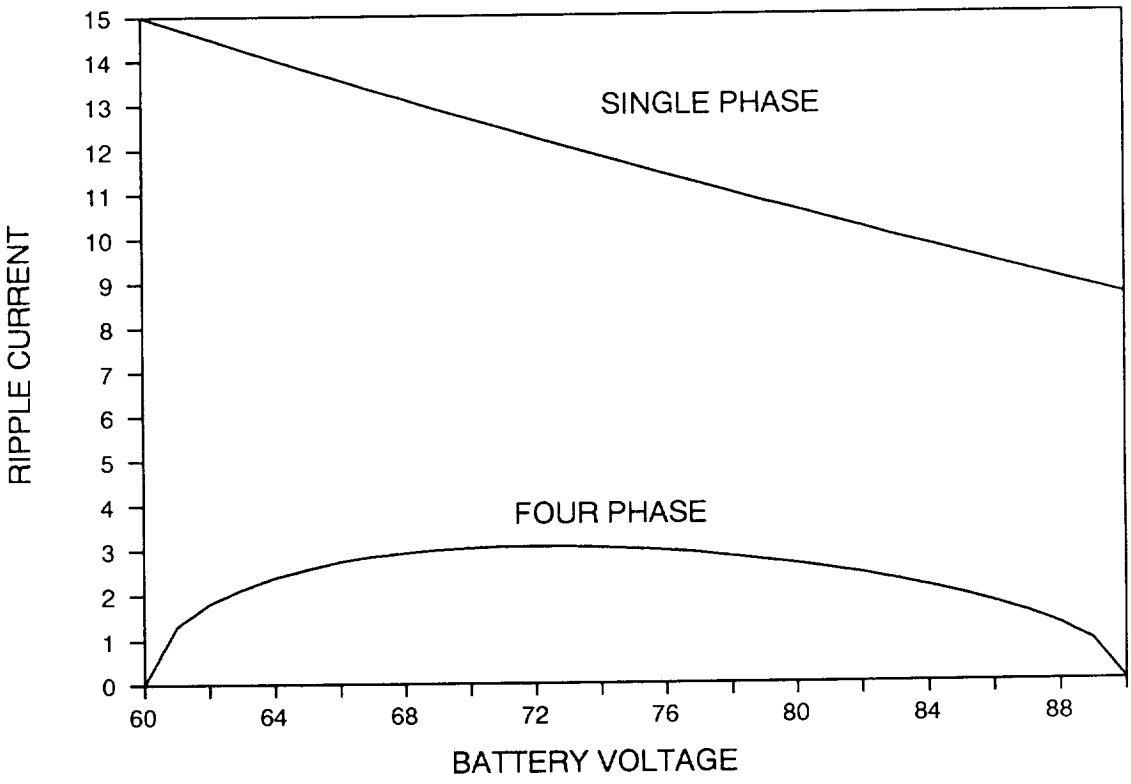


FIG. 2-5 COMPARISON OF CAPACITOR RIPPLE CURRENT

ripple current occurs at the 60 V input voltage and is 15 A. With multiphasing, the peak ripple current occurs at an input voltage of 72 V and is only 3.8 A. This can significantly reduce the size of the output filter.

Fig. 2-6 shows a schematic of the damped secondary output filter. Under the following conditions:

1) $L_2 >> L_1$

2) $\frac{L_1}{R} >> RC_1$

Then the resonant frequency and Q of the filter are given by:

$$\omega_o = \frac{1}{\sqrt{L_1 C_1}} \tag{2.9}$$

$$Q = \frac{1}{\omega_o C_1 R} \tag{2.10}$$

The advantage of this configuration is that the secondary resonance is independent of the bus capacitance and load capacitance. The first stage capacitor bank, C_1, is comprised of 12 μF of polypropylene capacitors sized to handle the RMS ripple current. L_1 is selected as 0.5 μH to place the resonance at about 60 kHz, a third of the 180 kHz ripple frequency. L_2 is selected as 5.0 μH to be 10 times larger than L_1. The resistor, R, is design to be 0.15 Ω in order to make the Q slightly greater than 1 to avoid peaking in the loop gain. The bus capacitor is approximately 2000 μF of aluminum capacitors. Although aluminum capacitors are not approved for flight use, they are electrically similar to the wet slug (CLR35) type capacitors which are flight approved. Upon advice from NASA, VPEC constructed the bus filter from aluminum capacitors to minimize costs.

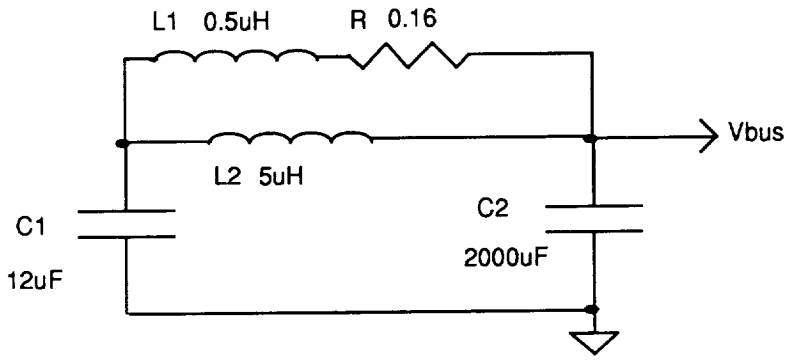


FIG. 2-6 DAMPED SECONDARY OUTPUT FILTER

2.3 DISCRETE PWM DESIGN

Several PWM integrated circuits are available for use in spacecraft applications, including some that support current-mode control. However, there are several problems with using a PWM integrated circuit in this application. With four modules operating out of phase an external oscillator will be needed to synchronize the PWM's. Hence the internal oscillator will be unused. Also, the comparator input of all PWM integrated circuits has only a small linear range, usually only about 2 V. When using current-injection-control over a wide load range, severe limitations are placed on the current sense gain just to ensure that the signal will be within the linear range of the comparator. This necessitates a small current sense gain making the PWM sensitive to noise. A large offset variation in the ramp bias voltage exists between different IC's. It is desirable that the PWM ramp bias voltage of the four modules be a common voltage. This helps reduce the error in current-sharing between modules. In order to maximize the small-signal benefit of current-injection-control, one needs precise control over the slope of the external ramp. The ramp slope of all PWM integrated circuits cannot be controlled without also changing the switching frequency. Finally, a maximum duty cycle limit of 75% is desirable for each module. PWM integrated circuits are not easily programmed with such a low duty cycle limit.

A discrete four phase pulse-width-modulator circuit is designed with the following features:

1) 10 V linear range on the PWM comparator,

2) easy interface to a CIC signal,

3) common bias voltage to reduce variations in the duty cycle,

4) precise 75% maximum duty cycle limit,

5) easy control of the external ramp slope without affecting the operating frequency, and

6) latching mechanism to eliminate chattering.

Fig. 2-7 shows a schematic of the four phase clock generator. A CMOS 555 timer outputs a 180 kHz square wave to a CD4017 Johnson counter. A set/reset latch divides the 180 kHz into four phases of 45 kHz, each having a 25% duty cycle. Fig. 2-8 shows the discrete four phase pulse-width-modulator. A high signal on the phase signal shorts the ramp capacitor and turns off the duty cycle output. When the phase signal goes high, the ramp capacitor is charged with a constant current source determined by the common zener voltage Va and resistor Rt. The D flip-flop is also clocked into the active low state, turning on the duty cycle output. When the summed ramp signal and CIC signal reaches the error signal, the comparator output goes high, seting the D flip-flop. Repetitive switching of the comparator will not effect the flip flop state until the next cycle.

2.4 PROTECTION CIRCUIT DESIGN

The four module boost converter contains undervoltage, overvoltage, overcurrent and soft-start protection circuitry. A schematic is shown in Fig. 2-9. The switch current in each channel is sensed and compared with a reference. The output of the comparator is logically ored with the PWM comparator output for each of the four channels.

To protect against an open mode control signal, the four module boost converter also has overvoltage protection. Output voltage is sensed at the output of the ORU and is compared with the reference. If the output voltage exceeds 130 V, the comparator output goes high forcing each of the PWM outputs low. There is a two volt hysteresis.

For smooth starting, battery voltage is sensed and compared with the reference. At battery voltages below 50 V, the comparator output is low, which holds down the error signal, keeping all channels off. When the battery voltage exceeds 50 V, the error signal is slowly increased through the soft start capacitor until it is back-biased.

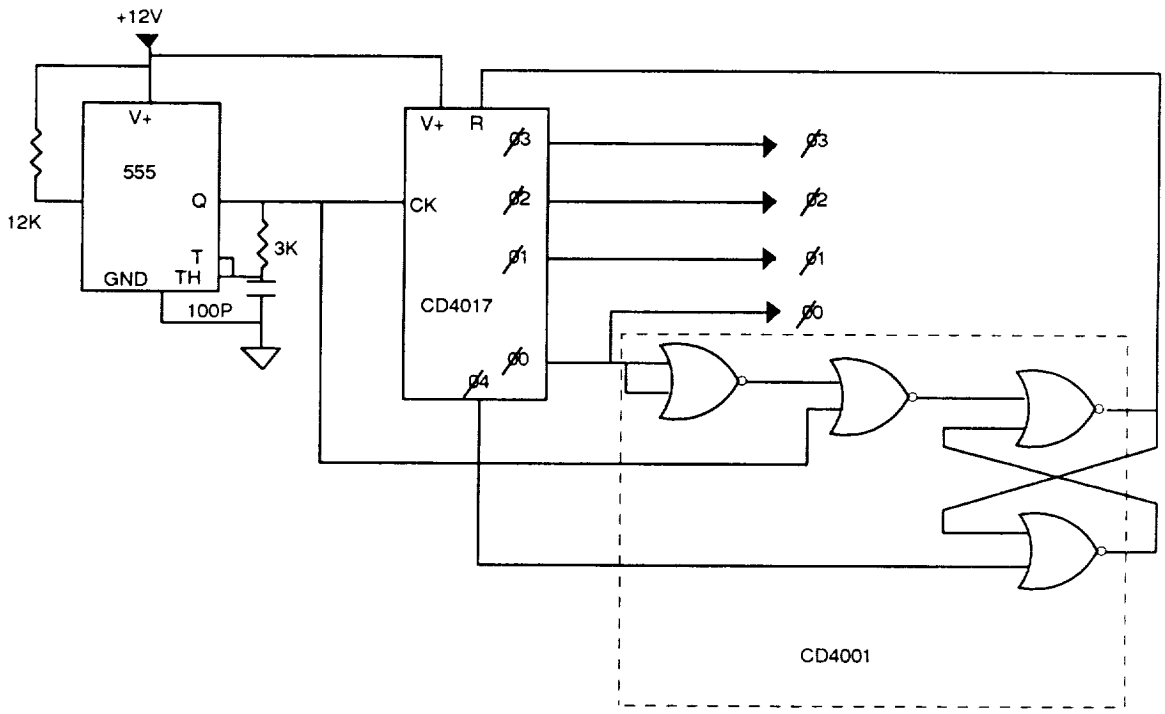


FIG. 2-7 FOUR PHASE CLOCK GENERATOR

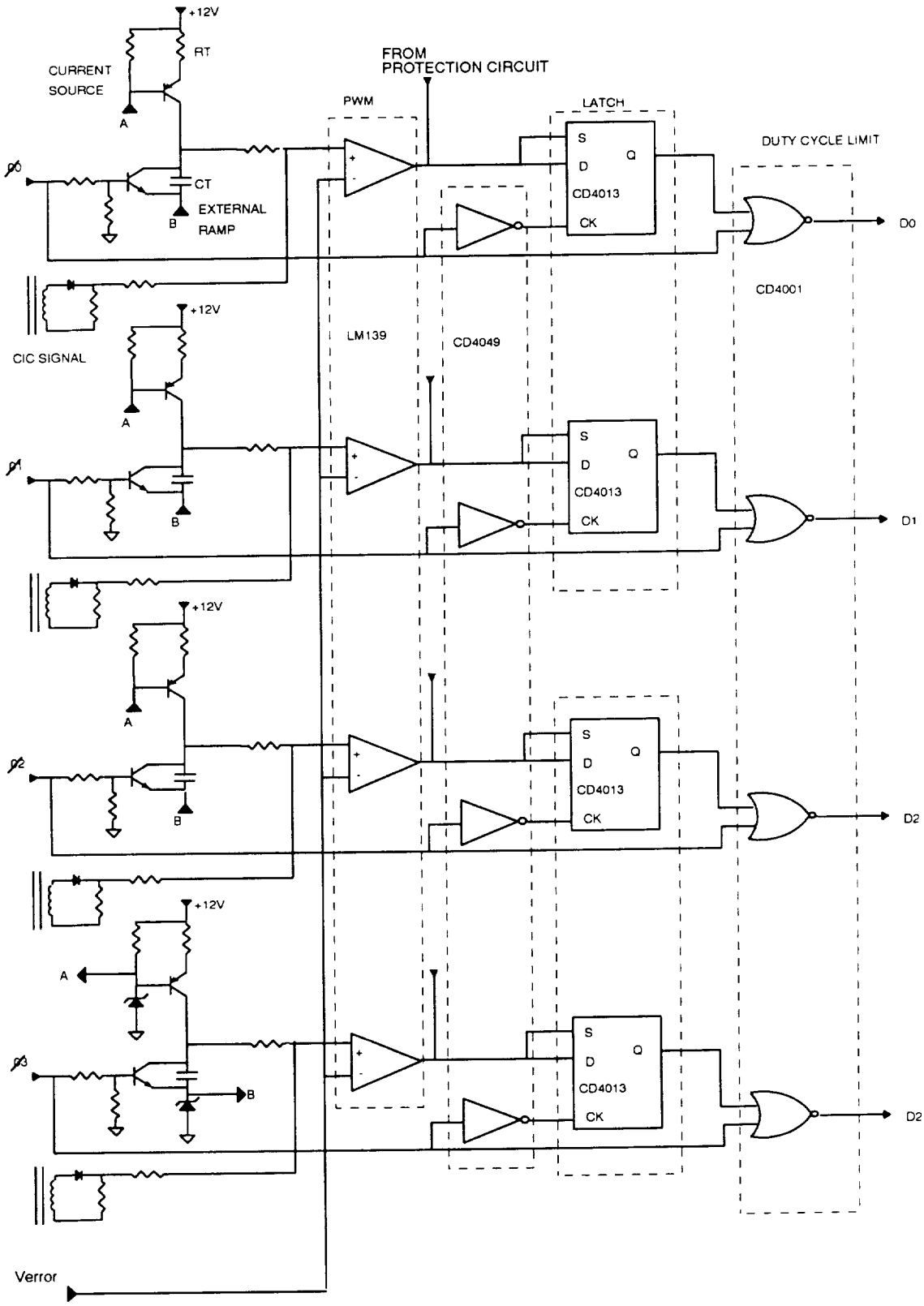


FIG. 2-8 DISCRETE FOUR PHASE PWM

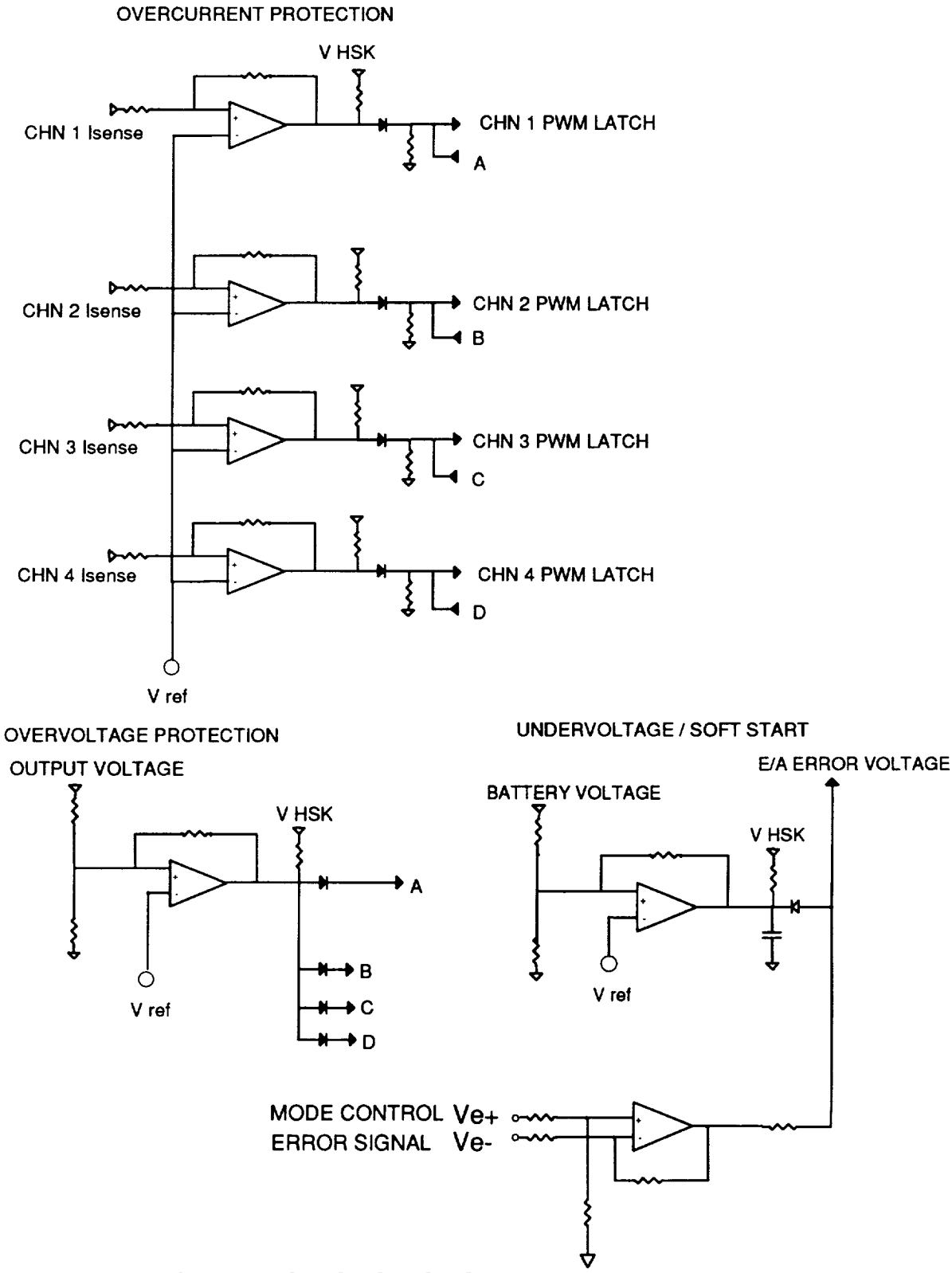


FIG. 2-9 PROTECTION CIRCUITRY

2.5 CONTROL LOOP DESIGN

The four module boost battery discharger employs current-mode control in order to ensure current sharing between modules, to improve the dynamic characteristics, and to provide a means for overcurrent protection. Recent analysis of current-mode control [3] has shown that the relative slopes of the current sense waveform and the external ramp waveform have a powerful impact on the control-to-output small-signal characteristics of a power converter. Current-mode control introduces a double pole at one-half of the switching frequency. The Q of this double pole is determined by the external ramp slope. With no external ramp and operation above 50% duty cycle, the Q becomes negative, causing the system to experience a subharmonic oscillation. The discrete PWM of the four module boost converter is specifically designed in order to allow high flexibility in selecting the external ramp slope and the current sense gain.

The four module boost converter operates in the discontinuous inductor current mode at power levels below 1200 W. This is unusually high for an 1800 W power converter, but was selected to keep the inductor weight to a minimum. Recent analysis of current-mode control in the discontinuous mode [4,5] has shown that the dynamic performance of converters which operate in continuous and discontinuous modes of operation can be greatly enhanced with current-mode control.

Included is a discussion of the small-signal characteristics of the four module boost converter in both the continuous and the discontinuous modes of operation. A simple PSPICE model is presented incorporating the current-controlled model of the PWM switch [6].

2.5.1 Small Signal Characteristics

There are two primary considerations in the small signal characteristics of the four module boost converter. The system should be stable over all line and load conditions, and the system should meet output impedance specifications over all line and load conditions. Audio susceptibility is not a prime consideration since the input voltage is a battery and is not subject to AC perturbations. Output impedance is important for several reasons. A low output impedance will better reject load-induced voltage ripple from the bus. Also, transient response peaking is minimized by minimizing the output impedance over a broad range of frequencies. Finally, a low output impedance will allow the converter to handle a wider variety of complex loads without stability problems.

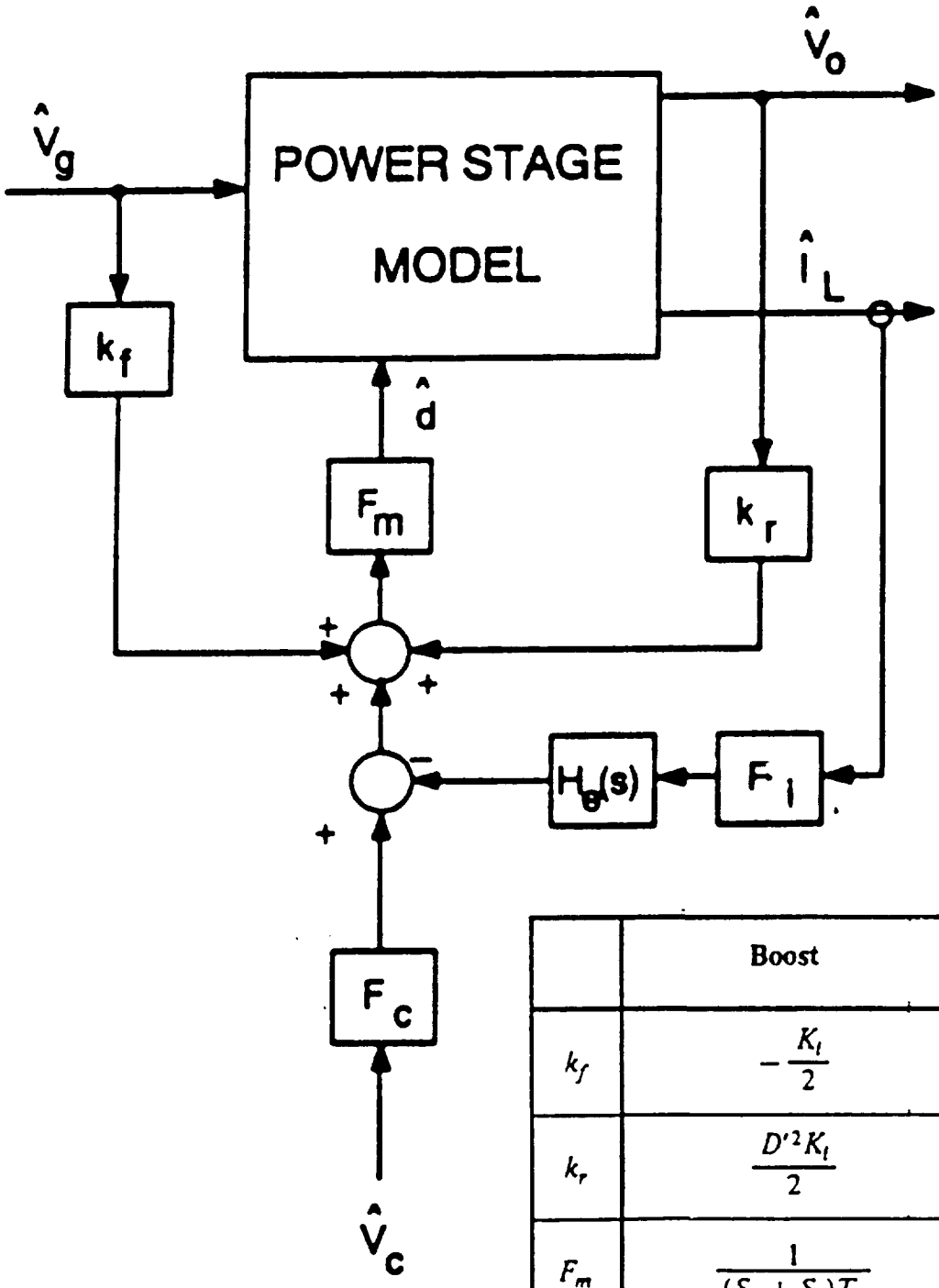
Included is a discussion of the loop gain stability analysis and output impedance analysis for the continuous and discontinuous mode four module boost converter.

2.5.1.1 Continuous Mode of Operation

Fig. 2-10 shows a block diagram of a single module, continuous mode, current-injection controlled power converter. The power stage model comes from the well-known state-space averaged model [7]. The block Kf accounts for the feedforward effect of the input voltage on the slope of the current sense waveform. The block Kr accounts for the feedback effect of the output voltage of the slope of the current sense waveform. The block He(s) forms a pair of complex right half plane zeroes at one-half the switching frequency to account for the sampling nature of the system. This new model predicts the second order effects of current-mode control, including the subharmonic oscillation at duty cycles above 50%.

The four module boost regulator can be analyzed as an effective single module system using an effective power stage inductance of one-fourth the inductance in each module [8]. This greatly simplifies the design of feedback controller.

2.5.1.1.1 PSPICE Modelling



	Boost
k_f	$-\frac{K_1}{2}$
k_r	$\frac{D'^2 K_1}{2}$
F_m	$\frac{1}{(S_n + S_e)T_s}$
F_c	1
$H_e(s)$	$1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}$ $\quad Q_z = \frac{-2}{\pi}$

$$K_1 = \frac{F_1 T_s}{L}$$

FIG. 2-10 Block Diagram Of CIC Converter

While the new model of current-mode control is effective for design and analysis, it is cumbersome to use in a circuit analysis program such as PSPICE. The current-controlled model of the PWM switch [6] is a simple means of implementing the new current-mode model in PSPICE. Fig. 2-11 shows how the switch, diode, current sense network, and external ramp can be effectively replaced with a linear network for easy modelling.

2.5.1.1.2 Control-to-Output Transfer Function Analysis

The control-to-output transfer function of the four module boost regulator with each of the current loops closed can be approximated as the product of three transfer functions:

$$\frac{\hat{v}_o}{\hat{d}} \cong F_p(s)F_h(s)F_o(s) \tag{2.11}$$

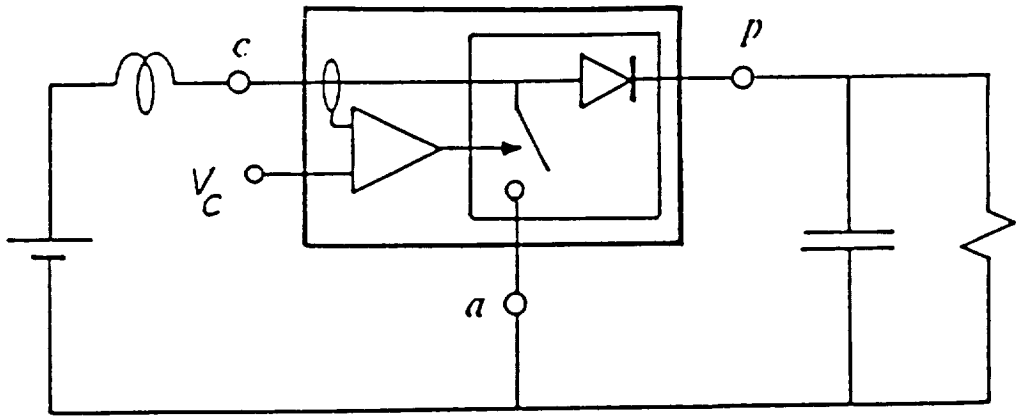
$F_p(s)$ is the power stage transfer function and is given by:

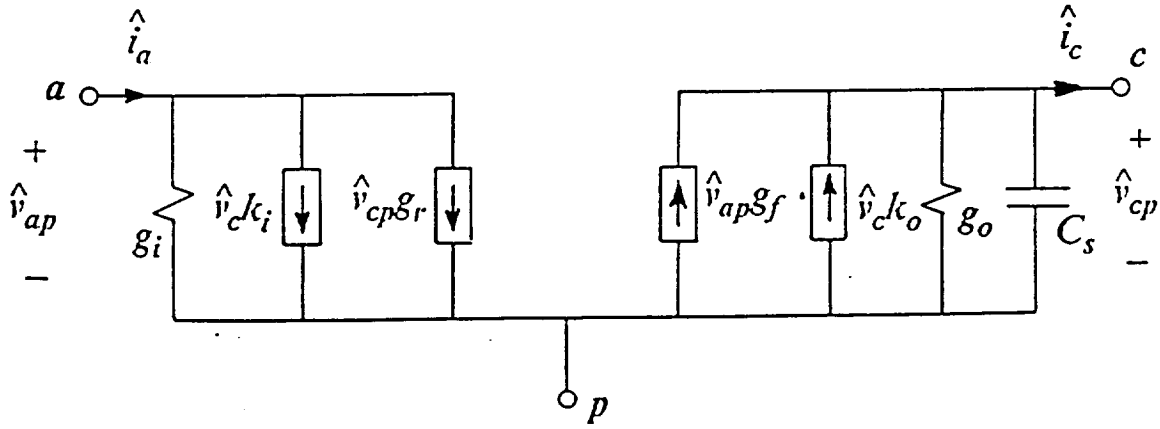
$$F_p(s) = \frac{R_L/2}{F_i/4} \quad \frac{(1 - s/\omega_a)(1 + sC_{bus}R_c)}{(1 + 2sC_{bus}R_L)} \tag{2.12}$$

where ω_a is a right-half-plane zero and is given by:

$$\omega_a = \frac{D'^2 R_L}{L/4} \tag{2.13}$$

$F_h(s)$ is the double pole introduced by the current loop and is approximated as:





$$k_i = \frac{D}{F_i} \qquad k_o = \frac{1}{F_i}$$

$$g_i = D\left(g_f - \frac{I_c}{V_{ap}}\right) \qquad g_o = \frac{T_s}{L}\left(D' \frac{S_e}{S_n} + \frac{1}{2} - D\right)$$

$$g_r = \frac{I_c}{V_{ap}} - g_o D \qquad g_f = D g_o - \frac{DD' T_s}{2L}$$

FIG. 2-11 Current-Controlled Model of The PWM Switch

$$F_h(s) \cong \frac{1}{1 + \frac{s}{\omega_n Q_i} + \frac{s^2}{\omega_n^2}} \tag{2.14}$$

where

$$Q_i = \frac{1}{\pi(m_c D' - 0.5)} \tag{2.15}$$

and

$$m_c = 1 + \frac{S_e}{S_n} \tag{2.16}$$

$F_o(s)$ is the double pole of the secondary output filter defined previously.

Fig. 2-12 shows the theoretical and experimental control-to-output transfer of the four module boost converter for increasing values of the external ramp slope. It is seen how the Q of the double pole at one-half of switching frequency is effectively damped for increasing external ramp slope.

2.5.1.1.3 Output Impedance Analysis

The output impedance of the four module boost regulator with each of the current loops closed can be approximated as:

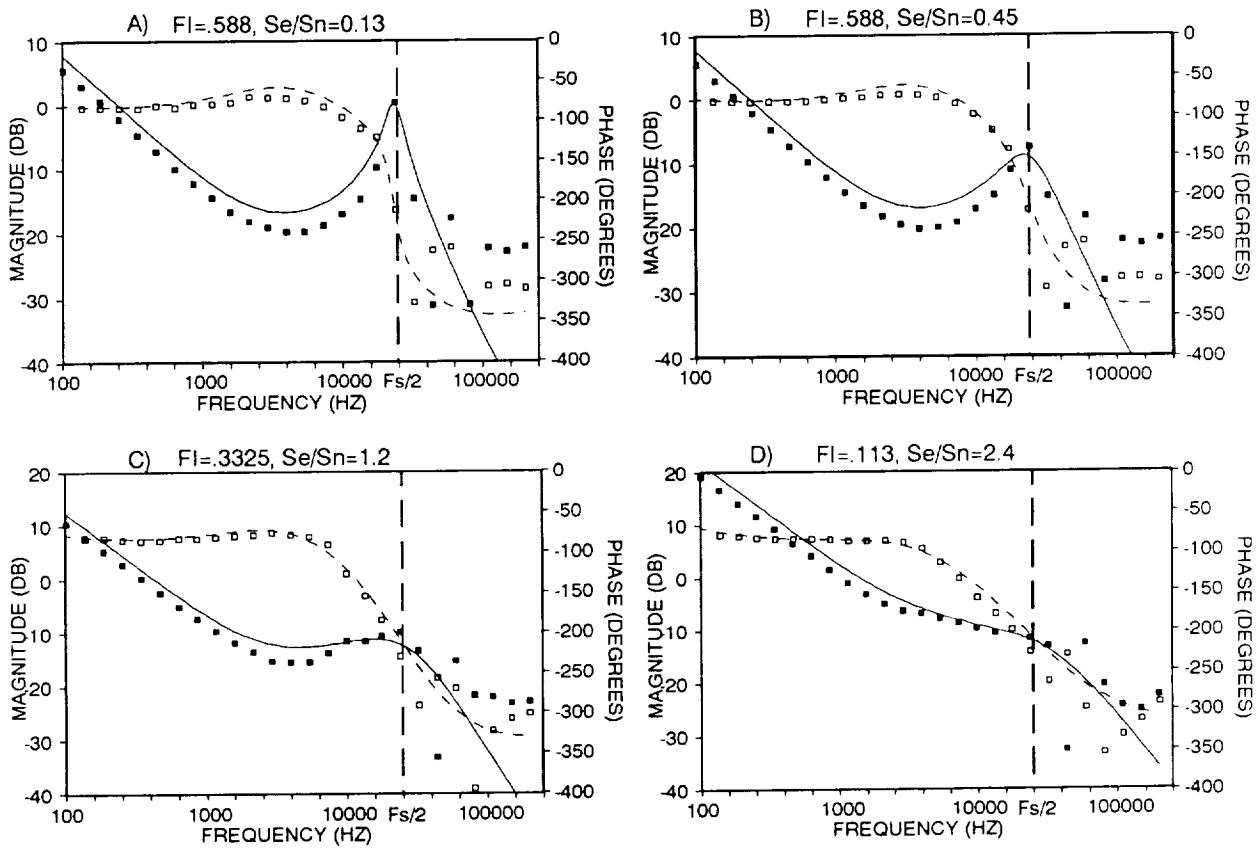


FIG. 2-12 CONTROL-TO-OUTPUT TRANSFER FUNCTION
CURRENT LOOP CLOSED

$$\frac{\hat{v}_o}{\hat{i}_o} = \frac{R_L}{2} \frac{(1 + sC_{bus}R_c)}{(1 + 2s/R_L)} \tag{2.17}$$

Current-mode control raises the low frequency output impedance of the converter, causing the converter to behave as a current source. However, the resonant peaking in the output impedance, which is characteristic of single-loop control, is no longer apparent.

2.5.1.2 Discontinuous Mode of Operation

A new model of current-mode control has also been formulated for the discontinuous mode of operation [4]. There the inductor current ceases to be a state with memory from cycle to cycle. At the start of each switching cycle, the inductor current always starts from zero. The state of the inductor current can be inferred by knowledge of the input voltage and inductance only. Hence the model of current-mode control in the discontinuous mode of operation does not contain a current loop. It only contains a feedforward gain input voltage. Fig. 2-13 shows the model of current mode control for discontinuous mode of operation. Since there is no input filter, and audio susceptibility is not a concern, the feedforward term can be ignored. Hence the discontinuous mode model for current-mode control is almost identical to the discontinuous mode model for single-loop control. The only difference is in the modulator gain, which is a function of the current sense slope.

2.5.1.2.1 PSPICE Modelling

The discontinuous mode model of the PWM switch [9] is employed to form the PSPICE model of the four module boost converter.

2.5.1.2.2 Loop Gain Stability Analysis

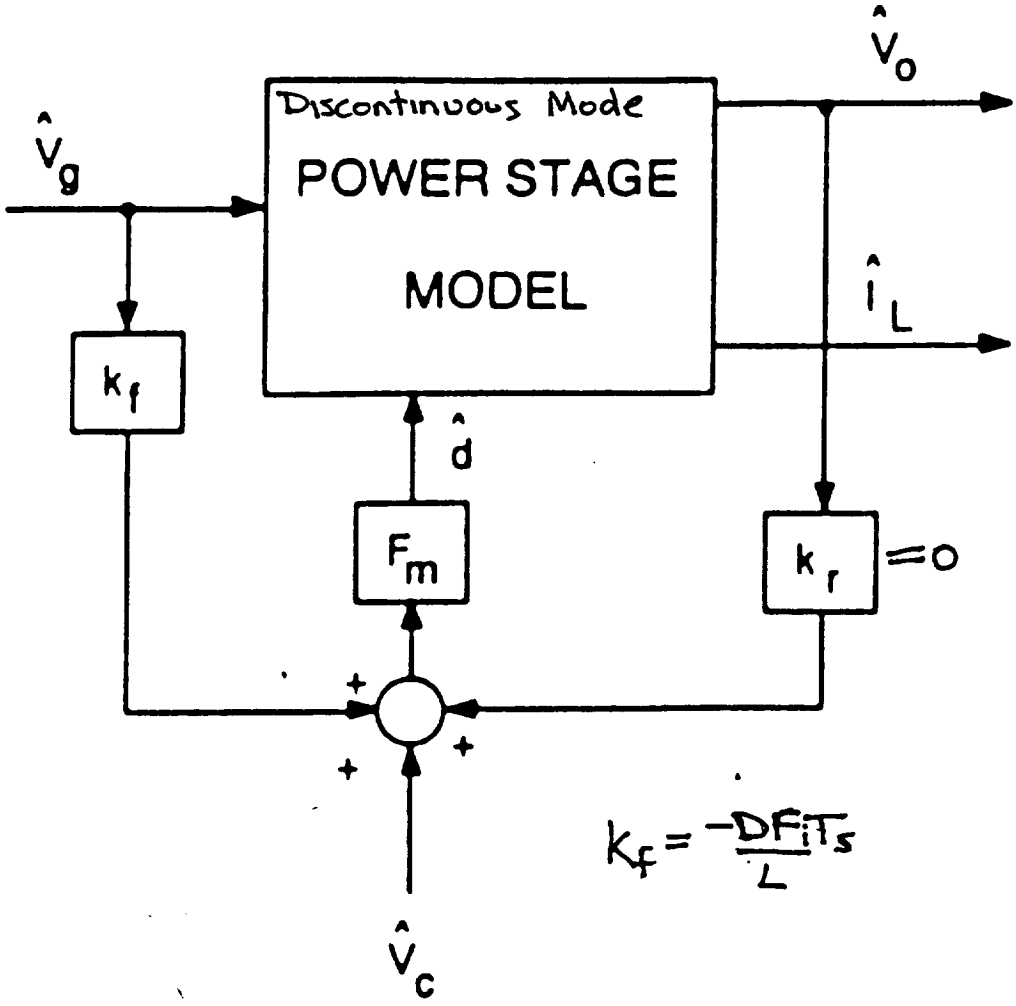


FIG. 2-13 Discontinuous Mode CIC Model

When using single-loop control, the control-to-output transfer function of a boost regulator in the continuous mode of operation contains a double pole at the resonant frequency, a right-half-plane zero, and an ESR zero. In the discontinuous mode, the double pole splits into a low frequency pole and a very high frequency pole, the right-half-plane zero moves to a high frequency, and the ESR zero remains the same.

Unlike current-mode control in the continuous mode of operation, the control-to-output transfer function in the discontinuous mode is dependent on the modulator gain, F_m. The control-to-output transfer function of the four module boost regulator with each of the current loops closed in the discontinuous mode can be approximated as:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{H_d F_m (1 + s/\omega_{zc})(1 - s/\omega_{a1})}{\Delta_1} \tag{2.18}$$

where:

$$H_d = \frac{2V_o(M-1)}{D(2M-1)} \tag{2.19}$$

M is the voltage conversion ratio, V_o/V_i, of the four module boost converter in the discontinuous mode of operation and is given by:

$$M = \frac{1 + \sqrt{1 + \frac{2D^2}{\tau_L}}}{} \tag{2.20}$$

where τ_L is the effective inductor time constant and is given by:

$$\tau_L = \frac{L/4F_s}{R_L} \tag{2.21}$$

ω_{a1} is the right-half-plane zero and is given by:

$$\omega_{a1} = \frac{R_L}{M^2 L/4} \tag{2.22}$$

Δ_1 represents the double complex pole denominator that splits into two real poles, one at a low frequency and one at a high frequency.

$$\Delta_1 = (1 + s/\omega_{p1})(1 + s/\omega_{p2}) \tag{2.23}$$

where ω_{p1} is the low frequency pole and is given by:

$$\omega_{p1} = \frac{1}{R_L C} \frac{2M - 1}{M - 1} \tag{2.24}$$

ω_{p2} is the high frequency pole and is given by:

$$\omega_{p2} = 2F_s \left(\frac{1 - 1/M}{D} \right)^2 \tag{2.25}$$

The right-half-plane zero, ω_{a1}, and the high frequency pole, ω_{p2}, are beyond twice the switching frequency. However, since they both result in additional phase lag, their effect can be seen in the loop gain at one-fifth of the switching frequency.

2.5.1.2.3 Output Impedance Analysis

The open loop output impedance in the discontinuous mode of operation is given by:

$$\frac{\hat{v}_o}{\hat{i}_o} = \frac{R_L(M-1)}{(2M-1)} \frac{(1+s/\omega_{zc})}{(1+\omega_{p1})}$$

Unlike single-loop control, the output impedance in the discontinuous mode of operation is very similar to the output impedance in the continuous mode of operation. This provides a smooth transition in the dynamic characteristics when crossing that boundary. It also greatly improves the no-load to full-load transient response.

2.5.2 Current Sense Design

Switch current is sensed in each module with a current transformer and half-wave rectifier and load resistor as shown in Fig. 2-14. The transformer contains 170 turns of #28 AWG wire around a 58076-1 supermalloy tape wound core. This is chosen for its low magnetizing current. A sense resistor of 100Ω is selected, The gain of the current sense, F_i, is given by:

$$F_i = \frac{R_s}{N_t} \times \frac{R_1}{R_1 + R_2} = 0.12 \qquad (2.26)$$

The slope of the sensed switch current, S_n, is given by:

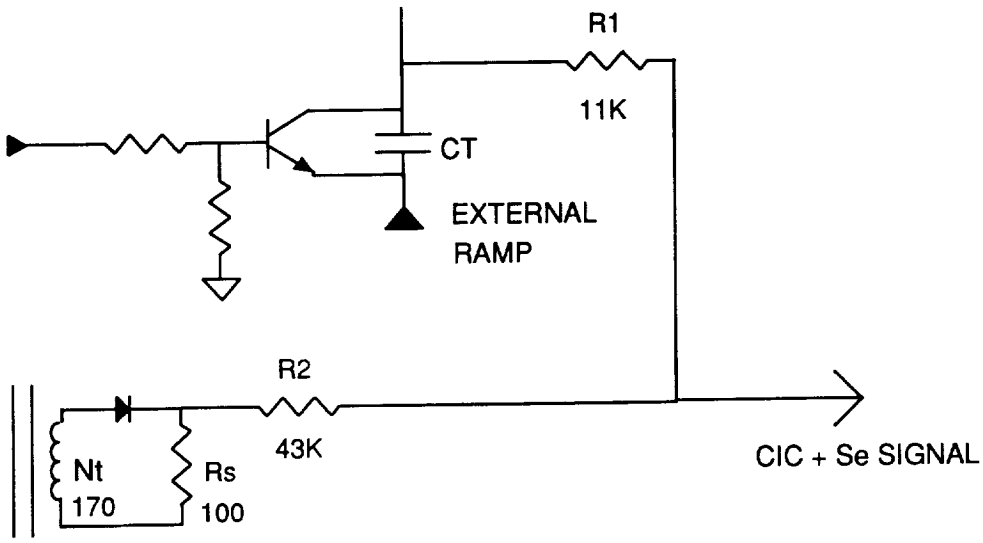


FIG. 2-14 CURRENT SENSE CIRCUIT

$$S_n = \frac{V_i F_i}{L} \tag{2.27}$$

The minimum slope to the current sense signal occurs at the minimum line voltage where the slope is approximately 8.6×10^4 V/s.

2.5.3 External Ramp Design

As previously described, the external ramp slope has a powerful impact on the peaking of the double pole at one-half of the switching frequency when operating in the continuous mode of operation. As shown in Fig. 2-12d, a large external ramp can cause the double pole to split into two real poles where one goes towards the origin and the other goes towards infinity. If selected properly, the lower frequency pole can cancel the power stage ESR zero, thus minimizing the phase lag in the control-to-output transfer function. This can be useful in optimizing the converter in the continuous mode of operation.

However, the external ramp slope also plays a significant but somewhat different role in the discontinuous mode of operation. There is no double pole at one-half of the switching frequency in the discontinuous mode. However, unlike the continuous mode, the control-to-output transfer function in the discontinuous mode of operation is a function of the modulator gain, F_m. The modulator gain is given by:

$$F_m = \frac{1}{(S_e + S_n)T_s} \tag{2.28}$$

A larger external ramp slope, S_e, relative to the sensed inductor slope, S_n, causes a reduction in the modulator gain. This will reduce the control-to-output transfer function gain in the discontinuous mode only, with a corresponding reduction in the loop gain. This can greatly increase the discontinuous mode output impedance. To optimize the external ramp slope for both the continuous and discontinuous modes requires as little slope as possible to avoid peaking in the loop gain in the continuous mode. This will result in the smallest loop gain reduction in the discontinuous mode. From Eq. (2.15), the maximum Q of the double pole at half the switching frequency in the continuous mode occurs at the minimum line voltage and is given by:

$$Q_{imax} = \frac{1}{\pi(D'_{\min}(1 + S_e/S_{nmin}) - 0.5)} \tag{2.29}$$

The system is designed so that the maximum Q = 1.2 at an input voltage of 53 V. This yields an external ramp slope of 6.25×10^4 Fig. 2-15 shows a photograph of the summed external ramp signal with the current sense signal.

2.5.4 Voltage Loop Design

The voltage loop feedback compensation network is shown in Fig. 2-16. This operation amplifier connection contains two poles and one zero. The first pole is placed at the origin in order to obtain tight DC regulation. The second pole is placed to cancel the ESR zero. The zero is placed in order to obtain the necessary phase boost in the loop gain. Finally, the integrator gain is selected in order to cross-over 0 db in the loop gain with acceptable phase margin.

2.6 THEORETICAL AND EXPERIMENTAL RESULTS

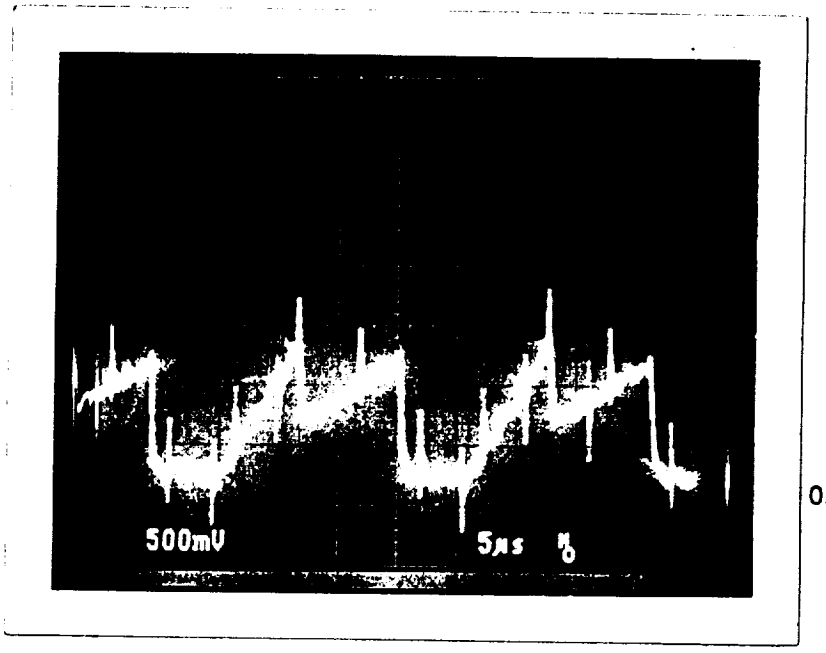


FIG. 2-15 PHOTOGRAPH OF SUMMED EXTERNAL RAMP WITH CURRENT SENSE SIGNAL

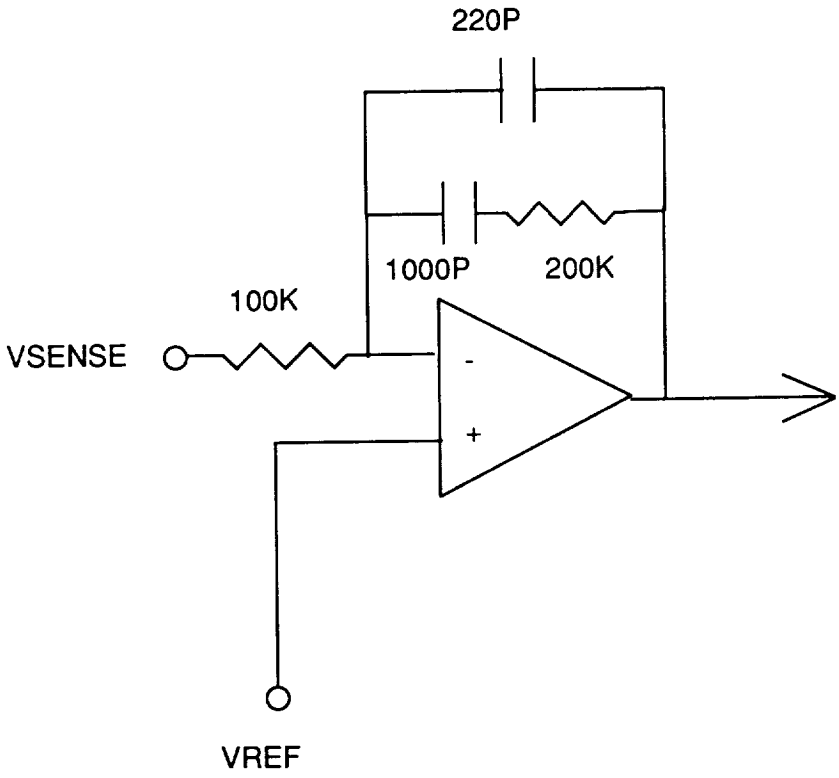


FIG. 2-16 VOLTAGE LOOP COMPENSATION

The small-signal and large-signal characteristics of the four module boost regulator were evaluated both theoretically and experimentally. Small-signal measurements include loop gain stability and output impedance over a wide range of load conditions. These measurements were performed prior to and after placement of a 20 foot cable from the discharger output to the bus capacitor. Large-signal measurements include the load transient response going from no load to max load and max load to no load, as well as the EMI characteristics.

2.6.1 Small-Signal Loop Gain and Output Impedance

Loop gain stability was measured by injecting a transformer-coupled AC signal into the loop. Fig. 2-17 shows the four module boost converter theoretical and experimental loop gain bode plot at four different load conditions: 15 A, 8.3 A, 4.5 A, and 1 A. The input voltage is 64 V. The solid line is the theoretical prediction, and the dots are the experimental measurement. There is excellent agreement between the prediction and measurement. The converter is in the discontinuous mode of operation for all the measurements except the 15 A load condition. The 0 db cross-over frequency ranges from about 4 kHz at the 15 A load condition to 800 Hz at the 1 A load condition. The worst case phase margin occurs at the 1 A load condition and is 45 degrees. The worst case gain margin occurs at the 15 A load condition and is about 10 db.

Output impedance was measured by injecting a sinusoidal current load disturbance on the four module boost converter output. Fig. 2-18 shows the theoretical and experimental output impedance under the same conditions. The output impedance is plotted on a log scale referenced to db ohms (0 db = 1 Ω, -20 db = 0.1 Ω). The phase of the output impedance is also presented because of its importance in evaluating the system stability when the converter is powering the complex loads of the spacecraft. There is excellent agreement between the theory and prediction. The peak output impedance at the 15 A load condition is about -26 db = 50 *m*Ω. At a 1A load, the output impedance peaks at about -15 db = 178 *m*Ω.

FIG. 2-17 THEORETETICAL AND EXPERIMENTAL LOOP GAIN

64 V INPUT

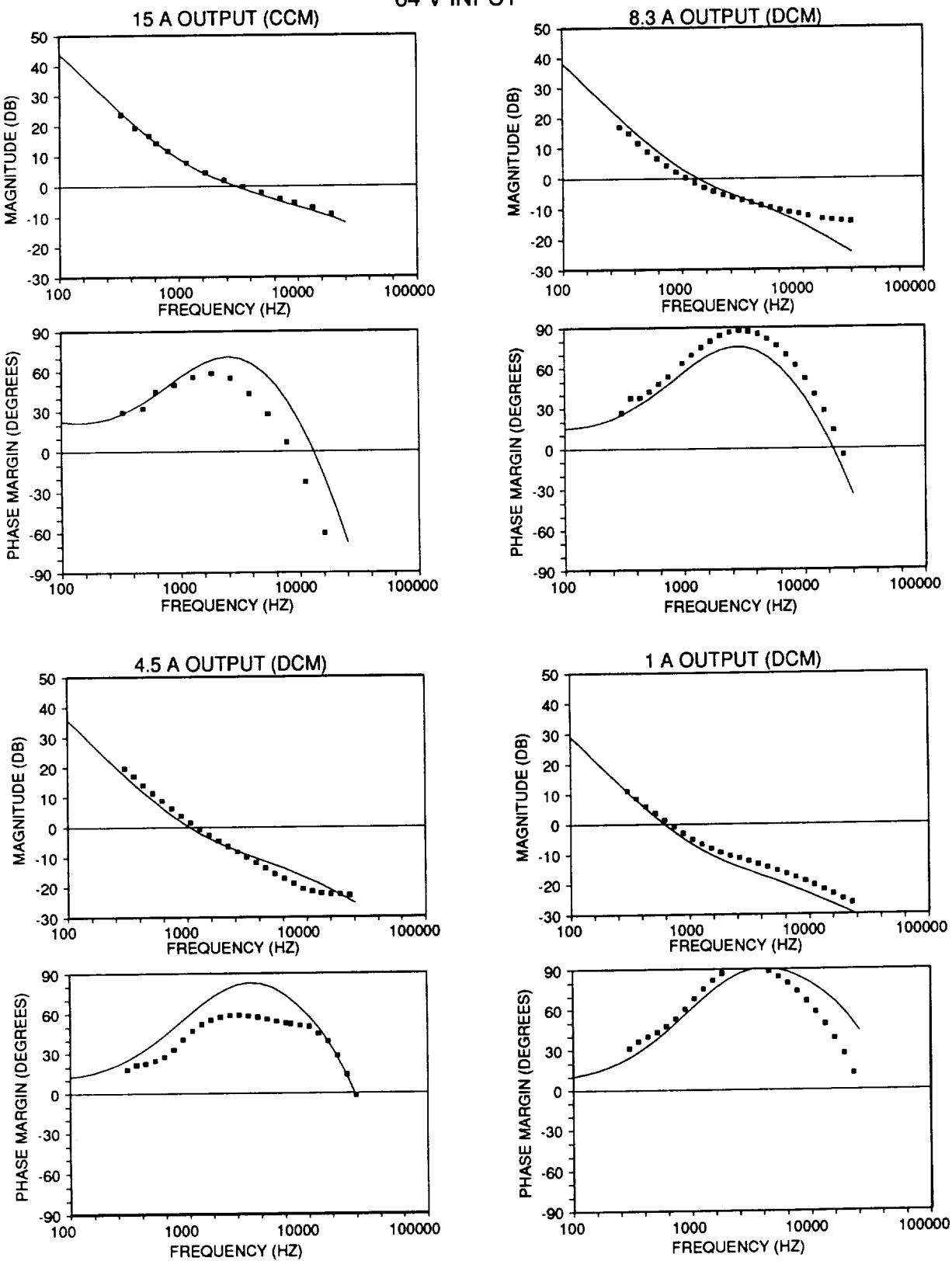
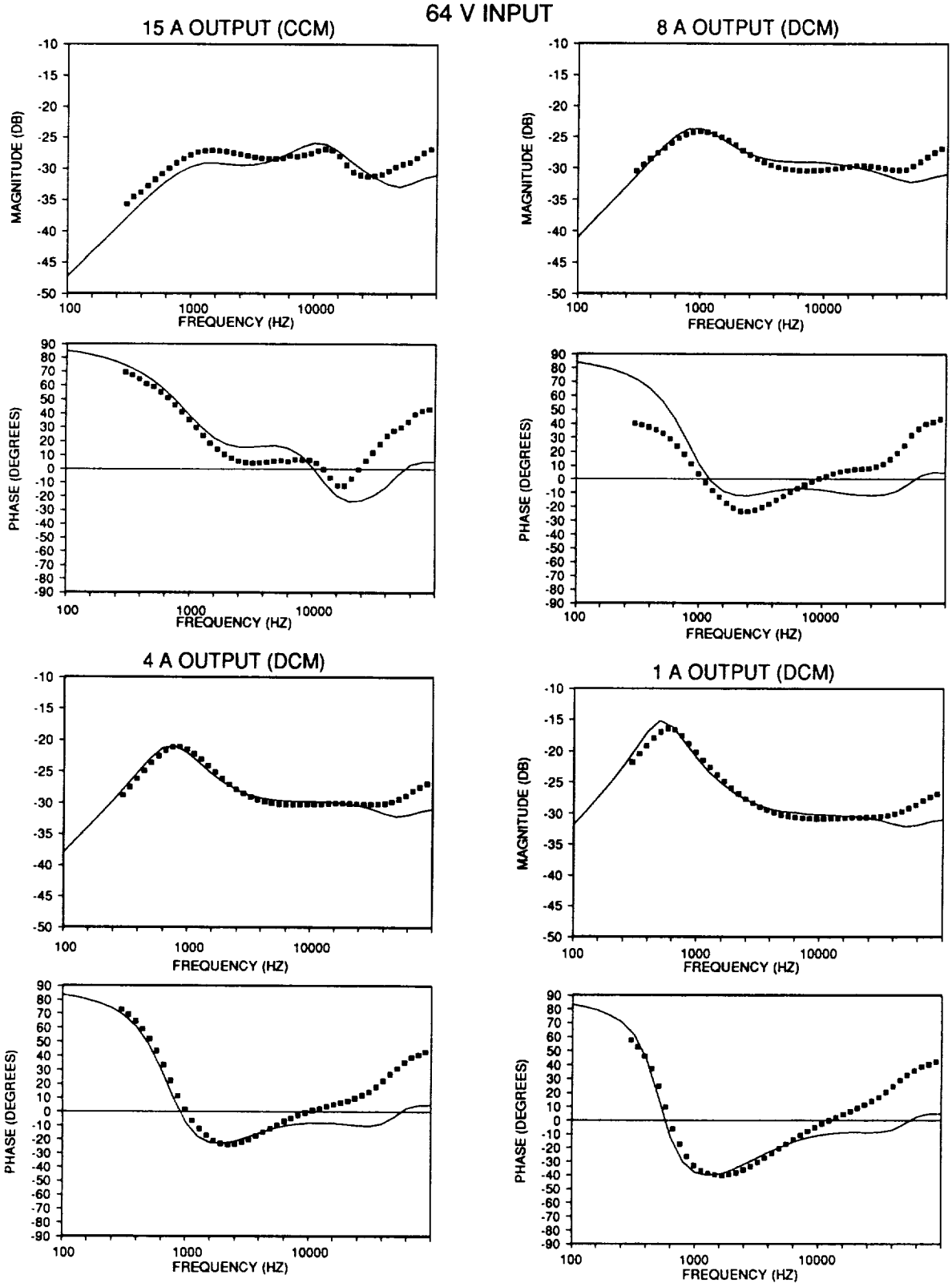


FIG. 2-18 THEORETICAL AND EXPERIMENTAL OUTPUT IMPEDANCE

64 V INPUT



2.6.2 Large-Signal Step Load Response

The four module boost converter was excited with a no-load to full load instantaneous step. This is much worst than the worst case transient that appears on the spacecraft bus. Fig. 2-19 shows two photographs of a large transient load. The top photograph shows a load step going from 15 A to 1.2 A back to 15 A. The top trace shows the current step at 5 A/Div. The second trace shows the output voltage at 1 V/Div., AC coupled. The third trace shows the switch current sense waveform of one of the four modules at 5 V/Div. When going from 15 A to 1.2 A, the output voltage experiences a positive peaking of about 1 V. At that point, the current sense waveform goes to zero, indicating that there is no switching being performed. The output voltage droops according to the the load current and output capacitance. When the output voltage droops to the regulation point (about 2 msec later), switching commences again with a minor overshoot in the current sense waveform. Following is an instantaneous load transient back to 15 A. The output voltage peaks down about 1 V and responds back to the regulation point within 800 μsec. The transient response time is determined by the zero in the voltage compensation.

This transient response is compared against a simulation under the same conditions. Fig. 2-20 shows the simulated 15 A to 1.2 A transient response. The bus voltage response and current sense response are in excellent agreement with the experimental result.

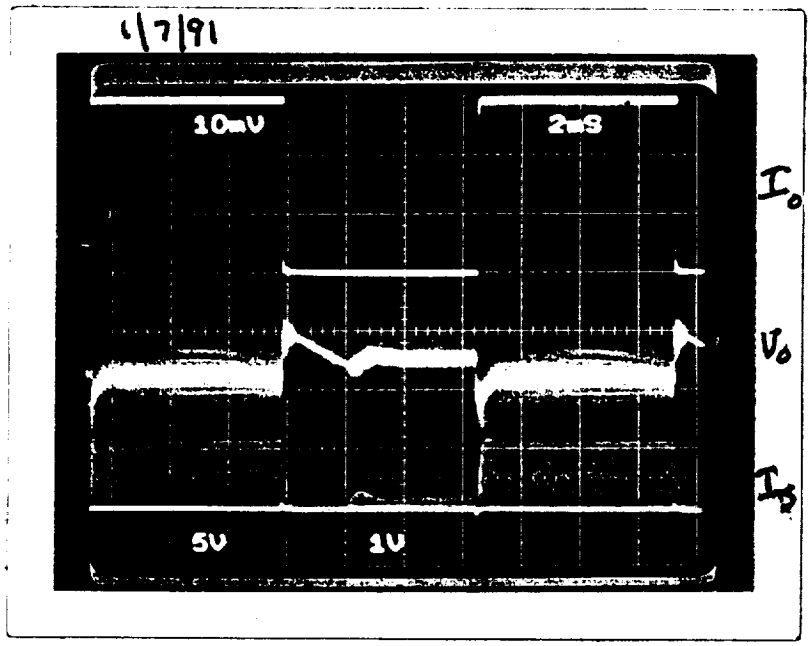
The second photograph of Fig. 2-21 shows a transient from 15 A to 5 A back to 15 A. Since the switch current does not drop to zero, this transient remains with the linear range of the converter. Hence both the positive transient and the negative transient are symmetrical.

2.6.3 EMI Characteristics

FIG. 2-19

TRANSIENT RESPONSE (NO CABLE LENGTH)

Vbatt = 64 V, 0 TO 15 A LOAD STEP



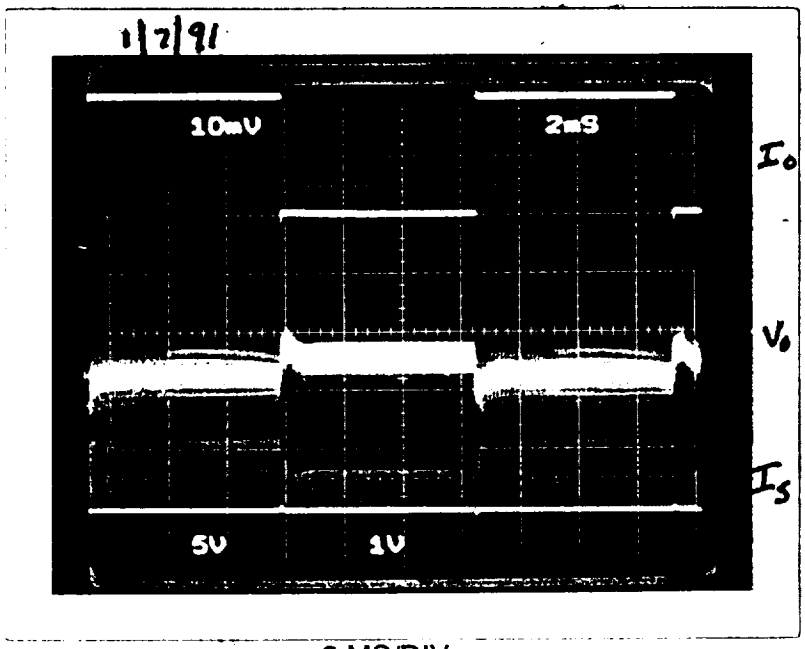
OUTPUT CURRENT 5A/DIV

OUTPUT VOLTAGE 1V/DIV

CURRENT SENSE 5V/DIV

2 MS/DIV

Vbatt = 64 V, 5 TO 15 A LOAD STEP



OUTPUT CURRENT 5A/DIV

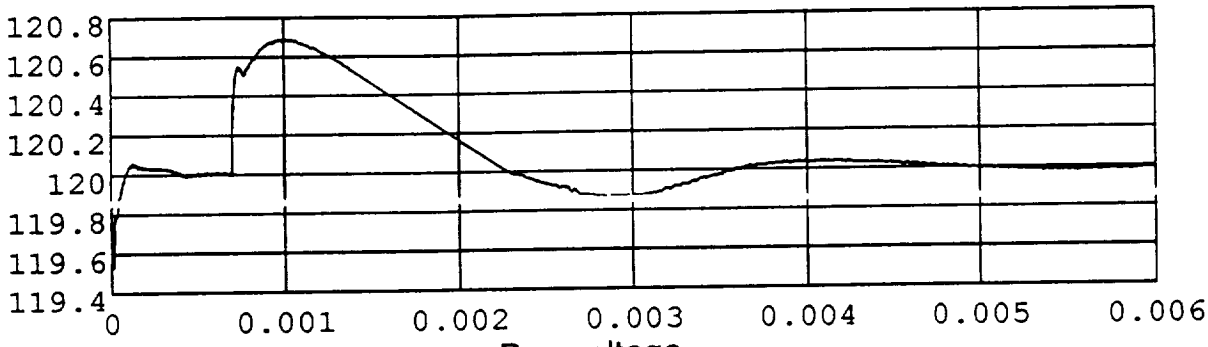
OUTPUT VOLTAGE 1V/DIV

CURRENT SENSE 5V/DIV

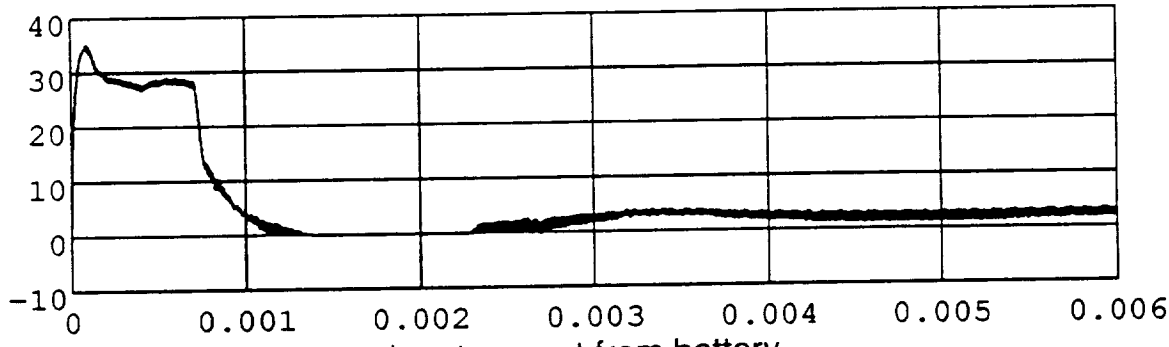
2 MS/DIV

FIG. 2-20

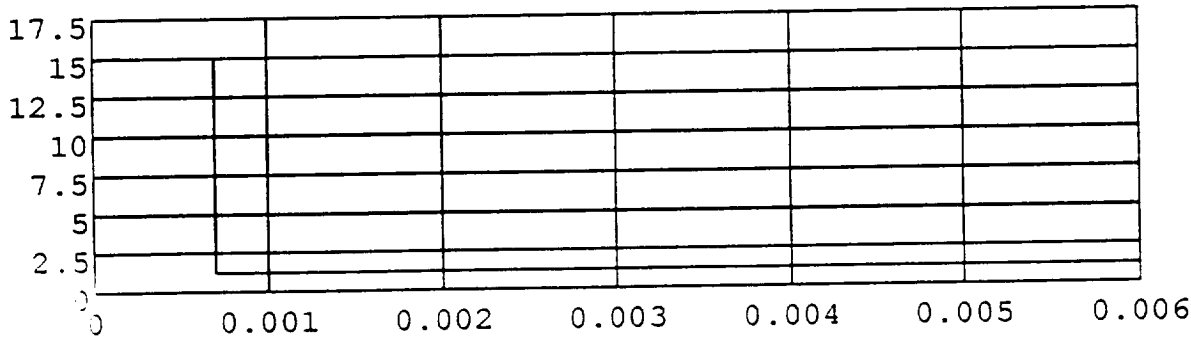
Load step change from 15A to 1.2A



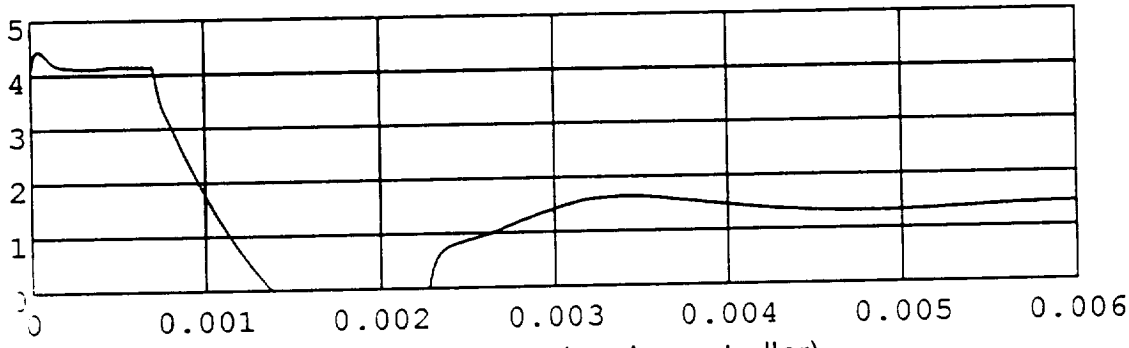
Bus voltage



Input current from battery



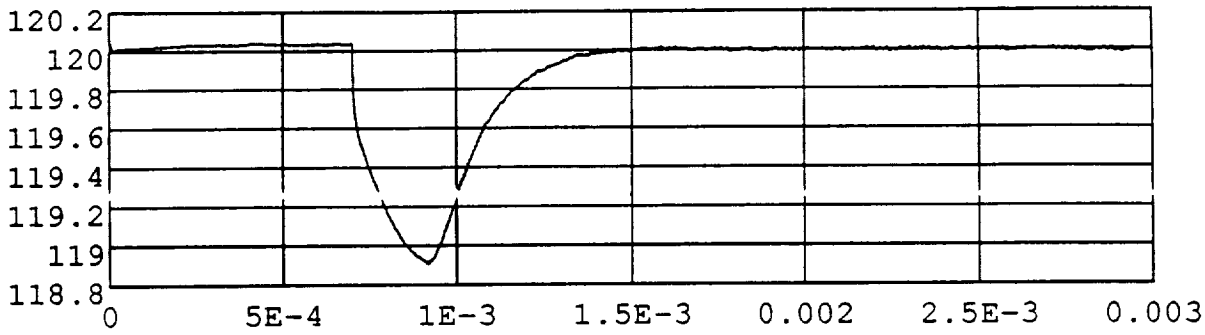
Load current



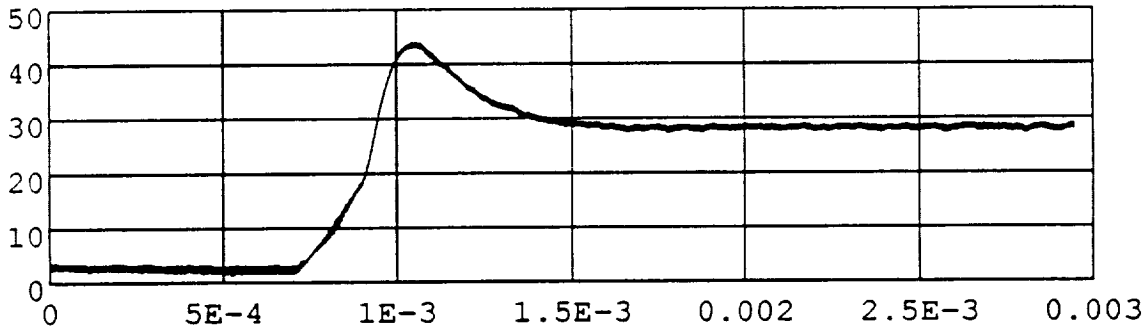
Control voltage (mode controller)

FIG. 2-21

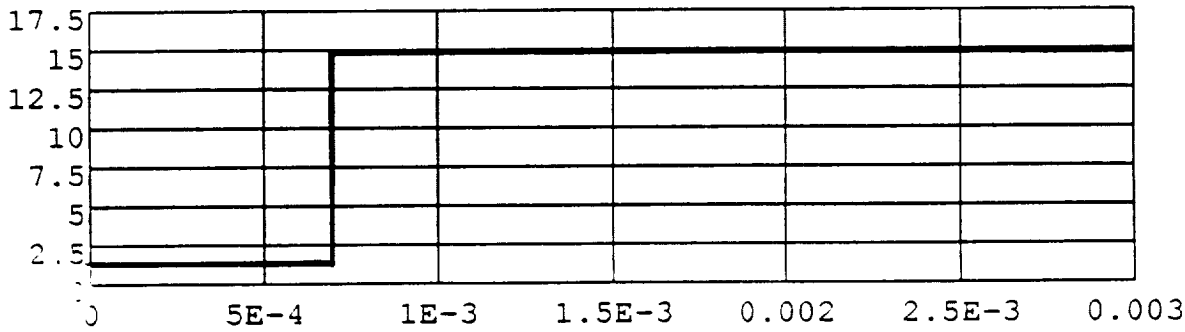
Load step change from 1.2A to 15A



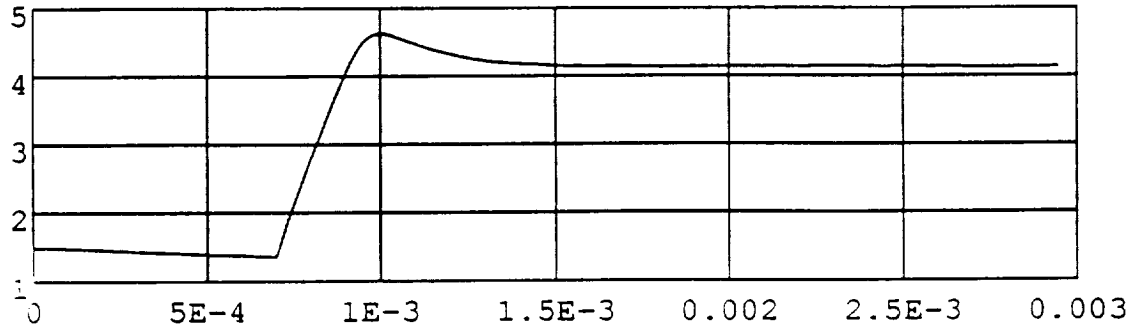
Bus voltage



Input current from battery



Load current



Control voltage (mode controller)

The EMI characteristics that were measured include the output voltage ripple and the input current ripple (conducted emmissions).

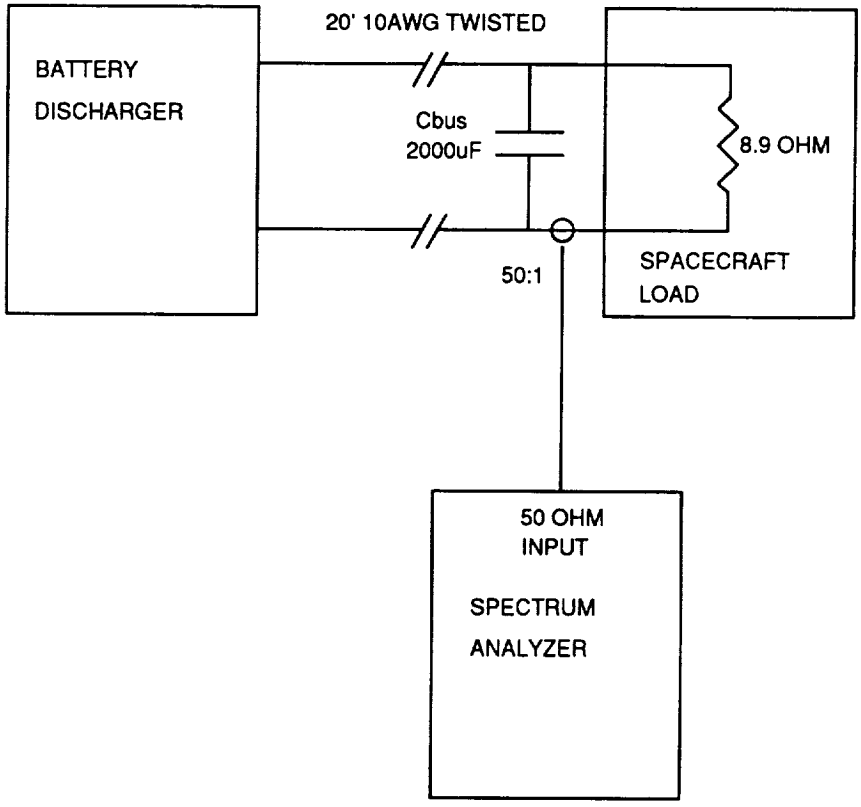
2.6.3.1 Output Voltage Ripple

Output voltage ripple was difficult to measure with an oscilloscope due to noise pickup and test equipment grounding. An attempt was made to measure the spectrum of the output noise by an isolated current measurement. This test set-up is shown in Fig. 2-22. Fig. 2-23 shows the results of the output EMI measurement at different line voltages. The upper left plot is taken at a line voltage of 64 V. The first peak occurs at the ripple frequency of 192 kHz and reaches -71 dbm, which corresponds to 5.6 mV AC. The second peak occurs at the second harmonic and reaches -62 dbm. When the input voltage is reduced to 62 V, there is a large drop in the output EMI. This is because the duty cycle is 50% resulting in almost perfect cancellation of the ripple current. The lack of any significant component at a subharmonic of the ripple frequency indicates that the current sharing between the four modules is performing very well.

Fig. 2-24 shows a simulation result of the output voltage ripple, including the effect of one failed module. The top four traces show the phased inductor currents. The bottom trace shows the output voltage ripple. With all modules active, the ripple is barely noticeable on the output. When one module fails, the phasing of the remaining modules is not longer symmetrical. The ripple increases many times to over 300 mV peak-to-peak. This demonstrates the advantage of symmetrical phasing of the boost regulator modules.

2.6.3.2 Input Current Ripple and Module Current Sharing

Fig. 2-25 shows a photograph of the battery input current. The peak-to-peak current ripple is approximately 20 mA. This is despite the fact that each individual module has a current ripple of over 10 A peak-to-peak, yet there is no input filter. The time scale on the photograph is 2



$$Vrms = \sqrt{10^{(Xdbm/10)} * 1mW/50 * 8.9 * 500}$$

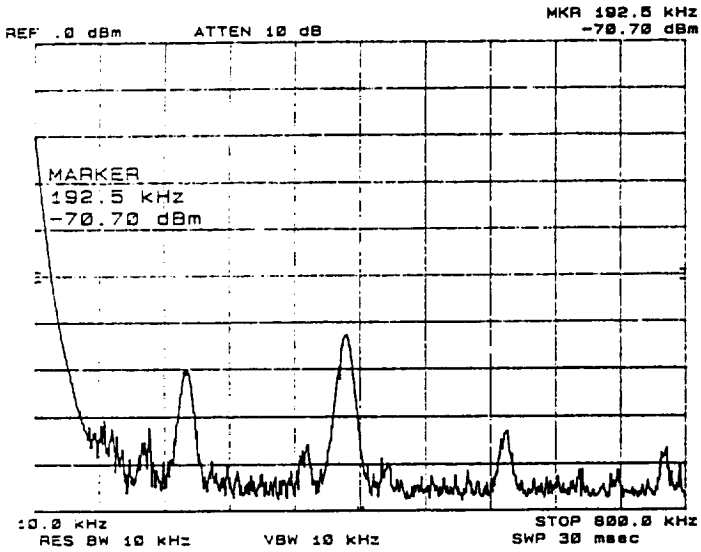
-60 dBM = 20mVAC

FIG. 2-22 EMI TEST SET-UP

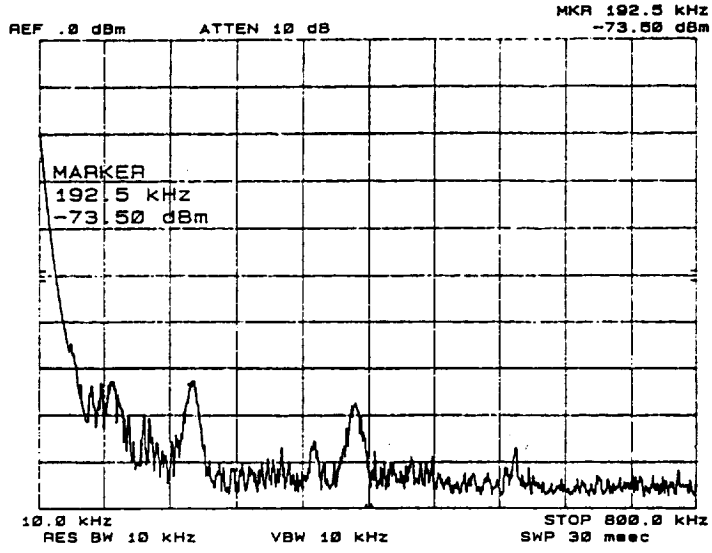
FIG. 2-23

OUTPUT EMI MEASUREMENT

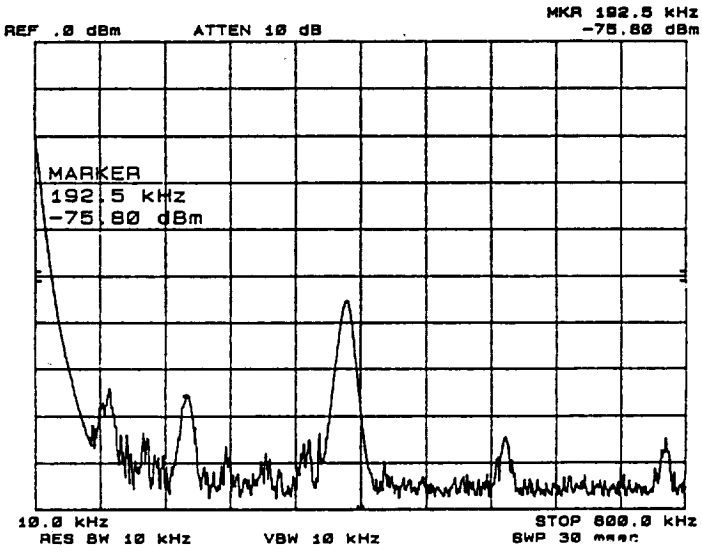
VIN=64V



VIN=62V



VIN=72V



VIN=80V

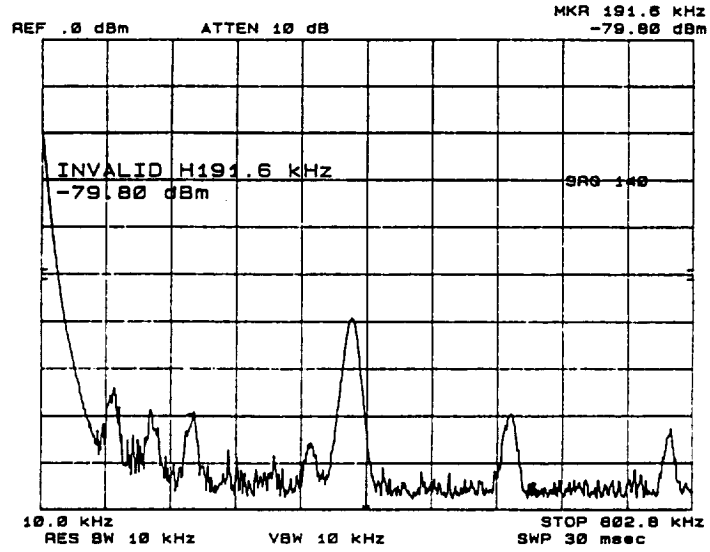
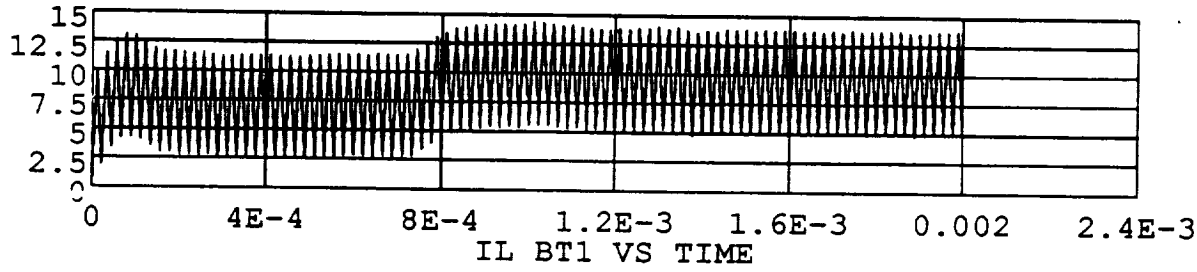
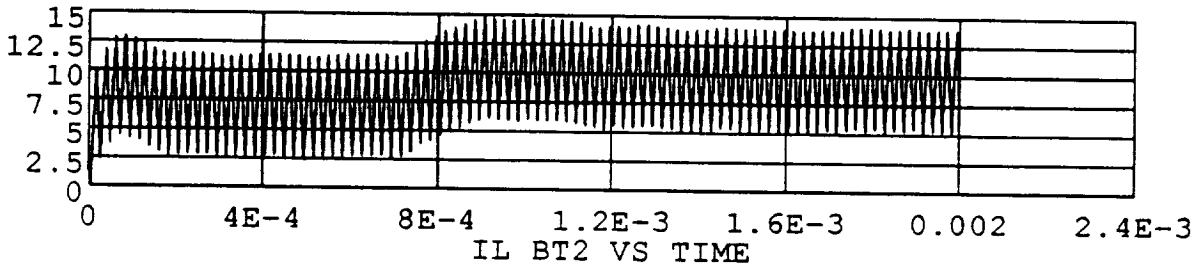
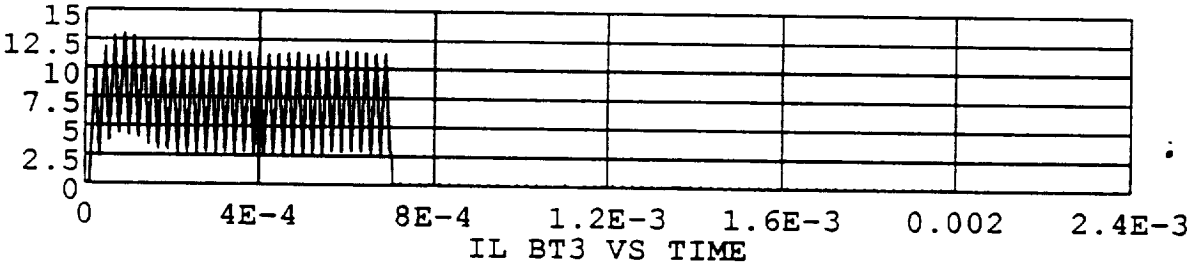


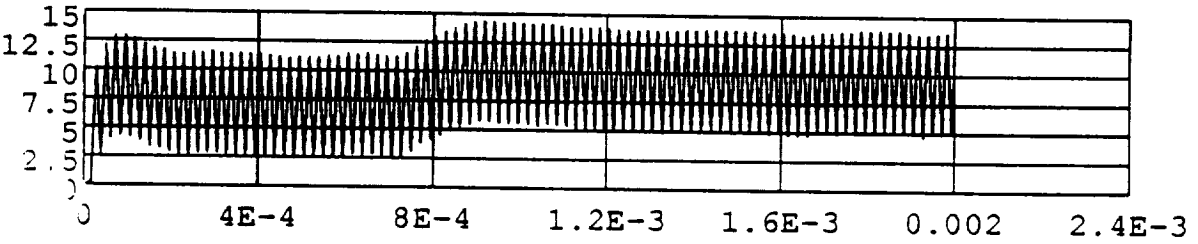
FIG. 2-24

Effect of disabling one boost module

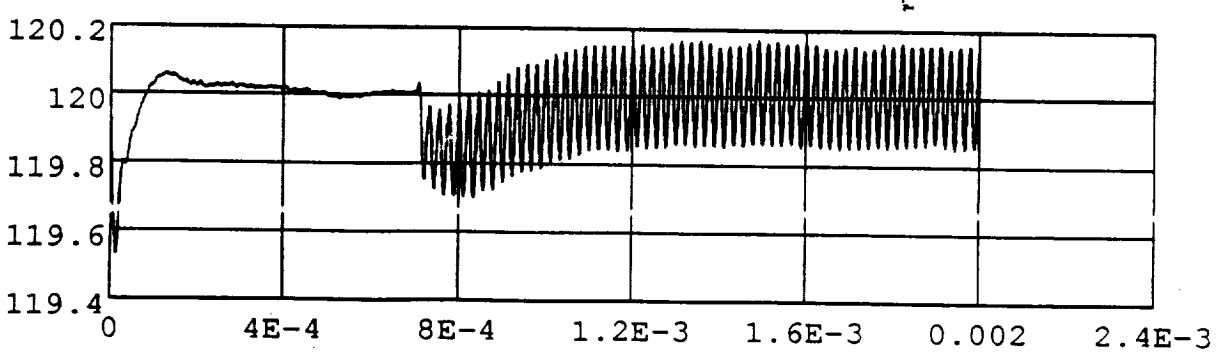








Inductor currents in the four modules

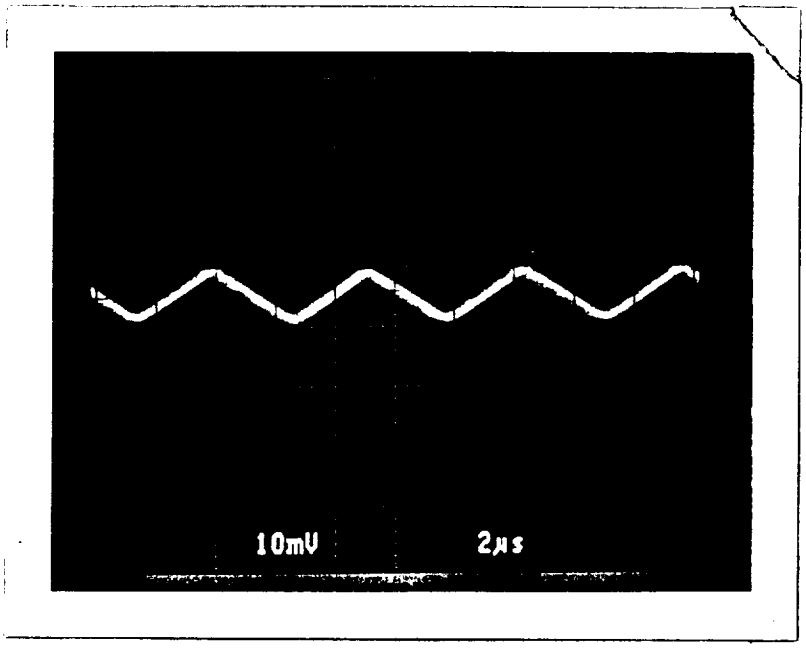


Bus voltage

FIG. 2-25

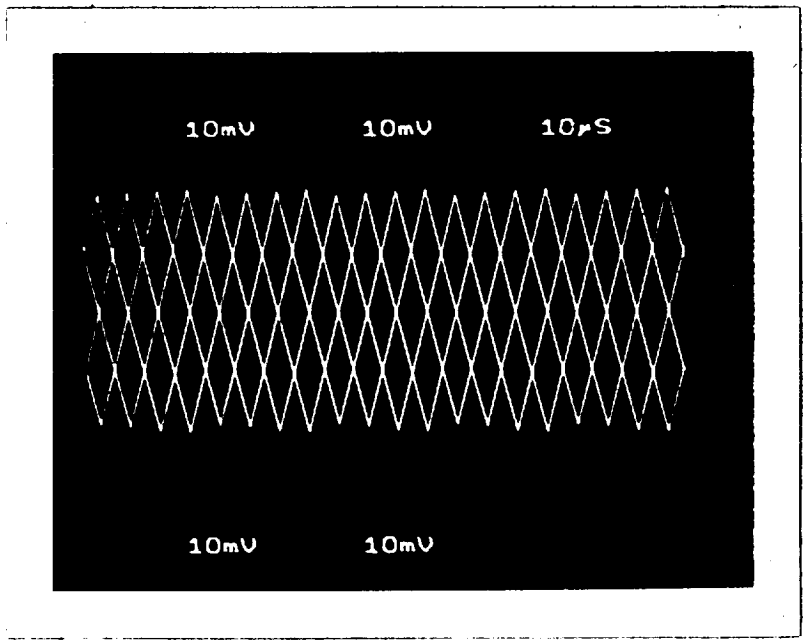
FOUR MODULE BOOST BREADBOARD WAVEFORMS

INPUT CURRENT
MAX. LOAD
20 mA/DIV



2 uS/DIV

INDUCTOR CURRENTS
2.0 A/DIV



10 uS/DIV

μsec per division, indicating that the fundamental frequency of the waveform is about 180 kHz. Successive peaks have equal amplitude, indicating that the current sharing between modules is very good. The lower photograph shows the four inductor currents.

CHAPTER 2 REFERENCES

[1] D.M. Sable, B.H. Cho and F.C. Lee, "Use of Nonlinear Design Optimization Techniques in the Comparison of Battery Discharger Topologies for the Space Platform," IECEC, August, 1990.

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3. VOLTAGE-FED, PUSH-PULL, AUTO-TRANSFORMER DESIGN

The voltage-fed, push-pull, autotransformer (VFPPAT) battery charger topology design and analysis are presented. The final breadboard stage of the VFPPAT topology was not integrated into the system as was the four-module, boost converter. However, the control loop has a provision for integrating the mode controller (Section 3.5) and analysis was performed with the 20', #8 AWG cable in place.

3.1 INTRODUCTION

The specifications for the battery discharger studied are given in Table 3-1. The main focus of [1] was to optimize the battery discharger for efficiency, weight and dynamic characteristics by using a computer-based electronic spreadsheet program to figure the power loss of each converter. By plotting weight vs. frequency for curves representing efficiencies of 95%, 96%, and 97%, an optimal topology was determined. The results show that the multi-module boost converter is an optimal battery discharger topology in terms of efficiency. The VFPPAT topology was a viable option for the battery discharger. A project research grant from NASA was awarded to the VPEC to further investigate the findings of [1].

Two power converter topologies were considered for the research program of the battery discharger for the Space Platform. These include a four-module boost converter (FMBC) shown in Figure 3-2, and a VFPPAT shown in Figure 3-3. This section reports on the optimization of the design, methods of the build and analysis of the test results of the VFPPAT topology. First, however, a brief comparison of the two topologies is presented.

Table 3-1 Battery Discharger Design Specifications

Parameter	Specification
Input Voltage Range	
Optimal Performance Range	64 Vdc to 84 Vdc
Regulation Range	53 Vdc to 84 Vdc
Output Voltage Range	120 Vdc ± 4%
Output Voltage Ripple	200mV peak-to-peak
Output Power Range	0 W to 1800 W
Output Current Range	0 Amps to 15 Amps
Input Current Ripple	250 mA peak-to-peak
Switching Frequency	40 kHz
Efficiency Goal (low line = 64 Vdc, high load = 15 Amps)	96 %
Transient Performance	
Output Voltage Peaking Range	115.2 Vdc - 124.8 Vdc
Output Settling Time	10 msec

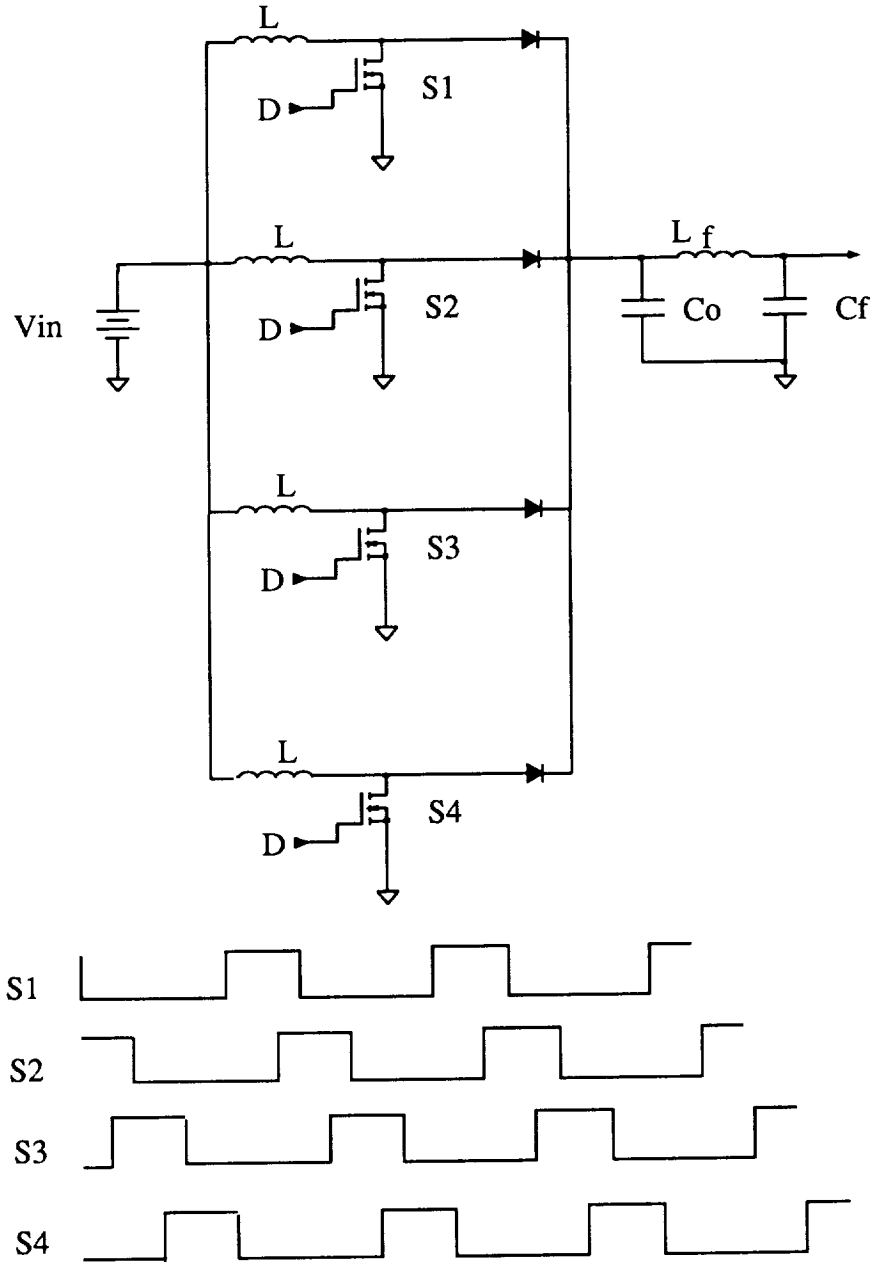


Figure 3-1 Power Stage Schematic and Waveforms of the Four Module Boost Converter

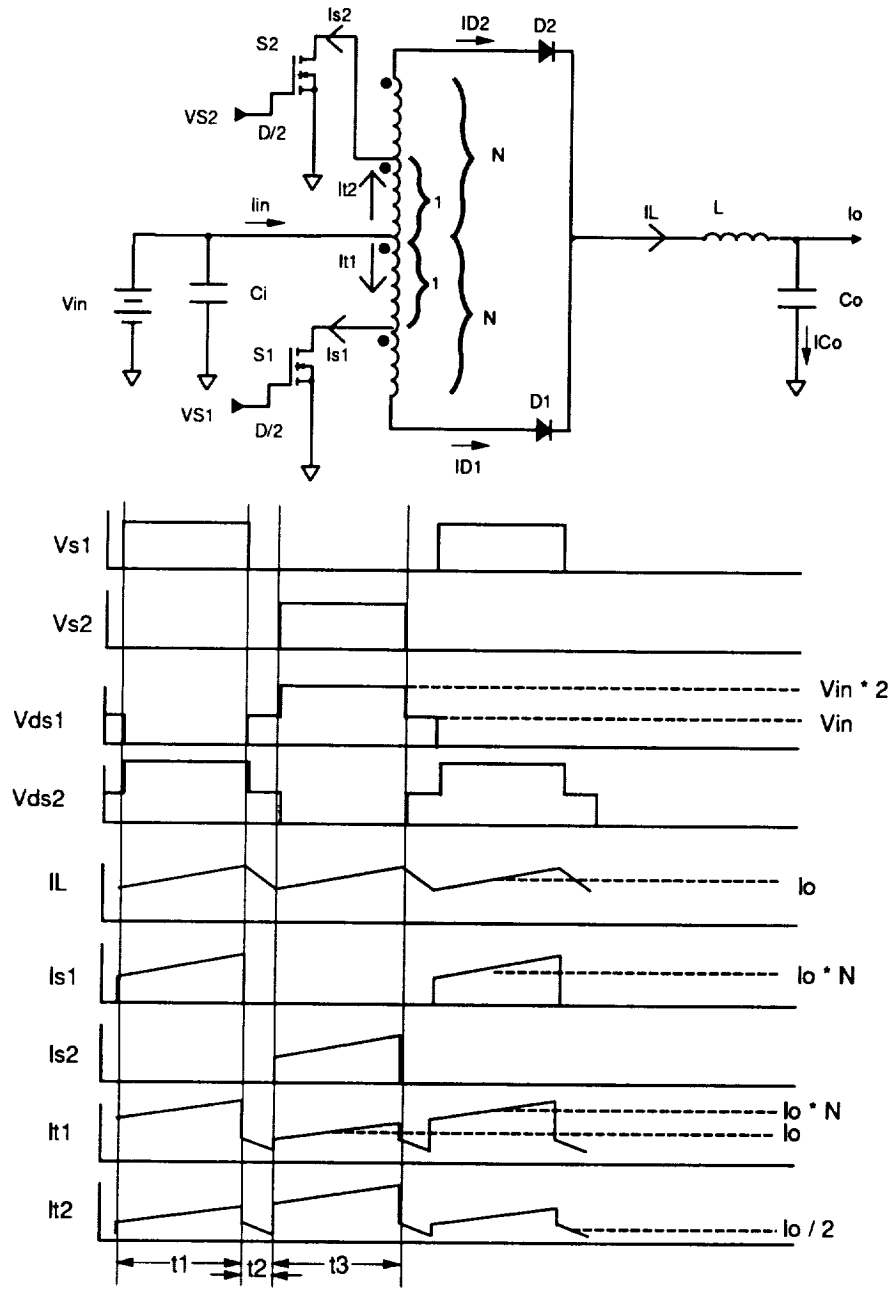


Figure 3-2 Power Stage Schematic and Waveforms of the Voltage-Fed, Push-Pull Autotransformer Converter

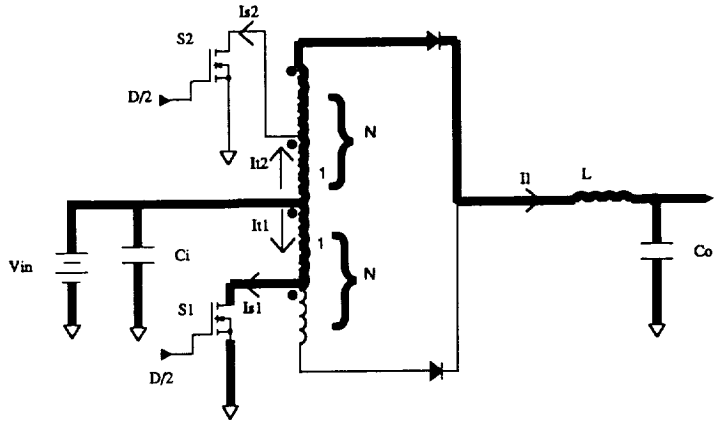
3.1.1 Voltage-Fed, Push-Pull Autotransformer (VFPPAT)

The VFPPAT presents several advantages. The push-pull operation along with the non-isolated nature of the autotransformer allows for a single PWM chip to be used to directly drive the MOSFETs (whose source terminals connect to the same ground as the input, output, and PWM reference). Because the push-pull operation requires only two switches operating 180° out of phase, a PWM IC (such as the UC1825) can be used; this is not the case for the FMBC with its four-phase PWM. The presence of the inductor on the output of this buck-derived converter allows for a continuous output current to flow over most of the power range. Peak-to-peak ripple current is less than for a boost converter, thus eliminating the need for an additional output filter stage.

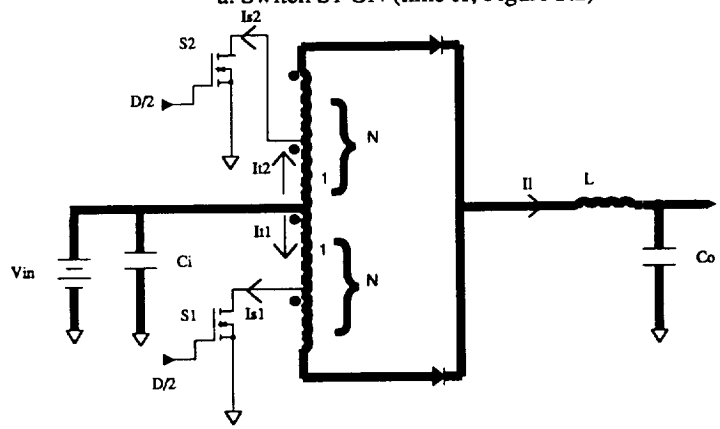
Many of the disadvantages of the VFPPAT result from its buck-derived nature. A discontinuous input current will require filtering to meet the ripple current specification. In addition, this high current ripple will not allow an input capacitor with a high equivalent series resistance (ESR) value. By using low ESR, polypropolene capacitors, the capacitor ripple current rating will not be exceeded. Any imbalance in the transformer may cause "flux walking" to occur. This problem may damage the switching devices by allowing the transformer to saturate and pass large current through the drain. The use of current-injection control (CIC) insures flux walking does not occur by level detecting both the dc and ac portions of the transistor drain current.

Figure 3-2 shows the tapped version of the VFPPAT along with the resulting waveforms. These waveforms illustrate the push-pull nature of the converter. Figure 3-3 uses thick lines to show that each time a switch is gated ON, the diode connected to the opposing winding conducts. This provides a voltage of Vin to each primary on every other gating of the switch, and a primary voltage of zero when both switches are OFF.

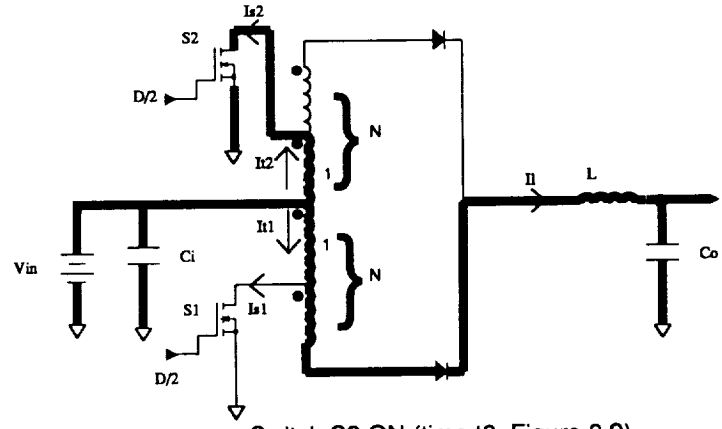
Because the switch transistors are operated 180° out of phase, the primary voltage is constantly reversed due to the polarity of the primaries, and complete flux balance will take place provided the circuit and waveforms are completely symmetrical.



a. Switch S1 ON (time t1, Figure 3.2)



b. Both Switches OFF (time t2, Figure 3.2)



c. Switch S2 ON (time t3, Figure 3.2)

(Note: Thick lines indicate conducting paths.)

Figure 3-3 VFPPAT Conduction Modes

By noting the applied voltages for times t1, t2, and t3, the voltage across the inductor can be found as shown in Eqs. 3.1 and 3.2. Where N is the turns ratio of one primary plus secondary (as shown in Figures 3-2 and 3-3).

$$VL_{ON} = (N+1) \times Vin - Vo \quad (\textit{either switch ON}), \text{ and} \tag{3.1}$$

$$VL_{OFF} = Vin - Vo \quad (\textit{both switches OFF}). \tag{3.2}$$

For steady state operation the flux for the ON-time of the inductor must equal the flux for the OFF-time. This phenomenon known as flux balance uses the switching period Ts and the duty cycle at the inductor D (Note that the duty cycle of each switch is D/2) multiplied by the inductor voltage. Using the flux balance relationship the gain is found in equation 3.3.

Flux Balance: $$\Delta\Phi_{ON} = VL_{ON} \times D \times Ts = \Delta\Phi_{OFF} = VL_{OFF} \times (1-D) \times Ts$$

$$Gain = M = (Vo/Vin) = N \times D + 1 \tag{3.3}$$

3.1.2 Summary

The results of the trade-off study [1] determined that the FMBC and VFPPAT topologies would provide the efficiency and size needed for the Space Platform battery discharger. Of these two topologies, the VFPPAT provides a challenge to optimize the design such that the resulting efficiency and performance is comparable to that of the FMBC. The VFPPAT can be designed in a manner which may make it more reliable than the FMBC. Finally, by investigating all areas of the power stage of the VFPPAT, a valuable lesson in optimizing the performance of high power converter operation can be learned.

3.2 VFPPAT POWER STAGE DESIGN AND PARAMETER VALUE SELECTION

Establishment of the parameter values of the circuit components to meet the design specifications is performed along with choice of each component in accordance with the approved parts list [2]. The autotransformer turns ratio and inductor value are chosen first, and the resulting voltage and current levels are used to determined the remaining power stage components.

A limited number of flight approved semiconductors causes the design to rely on optimization of the power stage magnetics for achievement of the best efficiency. Therefore the semiconductors are chosen and the values of the magnetic components are determined in this section, and the magnetics design is detailed in Section 3.3.

3.2.1 General Power Stage Analysis

The design of the power stage is begun by calculating the maximum duty cycle and then choosing a value for the autotransformer turns ratio. The resulting voltage levels are then calculated.

Autotransformer Turns Ratio and Converter Duty Cycle Range

The establishment of the gain equation along with the input specifications listed in Table 3-1 allows the design stage to begin. By noting that the input voltage regulation range from Table 3-1 is 53-84 Vdc and the output voltage is 120 Vdc, both the duty ratio D and the turns ratio N (Fig. 3-2) can be chosen. The choice of D is based on the maximum duty cycle a typical PWM IC can produce at the switch (D/2). This value reaches a theoretical maximum of 50% for the chosen UC1825 PWM. However, when variables such as rise and fall times are considered, this value can safely be assumed to be a maximum of 45%. The maximum duty cycle will occur at low line (53 Vdc). By using the gain Eq. 3.3 The minimum turns ratio is determined as follows:

$$N_{\min} = \frac{(Vo/Vin_{\min}) - 1}{D_{\max}} = \frac{(120V/53V) - 1}{0.9} = 1.405.$$

Because this is a minimum value, N=1.5 was selected to accommodate for any drops in the semiconductors or other components. Also, 1.5 is favorable for winding the autotransformer because it allows for an integer number of turns to be wound for a complete set of conductors for all primaries and secondaries. The design then simply taps two series windings for a primary (autotransformer winding ratio of 1 in Fig. 3-2) and taps a third winding for the secondary giving a total of N=1.5.

The establishment of a turns ratio allows the duty cycle range of the converter to be calculated. This ratio is found by using Eq. 3.3 as follows:

$$Dmin = \frac{(Vo - Vin_{\max} + Vde)}{((Vi_{\max} - Vqe) \times (N+1) - Vi_{\max})} = \frac{(120V - 84V + 1.5)}{((84V - 1.65V) \times (1.5+1) - 84V)} = 0.31, \text{ and}$$

$$Dmax = \frac{(Vo - Vin_{\min} + Vde)}{((Vi_{\min} - Vqe) \times (N+1) - Vi_{\min})} = \frac{(120V - 53V + 1.5)}{((53V - 1.65V) \times (1.5+1) - 53V)} = 0.91,$$

where the voltage drops are assumed to be:

Vqe = estimated primary voltage drop = 1.65 V, and

Vde = estimated secondary voltage drop = 1.50 V.

The duty cycles calculated are twice the duty cycle seen by the switch. Therefore the duty cycles seen at the switch are as follows:

$$Dswitch_{\min} = \frac{D_{\min}}{2} = \frac{0.31}{2} = 0.155, \text{ and}$$

$$Dswitch_{\max} = \frac{D_{\max}}{2} = \frac{0.91}{2} = 0.455.$$

The maximum duty cycle of 0.46 is attainable with the UC1825 IC chosen for this design. This value is achieved using the dead-time capacitor calculation specified by the manufacturer's data sheet, and it is calculated in Section 3.5.

Power Stage Voltage Levels

Voltage levels experienced by the power stage components can be determined by using Kirchoff's Voltage Law and Fig. 3-2. The voltage of the switch is equal to the input voltage or twice the input voltage when the opposing switch is OFF or ON, respectively and is given by Eq. 3.4:

$$Vds_{(opposing\ switch\ ON)} = 2Vin, \text{ and} \tag{3.4a}$$

$$Vds_{(opposing\ switch\ OFF)} = Vin. \tag{3.4b}$$

Autotransformer primary voltage levels are equal to Vin when either switch is ON and zero when the switches are OFF as given by Eq. 3.5:

$$Vprim_{(either\ switch\ ON)} = Vin, \text{ and} \tag{3.5a}$$

$$Vprim_{(either\ switch\ OFF)} = 0. \tag{3.5b}$$

Autotransformer secondary voltages are equal to the primary voltages through the turns ratio as shown in Eq. 3.6:

$$Vsec_{(either\ switch\ ON)} = Vprim \times (N-1) = Vin \times (N-1) = 0.5Vin, \text{ and} \tag{3.6a}$$

$$Vsec_{(either\ switch\ OFF)} = \frac{Vprim}{(N-1)} = 0. \tag{3.6b}$$

The voltage experienced by the inductor is established next (Eq. 3.7):

$$VL_{(switch\ ON)} = (N+1) \times Vin - Vo = 2.5Vin - Vo, \text{and} \tag{3.7a}$$

$$VL_{(switch\ OFF)} = Vin - Vo. \tag{3.7b}$$

The reverse voltage on the diode occurs only when the adjacent switch is conducting as found using Eq. 3.8:

$$Vrr = (VL + Vo) - Vin \times (N+1) = 2N \times Vin. \tag{3.8}$$

Finally, the voltage levels of the input and output capacitors are simply the input and output voltage, respectively, as shown in Eqs. 3.9 and 3.10:

$$VCi = Vin, \text{and} \tag{3.9}$$

$$VCo = Vo. \tag{3.10}$$

The resulting component voltage levels for low line and high line input voltages are shown in Table 3-2.

Table 3-2 Maximum Voltages Levels of Power Stage Components

Voltage Designation	Voltage Level Low Line (Vin = 53 Vdc)	Voltage Level High Line (Vin = 84 Vdc)
$Vds_{(opposing\ switch\ ON)}$	106.0 V	168.0 V
$Vprim_{(either\ switch\ ON)}$	53.0 V	84.0 V
$Vsec_{(opposing\ switch\ OFF)}$	26.5 V	42.0 V
$VL_{(either\ switch\ ON)}$	12.5 V	90.0 V
Vrr	159.0 V	252.0 V
VCi	53.0 V	84.0 V
VCo	120.0 V	120.0 V

3.2.2 Power Stage Component Selection

Now that the voltage levels are known, the inductor value is determined, and the resulting peak current and root-mean-square (rms) current levels are then found. Based on these levels, the input and output capacitors and the semiconductor devices to be used for the switches and rectifiers are chosen.

3.2.2.1 Inductor

Inductor Value

The choice of an inductor value for the VFPPAT is related to many factors such as: ripple current, power loss, power level at which discontinuous operation begins, size, and weight. An optimization program was conducted [1] and the resulting value of 94 uH was chosen for optimal efficiency. The following discussion illustrates how the inductor value affects the output ripple current (for other factors in the optimization refer to [1]).

The presence of the inductor on the output of the converter is advantageous only if the peak-to-peak inductor current level can be kept to a minimum, thereby reducing the output ripple current and the ripple voltage produced by the capacitor ESR. The peak-to-peak inductor current is most affected by the applied voltage VL, and by the duty cycle value (which was shown to be a function of the input voltage level in Eq. 3.1). Eq. 3.11 shows the peak-to-peak inductor current relationship to the voltage across the inductor:

$$\Delta IL = \frac{VL \times D}{2f \times L}. \tag{3.11}$$

The peak-to-peak inductor current will be greatest at high input voltage, where the applied inductor voltage will be 90 V as shown in Table 3-2. A plot of the ΔIL versus

inductor values illustrates this relationship and provides insight into the optimized inductor value (Fig. 3-4). The inductor value of 94 uH chosen produces a relatively low peak-to-peak inductor current of 3.68 A which allows for a minimal output voltage ripple. This choice of inductance value will produce a respectable sized inductor with minimal gap loss as will be shown in the power loss analysis (Section 3.6).

$$\Delta IL = \frac{90V \times 0.31}{2 \times 40kHz \times 94uH} = 3.68\,A\ \ peak - to - peak$$

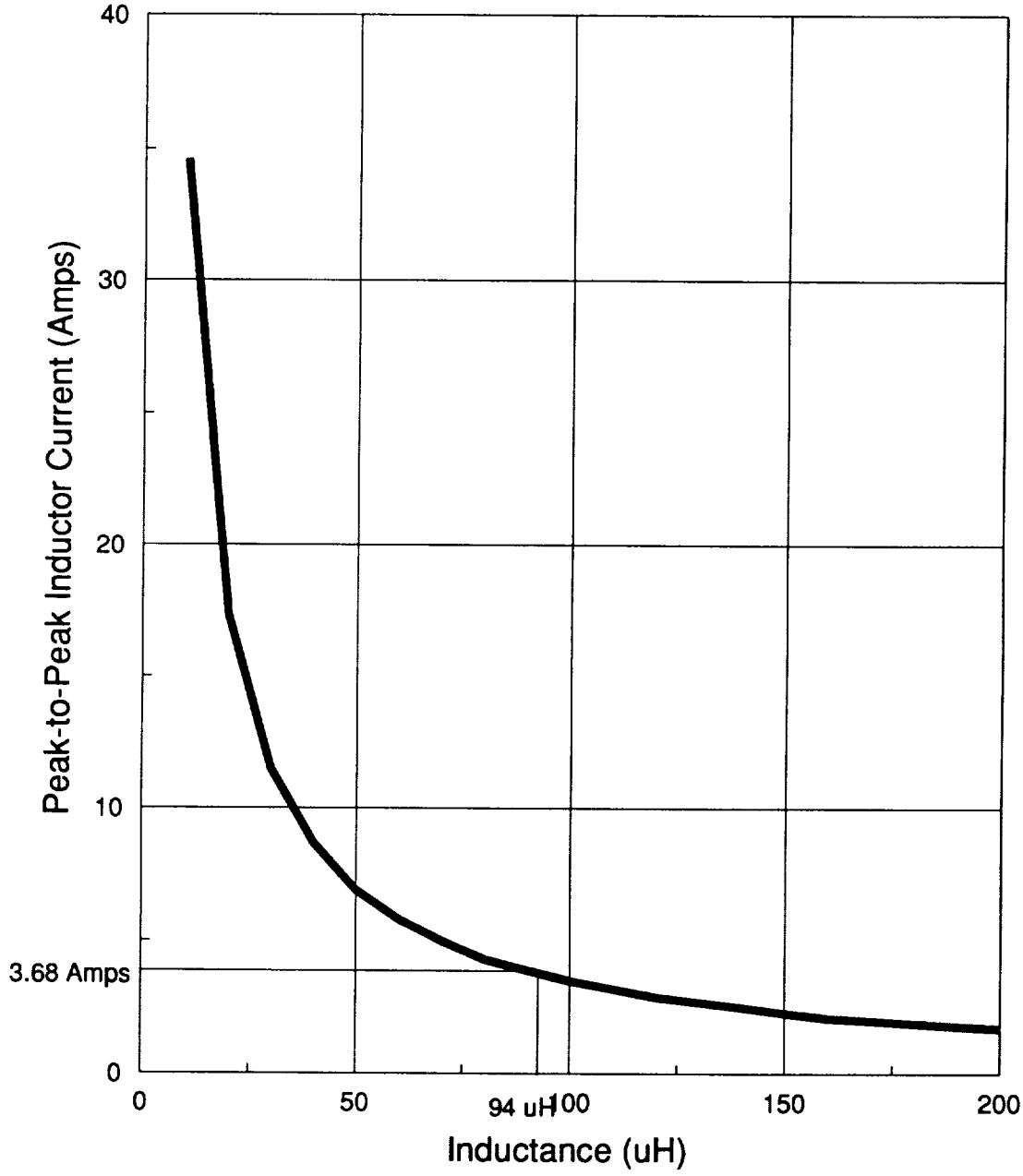


Figure 3-4 Peak-to-Peak Inductor Current vs. Inductance

Inductor Current

Now that the inductor value is determined, the peak and rms current levels are developed and values are presented. Because the load range has a minimum level of 0 A, the inductor current will have to become discontinuous at an output level between the specified 0 and 15 A. The output current level at which discontinuity occurs is half of the 3.68 A determined for Vin=84 Vdc earlier. Therefore discontinuous inductor current was chosen in [1] and occurs at 1.84 A dc load current or 216 W output power for Vin=84 Vdc. Maximum peak inductor current will occur at maximum load current as shown in Eq. 3.12:

$$ILpk=Iload_{max}+\frac{(\Delta IL_{max})}{2}=15A+\frac{(3.68A)}{2}=16.84\,A. \tag{3.12}$$

Remaining Power Stage Current Levels

As shown in Fig 3-2, the primary of the autotransformer will experience three different waveform levels depending on whether the adjacent MOSFET switch is in the ON state, the opposite MOSFET is in the ON state, or both MOSFETs are OFF, as shown in Eq. 3.13. The peak primary current from Fig. 3-2 is the autotransformer turns ratio multiplied by the inductor current:

$$Itl_{(S1\ ON)}=N\times IL=Is1\text{, and} \tag{3.13a}$$

$$Itl_{(S2\ ON)}=IL\text{, and} \tag{3.13b}$$

$$Itl_{(S1\ \text{and}\ S2\ OFF)}=\frac{IL}{2}. \tag{3.13c}$$

Similarly, the diode currents will conduct the inductor current when the opposite switch is ON, no current when the adjacent switch is ON, and half the inductor current if both switches are ON, as shown in Eq. 3.14. Note that the secondary currents of the autotransformer are equal to the diode currents which are developed below:

$$ID1_{(S1\ ON)} = IL, \text{ and} \tag{3.14a}$$

$$ID1_{(S2\ ON)} = 0, \text{ and} \tag{3.14b}$$

$$ID1_{(S1\ \text{and}\ S2\ OFF)} = \frac{IL}{2}. \tag{3.14c}$$

The input current is the sum of the two primary currents (It1 and It2), and the capacitor current is the input current without the dc level, as shown in Eq. 3.15:

$$ICi_{(either\ switch\ ON)} = (It1 + It2) - \frac{((N+2) \times Io)}{2}, \text{ and} \tag{3.15a}$$

$$ICi_{(both\ switches\ OFF)} = IL - \frac{((N+2) - Io)}{2}. \tag{3.15b}$$

The output capacitor will experience the peak-to-peak inductor current (ie. the ac portion of the inductor current) as shown in Eq. 3.16:

$$ICo = \Delta IL. \tag{3.16}$$

The peak current level values are presented in Table 3-3.

Table 3-3 Peak Current Values of Power Stage Components

Current Designation	Maximum Current Value Low Line (Vin = 53 Vdc)	Maximum Current Value High Line (Vin = 84 Vdc)
Isw_{peak}	23.6 A	25.3 A
$Iprim_{peak}$	23.6 A	25.3 A
$Isec_{peak} = ID1_{peak}$	15.8 A	16.8 A
IL_{peak}	15.8 A	16.8 A
ICo_{peak}	0.8 A	1.8 A
Iin_{peak}	42.1 A	39.4 A
ICi_{peak}	15.9 A	13.1 A

The rms current levels are based on the peak current levels which were developed in the previous section. The waveforms and time periods mentioned are illustrated in Fig. 3-2. Starting with the transformer the rms currents are shown in Eqs. 3.17 and 3.18:

$$Itprim_{rms} = \sqrt{\frac{1}{T}\left(\int^{t1} (It1(t))^2 dt + 2\int^{t2} (It1(t))^2 dt + \int^{t3} (It(t))^2 dt\right)}, \text{ and} \quad (3.17)$$

$$Itsec_{rms} = \sqrt{\frac{1}{T}\left(2\int^{t2} (ID1(t))^2 dt + \int^{t3} (ID1(t))^2 dt\right)}. \quad (3.18)$$

The rms current level as experienced by either switch is shown in Eq. 3.19:

$$Is1_{rms} = Is2_{rms} = \sqrt{\frac{1}{T}\left(\int^{t1} (It1(t))^2 dt\right)}. \quad (3.19)$$

The rms current level of the output inductor is found using Eq. 3.20:

$$IL_{rms} = \sqrt{\frac{2}{T}\left(\int^{t1} (IL(t))^2 dt + \int^{t2} (IL(t))^2 dt\right)}. \quad (3.20)$$

The output capacitor rms current is shown by Eq. 3.21:

$$ICo_{rms} = \sqrt{\frac{2}{T}\left(\int^{t1} (IL(t) - Io)^2 dt + \int^{t2} (IL(t) - Io)^2 dt\right)}. \quad (3.21)$$

Finally, the input capacitor current can be found using Eq. 3.22:

$$ICi_{rms} = \sqrt{\frac{2}{T}\left(\int^{t1} (It1(t) + It2(t))^2 dt + \int^{t2} (It1(t) + It2(t))^2 dt\right)}. \quad (3.22)$$

A summary of the expected power stage rms current levels is presented in Table 3-4.

Table 3-4 RMS Current Values of Power Stage Components

Current Designation	Maximum Current Level Low Line (Vin = 53 Vdc)	Maximum Current Level High Line (Vin = 84 Vdc)
Isw_{rms}	15.2 A rms	8.9 A rms
$Iprim_{rms}$	18.3 A rms	11.1 A rms
$Isec_{rms} = ID1_{rms}$	10.2 A rms	6.7 A rms
IL_{rms}	15.0 A rms	14.9 A rms
ICo_{rms}	0.5 A rms	1.2 A rms
Iin_{rms}	36.1 A rms	24.4 A rms
IC_{irms}	11.2 A rms	11.6 A rms

3.2.2.2 MOSFET Switch Transistors

The switching transistor will experience the following maximum voltage and current levels (from Tables 3-2, 3-3, and 3-4):

$$Vds_{max} = 168.0 \text{ V},$$

$$Isw(pk)_{max} = 25.3 \text{ A peak, and}$$

$$Isw(rms)_{max} = 15.2 \text{ A rms.}$$

MOSFET switch transistors are approved for flight by NASA and will be used because implementation is easier and performance is better than for bipolar switch transistors. The MOSFET chosen for this design is the IRF350; an approved part. The data for this device is listed in Table 3-5.

Table 3-5 IRF350 MOSFET Switch Transistor Parameters

Parameter	Value
Vds_{max}	400 V
Id_{max} (T_C= 25° C)	15 A Continuous
Id_{max} (T_C= 50° C)	11.6 A Continuous
Id_{max} (T_C=100° C)	9 A Continuous
Id_{max}	60 A (Repetitive Pulse)
Pd_{max} (T_C=87° C, T_j=105° C)	72 W
Rds_{ON}	0.34 Ω (Id_{pk}=20 A, Vgs=15 V)
$Ciss_{max}$ (Vgs=0V, Vds=50V, f=1MHz)	2000 pf
$Coss_{max}$ (Vgs=0V, Vds=50V, f=1MHz)	200 pf
$Crss_{max}$ (Vgs=0V, Vds=50V, f=1MHz)	50 pf
Vgs_{max}	±20 V

The derating guideline [2] requires the rated maximum transistor values be reduced to the following levels:

$$Vds_{(\max(derated))} = 75\% \times Vds_{\max} = 0.75 \times 400V = 300V,$$

$$Id_{(\max(derated))} = 75\% \times Id_{\max} = 0.75 \times 11.8A = 8.7A\,(T_C = 50^\circ C),$$

$$Pd_{(\max(derated))} = 60\% \times Pd_{\max} = 0.6 \times 72W = 43.2W\,(T_j = 105^\circ C), \text{ and}$$

$$Tj_{(\max(derated))} = 60\% \times Tj_{\max} = 0.6 \times 150^\circ C = 90^\circ C.$$

Each switch requires the use of two IRF350 MOSFETs in parallel for each switch. This will allow the derated continuous drain current requirement to be met by having each switch pass a drain current of 7.6 As rms, and, it will reduce the total ON resistance of the one switch leg to one-half of the 0.34 Ω exhibited by the IRF350. This lowering of the switch ON resistance will reduce conduction loss.

The 400 Vdrain-to-source voltage rating (which is derated to 300 V) is the main reason for choosing this device, because it will allow the 168 V applied level to exist with some overshoot. Otherwise, a smaller device would be specified to reduce the parasitic capacitances and the ON resistance of the drain.

Paralleling MOSFETs is not without its problems, however. The output capacitance (Coss) is doubled when MOSFETs are paralleled, and problems can develop due to using devices with unequal parasitics, resulting in unsynchronized switching and/or unequal sharing of drain current. These problems have been solved through the use of a reliable drive scheme (Section 3.5) and careful circuit layout to reduce and equate parasitics.

The expected power dissipation due to conduction is:

$$PQ1_{ON}(\max) = Id^2 \times Rd_{ON} = \frac{(15.2\,A\ rms)^2}{2} \times 0.34\Omega = 19.6\,W.$$

The power dissipation of the device when it is ON should compare favorably with the derated 43.2 W at Tj=105° C when the switching losses are added (provided proper heat sinking is implemented).

3.2.2.3 Rectifier Diodes

Rectifier diodes are subject to the following voltage and current levels (from Tables 3-2, 3-3, and 3-4):

$$Vrr_{max} = 252.0 \text{ V},$$

$$IDpk_{max} = 16.8 \text{ A peak, and}$$

$$IDrms_{max} = 10.2 \text{ A rms.}$$

A check of the approved parts list [2] shows that no diodes can meet the required derated voltage and current levels. Initially the design was to use two 1N5816 diodes (Vrr_{max} = 150 V) in series to handle the 252 V reverse voltage. This set of two diodes was to be paralleled so that each string would conduct half of the 10.2 A rms rectifier current ($Iavg_{max}$ = 20 A). NASA determined that a failure of one of the series diodes could go undetected and was difficult to test for.

The next design chosen used UES706 diodes as a viable replacement. These diodes are rated for a reverse voltage of 400 V peak (which is derated to 325 V), an average forward current of 20 A each (which is derated to 60% provided the junction temperature stays below T_D), and a peak forward current of 300 A for 8.3 msec. The temperature T_D is found from the derating guideline [2] to be:

$$T_D = T_{(j(derated))} - (Derating Factor) \times (T_{(j(max))} - T_M),$$

$$T_D = 60\% \times 105° C - 60\% \times (105° C - 90° C) = 54° C.$$

The maximum temperature of the case should remain around 50° C, which is the heat sink temperature. Therefore the junction temperature will be more than 54 ° C, and the diodes will have to be paralleled to meet the current specification. Paralleling the diodes will reduce the power loss due to the forward voltage drop. These rectifiers will not have to be put in series to meet the applied reverse voltage. However, ringing will have to be kept to less than a 325 V peak. The UES706 diodes are available in a D0-4 package and must meet final approval for space flight. The number of these diodes required will be half of the number of 1N5816 diodes, therefore increasing mean time between failure (MTBF) and reliability.

3.2.2.4 Output Capacitor

The output capacitance value for the 120 V bus has been determined by NASA to be 2000 uf. However, fifteen to twenty-five feet of twisted, shielded, #10 AWG wire is between the converter and the output capacitor bank, making it necessary to have some capacitance placed at the converter output. The value chosen for the output capacitor was 10 uf. This value is low enough not to alter the final capacitance of the capacitor bank when the converters are paralleled, and high enough to support transients at the converter outputs.

For the test circuit, the output capacitor value of 10 uf was implemented using two 5 uf polypropolene capacitors with the following information:

Part number	= CFR13ALC505
Voltage rating	= 200 Vdc
ESR value	= 0.011 Ω
Maximum ripple current (T_C=85° C)	= 8.5 A rms.

These parts meet the applied rms current of 0.6 A each (Table 3-4) and can be used for the 120 V output provided the derating is not less than 50%. Note that although these capacitors were chosen for breadboard testing, their size is rather large when compared to other approved styles such as the M39006 series. The choice of another style for flight use may reduce the size and must have an ESR value and rms current rating compatible with the applied 1.2 A rms current.

3.2.2.5 Input Capacitor

The input capacitor has two restrictions placed on it by this topology. The rms input current is a maximum 11.6 A (Table 3-4), and the converter input impedance will need to see a rather low impedance from the input capacitor. For these reasons the input capacitor was chosen at 20 uf; it is composed of two 10 uf polypropolene capacitors in parallel. The information for these capacitors is as follows:

Part Number	= CFR14LLC106
Voltage Rating	= 200 Vdc
ESR Value	= 0.009 Ω
Maximum Ripple Current (T_C=85°C)	= 10.9 A rms.

The maximum rms current applied to each capacitor is 5.8 A. This value easily meets the rated level of 10.9 A rms. The maximum applied voltage of the input capacitor is 84 Vdc vs. a rated value of 200 Vdc.

3.2.3 Summary

Establishment of an autotransformer turns ratio and resulting duty cycles allowed the power stage voltage levels to be calculated and an inductor value to be determined. Power stage current levels were then determined, and components were chosen in accordance with the approved parts list [2].

3.3 POWER STAGE MAGNETICS

Section 3.2 established the required autotransformer turns ratio and inductor value for the VFPPAT power stage. This chapter will present the design considerations of the autotransformer and inductor. Optimization of these two components is crucial to the choice of the VFPPAT as the final battery discharger topology. The limitations set on the design by the power stage semiconductor devices and capacitors requires the design of efficient, light-weight magnetics for this topology to maintain a respectable efficiency and size. Select design equations are presented, as are measured and manufacturer's data.

3.3.1 Autotransformer

The design of the autotransformer began by choosing a core based on an area product calculation. It proceeded to the design of the windings to fit the window area of the chosen core. The ultimate goal of the final design was to achieve a balance of power dissipation so that the winding and the core each account for half of the total autotransformer power loss.

3.3.1.1 Core Design

Calculation of the area product begins with basic magnetics equations (which are derived from Faraday's law and Ohm's law). From Faraday's law, the law of flux bal-

ance can be stated as shown in Eq. 3.22, where Ae is the effective area of the core, ΔB is the flux excursion, V_{eff} is the voltage applied to the primary, and B_{max} is the maximum flux density of the core material:

$$V_{eff} = \frac{Np \times \Delta\Phi}{\Delta T} = \frac{Np \times \Delta B \times Ae \times f}{0.5 \times D} = \frac{Np \times 2B_{max} \times Ae \times f}{0.5 \times D}. \quad (3.22)$$

The flux density usage of the H7C4 material is illustrated in Fig. 3-5.

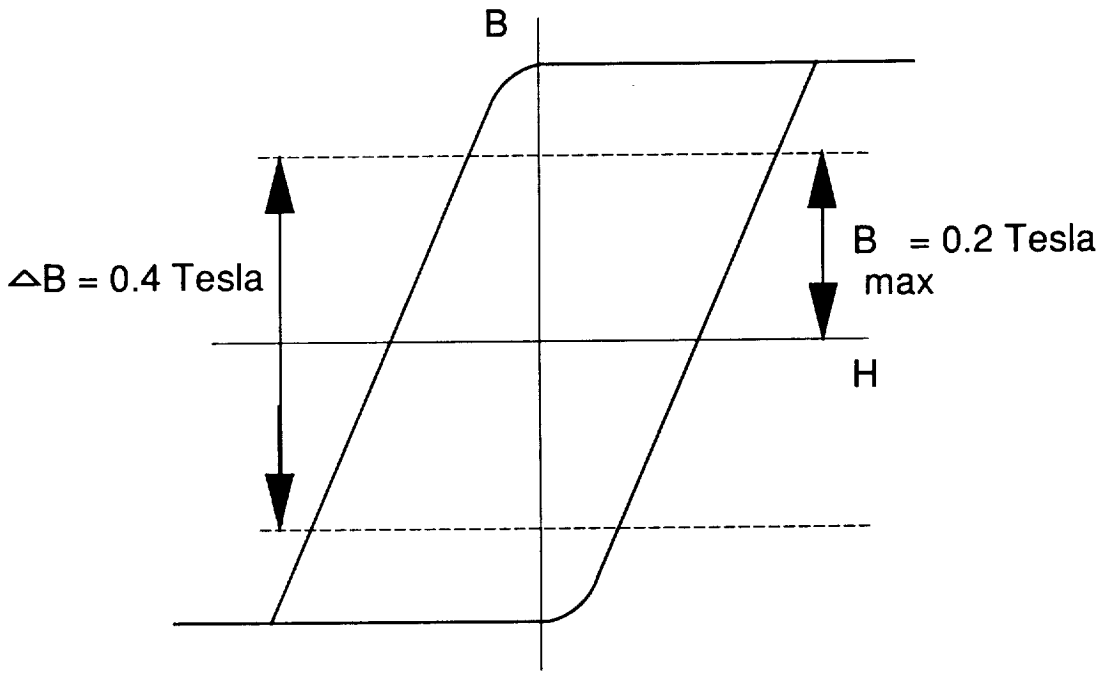


Figure 3-5 Flux Density Usage of TDK H7C4 Material

The choice of a core will be based on the area product (Ap = Ae Aw) value of the core where Aw is the window area of the core. Solving for the effective area Eq. 3.22 becomes Eq. 3.23:

$$Ae = \frac{Vp \times D}{4 \times Np \times B_{max} \times f} = \frac{(Vin - Vqe) \times D}{4 \times Np \times B_{max} \times f}. \tag{3.23}$$

To find the area of the window, the area of the windings (Wra) must be determined from the area of the primary (Ap), the area of the secondary (As), and the assumed current density (J = 300 A/m^2) using Eq. 3.24.

$$Ap = \frac{Itprim_{rms}}{J}, \tag{3.24a}$$

$$As = \frac{Itsec_{rms}}{J}, \text{and} \tag{3.24b}$$

$$Wra = 2 \times (NpAp + NsAs) = 2 \times \frac{NpItprim_{rms} + NsItsec_{rms}}{J}. \tag{3.24c}$$

The winding is assumed to use about forty percent of the window area; therefore, the window utilization factor Ku is set to 0.4, and Eq. 3.25 is used to solve for the area of the window (Aw):

$$Aw = \frac{Wra}{Ku} = 2 \times \frac{NpItprim_{rms} + NsItsec_{rms}}{J \times Ku}. \tag{3.25}$$

By using the autotransformer turns ratio N and combining equations 3.22 and 3.25 into Eq. 3.26, the minimum area product in m^4 is determined:

$$Ap = AeAw = \frac{(Iprim_{rms} + (N-1) \times Isec_{rms}) \times D \times Vp}{Ku \times 2B_{max} \times f \times J}. \tag{3.26}$$

By operating H7C4 ferrite material by TDK corporation at a conservative maximum flux density of 0.2 Tesla (Fig. 3-5), the value of the area product is found to be 5.759 x 10^{-8} m^4:

$$Ap = \frac{(18.3A + (1.5-1)\times 10.2A)\times 0.91\times 51.35V}{40\%\times 2\times 0.2Tesla\times 40kHz\times 300\frac{A}{m^2}}, \text{ and}$$

$$Ap = 5.759\times 10^{-8}\, m^4 = 5.759\times 10^{4}\, mm^4.$$

Several transformer designs were attempted based on the required area product of 5.759 x 10^4 mm^4. Initially a TDK PQ40/40 core with an area product of 6.55 x 10^4 mm^4 was chosen. However, it was determined that a TDK ETD44 core with an area product of 5.334 x 10^4 mm^4 would provide similar performance and would be easier to wind. The actual benefits of choosing this core will become apparent in the following sections. The TDK information [1] on the two cores is provided in Table 3-6 for reference during the design of the windings.

Table 3-6 Autotransformer Core Data

(Source: TDK Ferrite Cores Catalog [3])

Parameter	ETD44 Core	PQ 40/40 Core
Effective Core Area (Ae)	175 mm^2	201 mm^2
Window Area (Aw)	305 mm^2	326 mm^2
Area Product (Ap)	57590 mm^4	65530 mm^4
Core Volume (Ve)	18000 mm^3	20450 mm^3
Inductance/$turns^2$ (AL)	4000 nH/N^2	4300 nH/N^2
Maximum Foil Width (FW)	1.0 "	1.0 "

3.3.1.2 Windings Design

Because of the desire to optimize the autotransformer design, an evaluation of several types of windings was performed and the resulting design equations are presented. Windings considered for the autotransformer include Litz wire, standard transformer wire, and copper foil. Each type of winding has several advantages and disadvantages.

Litz Wire

Litz wire is normally used for high-frequency power converters with switching frequencies on the order of 200 kHz and higher. The design of Litz wire reduces loss due to the skin effect at these higher frequencies. It also is a stranded wire which is much more flexible than standard transformer wire. The manner in which Litz wire is insulated does not allow for the conductor to comprise as great of a percentage of the window as standard transformer wire or copper foil. Due to the VFPPAT switching frequency of 40 kHz and lower percentage of the window used by the copper, Litz wire was not used for this design.

Standard Transformer Wire

Standard transformer wire offers excellent coupling properties along with the effective use of the core window. However, the rms currents the primary and secondary windings carry cause the required diameter of the transformer wire to be large in order to meet the targeted current density value of $J = 300\ A/m^2$. The use of several twisted wires of a reduced diameter will reduce losses due to the skin effect while still achieving the desired current density. However, this method does reduce the effective use of the window because of the additional insulation of several twisted wires vs. for one wire. In addition, the twisted wire can never be wound tightly enough to occupy the same amount of space as a single wire. Physically, the friction created while twisting and winding the twisted bundle of wires stresses the insulation to a point that may jeopardize reliability.

Two autotransformers were built using the twisted wire method with three #18 AWG wires and one #18 AWG wire used for the primary and secondary, respectively. This configuration did allow for a design with a respectable power loss of the winding. However, the physical implementation of a standard transformer wire design required the core window size to increase, and the design reverted from a PQ40/40 core to a PQ50/50 core. By using the larger core, the design did not achieve the desired balance of power loss between the core and winding. The added core size and difficulty of physical implementation of the windings caused the use of the standard transformer wire to yield to the use of foil windings in the autotransformer.

Foil Windings

When wound correctly, foil windings allow for the most effective use of the core window. The coupling of foil windings is not as effective as standard transformer windings since foil must be wound in layers, therefore increasing the distance of the outer windings from the center leg of the core. Also, the act of layering the foil can cause a design to exhibit larger winding capacitance than for the use of either wire style.

Physically the tapping of the windings for a foil autotransformer can create problems and cause the design to favor physical considerations in place of electrical characteristics. For example, the tapping may require two windings to be adjacent to each other even though the arrangement does not provide the most desirable coupling for the windings. Problems like this can lead to a transformer imbalance, which can cause flux walking or transmission of the 40 kHz switching frequency to the output as an undesired harmonic.

Copper foil is available in various thicknesses using the units of mils (0.001") and widths in integer values of inches (1", 2", etc.). The best method to insulate foil is to use capton tape, which is available in widths based on integer units of inches. This creates an insulating problem by not allowing the tape to extend beyond the foil enough to electrically insulate it. Capton tape can be ordered in custom widths, but the required minimum orders result in a great expense and a large amount of unused stock. A solution is to reduce the foil width, which decreases the cross sectional area of the copper and raises its resistivity and increases the windings losses. A second solution of overlaying the tape was implemented even though it increased the amount of window area taken up by the tape and therefore reduced the amount of window area the copper foil could use.

Foil windings were determined to be the most effective for the autotransformer design. Many of the problems associated with the use of foil windings can be solved by careful use of insulating and winding methods. The most desirable foil width is one inch. Both of the cores chosen thus far can accommodate a foil width of one inch (FW = 1").

Autotransformer Windings Design Equations

The final autotransformer design is shown in Fig. 3-7. To calculate the number of primary windings (Np), Eq. 3.23 is rearranged and the result is rounded to the next highest even integer (even integers assure the secondary can be wind in full turns rather than fractional turns). This calculation is performed using the ETD44 data from Table 3-6:

$$Np = \frac{D_{max} \times Vp}{\Delta B \times Ae \times 2f} \times 10^6 = \frac{0.91 \times (53V - 1.65V) \times 10^6}{0.4Tesla \times 175mm^2 \times (2 \times 40kHz)} = 8.4\ Turns.$$

Rounding 8.4 to the next highest even integer results in the number of primary turns being Np=10 turns. Eq. 3.23 is rearranged to verify that the number of primary turns will not cause the transformer to exceed the desired of flux excursion of 0.4 Tesla:

$$\Delta B = \frac{D_{max} \times Vp}{Np \times Ae \times 2f} \times 10^6 = \frac{0.91 \times (53V - 1.65V) \times 10^6}{10T \times 175mm^2 \times (2 \times 40kHz)} = 0.335\ Tesla.$$

After determining the flux excursion to be appropriate with Np=10 turns, it is a simple manner to determine the number of secondary turns Ns:

$$Ns = Np \times (N - 1) = 10T \times (1.5 - 1) = 5\ turns.$$

With the number of primary and secondary windings determined for optimal core operation, all that remains is to calculate the foil thickness, number of foil strips to use in parallel, and the resulting window utilization factor (Ku_{actual}). The use of one 5 mil foil winding (FlTh = 0.005") was determined to be optimal for the primary and the secondary. The skin effect will not be present since the skin depth will be greater than 5 mils. Note that the thickness of the capton tape used to insulate the windings is approximately 1.5 mils (TpTh = 0.0015"). Window usage was calculated to be an achievable 41.2%:

$$Total\ Foil\ Area = 2 \times (FlTh + TpTh) \times (Np + Ns) \times FW,$$

$$Total\ Foil\ Area = 2 \times 0.0065" \times 15 Turns \times 1" = 0.195\ sq,"\text{and}$$

$$Ku_{actual} = \frac{TWA\ sq\ inches}{Aw\ mm^2} \times 645.16 = \frac{0.195\ sq\ inches}{305\ mm^2} \times 645.16 = 0.412.$$

3.3.1.3 Autotransformer Measured and Performance Testing Results

The choice of the TDK ETD44 core with the 5 mil foil used for the windings resulted in the autotransformer parameters shown in Table 3-7. An initial comparison of the efficiency of the VFPPAT converter was performed for each of the autotransformers which were wound. This comparison, along with the description of the four transformers, is presented in Fig. 3-6. The results show the foil design using the ETD44 core provides the best converter efficiency. These results directed the study towards pursuing the foil/ETD44 core as the autotransformer of choice for the VFPPAT battery discharger topology.

Table 3-7 Autotransformer Parameter Values

(ETD44 Core, 5 mil foil, Np=10 turns, Ns= 5 turns)

Parameter	Measured Value (40 Khz)
Primary Inductance (Magnetizing Inductance)	472 uH
Secondary Inductance	117 uH
Primary Leakage Inductance	220 nH
Secondary Leakage Inductance	117 nH
Primary Capacitance	11 nf
Secondary Capacitance	5.5 nf
Primary DCR	4 mΩ
Secondary DCR	2 mΩ

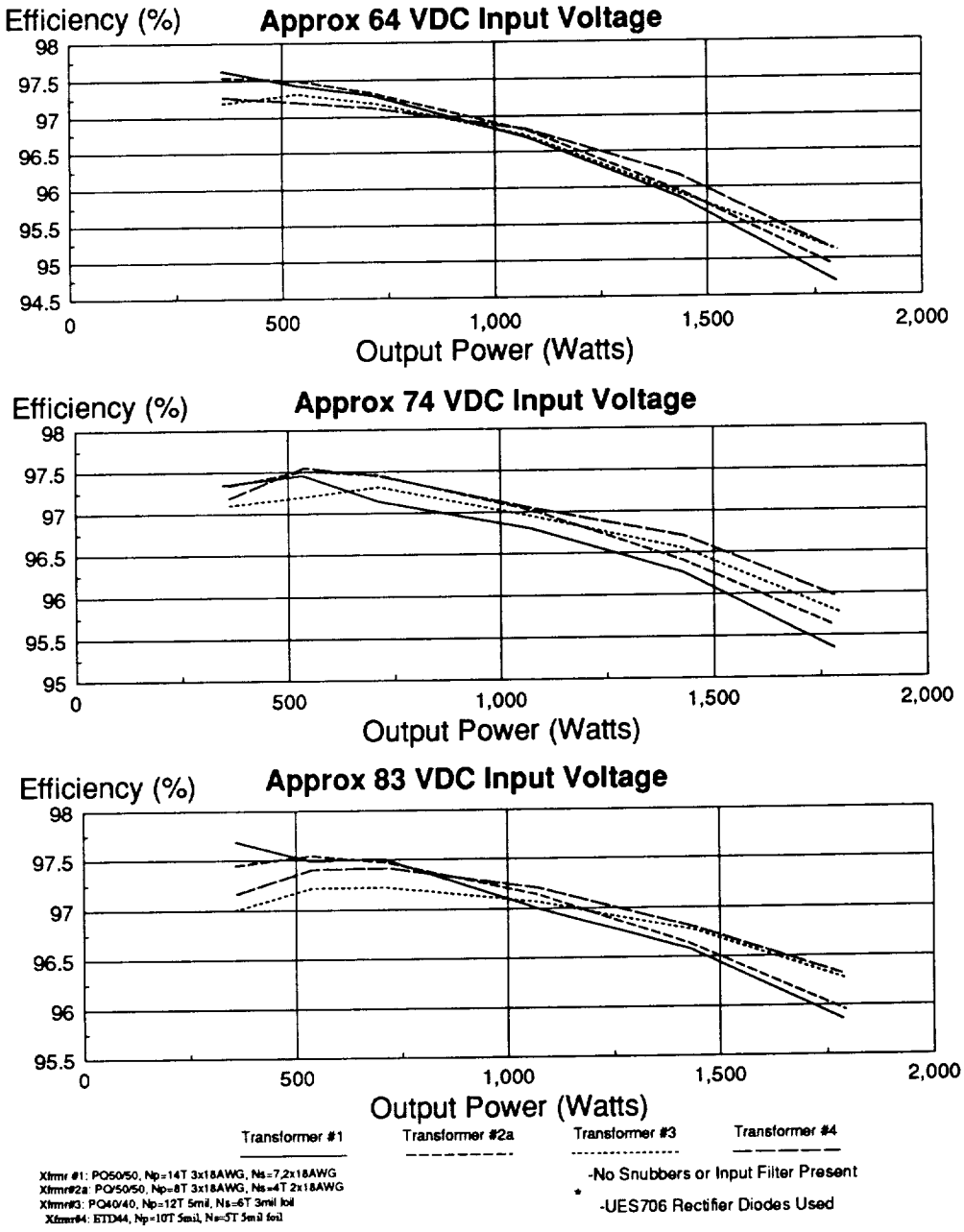


Figure 3-6 VFPPAT Efficiency Measurements Comparing Four Autotransformers

3.3.2 Inductor

The inductance value used by the VFPPAT was chosen to be 94 uH in Section 3.2. The inductor core choice and the windings design are performed in this section. As with the autotransformer, design equations are presented, and the inductor parameters are then calculated.

The core type considered for this design is the Magnetics, Inc. MetGlas class of cut "C" cores. These cores were chosen initially for their high saturation flux density. In addition, the low ac flux of the VFPPAT design will prove beneficial when determining the amount of power dissipated in the air gap.

Due to the desire to use one inch wide foil windings in the inductor, cores that accommodate this foil width were sought. After initial consideration of power handling capability and manufacturer's data, the core chosen was the MetGlas MC0007 cut "C" core. The data for this core is presented in Table 3-8.

Table 3-8 Inductor Core Data

(Magnetics Inc. MetGlas Cut "C" Core # MC0007)

Parameter	Parameter Value
Effective Core Area (AeL)	0.43 cm^2
Window Area (AwL)	2.028 cm^2
Area Product (ApL)	0.872 cm^4
Core Volume (VeL)	3.526 cm^3
Stacking Factor	0.8
Maximum Foil Width (FWL)	1.0 "
Saturation Level (Begins)	0.6 Tesla
Saturation Level (75% Permeability)	1.1 Tesla
Saturation Level (Hard Saturation)	1.6 Tesla
Core Loss (1.1 Tesla, 80kHz)	50 Watts/lb
Weight	0.077 lbs.
Power Handling	0.025 $in.^4$

The important parameter in determining the core effectiveness is the flux density level, BL_{max}. To calculate this value the area of the winding WraL must first be calculated. By assuming two 2 mil foil strips will be 7 mils thick when insulated with capton tape and by assuming the winding can use 75% of the window with bobbin in place, the winding area is calculated in Eq. 3.27 (where 6.5416 scales inches to cm):

$$WrL = \frac{Winding\ Area}{75\%} \times 6.5416, \text{ and} \tag{3.27}$$

$$WrL = \frac{0.007 sq\ inches}{0.75} \times 6.5416 = 0.061\ cm^2.$$

The maximum flux level BL_{max} is calculated in Eq. 3.28:

$$BL_{max} = \frac{WrL}{ApL} \times \left(Iload_{max} + \frac{VL_{max} \times D_{min}}{4L \times f} \right) \times L \times 10^4, \text{ and} \tag{3.28}$$

$$BL_{max} = \frac{0.061 cm^2}{0.872 cm^4} \times \left(15A + \frac{90V \times 0.31}{4 \times 90uH \times 40Khz} \right) \times 94uH \times 10^4 = 1.11\ Tesla.$$

The maximum flux density level of 1.1 Tesla is within the capability of the core material. Tests showed the inductor would saturate at 20 A of dc current, therefore, the peak inductor current of 16.8 A from Table 2.2 should not jeopardize operation of the inductor.

Using the equation provided by the manufacturer, the power handling capability is determined (Eq. 3.29). The resulting value of 0.0264 in^4 is near the core value of 0.025 in^4 from Table 3-8:

$$Power\ Handling = \frac{13 \times Vo \times Iload_{max}}{10 \times BL_{max} \times 2f}, \text{ and} \tag{3.29}$$

$$Power\ Handling = \frac{13 \times 120V \times 15A}{10 \times 1.1 Telsa \times 2 \times 40kHz} = 0.0264\ inches^4.$$

To determine the number of turns for the inductor winding (NL), Eq. 3.30 and IL_{peak} from Table 3-8 are used:

$$NL_{max} = \frac{IL_{peak}}{BL_{max} \times AeL \times 10^{-4}} \times L, \text{ and} \tag{3.30}$$

$$NL_{max} = \frac{16.8A}{1.1Tesla \times 0.43cm^2 \times 10^{-4}} \times 94uH = 34\ turns.$$

Eq. 3.30 is rounded to the next highest integer value. Physically the design is able to accommodate thirty-two turns (NL_{actual}= 32 turns) of the parallel 2 mil copper strips insulated with capton tap.

The gap needed to produce an inductance value of 94 uH is determined by Eq. 3.31. The results are rounded to the integer value of 24 mils. The nature of the cut "C" core requires insertion of 12 mils of paper in each gap to achieve the required gap of 24 mils:

$$lg(mils) = \frac{0.4 \times \pi \times (NL)^2 \times AeL \times 10^{-4}}{2.54 \times L} \times 0.1, \text{ and} \tag{3.31}$$

$$lg(mils) = \frac{0.4 \times \pi \times (32T)^2 \times 0.43cm^2 \times 10^{-4}}{2.54 \times 94uH} \times 0.1 = 24\ mils.$$

The inductor was built and tested, and the resulting parameters are presented in Table 3-9. The actual inductance value was approximately 100 uH, and the device performed well. Therefore the design was considered successful.

Table 3-9 Power Inductor Parameter Values

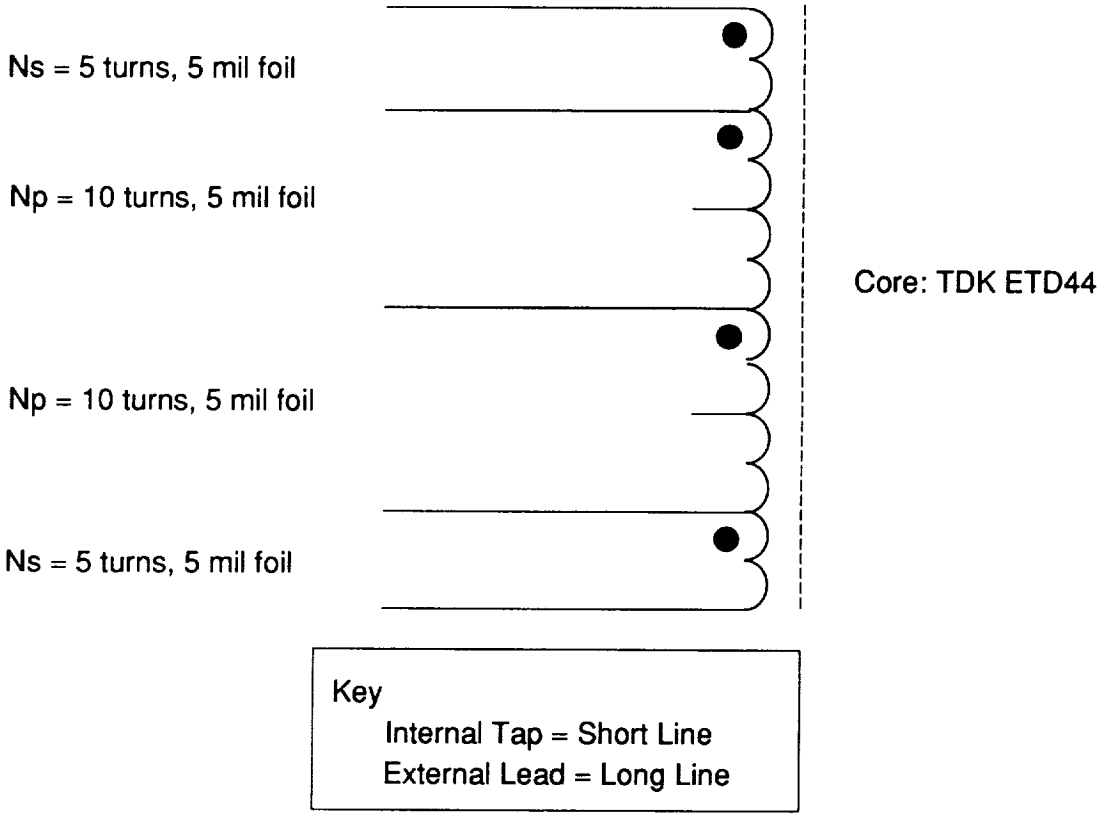
(Core: MC007 Magnetics Inc. Cut "C" Core, 24 mil gap)

(Winding: Two-2 mil foil strips in parallel, NL = 32 turns)

Parameter	Measured Value (80 kHz)
Inductance (No DC Current Applied)	100 uH
Inductance (0-20 A of DC Current Applied)	100 uH
DCR	23 mΩ

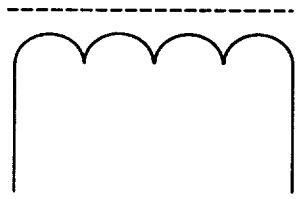
3.3.3 Summary

Design optimization of the magnetics was performed, and the resulting measured parameters of the autotransformer and power inductor were presented. The final schematic of the magnetics is presented in Fig. 3-7. All power stage components have been determined, and the resulting power stage schematic is presented in Fig. 3-8.



a. Autotransformer

Core : Magnetics Inc. Cut "C" Core #MC0007



Windings : 32 turns of two 2 mil foil strips in parallel

b. Inductor

Figure 3-7 Power Stage Magnetics Schematics

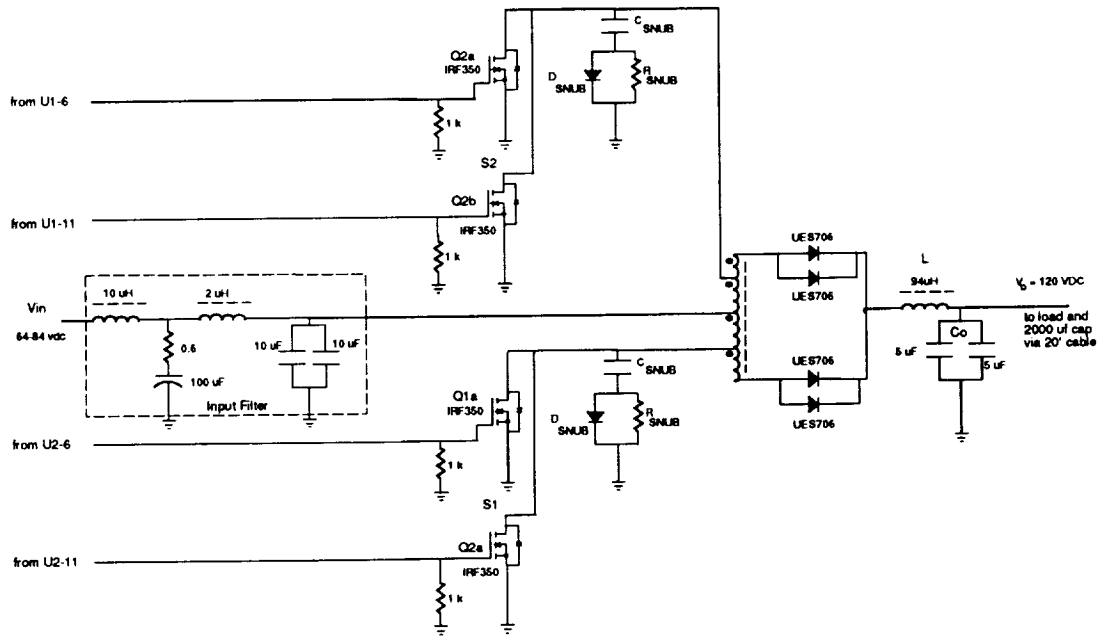


Figure 3-8 Final Power Stage Schematic

3.4 INPUT FILTER

The completion of the power stage design requires that an input filter be considered before the control loop is addressed in order to compensate for any interaction between the converter and filter.

3.4.1 Input Filter Design

The VFPPAT topology is buck-derived and therefore, has a high peak-to-peak input current value which is given by Eq 3.32 (using values from Table 3.3):

$$Iin_{p-p}(\max) = Iprim_{peak} - (Iload_{\max} - (IL_{peak} - Iload_{\max})), \tag{3.32}$$

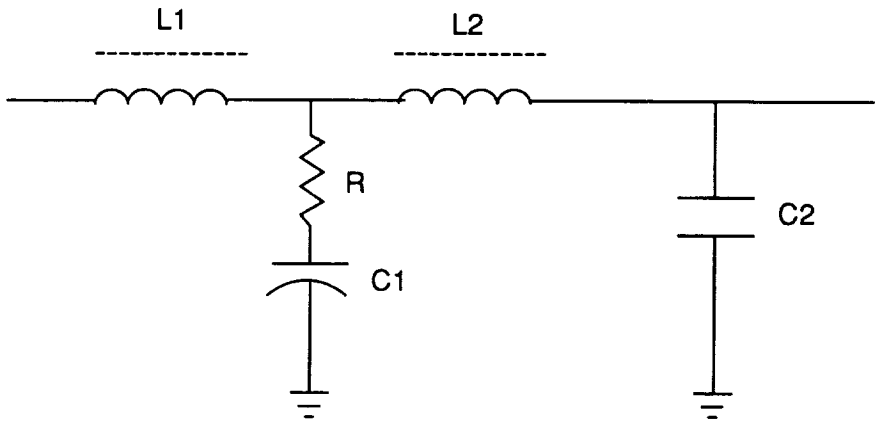
$$Iin_{p-p}(\max) = 42.1Apk - (15Adc - (15.8Apk - 15Adc)) = 29.7\ A\ p-p$$

The specified input current ripple is 250 mA peak-to-peak. In view of the large difference between specified and actual input current, it is obvious that an input filter is needed to attenuate the ripple current. The amount of attenuation (IFAtten) is calculated as follows:

$$IFAtten = 20 \times \log\left(\frac{27.9A_{p-p}}{250mA_{p-p}}\right) = 41\ dB.$$

This 41 dB attenuation will have to take place at the inductor switching frequency 0f 80 kHz. The large amount of attenuation required of the input filter could result in substantially large filter components that could jeopardize the choice of the VFPPAT for the battery discharger topology. Therefore it is necessary to optimize the filter design for

performance and size. Several methods of filtering were investigated. Reference [5] provided insight into reducing the task of filter design, and as a result, a two section filter was chosen. The two-stage filter used is shown in Fig. 3-9.



L1 = 10 uH, L2 = 2 uH, R = 0.6, C1 = 100 uf, and C2 = 20 uf

Figure 3-9 Input Filter Schematic

The gain of the filter is found by analysis of the impedances of the components, and the result is reproduced in Eq. 3.33:

$$Gain = \frac{1 + sRC1}{(1 + sRC1)\left(1 + s\frac{L1}{R}\right)\left(1 + s\frac{L2}{R}\right)(1 + sRC2)}. \tag{3.33}$$

Several assumptions on the relations of the component values reduces Eq. 3.33 to Eq. 3.34:

$$Gain \approx \frac{1}{(1 + sRC2)\left(1 + s\frac{L2}{R}\right)\left(1 + s\frac{L1}{R}\right)}: \tag{3.34}$$

Assumptions:

$$C1 \gg C2, \quad L1 \gg L2, \quad \frac{L1}{R} \ll RC1, \quad \frac{L2}{R} \ll RC1$$

Pole Frequencies:

$$\omega_1 = \frac{1}{RC2}, \quad \omega_2 = \frac{R}{L2}, \quad \omega_3 = \frac{R}{L1}.$$

Thus, the methods used in [5] result in the input filter impedance approximation shown in Eq. 3.35:

$$IFZ \approx \frac{sL1}{\left(1 + s\frac{L1}{R}\right)(1 + sRC2)}. \tag{3.35}$$

The output impedance of the input filter must be less than the closed loop input impedance of the converter by a desired margin in order for the filter to work properly and to avoid interaction with the converter. At this stage the filter design is approximated. The closed loop input impedance of the converter will be verified later.

3.4.1.1 Component Values

The establishment of the filter characteristic can produce the desired Q if the position of the three poles is determined correctly. In order for proper damping to occur, the Q value must be around one. Positioning of the poles was determined by trail and error using a PSPICE program. Pole frequencies are shown below:

$$f1 = 13.26\,kHz,$$

$$f2 = 47.75\,kHz, \text{ and}$$

$$f3 = 9.55\,kHz.$$

This particular input filter requires that C1>C2, which allows the input capacitor value of C2=20 uf chosen in Section 3.2 to remain. The large peak-to-peak current produced by the converter will be seen across C2, which is two low ESR polypropolene style capacitors in parallel. Had another filter style been chosen so that C2>C1, the implementation of a large C2 value would have made for several tantalum capacitors in parallel in order to meet rms current ratings. With the chosen filter C1>C2 requirement, C1 will see very little rms current due to the presence of L2, and C1 can be a tantalum style capacitor, thereby reducing the filter size.

Having determined the size of C2 and the amount of attenuation, the size of the damping resistor is determined by setting the corner frequency of R and C2 at the first corner frequency f1:

$$R = \frac{1}{2\pi C2\,f1} = \frac{1}{2\pi \times 20uf \times 13.26kHz} = 0.6\Omega.$$

The second resonant frequency, f2, is based on the value of R and L2:

$$L2 = \frac{R}{2\pi f2} = \frac{0.6\Omega}{2\pi \times 47.75kHz} = 2\,uH.$$

The third resonant frequency, f3, is based on the value of R and L1:

$$L1 = \frac{R}{2\pi f3} = \frac{0.6\Omega}{2\pi \times 9.55kHz} = 10\ uH.$$

A check of the assumptions reveals that the component values are as desired by the approximation:

$$C1 = 100uf \gg C2 = 20uf, \quad L1 = 10uH \gg L2 = 2uH,$$

$$\frac{L1}{R} = 1.7 \times 10^{-5} \ll RC1 = 6 \times 10^{-5}, \text{ and } \quad \frac{L2}{R} = 3.3 \times 10^{-6} \ll RC1 = 6 \times 10^{-5}.$$

The Q value can now be calculated from the chosen inductor values. As shown the Q value of 1.5 is near the value of 1 desired for optimal damping:

$$Q = \left(\frac{L1}{L2}\right)^{\frac{1}{4}} = \sqrt[4]{\frac{10uH}{2uH}} = 1.5.$$

3.4.1.2 Component Selection

C1 will experience the entire input voltage range of 53 Vdc to 84 Vdc. As was mentioned earlier, C1 carries an insignificant amount of ripple current. Therefore, C1 was chosen based exclusively on the desired value and voltage rating. The style chosen for C1 was a tantalum CLR style capacitor which has a voltage derating of 50% of rated voltage. Therefore, the rated voltage will have to be twice the maximum input voltage or 168 Vdc minimum. The part chosen for the breadboard was rated at 250 Vdc.

The value of L1 was determined earlier to be 10 uH. Implementation of this design was performed using a Magnetics, Inc. MPP core #55071 with 13 turns of three #16 AWG transformer wires in parallel. The paralleling of transformer wires was the result of optimizing the power loss due to the dc resistance of the winding and the skin effect. Core losses for this design are negligible due to the presence of a low ac flux.

L2 is a 2 uH inductor and operates under conditions similar to L1. Therefore, the windings consist of seven turns of three #16 transformer wires in parallel, and the core is a Magnetics, Inc. MPP #55059. The actual measured values of L1 and L2 are shown in Table 3-10. These values are used for analysis of the power dissipation and small-signal performance later in this document.

Table 3-10 Input Filter Measured Magnetics Components Values

Component	Parameter	Measured Value (80 kHz)
L1	Inductance	10.2 uH
L1	DCR	1.5 Ω
L2	Inductance	2.4 uH
L2	DCR	649 mΩ

L1 Core: MPP55071; Magnetics, Inc.

Windings: 13 turns of 3-#16 AWG in parallel

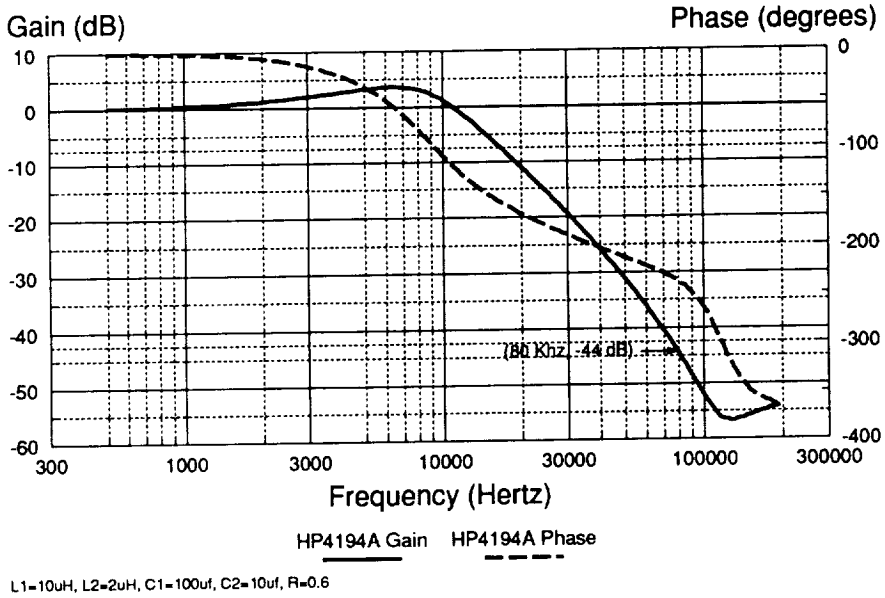
L2 Core: MPP55059; Magnetics, Inc.

Windings: 7 turns of 3-#16 AWG in parallel

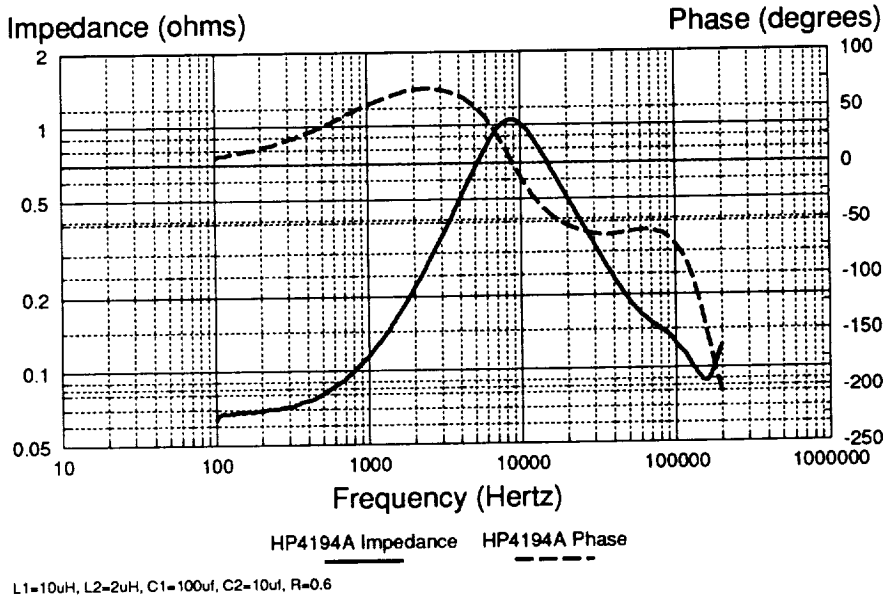
3.4.2 Input Filter Performance

Although [5] is an approximation procedure and not an optimization routine, the filter performance provided the desired attenuation at the inductor ripple frequency of 80 kHz. Figs. 3.10a and 3.10b show the measured gain and impedance, respectively. Each plot also includes the associated phase. The gain diagram shows the attenuation to be 44 dB at 80 kHz, which is in excess of the required 41 dB attenuation.

Fig. 3.11 shows the output impedance of the input filter and the input impedance of the converter. Note that the input impedance of the converter gain plot never crosses that of the output impedance of the input filter. By the input filter having a lower output impedance than the converter impedance, the converter will not interact with the filter, which is the indication of a properly designed input filter.



a. Filter Gain and Associated Phase



b. Filter Output Impedance and Associated Phase

Figure 3-10 Input Filter Measured Characteristics

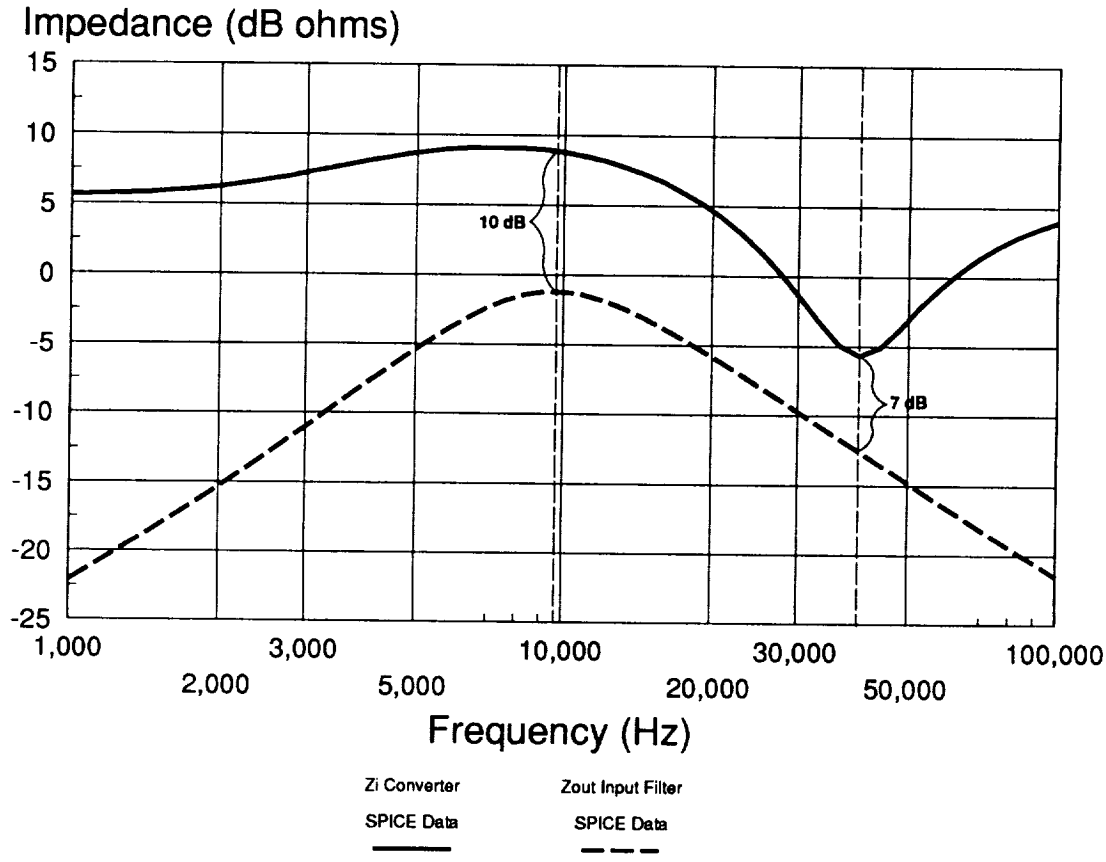


Figure 3-11 PSPICE Model Comparison of the Input Filter Output Impedance with the Input Impedance of the Converter

(Model Conditions for Input Impedance: Low Line, Full Load)

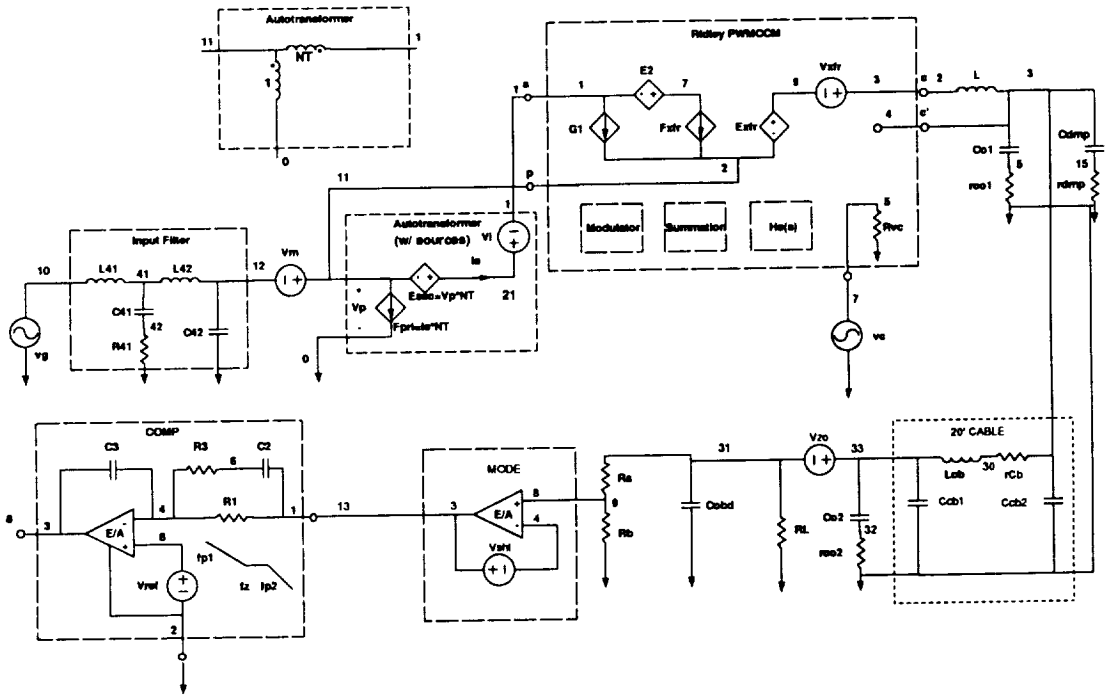


Figure 3-12 Small-Signal PSPICE Model of the VFPPAT

(Using Ridley PWMCCM [7])

3.4.3 Summary

The amount of attenuation required for the input current ripple to meet specified level of 250 mA was found to be 41 dB. From this a two section filter was designed, and the required values were calculated. The selection of the components was then performed.

The performance results indicated the filter would provide proper attenuation without interfering with the converter operation. The small-signal model was also introduced and is used in Section 3.5 for analyzing the small-signal characteristics.

3.5 CONTROL BOARD DESIGN OPTIMIZATION

This section contains the design of all of the control board components, including the PWM and drive circuitry, along with the CIC loop and voltage loop. For convenience, the final control board schematic is presented in Fig. 3-13. Note that the power stage was designed to the input voltage **regulation range** of 53 Vdc minimum, while optimization of the efficiency, and the small and large-signal performance is related to the input voltage **performance or efficient operating range** with a minimum of 64 Vdc input (refer to Table 3.1). Survival related items (such as Vsense in Fig. 3-14) are designed to perform over the regulation range.

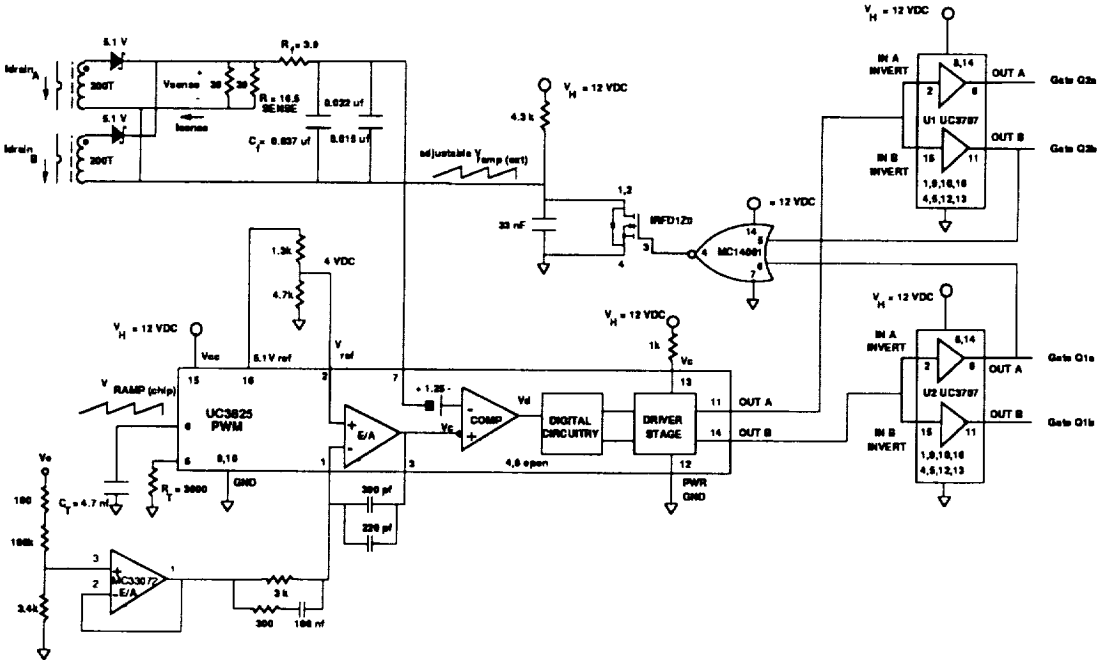


Figure 3-13 Control Board Schematic

3.5.1 Design of PWM and MOSFET Gate Drive Circuitry

PWM Circuitry

The initial choice of a UC1825 PWM was determined in Section 3.2. The choice of this IC was based on the need for dual output drivers which operated 180°out of phase and on the approved parts list [2] available selection.

The manufacturer's data sheet [6] on the UC1825 PWM provides a graph for the user to program the dead time of the gate drive using the timing capacitor C_T. The amount of dead time needed is found from the maximum duty cycle required by the gain (Dmax = 0.91):

$$Dead\ Time = \frac{1}{2} \times \frac{1 - D_{max}}{2 \times f} = \frac{1}{2} \times \frac{1 - 0.91}{80kHz} = 0.56\ usec.$$

The value provided by the data sheet graph is 7 nf. A value of C_T = 4.7 nf was chosen to allow for regulation under worst case conditions and was proven to provide proper regulation at low line (53 Vdc), full load (15 A).

Once the timing capacitor value was chosen, the timing resistor value was selected from the manufacturer's chart for the switching frequency of 40 kHz. A value of R_T = 3900 Ω was chosen, and the resulting switching frequency was 40.2 kHz.

Gate Drive Circuitry

The use of parallel IRF350 MOSFET switching transistors for each primary was discussed in Section 3.1. Implementation of a drive circuit for parallel MOSFETs can become complicated due to mismatched parasitics of the device or wiring. Slow triggering by one device can result in all of the drain current flowing through the parallel device, threatening reliability. For this reason the use of one UC1707 driver chip per switch (ie. per pair of IRF350 MOSFET switches) was used.

The use of the drivers provide fast switching of the MOSFETs. Even though the drive capabilities of the UC1825 PWM are similar to the drivers found in the UC1707 IC, the UC1707 has dual drivers that drive one MOSFET each; this makes for a more desirable arrangement. The UC1707 chips were removed to test the ability of the UC1825 PWM to drive the parallel IRF350 MOSFETs. Although switching times were comparable, the overall current drawn by the control circuit increased and the PWM ran hotter to the touch. Gate switching waveforms are included with the power loss analysis section of this document.

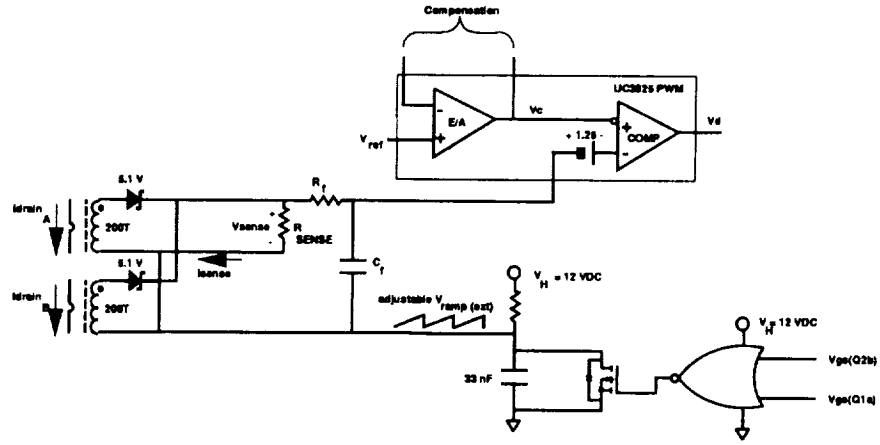
It was necessary to insert a 1 kΩ resistor between the 12 Vdc housekeeping voltage and the driver Vc connection on the UC1825 PWM (pin 13 in Fig. 3-13). This is due to the presence of a 5.7 V zener within the UC1707 driver IC which clamps all input voltages to a digital level. The 1 kΩ resistor limited the current through the zener and avoided the application of the 12 V housekeeping level across a 5.7 V zener. Note that the OR gate (Fig. 3-13) for the timing ramp must be tied to the output of the driver to minimize effects due to delays within the driver. Fig. 3-13 shows a 1kΩ resistor across each MOSFET's gate and source terminals. This resistor is recommended by the manufacturer to prevent false triggering of the gate.

3.5.2 Current-Injection Control (CIC) Loop

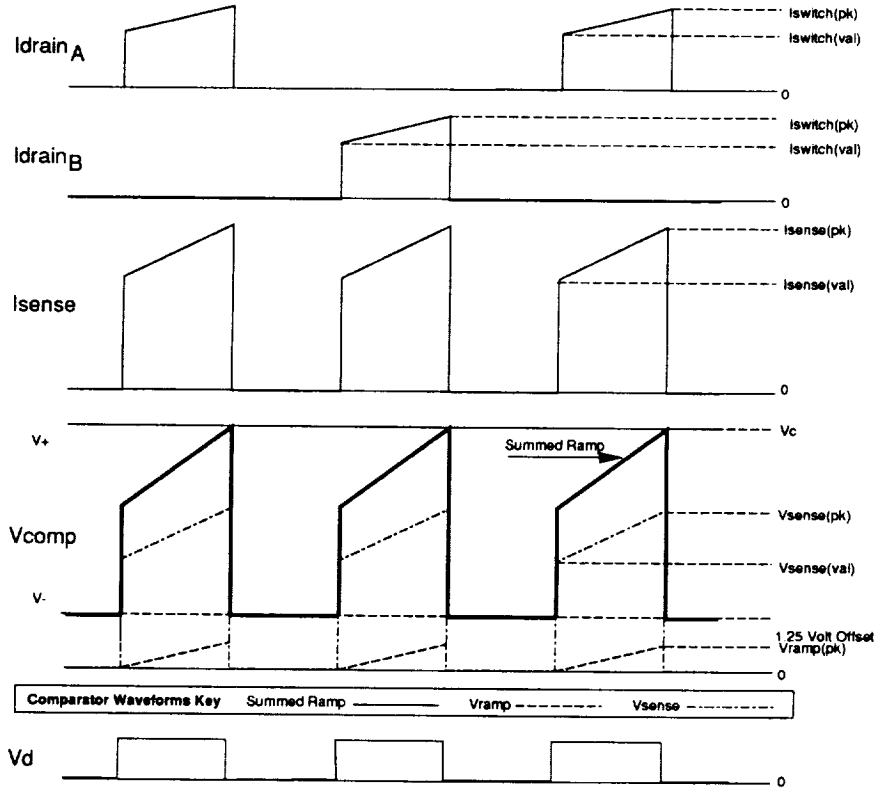
As mentioned earlier, the CIC loop senses the switch current. This allows both the dc and ac components to be fed back. The use of the dc level is essential to maintaining flux balance within the autotransformer. The ac slope of the waveform contributes to the performance of the CIC gain characteristic by its relation to the external ramp slope [7].

Determining Parameter Values

The current loop schematic and accompanying waveforms are pictured in Fig. 3-14. In deciding to use the UC1825, one of the limiting factors was the low output level produced by the error amplifier. This level of 4.5 V is further reduced by an internal offset voltage of 1.25 Vdc at the other comparator input as shown in Fig. 3-14 (pin 7 Fig. 3-13). The summation of a ramp and sense voltage (Vsense) would have to be lower than 4.5 V - 1.25 V = 3.25 V. This level could be difficult to achieve due to the amount of attenuation required to step down the peak switch current (Isw_{peak} = 25.3 A) to a level of Isense. Any large switching spikes could generate noise and false trigger the PWM comparator. With the alternative of the design of a discrete PWM circuit, the goal was to retain the use of the UC1825 PWM.



a. Schematic



b. Waveforms

Figure 3-14 CIC Loop Schematic and Waveforms

With reference to Fig. 3-14, the design of the CIC loop components began with the calculation of the sense voltage (Vsense). This value was based on the error amplifier output voltage, the 1.25 V offset, and the maximum external ramp value $Vramp_{max}$. $Vramp_{max}$ was chosen to be 1 V. The actual ramp value was varied to attenuate the peaking of the converter at half of the switching frequency [7]:

$$Vsense_{max} = VE/A_{min} - Vramp_{max} - 1.25\ V\ offset, \tag{3.36}$$

$$Vsense_{max} = 4.5V - 1.0V - 1.25\ V\ offset = 2.25\ V.$$

Design of the sense resistor is based on the turns ratio of the current sense transformer (N2) and the value of Vsense. The desire to reduce the current in the secondary of the current sense transformer results in values of N2 between 100 and 200. This will reduce the peak current $Isense_{peak}$ to levels of 253 mA and 127 mA, respectively, allow for a reasonable sense resistor value (Rsense), and reduce the wire gauge of the secondary winding. Based on these predictions, N2 was selected to be 200. The primary carries high current and will remain a straight wire of one turn. The value of Rsense can now be determined:

$$Rsense_{max} = \frac{Vsense_{max}}{Isense\ \max} = \frac{Vsense_{max}}{\frac{Isw_{peak}}{N2}}, \tag{3.37}$$

$$Rsense_{max} = \frac{2.75V}{25.3A} \times 200Turns = 21.73\Omega.$$

The actual value used for Rsense was 16.5 Ω.

The leading edge of the Vsense waveform will exhibit a large spike which can be attributed to the peaking of the switch current at turn ON. This peak must be filtered or it will cause false triggering of the switches. The filter arrangement consists of an RC filter network (R_f and C_f in Fig. 3-14). The value of C_f is determined experimentally to be 37 nf which allows proper regulation to occur over all line and load ranges. The value of R_f

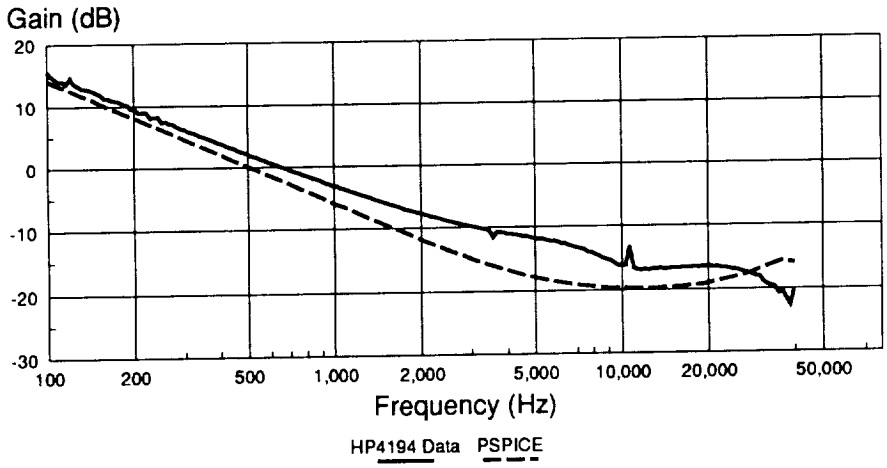
is then calculated so that the corner frequency of the filter is at least ten times greater than the 80 kHz switching frequency to avoid introducing additional phase lag in the loop. The calculation of R_f is as follows:

$$R_f \leq \frac{1}{2\pi \times C_f \times 10f} = \frac{1}{2\pi \times 37nf \times 10 \times 80kHz} = 5.4\Omega.$$

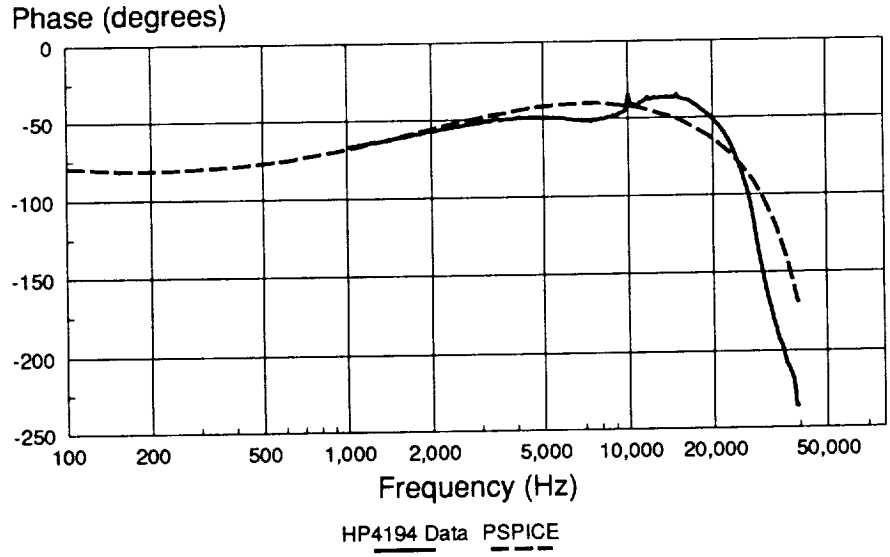
The value used for R_f was 3.9 Ω.

Resulting New Plant Characteristics (CIC Loop Closed)

The use of a CIC loop reduces the open-loop control-to-output transfer function to a single pole role off (where the single pole replaces the double pole formed by the output capacitor and inductor) as shown in [7]. This makes compensating the current loop easier. The open-loop transfer function was measured only after the slope of the external ramp was determined experimentally to be 7.9×10^4 V/sec. Fig. 3-15 shows the predicted and measured gain and phase of the new plant. The plot shows the gain exhibiting a slope of -1 up to the ESR zero of the 2000 uf bus capacitor which is at 3.4 kHz and a cross-over frequency of 664 Hz. Agreement with the model is good.



a. Gain



b. Phase

Figure 3-15 Open-Loop Control-to-Output Characteristic with CIC Loop Closed

3.5.3 Voltage Loop Design and Optimization

The introduction of the new plant obtained when measuring the control-to-output transfer function with the CIC loop closed allows the designer to begin developing the compensation network. The chosen compensation network and resulting characteristics are presented in Fig. 3-16. Note that the voltage follower is present for two reasons. First, the voltage follower represents the mode controller amplifier that will be incorporated when the battery discharger is mated to the system. Second, the output of the op amp provides a virtual impedance of zero which eliminates the impedance interaction of the attenuation resistors Ra and Rb so that the control loop performance is easier to calculate and obtain. The amount of attenuation provided by Ra and Rb is given in Eq. 3.38:

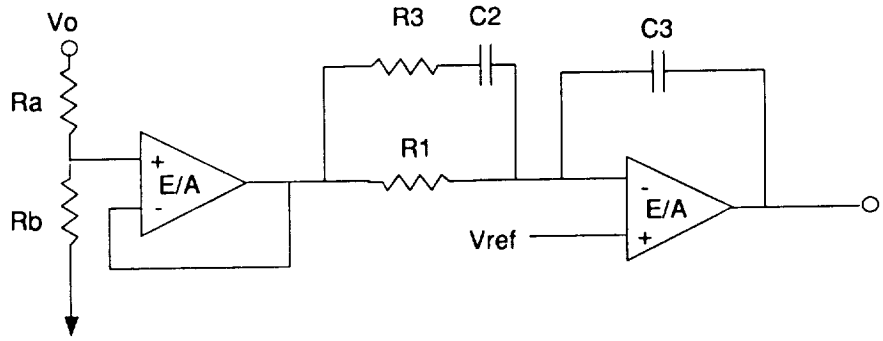
$$Output\ Attenuation = 20 \times \log \frac{Rb}{Ra + Rb}, \tag{3.38}$$

$$Output\ Attenuation = 20 \times \log \frac{3.4k\Omega}{100k\Omega + 3.4k\Omega} = -29.7\ dB.$$

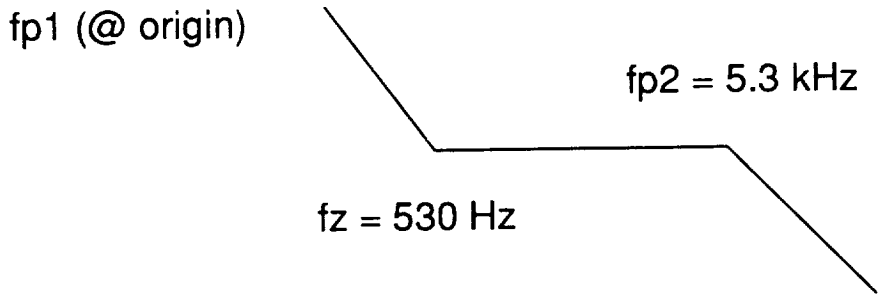
The resulting reference voltage for dc bias of the compensator is 4 Vdc as shown:

$$Reference\ Voltage = \frac{120V \times 3.4k\Omega}{100k\Omega + 3.4k\Omega} = 3.95 \quad Vdc.$$

The compensator characteristic shows that components C2, R1, and R3 determine the poles and zero, while the gain can be manipulated by changing C3. The values chosen for these components were the result of optimization of the loop performance.



a. Schematic



$$Gain = \frac{sC2(R1+R3)+1}{sC3R1(sC2R3+1)}$$

$$Gain \approx \frac{sC2R1+1}{sC3R1(sC2R3+1)} \quad R1 \gg R3 \quad C2 \gg C3$$

$$fp2 = \frac{1}{2\pi C2R3} \quad ; \quad fz = \frac{1}{2\pi C2R1}$$

$$R1 = 3k\Omega, \quad R3 = 300\Omega, \quad C3 = 610pf, \quad C2 = 100nf$$

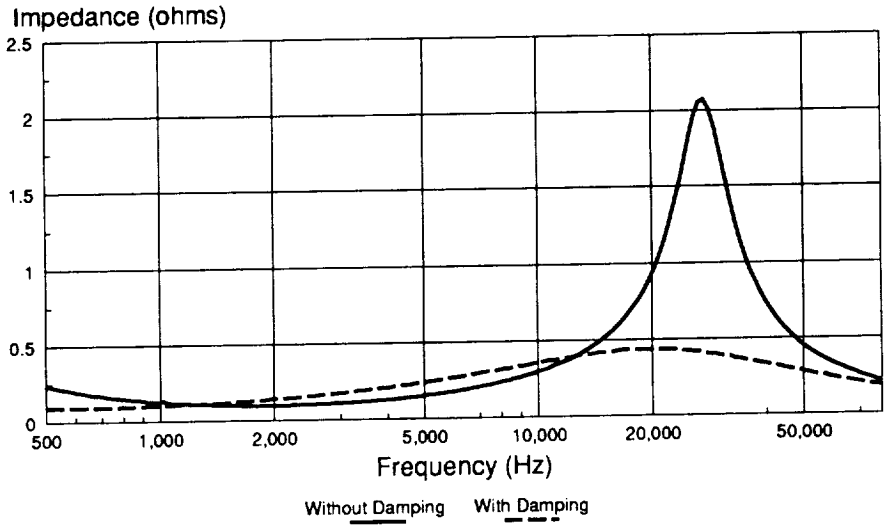
b. Characteristic

Figure 3-16 Compensation Schematic and Characteristic

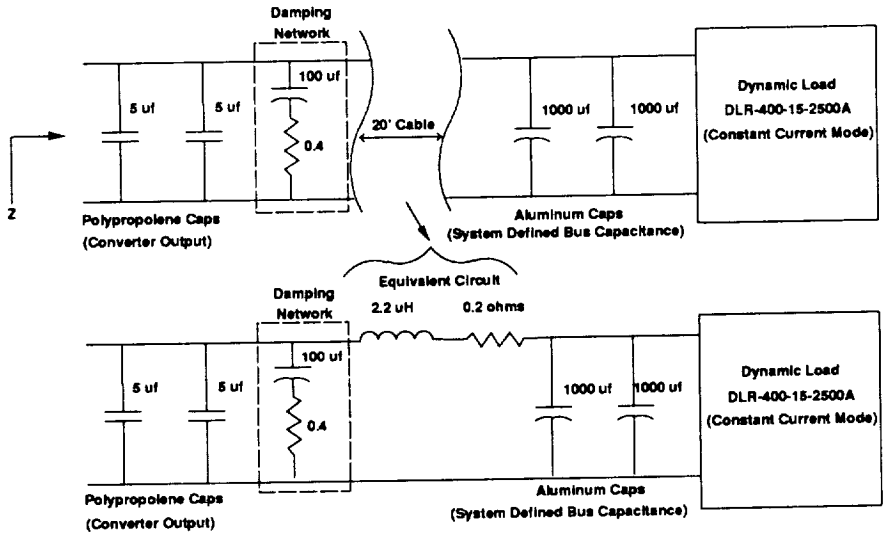
Effects of the 20'Cable

A twenty foot cable of #10 AWG wires exists between the output of the converter and the system-required 2000 uf bus capacitor. The optimization procedure for the compensator took place with the twenty foot, twisted pair of #10 AWG wires taken into consideration. These wires will simulate the actual spacecraft's twisted, shielded pair that will be present between the output of the converter and the 2000 uf capacitor of the load. The resulting inductance of this cable tended to resonate with the output capacitors of the power converter at 27 kHz. This resonance interacted with the optimization of the control loop performance. Therefore, the analysis of the cable and damping network is presented before the small-signal performance data.

The impedance of the output capacitors, cable, and load are shown in Fig. 3-17. Note the load resonates at 27 kHz without the damping network. As will be shown with the small-signal performance data, the addition of the damping network eliminated peaking in the voltage loop and reduced its effect on the output impedance.



a. Measured Characteristic



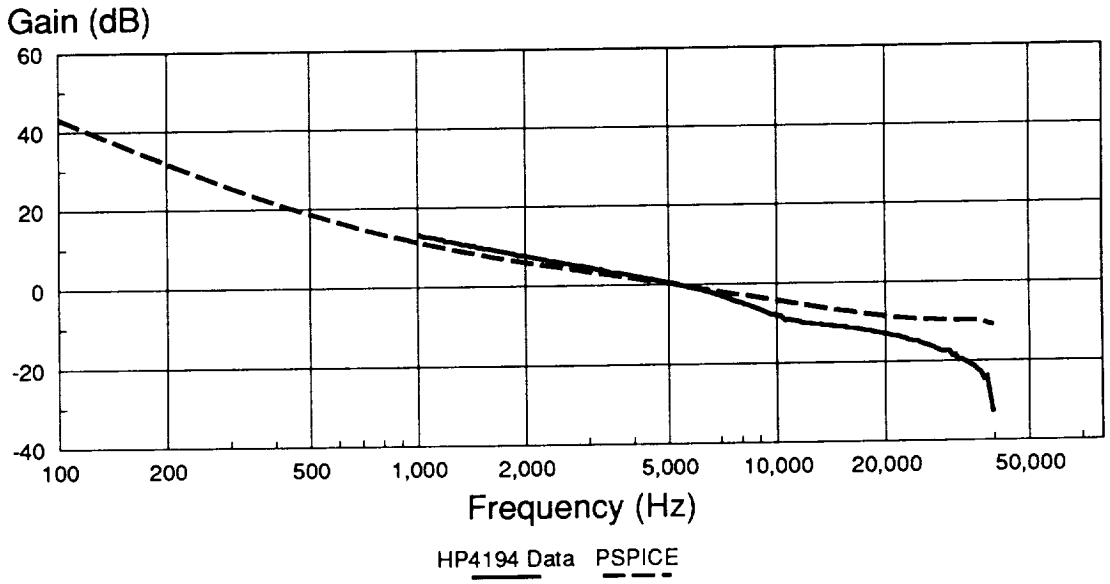
b. Actual and Equivalent Parasitic Schematic

Figure 3-17 Impedance of Output Capacitors, Dynamic Load, and 20' Cable

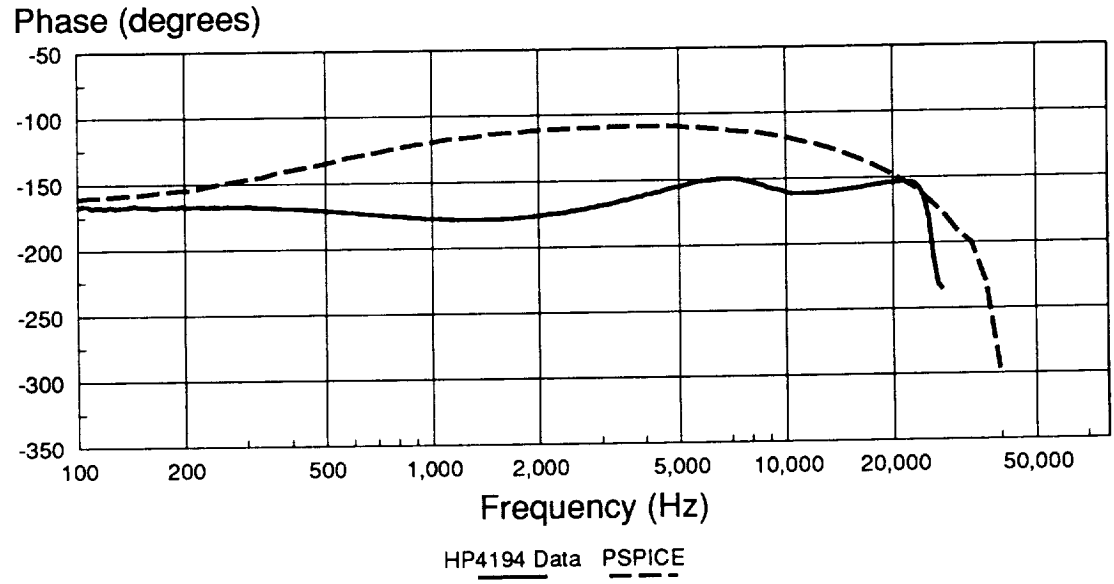
3.5.4 Measured Small-Signal Performance

Voltage Loop Performance

The resulting loop gain performance of the voltage loop (CIC loop closed) is shown in Fig. 3-18 for the case of low line, full load. The loop exhibits a wide bandwidth with a cross-over frequency of 5.3 kHz and a phase margin of 63°, this indicates a stable design. Once again, the model agrees with the measured data. A full performance analysis of the loop over line and load is shown in Figs. 3-19 and 3-20.



a. Gain



b. Phase

Figure 3-18 Loop Performance with 20' Cable; Low Line, Full Load

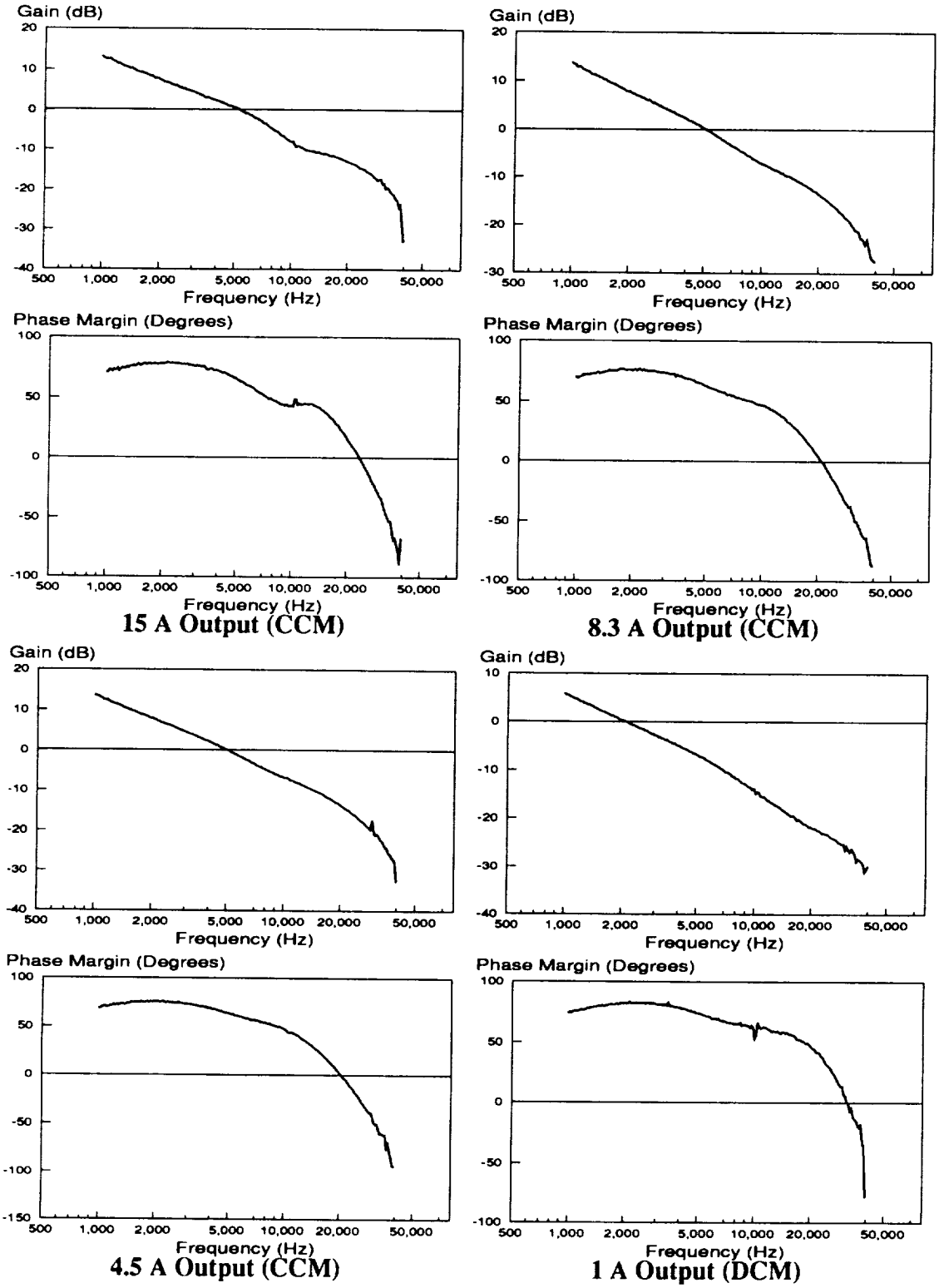


Figure 3-19 Loop Gain With 20 Foot Cable (64 V Input)

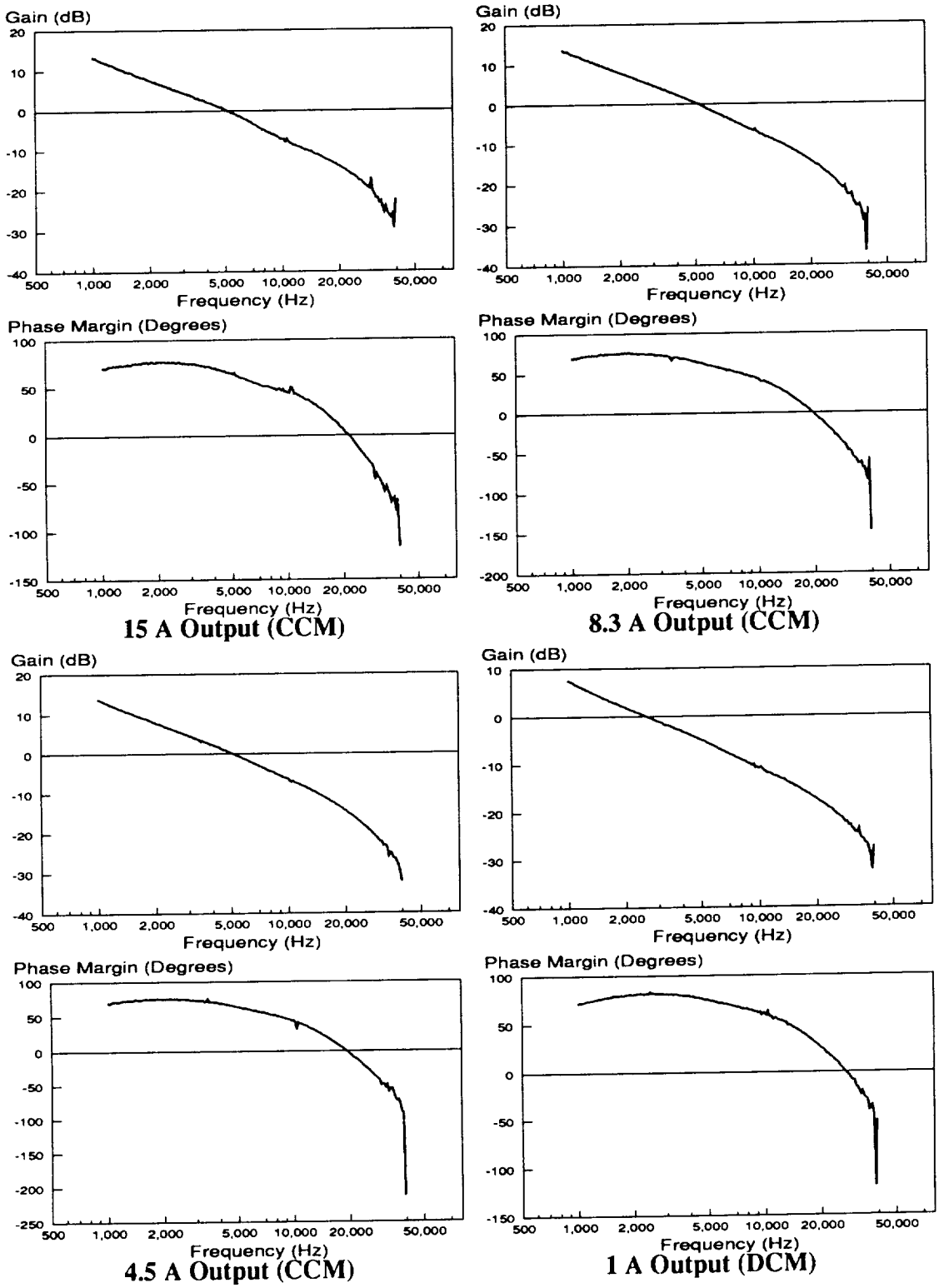
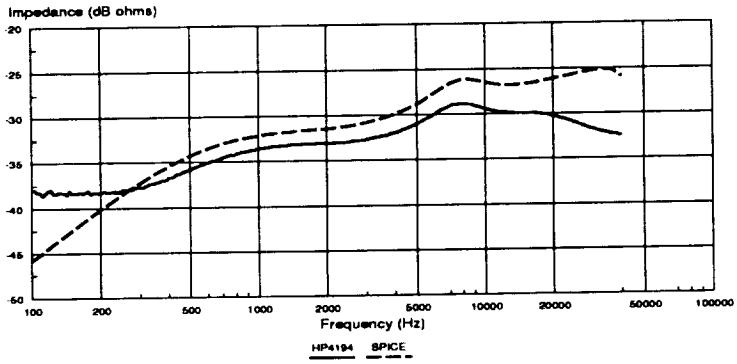


Figure 3-20 Loop Gain With 20 Foot Cable (84 V Input)

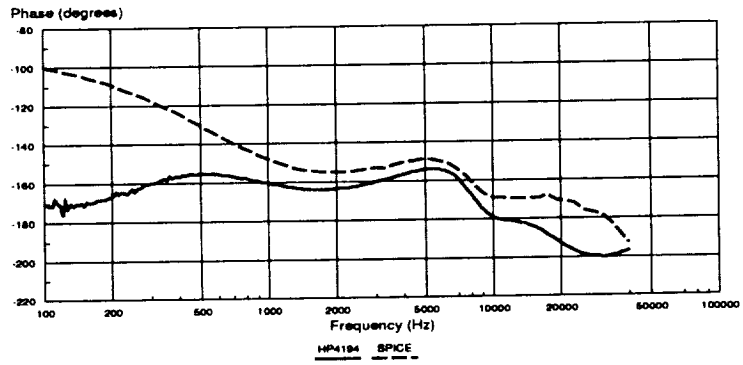
Output Impedance

Output Impedance of the system is shown in Fig. 3-21 in magnitude of dB ohms along with the associated phase. The damping network (Fig. 3-17) reduced the peaking of the output impedance at the frequencies above 5 kHz. Below 5 kHz, the converter has an average of less than 25 mΩ. Above 5 kHz the impedance peaks at 45 mΩ which is the approximate value of the ESR of the 2000 uf capacitor bank. The PSPICE plot verifies the measured data from the HP4194a impedance analyzer to 10 kHz. The accuracy of the measured data above 10 kHz is questionable due to the limited bandwidth of the Dyna-load when used in the constant current mode (which is the only mode available for full output power) .

It is noted that the final spacecraft system will require investigation and optimization of the cable interacting with the battery discharger. The methods discussed here were applied to a cable and 2000 uf capacitor similar to the final product. The actual system will need to be characterized and optimized in order to obtain good performance. A reduction in the peak output impedance is expected to take place when using the actual capacitors due to the reduced ESR. Similarly, using the actual shielded cable should result in improved performance. Figs. 3-22 and 3-23 show the effects a varying load has on the output impedance at input voltages of 64 Vdc and 84 Vdc, respectively.



a. Magnitude



b. Phase

Figure 3-21 Output Impedance with 20' Cable

(Low Line, High Load)

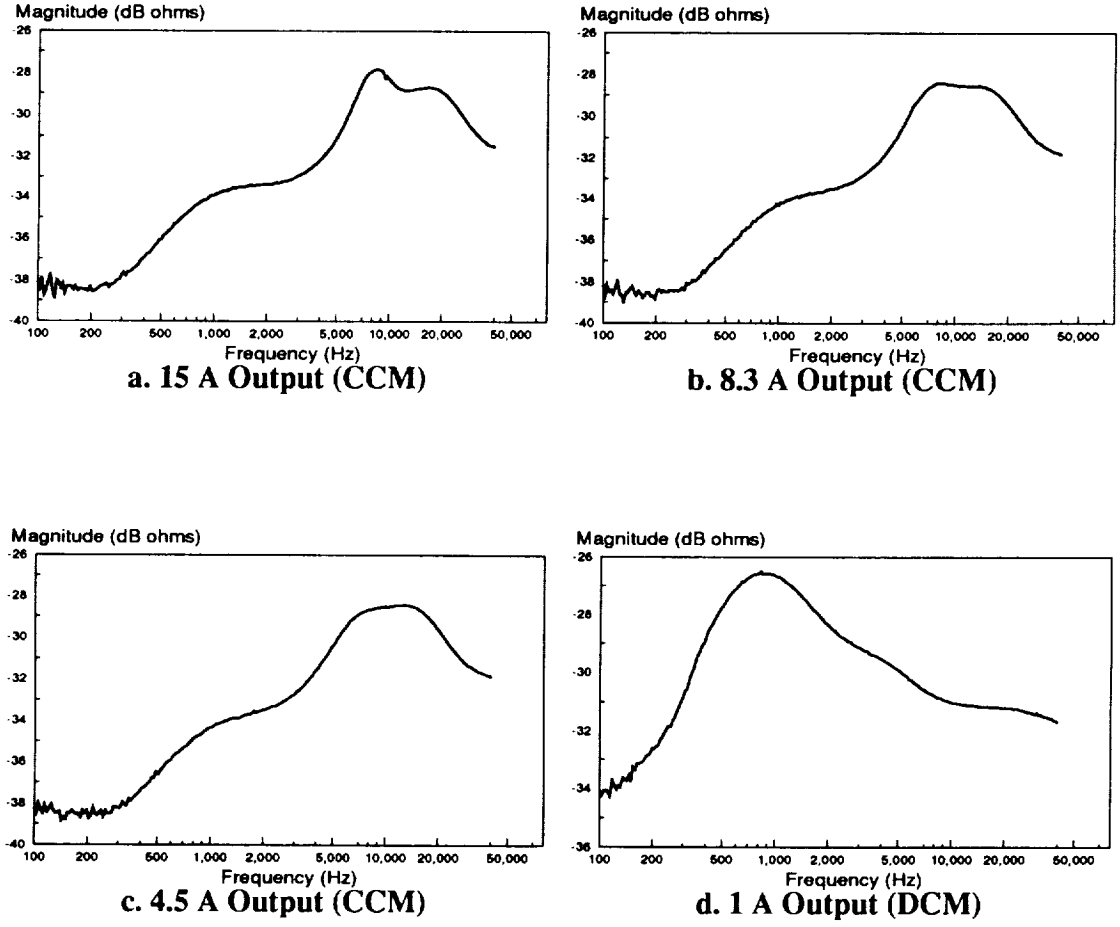
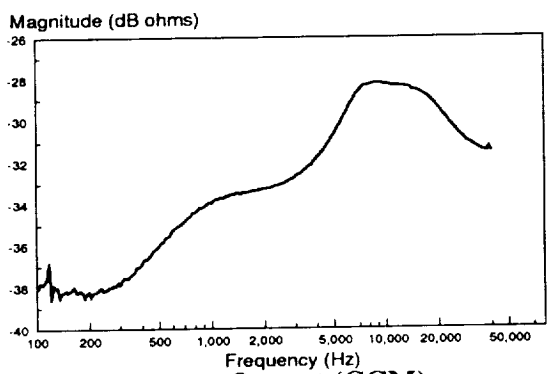
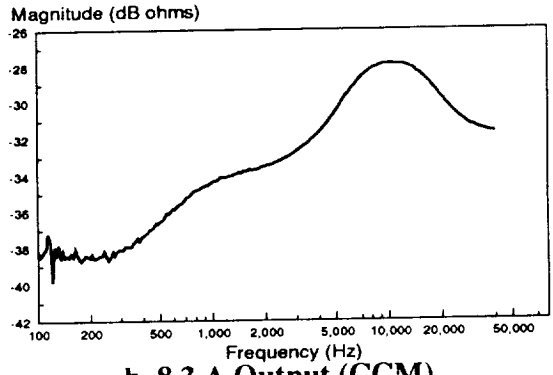


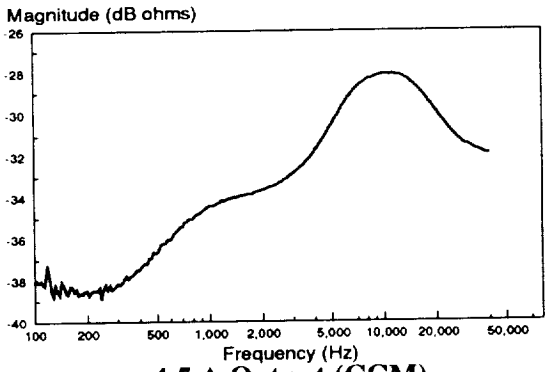
Figure 3-22 Output Impedance With 20 Foot Cable (64 V Input)



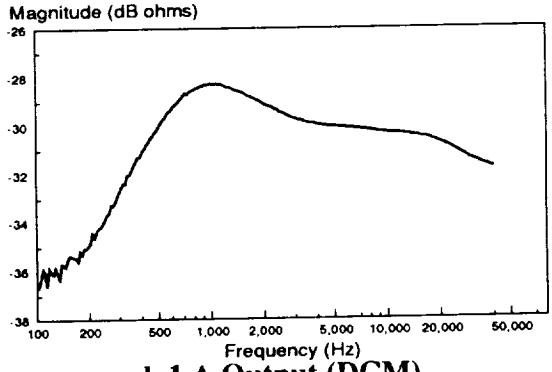
a. 15 A Output (CCM)



b. 8.3 A Output (CCM)



c. 4.5 A Output (CCM)



d. 1 A Output (DCM)

Figure 3-23 Output Impedance With 20 Foot Cable (84 V Input)

3.5.5 Measured Large-Signal Performance

Stepped Output Current

The specifications (Table 3.1) call for the transient performance to achieve a settling time of 10 msec and to retain a peaking range of 115.2 V to 124.8 V. The converter performance shown in Fig. 3-24 achieves a settling time of 0.4 msec with and a critically-damped voltage waveform with peaks of 119.9 V maximum and 119.7 V minimum. The output level difference for the two different current levels can be attributed to the measured breadboard values having a finite gain of the error amplifier and a finite output impedance at dc.

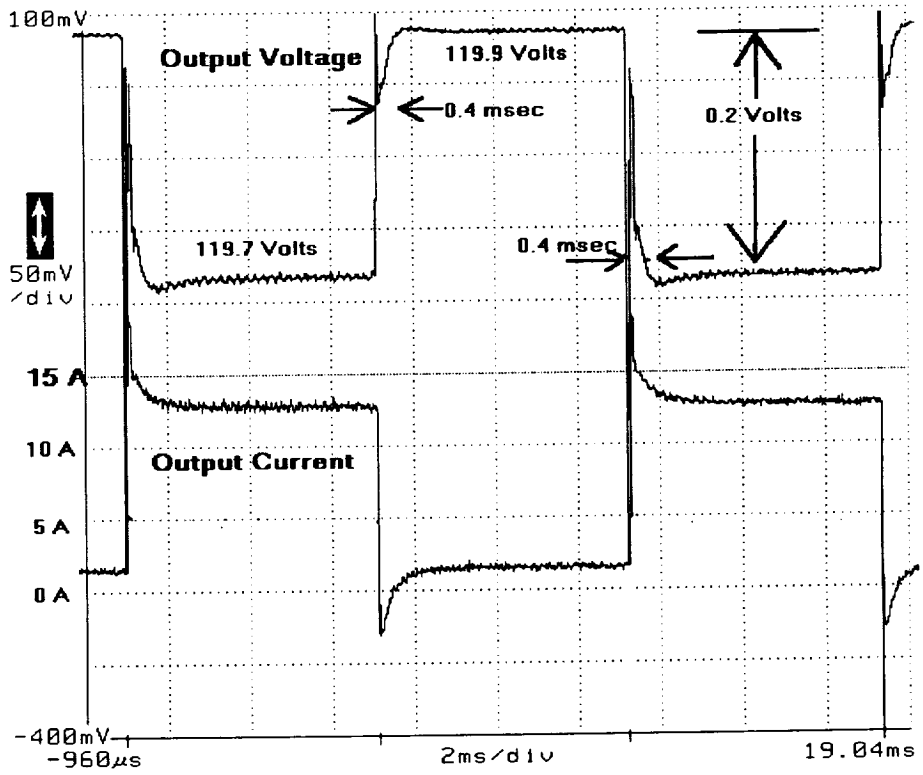


Figure 3-24 Stepped Load Response

(2 A to 13 A)

Output Voltage Ripple

The specified output voltage ripple is 200 mV peak-to-peak as defined in Table 3.1. The actual ripple voltage for inputs of 64 Vdc and 84 Vdc are shown in Figs. 3-25 and 3-26, respectively. The converter complies well with the specified maximum ripple voltage by producing output ripple voltage levels of 50 mV and 70 mV for input voltage levels of 64 Vdc and 84 Vdc, respectively. Note that the higher output ripple voltage which occurs at 84 Vdc input voltage is expected due to the higher peak-to-peak inductor current.

Input Current Ripple

Input ripple current is specified as 250 mA peak-to-peak in Table 3.1. The measured peak-to-peak ripple is shown in Figs. 3-25 and 3-26. The input ripple current levels are 220 mA peak-to-peak and 150 mA peak-to-peak for input voltages of 64 Vdc and 84 Vdc, respectively. Note that the value is higher for the 64 Vdc case as expected due to the higher peak currents entering the autotransformer at the lower voltages.

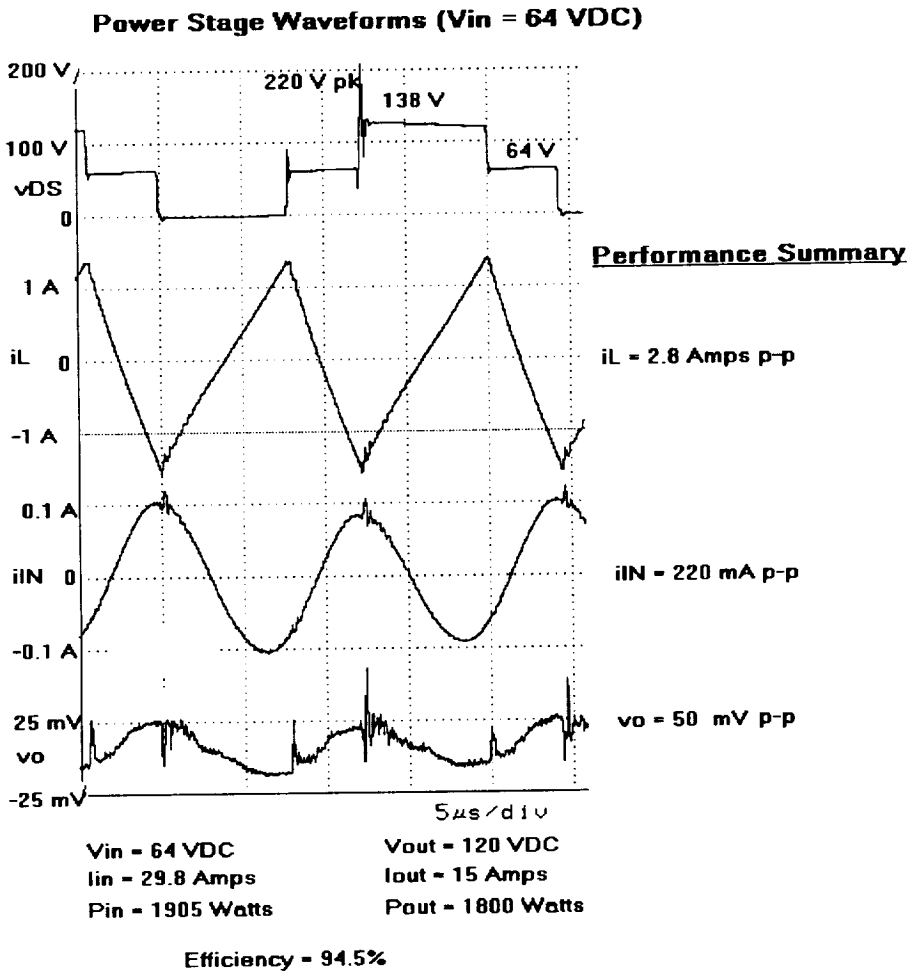


Figure 3-25 Input Current Ripple and Output Voltage Ripple (Vin = 64 Vdc)

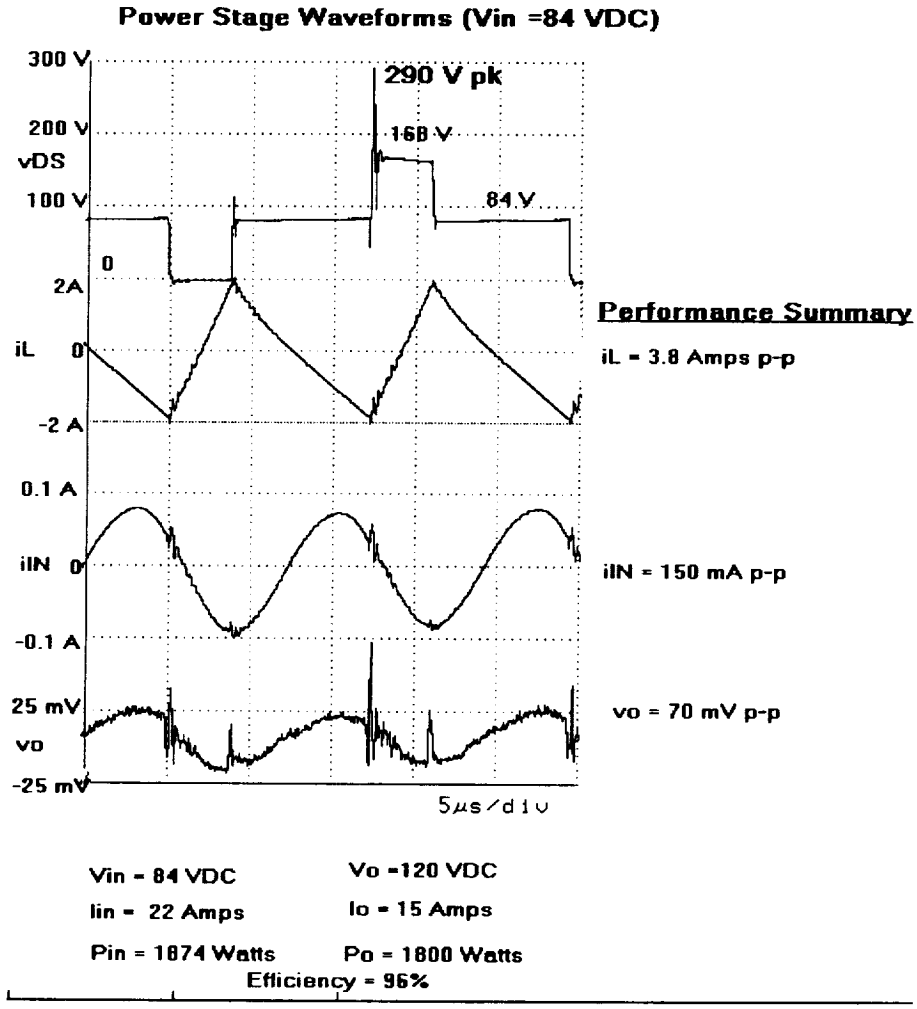
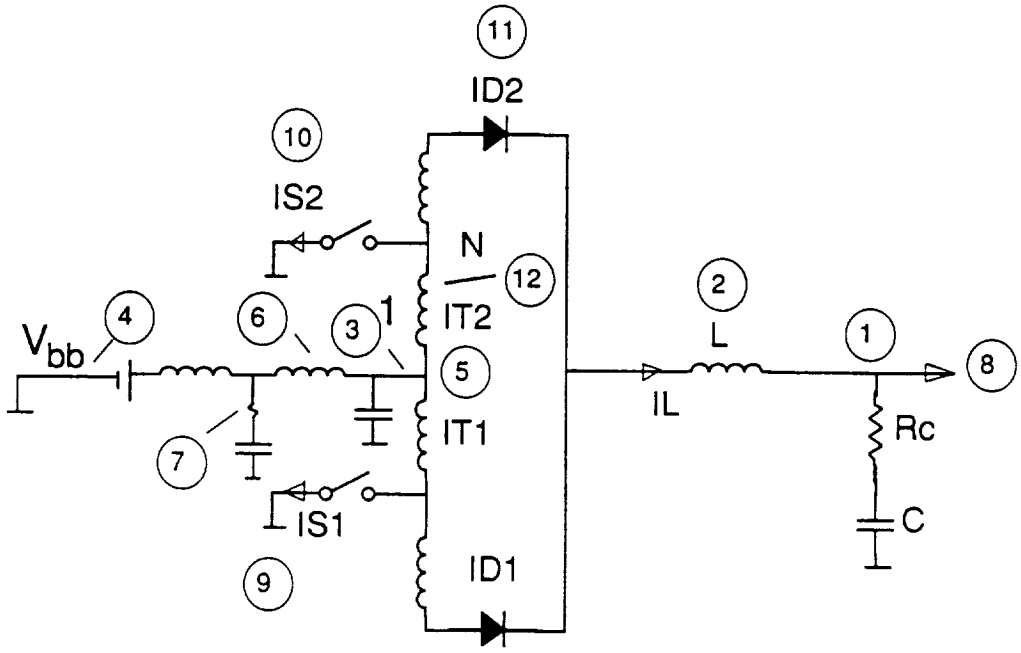


Figure 3-26 Input Current Ripple and Output Voltage Ripple (Vin = 84 Vdc)

3.5.6 EASY5 Model Analysis and Results

The large-signal performance modelling was not within the capabilities of the PSPICE small-signal model shown in Fig. 3-12. Therefore, the large-signal analysis was performed on EASY5 software which was created by the Boeing, Corporation. The following figures (Figs. 3-27 through 3-32) show the basic model and the analysis results of the large-signal simulation to be in good agreement with the measured results of Section 3.6.5.

VFPPAT discharger waveforms



1. Bus voltage
2. Inductor current IL
3. converter input current
4. filtered battery current
5. Converter input voltage
6. Filter (second) inductor current
7. filter damping resistor current
8. Load current
9. Current in switch S1
10. current in switch S2
11. Diode current
12. Transformer winding current IT2

Figure 3-27 EASY5 Power Stage Model Schematic

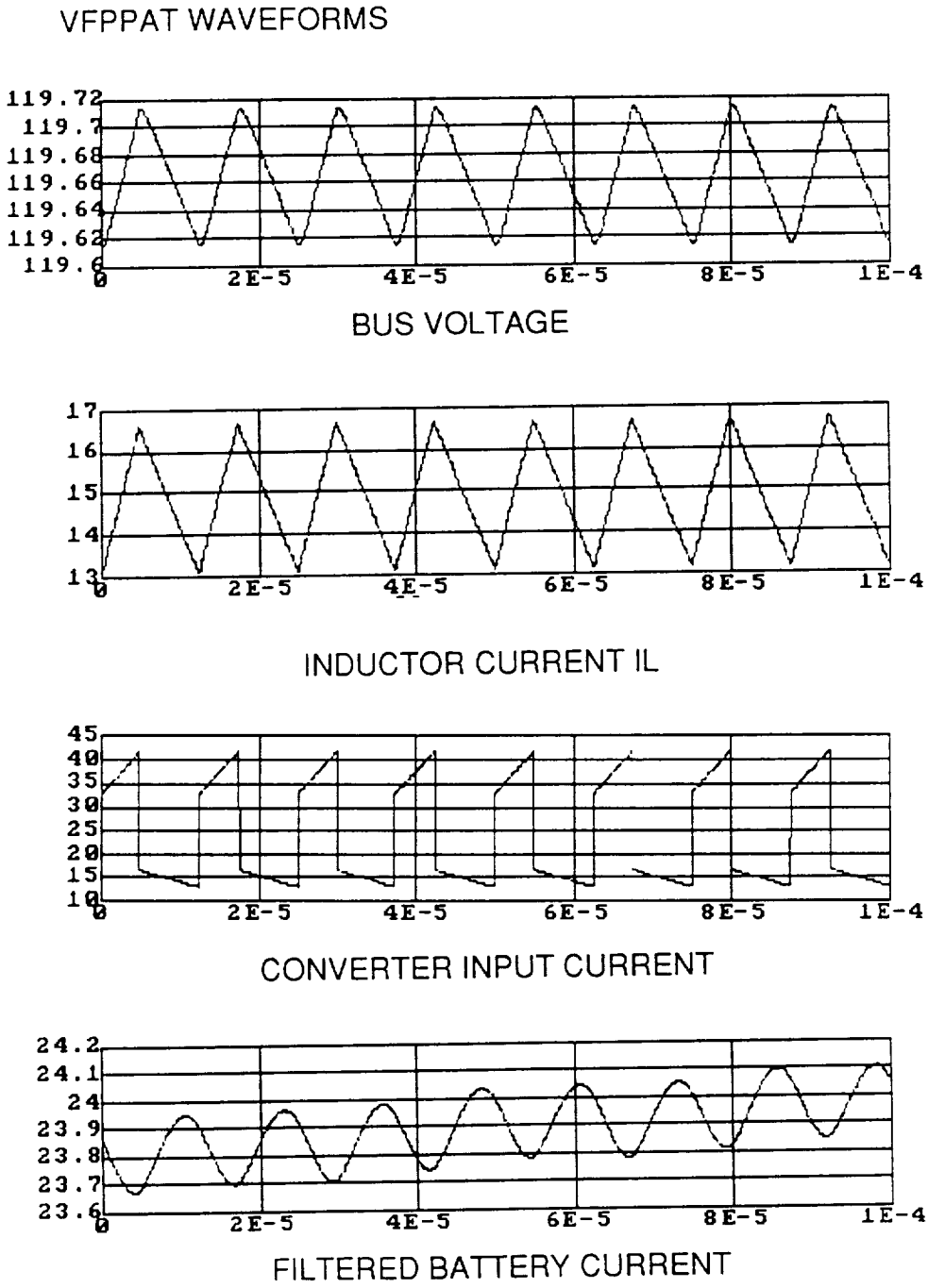


Figure 3-28 VFPPAT EASY5 Waveforms (Low Line, Full Load)

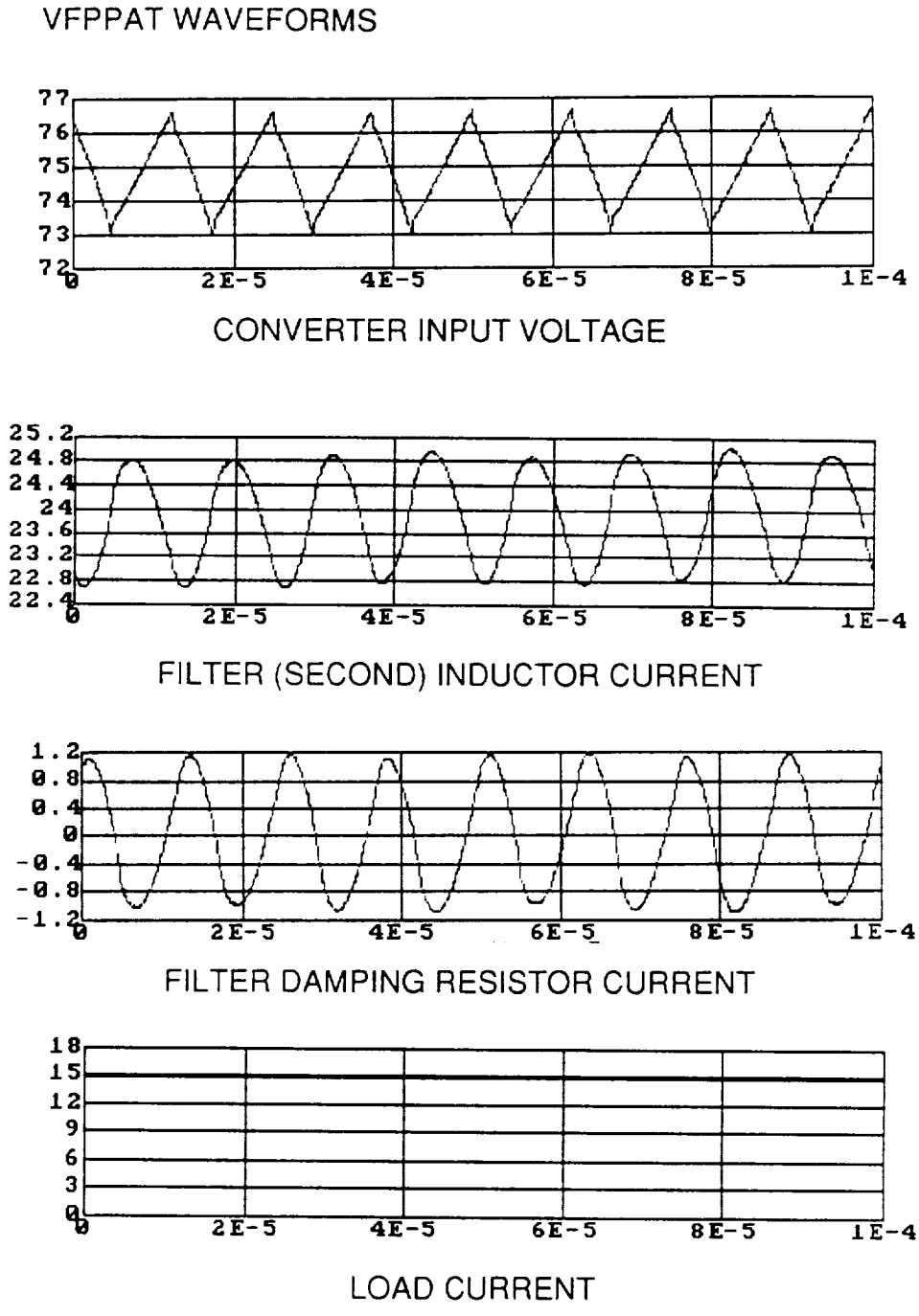
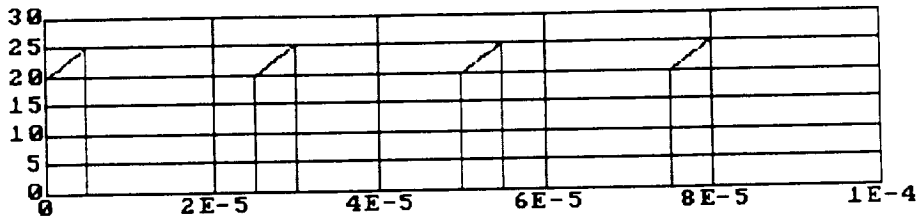
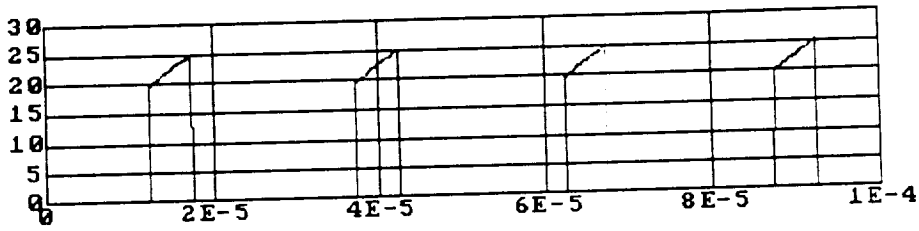


Figure 3-29 VFPPAT EASY5 Waveforms (Low Line, Full Load)

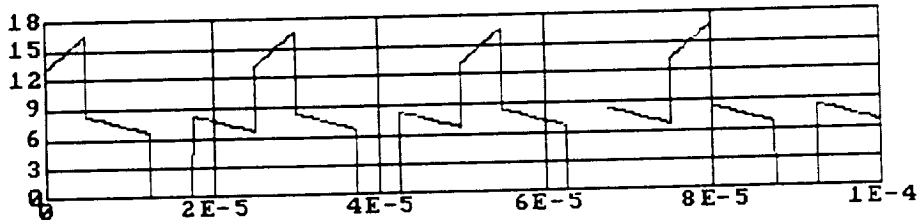
VFPPAT WAVEFORMS



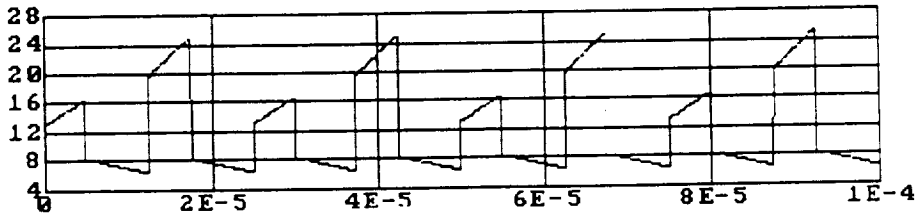
SWITCH CURRENT IS1



SWITCH CURRENT IS2



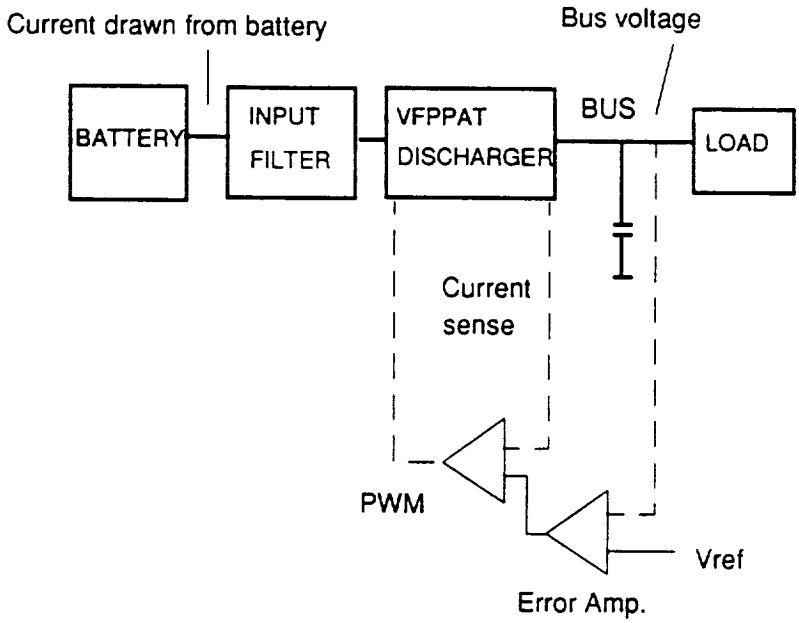
DIODE CURRENT ID2



TRANSFORMER WINDING CURRENT IT2

Figure 3-30 VFPPAT EASY5 Waveforms (Low Line, Full Load)

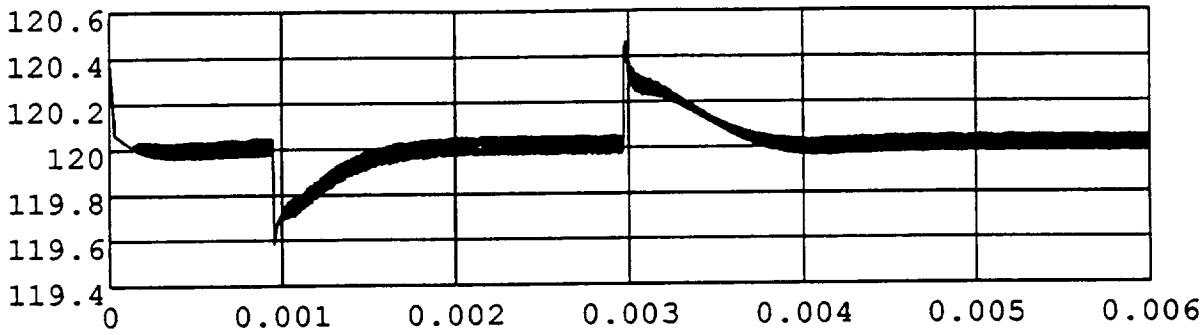
VFPPAT discharger step load test



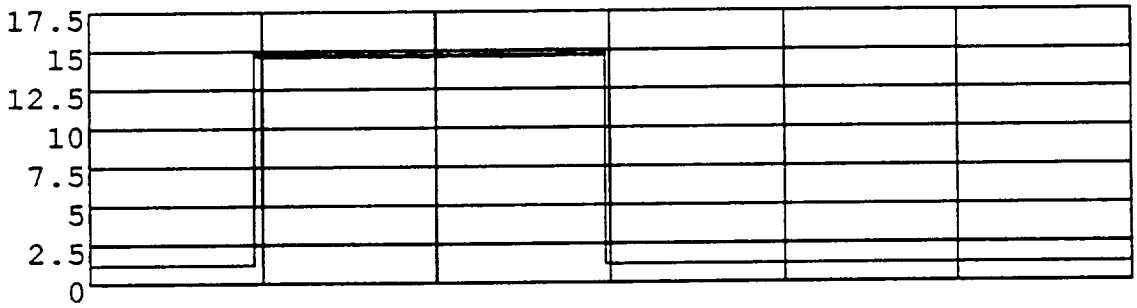
A load step from 1.2 to 15 A is applied
to test bus regulation by the discharger

Figure 3-31 EASY5 Step Load Test Schematic

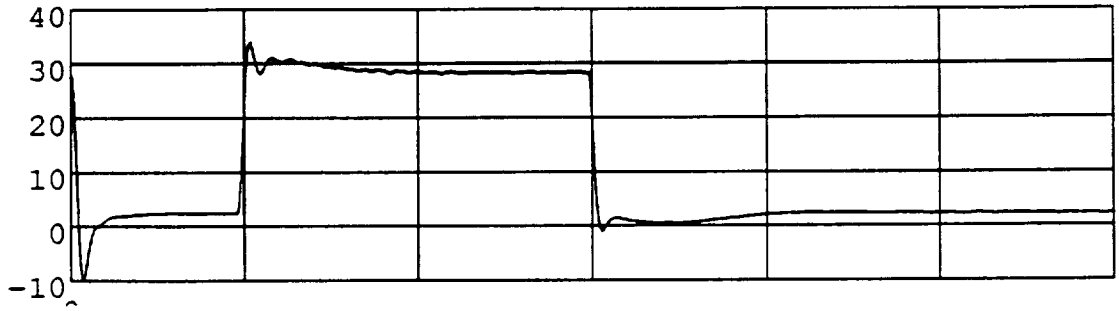
VFPPAT discharger step load test



Bus voltage (V)



Load current (a)



Battery current (A)

Figure 3-32 EASY5 Step Load Test Waveforms

3.5.7 Summary

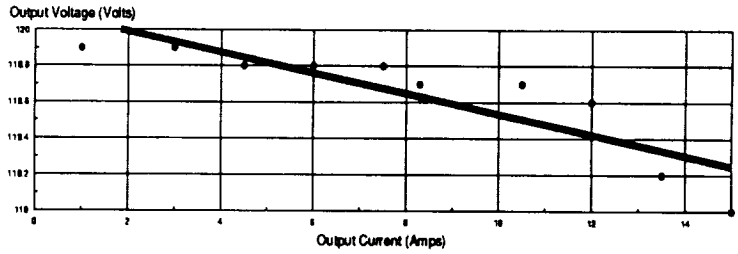
The use of CIC was shown to make closing the voltage loop a much easier process and to help performance. The closed loop design has been presented and the resulting small and large-signal tests show the converter exhibiting excellent performance within the specified levels. Cross over of the voltage loop is 5.3 kHz with a 63° phase margin. The output impedance shows some disagreement between the measured and predicted data. The predicted level for the output impedance never exceeds -27 dB (45mΩ).

3.6 POWER STAGE PERFORMANCE

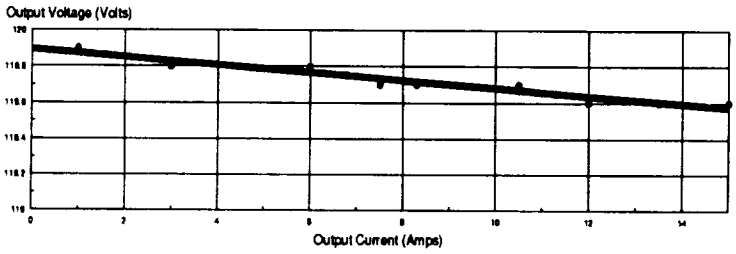
The efficiency and converter regulation are presented as measured at the converter outputs, and power loss of the 20' cable is studied. Analysis of the efficiency includes power losses of the individual components of the power stage and the effects design optimization has on increasing the efficiency. Note that the heat sink temperature during most of the measurements reaches a maximum of 50° C.

3.6.1 Regulation

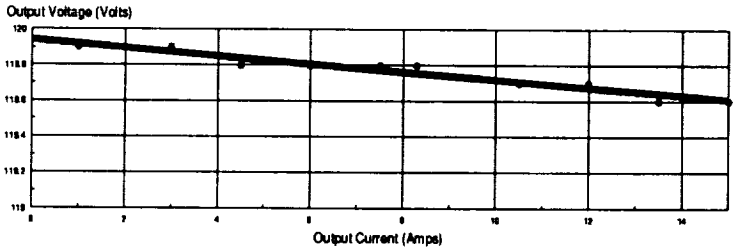
The converter exhibits excellent regulation over varying line and load conditions as shown in Fig. 3-33 where actual data is supplemented with a straight-line approximation. The required regulation range allows the input to be a minimum of 53 Vdc and a maximum of 84 Vdc. Note that the converter output varies only one volt or 0.8% for all line and load changes. The allowed change on the output is $\pm 4\%$ as specified in Table 3-1. Loads measured are from 1 A (120 W) to 15 A (1800 W) out.



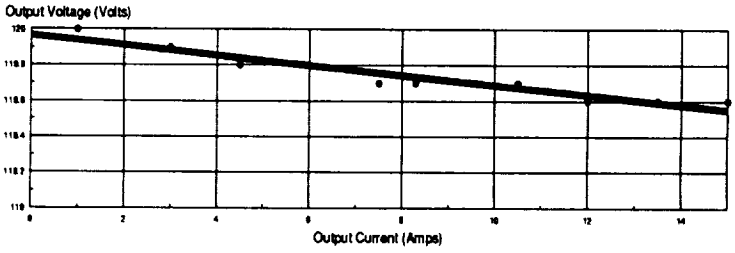
a. Input Voltage = 53 Vdc



b. Input Voltage = 64 Vdc



c. Input Voltage = 74 Vdc



d. Input Voltage = 84 Vdc

Figure 3-33 Output Voltage Regulation Data and Straight-Line Approximation

3.6.2 Efficiency

The efficiency is first presented as it was measured at the input and output terminals of the converter with the 20' cable attached but not included in the efficiency calculations. The individual power loss of the power stage components is then presented, and a loss contribution of the power stage components is shown.

3.6.2.1 Efficiency at the Terminals

The converter efficiency is shown in Fig. 3-34 where the input voltage spans the range of 64 Vdc to 84 Vdc. The targeted efficiency for the converter is 96% at low line (64 Vdc), full load (15 A). The cable robs the converter of 12 W (0.7%) at this operating point as shown in Fig. 3-35. Therefore, at the converter output, the converter will actually see the 94.5% efficiency (Fig. 3-34) at the converter and 93.8% at the end of the 20' cable.

The targeted efficiency for low line, full load was 96%, and the value achieved was 94.5%. An assessment of the difference is provided in the summary at the end of the section.

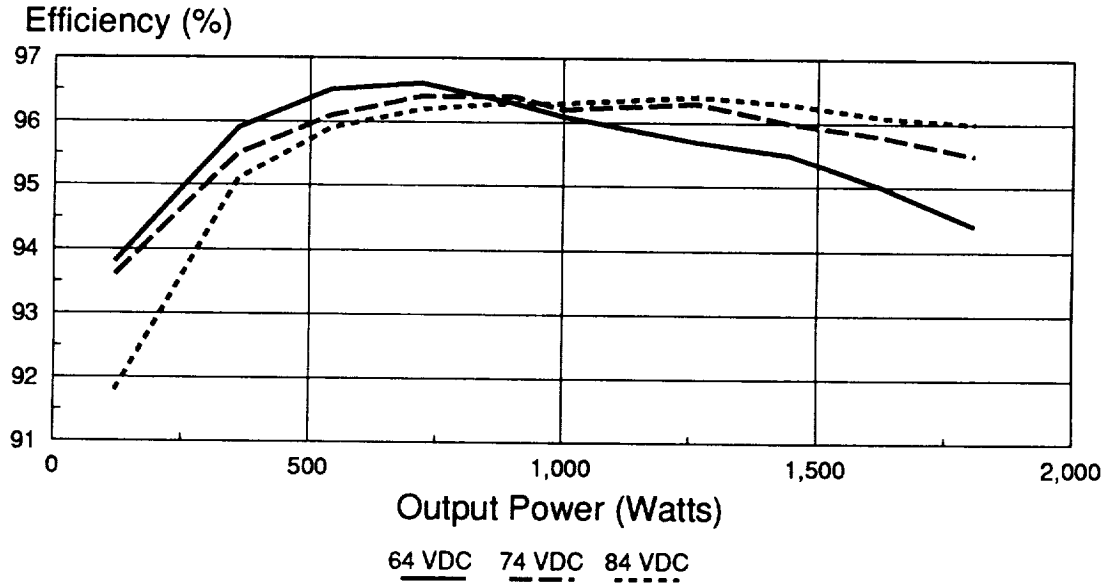


Figure 3-34 Efficiency over Line and Load

(Power loss of the 20' cable has been subtracted.)

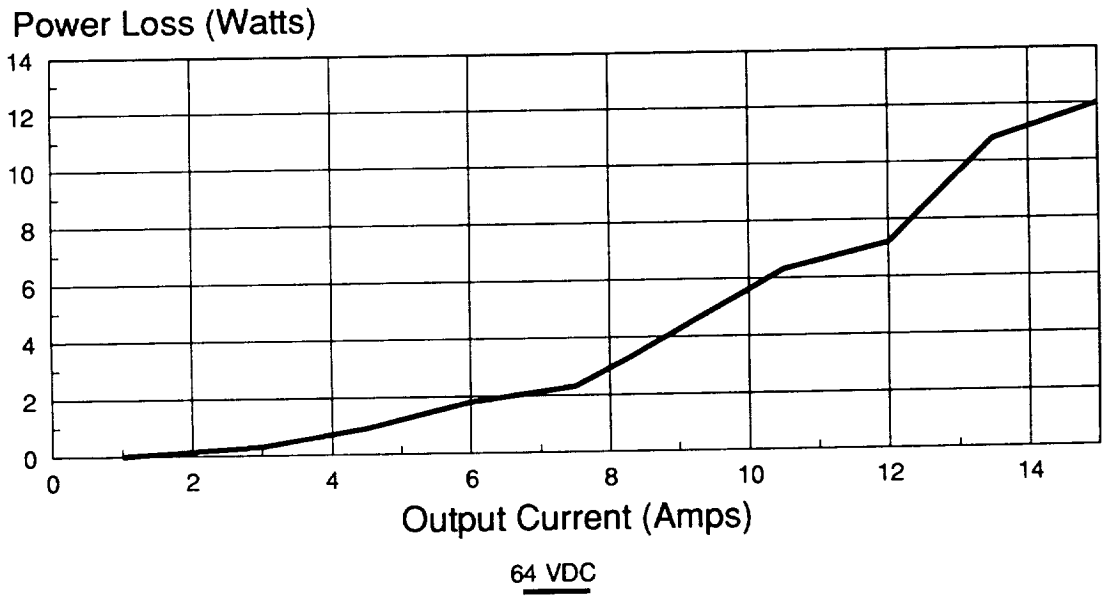


Figure 3-35 Power Lost to 20' Cable Based on Output Current

3.6.2.2 Power Dissipation in the Power Stage Components

The desired efficiency of 96% mentioned in the specifications (Table 3-1) must occur at low line (Vin = 64 Vdc) and full load (Io = 15 A). Therefore, the analysis of the power dissipated by each component will be performed for this operating point.

Figures 3-36, 3-37, and 3-38 show the waveforms for the diode current and voltage, inductor current and voltage, and current into the autotransformer, respectively. These currents are essential for establishing the power dissipation of each component. From Fig. 3-36 the time one switch is on is Ton=7.8 us, and the period is Tp=23.9 us. From these values the duty cycle for low line, full load and the period can be calculated:

$$f = \frac{1}{Tp} = \frac{1}{23usec} = 41.8kHz,$$

$$D_{(low\,line,\,full\,load)} = \frac{Ton}{Tp} = \frac{7.8}{23.9} = 0.326.$$

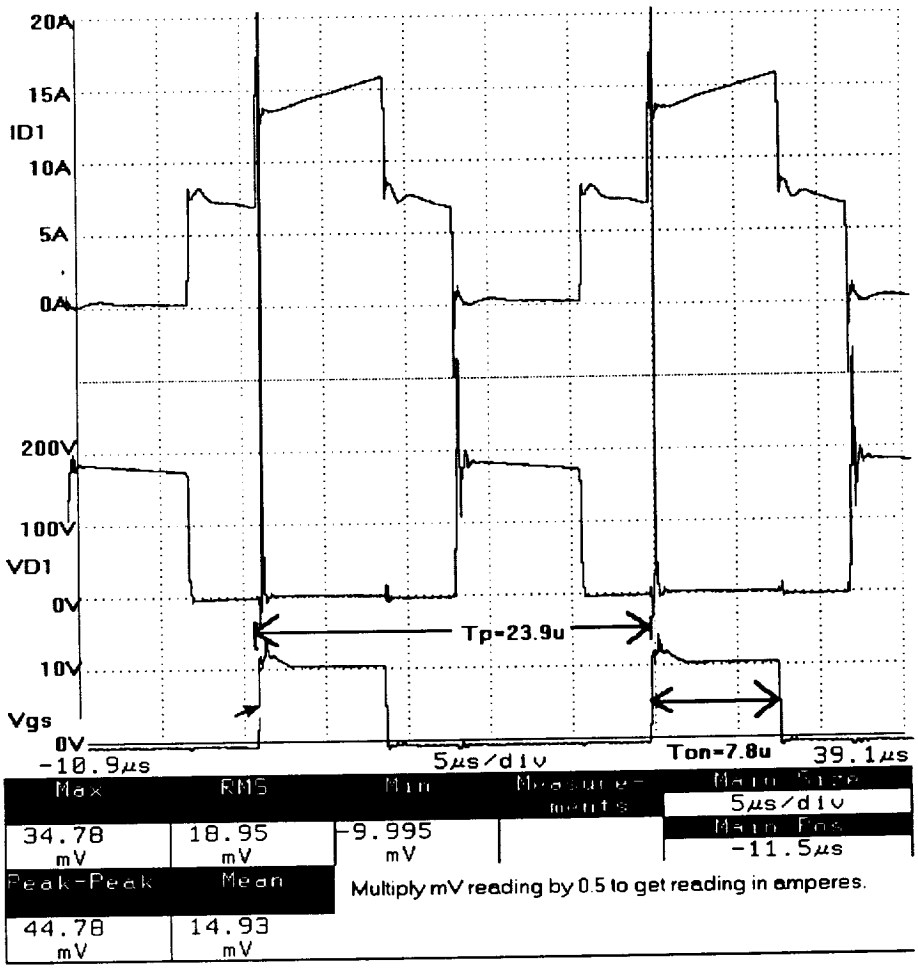


Figure 3-36 Diode Current and Voltage (Low Line, Full Load)

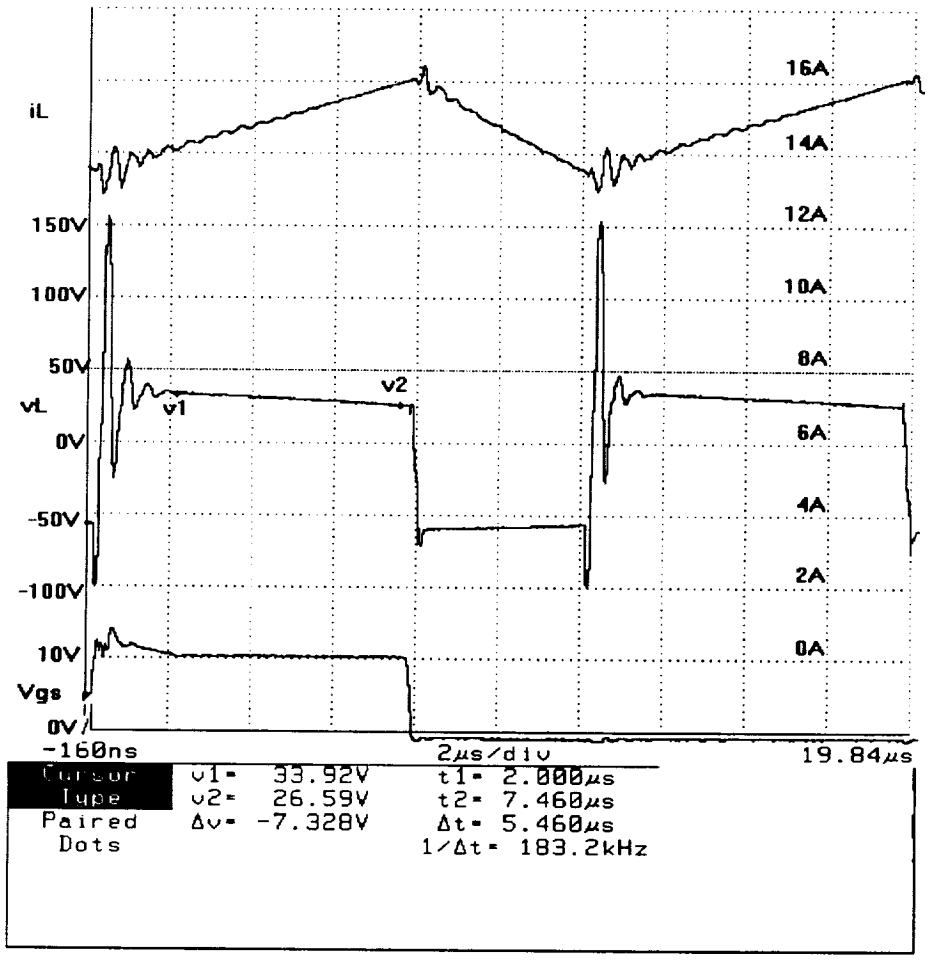


Figure 3-37 Inductor Current and Voltage (Low Line, Full Load)

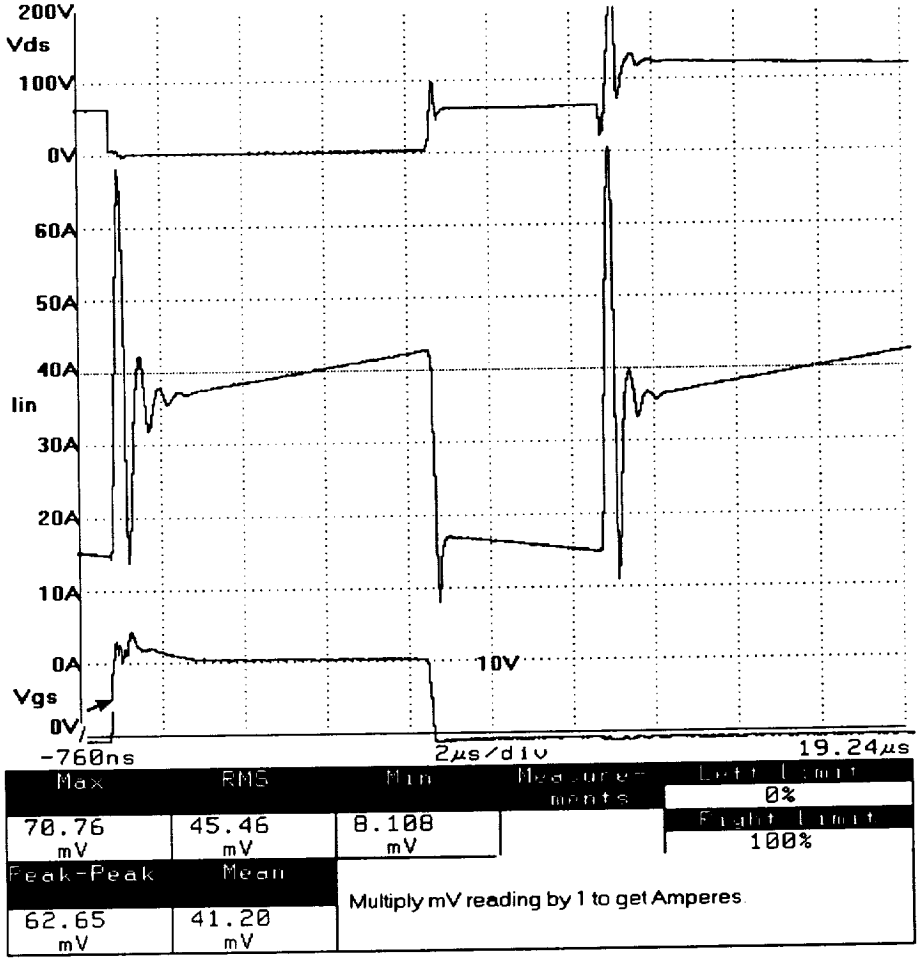


Figure 3-38 Autotransformer Input Current (Low Line, Full Load)

Inductor Power Dissipation

The inductor will have three major contributors to the total power loss. These include: windings loss due to the dc resistance, core loss, and gap loss. The windings loss (PL_{DCR}) is based on the inductor rms current as measured by the Tektronix 11401 oscilloscope:

$$PL_{DCR} = ILrms^2 \times DCR = (14.9A)^2 \times 0.023\Omega = 5\ W.$$

The core loss (PL_{core}) and gap loss (PL_{gap}) were estimated using manufacturer's data and graphs. Note that Ki=0.78 is the gap loss coefficient, and D=0.375" is the lamination width of the MC0007 core [8]:

$$PL_{core} = 50\left(\frac{W}{lbs}\right) \times weight = 50\left(\frac{W}{lbs}\right) \times 0.077lbs = 3.85\ W,$$

$$PL_{gap} = Ki \times D \times lg \times 2f \times B_{ac}^2,$$

$$PLgap = 0.78 \times 0.375cm \times \left(2.54\frac{cm}{"}\right) \times 0.024" \times (0.124Tesla)^2 = 0.86\ W.$$

The total loss of the inductor is the sum of the windings loss, core loss, and gap loss and is equal to 9.7 W.

MOSFET Power Dissipation

The MOSFET power dissipation was mainly due to the ON resistance of the device. The use of a snubber eliminated most of the switching loss as shown by the 50 nsec delay in the drain current (Fig. 3-40). The rms drain current of the MOSFET was a measured value of 13.625 A for one set of switches in parallel, and the measured drain-to-source voltage drop was 3.5 V. The total power loss for all of the switches is shown in the following equation:

$$PQ_{ON} = 2 \times Isw_{rms} \times Vds_{ON} = 2 \times 13.625A_{rms} \times 3.5V = 31.2\ W.$$

Snubber Power Dissipation

The snubber circuit that best damped the ringing of the autotransformer leakage inductance and Coss of the MOSFETs was found experimentally and had a capacitance value of 10 nf and a resistance of 9 Ω (6-56 Ω, 2 W resistors in parallel). The power dissipation of this circuit is shown below:

$$Psnub = 4 \times Csnub \times Vin^2 \times f = 4 \times 10nf \times (64Vdc)^2 \times 40kHz = 6.8\ W.$$

Rectifier Diodes Power Dissipation

Oscilloscope observations showed the rectifiers switching very fast and exhibiting no crossing of the current and reverse voltage waveforms, and therefore, little switching loss. Only the ON loss contributions to the power dissipation were considered. This loss is shown in the following equation (where the current and voltage are from Fig. 3-36):

$$PD_{ON} = 2 \times IDrms \times VD_{ON} \times \frac{Ton_{diode}}{Tp} = 2 \times 9.1A_{rms} \times 2.7V \times \frac{16.1usec}{23.9usec} = 33W.$$

Autotransformer Power Dissipation

The autotransformer will dissipate power in the dc resistance of the winding, the leakage inductance of the winding, and in the core. These losses are summarized in the following equations:

$$Pwind = 2 \times ((Isw_{rms})^2 \times PrimDCR + (ID_{rms})^2 \times (PrimDCR + SecDCR)),$$

$$Pwind = 2 \times ((13.625A_{rms})^2 \times 0.004\Omega + (9.1A_{rms})^2 \times (0.004\Omega + 0.002\Omega)) = 2.5\ W,$$

$$Plk = (lkp \times Isw_{rms}^2 + (lkp + lks) \times ID_{rms}^2) \times 2f,$$

$$Plk = (220nH \times 13.6A_{rms}{}^2 + (220nH + 117nH) \times 9.1A_{rms}{}^2) \times 2 \times 40kHz = 5.7\ W,$$

$$Total\ Windings\ Loss = Pwind + Plk = 2.5W + 5.7W = 8.2\ W,$$

$$Pcore = Iin^* \times Vin - 2 \times Psnub = 266mA \times 64Vdc - 6.8W = 10.2\ W,$$

where Iin* is the input current into the autotransformer measured with the secondaries disconnected.

The power loss of the transformer is 44.6% loss to the windings and 55.4% to the core. The almost equal division of the power loss between the core and windings indicates a good transformer design.

Output Capacitor Power Dissipation

The output capacitor power dissipation occurs when the ac inductor current passes through the ESR of the capacitor. The measured ac inductor current is 798 mA rms, and the equivalent ESR of two-5 uf capacitors in parallel is 6.5 mΩ. The resulting power is a mere 4 mW:

$$PCo = ILac_{rms}^2 \times ESR_{Co} = (798mA_{rms})^2 \times 6.5m\Omega = 4\ mW.$$

Input Capacitor Power Dissipation

Because of the large input rms current flowing in the input capacitors, the power dissipation is considered separately from the remaining input filter components. The input capacitor power dissipation is a result of the ac input current into the autotransformer passing through the ESR of the capacitor. The measured ac autotransformer inductor current is 7.9 A rms (Fig. 3-38), and the equivalent ESR of two-10uf capacitors in parallel is 4.5 mΩ. The total power dissipation of the two-10 uf input capacitors is only 0.3 W, therefore, the choice of polypropolene capacitors is optimal:

$$PCi = Iinac_{rms}^2 \times ESR_{Ci} = (7.9A_{rms})^2 \times 4.5m\Omega = 0.3\ W.$$

Input Filter Power Dissipation

The input filter inductors experience loss only to the windings. The small ac flux makes the core loss negligible. Also, the small ac current through the 0.6Ω resistor and 100uf capacitor (C1) do not contribute to the power loss of the filter. The entire filter power loss was found to be 4 W which is excellent.

$$Pfilter = Ifilter_{rms} \times (VL1 + VL2) = 31.4A_{rms} \times (85mV + 43mV) = 4\ W$$

Total Power Loss

The total power converter loss was measured to be 109.5 W and the summation of the power component losses was a total of 103.3 W proving the analysis was accurate to within 5.6%. This accuracy is acceptable with the measurement methods used and considering that no drops due to connectors or miscellaneous items were considered. Fig. 3-39 shows a pie chart of the loss contribution (where the loss due to the output capacitor is omitted because of its small value).

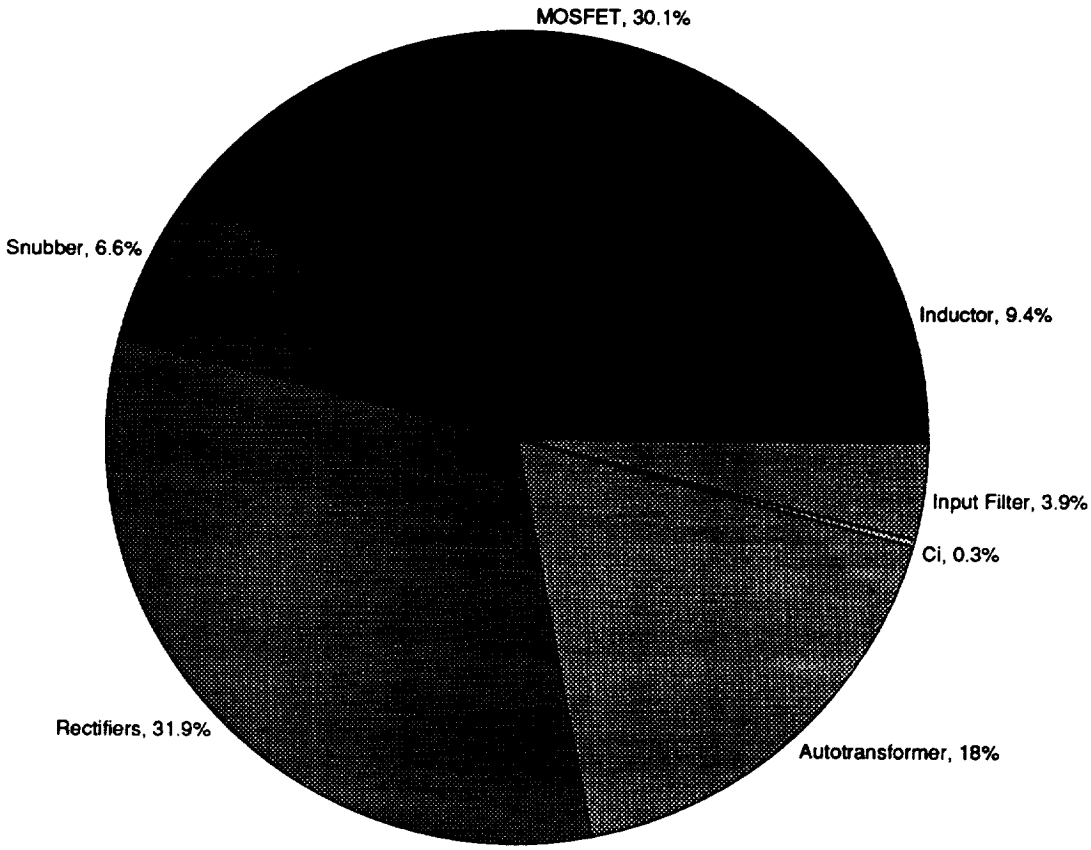


Figure 3-39 Power Loss Analysis Pie Chart

(The loss due to the output capacitor was small enough to be omitted.)

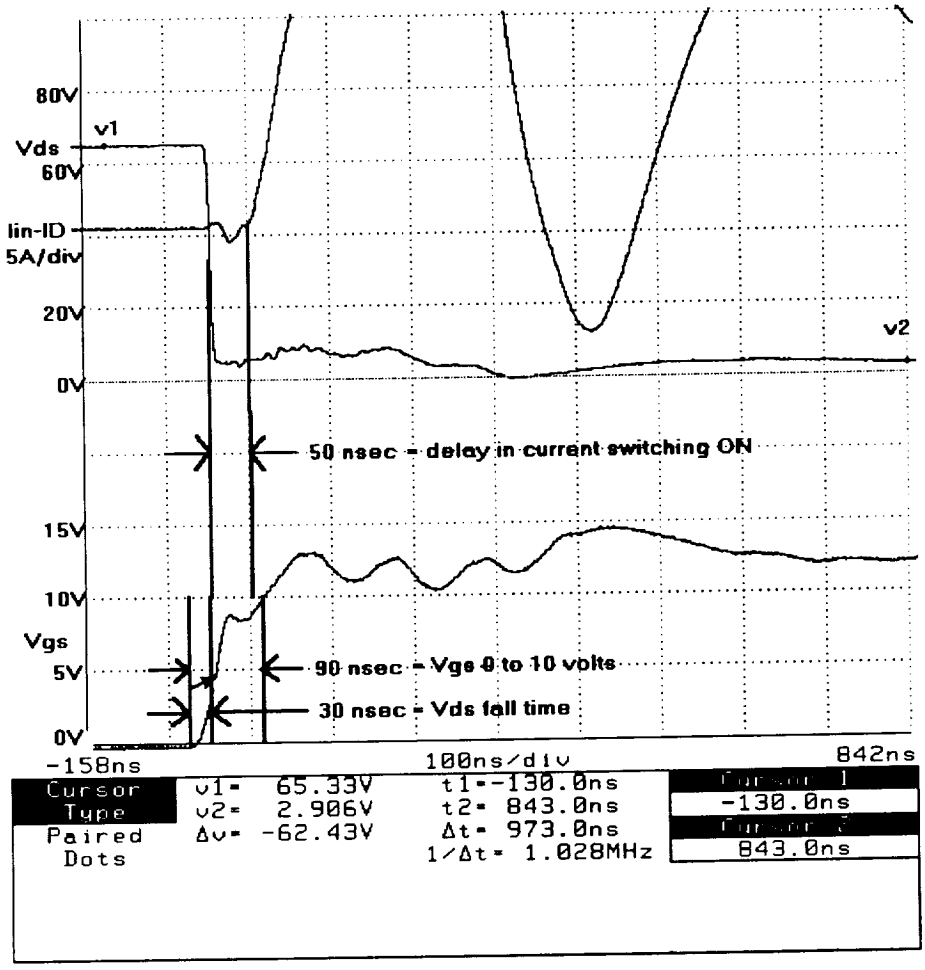


Figure 3-40 Gate Turn ON and Drain Turn OFF Waveforms

3.6.3 Summary

The goal of a 96% efficient design at low line, full load was not achieved. However, two changes in the specifications were implemented after the 96% goal was established in [1]. The input voltage minimum for regulation was lowered from 53 Vdc to 64 Vdc, making it necessary to add secondaries to the autotransformer windings. The additional windings increased the power loss of the autotransformer and MOSFETs. Also, the recently established input current ripple value of 250 mA resulted in losses in the input filter inductor windings. These losses can be reduced at the expense of using larger inductors, which is not recommended since the filter inductors were optimized for size.

The measured converter efficiency at the terminals matches well with the loss contribution analysis. The loss contribution chart (Fig. 3-39) shows that the optimization in the design of the power stage magnetics benefits the overall performance. The largest loss contribution to the total loss is in excess of 60%, and this is due to the semiconductor devices. The MOSFET switch voltage rating resulted in choosing a device with higher drain resistance, which caused increased power loss. Rectifier diode losses are about as low as the choice of diodes will allow (the devices currently being used are not on the approved parts list [2]). The use of synchronous rectifiers may help increase efficiency but will also increase complexity. Finally, the large semiconductor losses have a direct effect on the heat sink size since all of the semiconductor devices are heat sink mounted.

3.7 SUMMARY

A possible candidate for the battery discharger topology has been optimally designed and the performance results presented. The converter performed well for the duration of the testing and produced clean waveforms (ie. waveforms that did not exhibit substantial amounts of ringing). Estimated power density of the power stage for the final design was 50 W/in^3. The final performance summary of the VFPPAT battery discharger is shown in Table 3-11.

All of the specified levels were obtained with the exception of efficiency. Unfortunately, efficiency is the most important parameter in the choice of the final battery discharger topology. As mentioned earlier, the original specifications did not require the input voltage range to be less than 64 Vdc. The minimum input voltage level of 53 Vdc required secondaries on the autotransformer, and the demanding input current ripple specification of 250 mA required a two section input filter. These additions caused additional power loss. Had the specifications not been changed, 96% efficiency would most likely have been possible as predicted in [1].

Optimization of the magnetics design proved to be beneficial to the final efficiency. The autotransformer was designed three times and four devices were built. In order to balance the core losses of the autotransformer with the windings loss, foil windings had to be used. Each device resulted in increased efficiency and a reduction in size over its predecessor. The final design achieved an almost equal division of power loss between the winding and the core. The power inductor as well as the autotransformer are compact in size with very efficient use of the window for each device.

One area in which the VFPPAT topology exhibited exceptional performance was related to the control loop. Current loop control benefited the large- and small-signal performance. The resulting voltage loop cross over frequency of 5.3 kHz at 63° phase margin is very good. The settling time of the converter to a stepped load is excellent at 0.4 msec.

Table 3-11 Battery Discharger Adherence to Design Specifications

Parameter	Specification	Value Achieved
Input Voltage Range		
Efficient Operating Range	64 Vdc to 84 Vdc	64 Vdc to 84 Vdc
Regulation Range	53 Vdc to 84 Vdc	53 Vdc to 84 Vdc
Output Voltage Range	120 Vdc ± 4%	119.5 Vdc ± 0.4%[1]
Output Voltage Ripple	200mV peak-to-peak	70mV peak-to-peak[2]
Output Power Range	0 W to 1800 W	0 W to 1800 W
Output Current Range	0 A to 15 A	0 A to 15 A
Input Current Ripple	250 mA peak-to-peak	220 mA peak-to-peak[3]
Switching Frequency	40 kHz	41.8 kHz[4]
Efficiency (low line, full load)	96 %	94.5%[5]
Transient Performance		
Output Voltage Peaking Range	115.2 - 124.8 Vdc	119.7 - 119.9 Vdc[6]
Output Settling Time	10 msec	0.4 msec[7]

[1] Figure 3-33
[2] High Line (Vin = 84 Vdc), Full Load (Io = 15 Adc); Figure 3-26
[3] Low Line (Vin = 64 Vdc), Full Load (Io = 15 Adc); Figure 3-25
[4] Figure 3-36
[5] Figure 3-34
[6] Low Line (Vin = 64 Vdc), Load Cycled 2 Adc to 13 Adc; Figure 3-24
[7] Figure 3-24

CHAPTER 3 REFERENCES

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4 BATTERY CHARGER DESIGN

4.1 DESIGN SPECIFICATIONS AND TRADEOFFS

Listed below are the battery charger design specifications:

Input Voltage = 120 VDC ±4%,

Output Voltage = 53 to 84 V,

Output Power = 1470 W Ave/1930 W Pk,

Nominal Efficiency = 96%,

Switching Frequency = 90 KHz,

Output Current = 0.85 A to 23 A DC

(in 16 equal steps of 1.5 A each),

Output Ripple Current = 0.23 A Pk-to-Pk,

Bus Ripple Voltage = 200 mV Pk-to-Pk,

Bus Voltage Transient Settling Time < 10 mS.

Given the input and output voltage levels, a natural and effective switchmode topology for the battery charger is a buck converter. Though other suitable topologies exist for an application such as this, the buck converter was chosen for its simplicity and well documented behavior. Future efforts on this research project will evaluate alternative charger topologies. Therefore, a tradeoff analysis can later be performed to determine the benefits of each topology. Such an analysis has already been performed on the Space Platform battery discharger [1].

The spacecraft batteries will have a 50 AH capacity and will consist of 54 series nickel hydrogen

cells. For a normal 30% depth of discharge (DOD), the battery voltage will range from 64 to 84 V. However, the charger is designed to operate with a 53 V battery, an abnormal condition occuring at 100% DOD with cell voltages falling to near 1 V. The batteries will be charged at 16 different commanded rates ranging from 0.85 A (C/60) to 23 A (C/2.2), with 1.5 A increments between each charge rate. As for most batteries, the current ripple must be kept to a minimum, so the charger's output current is attenuated to below 1% of the maximum charge rate (230 mA Pk-to-Pk). The charger is to have eight volt/temperature (V/T) curves to ensure adequate charging under all conditions of battery voltage, temperature, and life. For simplicity, three V/T curves are designed into the charger described in this report.

The charger is designed to maintain a nominal efficiency of 96% while delivering 1500 W to the battery. A 90 KHz switching frequency was chosen because of the stipulation that the charger and discharger frequencies must contain the same harmonics. Since the optimum power conversion frequency for the discharger was found to be 45 KHz, the 90 KHz frequency for the charger satisfies the harmonic requirement and produces a compact and lightweight charger design.

During the bus voltage regulation mode, the charger must produce less than 200 mV Pk-to-Pk of switching ripple across the 120 V bus. The charger must also keep bus voltage transients less than ±4.8 V with a settling time less than 10 mS.

Designing a battery charger to meet the above specifications involves trading off mass, efficiency, and reliability. Increasing the efficiency of the charger produces a heavier design: reduction of ohmic and magnetic losses requires larger power circuit components. Similarly, designing a charger for minimum mass yields a converter with a low efficiency. Therefore, a careful balance between these critical design parameters is required. To ensure high reliability, component selection and derating was guided by the Goddard Space Flight Center Preferred Parts List (PPL-18).

4.2 POWER STAGE DESIGN

4.2.1 Power Switches

The design of the battery charger power stage is shown in Fig. 4-1. Four IRF250 MOSFETs are placed in parallel to form the active power switch. Two of these MOSFETs have adequate capacity to handle the maximum RMS switch circuit, but to increase efficiency, four are used, thus lowering the effective R_{DSon} to 22 mΩ. This reduced conduction loss is partially offset by an increase in the switching loss due to the capacitance of the additional MOSFETs. Neglecting gate drive losses, the MOSFET loss that is dependent on the number of parallel devices is given below:

$$P_T = \frac{1}{2} C_T V_{BUS}^2 f n + \frac{1}{n} I_{BAT}^2 D R_{DSon} \quad , \tag{4.1}$$

where $C_T = C_{DS} + C_{DG}$, f is the switching frequency, I_{BAT} is the battery current, D is the duty cycle, and n is the number of MOSFETs. To find the value of n that yields the lowest value of P_T , the partial derivative of P_T with respect to n is set equal to zero, and the following result is obtained:

$$n = \frac{I_{BAT}}{V_{BUS}} \sqrt{\frac{2 R_{DSon} D}{C_T f}} \quad . \tag{4.2}$$

For nominal values of R_{DSon} , D, and C_T , the value n=4 satisfies Eq. (4.2) for a median I_{BAT} value of 15 A. Clearly, at low charging currents, the switching loss is much greater than the conduction loss. As the battery current increases, the conduction loss claims a much larger portion of the total MOSFET loss.

In order to meet current derating, two UES706 rectifiers are needed in parallel to form the passive power switch. Additional parallel rectifiers produce minimal gains in efficiency due to their exponential voltage/current characteristic. Furthermore, the efficiency gain is offset by the additional rectifier mass.

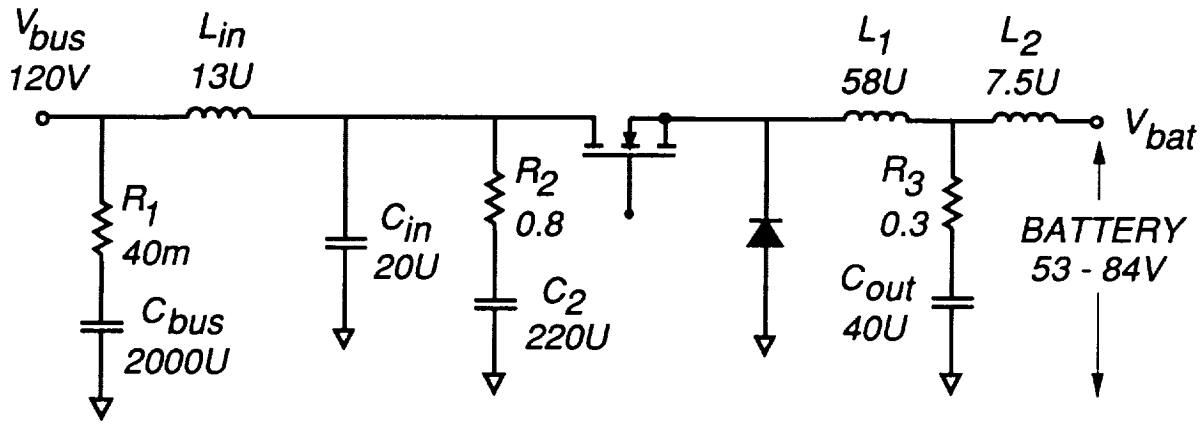


Fig. 4-1. Battery charger power stage

4.2.2 Drive Circuit

Designing a circuit to drive the four MOSFETs in parallel proved to be a very challenging task. As shown in Fig. 4-2, the 90 KHz PWM drive signal is transformer coupled up to a 120 V level. A 12 VDC bias supply, referenced to the MOSFET sources, provides the current necessary to drive each gate capacitance. Therefore, the drive transformer does not carry large pulsating currents which could couple noise back into the UC3823 pulse width modulator (PWM) chip. In order to minimize the interactions between the individual MOSFETs, a bipolar buffer stage drives each MOSFET. Without these buffer stages, it is very difficult to switch the MOSFETs cleanly. The differing V_{GS} thresholds cause the devices to turn on at different times, thus upsetting the current balancing. The resulting MOSFET turn-on transients are skewed, and unless the individual gates are decoupled from each other, the device switching can become erratic.

The speed of the drive circuit is controlled by the value of C_3. The selected speed is fast enough to efficiently switch the MOSFETs while minimizing the generation of electromagnetic interference (EMI). Very fast switching speeds also produce higher rectifier reverse recovery current spikes which, not only exacerbate EMI problems, but also increase rectifier and MOSFET switching losses. In order to reduce the propagation delay of the PWM signal, zener diodes are placed in series with C_3.

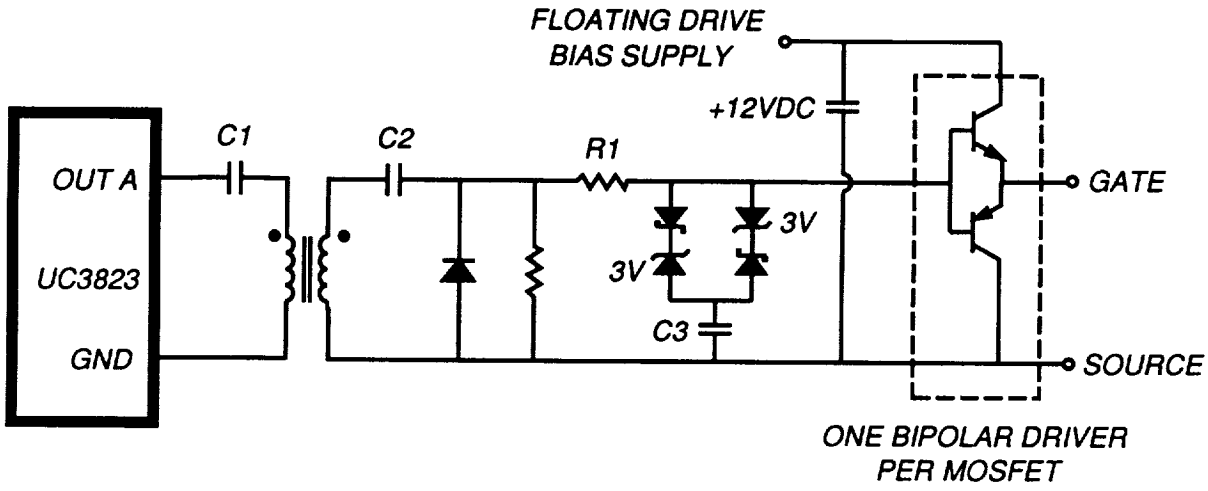


Fig. 4-2. MOSFET drive circuit

4.2.3 Input Filter

Due to the pulsating nature of the input current to the battery charger, an input filter is needed to attenuate the conducted emissions to the spacecraft bus. As shown in Fig. 4-1, the input filter is primarily composed of a single section formed by L_{in} and C_{in} . Lossless damping of this LC filter is provided by the AC coupling of R_2 across C_{in} . When the charger is in the current regulation mode, the bus voltage is controlled by the solar array shunt regulator. Consequently, the solar array appears as a voltage source in this mode. Thus the bus capacitor, being in parallel with the solar array, does not affect the properties of the charger input filter. However, when the charger is in the bus voltage regulation mode, the solar array appears as a current source. In this case, the bus capacitor becomes part of the existing charger input filter. Therefore, the transfer function and impedance of the input filter are different for each operating mode.

Since the bus capacitor is much larger than the parallel combination of C_{in} and C_2 , the input filter transfer function for each mode is essentially the same. Because $C_2 \gg C_{in}$, the damping resistor, R_2 , appears in parallel with C_{in} and L_{in} at the filter resonant frequency. Therefore, the filter effectively has a second order response [2]. The input filter transfer function, $T_I(s)$, is given below:

$$T_I(s) = \frac{1}{1 + \frac{L_{in}}{R_2}s + L_{in}C_{in}s^2} \quad . \tag{4.3}$$

The value of R_2 is chosen to give a filter Q of 1, thus producing low peaking in the transfer function at the resonant frequency. To reduce mass, the filter resonant frequency is chosen as high as possible while maintaining low impedance and adequate ripple current attenuation. The filter resonant frequency is placed at 10 KHz, thus providing a 38 dB attenuation of the 90 KHz current harmonic.

4.2.4 Output Filter

Since the battery current must have a very low ripple content, a two section output filter is used. As shown in Fig. 4-1, this T output filter is composed of L_1 , L_2 , and C_{out} . The filter component values are selected to give the required current attenuation while minimizing losses and mass. The first inductor, L_1 , is sized to reduce the ripple current to 5.5 A pk-pk. The second inductor, L_2 , reduces the ripple to below 230 mA for an overall filter attenuation of -42 dB. The center leg of the output filter contains C_{out} in series with R_3 , a damping resistor. Since the filter $Q = Z_O/R_3$, the value of R_3 is kept close to the filter characteristic impedance Z_O for effective damping. The R_3 value, however, must also be minimized to reduce losses. The transfer function of this filter, interpreted as the response of i_{BAT} to a change in the filter input (rectifier) voltage, is given below:

$$T_O(s) = \frac{1 + R_3 C_{out} s}{L_S s (1 + R_3 C_{out} s + L_T C_{out} s^2)} \quad , \tag{4.4}$$

$$\text{where} \quad L_S = L_1 + L_2 , \quad \text{and} \quad L_T = \frac{L_1 L_2}{L_S} \quad .$$

The design of L_1 , the main energy storage inductor, is crucial since this component has a great impact on the charger's efficiency and mass. A cut C-core with 1 mil laminated Metglas was chosen for this inductor. Because the saturation flux density, B_{max} , is so high (1.4 Tesla) for this magnetic material, the mass of this inductor can be minimized. This fact is seen in the relation used to select the core size through the area product A_p :

$$A_P = 0.84 \left[\frac{L_1 I_{BAT\,PK}^2}{B_{MAX} K_W} \right]^{1.16} \qquad (in^4) \quad , \tag{4.5}$$

where K_W is the core window utilization factor [3]. Due to the high permeability of the core material, the inductance is determined from the length of the core gap. The gap length, l_g , must be minimized to reduce the fringing flux, which causes a gap loss due to eddy currents induced in the core laminations. As shown below, the gap loss, P_G , is largely dependent on the AC flux density (B_{AC}):

$$P_G = 0.099 D_W l_g f B_{AC}^2 \quad (W) \quad , \tag{4.6}$$

where D_W is the lamination width. The core loss, P_C, is highly dependent on the switching frequency as given by

$$P_C = 3.42 \times 10^{-10} A_C l_M B_{AC}^{2.04} f^{2.23} \quad (W) \quad , \tag{4.7}$$

where A_C is the core cross section and l_M is the core magnetic path length. Copper foil was used as the conductor, allowing for a high window utilization factor, thus reducing ohmic losses. The design for this inductor minimizes the loss and mass for the required amount of energy storage.

4.2.5 Power Stage Performance

The worst case condition for power stage stress occurs at a battery voltage and current of 64 V and 23 A. This high current condition causes maximum conduction losses in the filters and power semiconductors. With the low battery voltage, the input current to the charger will also be maximum. Therefore, the charger efficiency is the lowest under these operating conditions. As expected, the efficiency increases with battery voltage as shown in Fig. 4-3.

Under the 64 V/23 A battery conditions, the bus voltage ripple and the charger input and output current ripple will be maximum. The bus voltage ripple is primarily the product of the charger input current ripple and the equivalent series resistance (ESR) of the bus capacitor. Measurements of the worst case ripple waveforms are shown in Fig. 4-4 with the charger in the voltage regulation mode.

As described in Chapter 7, a large signal EASY5 model of the battery charger was developed. The predicted ripple waveforms from this EASY5 model are shown in Fig. 4-5.

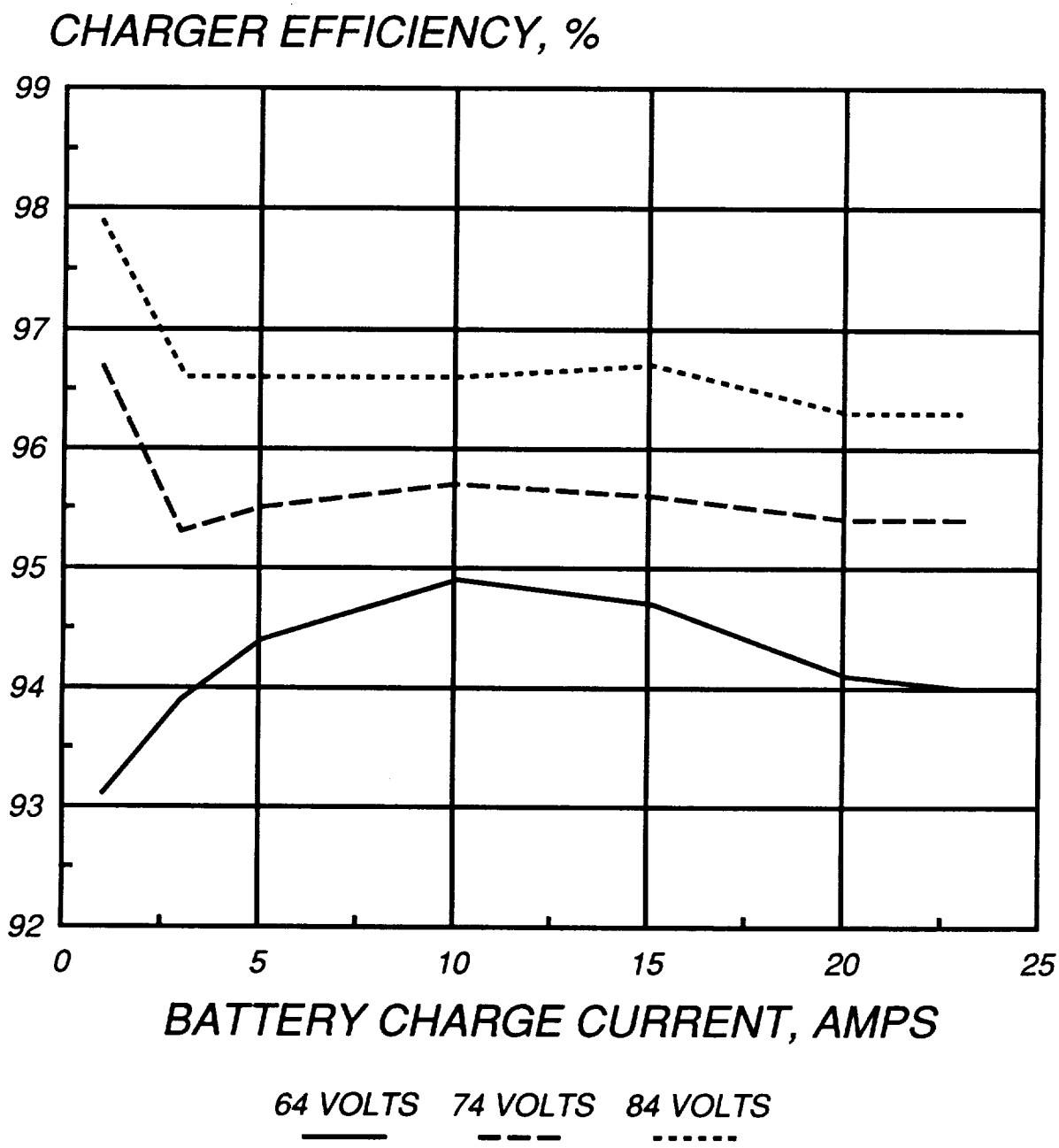
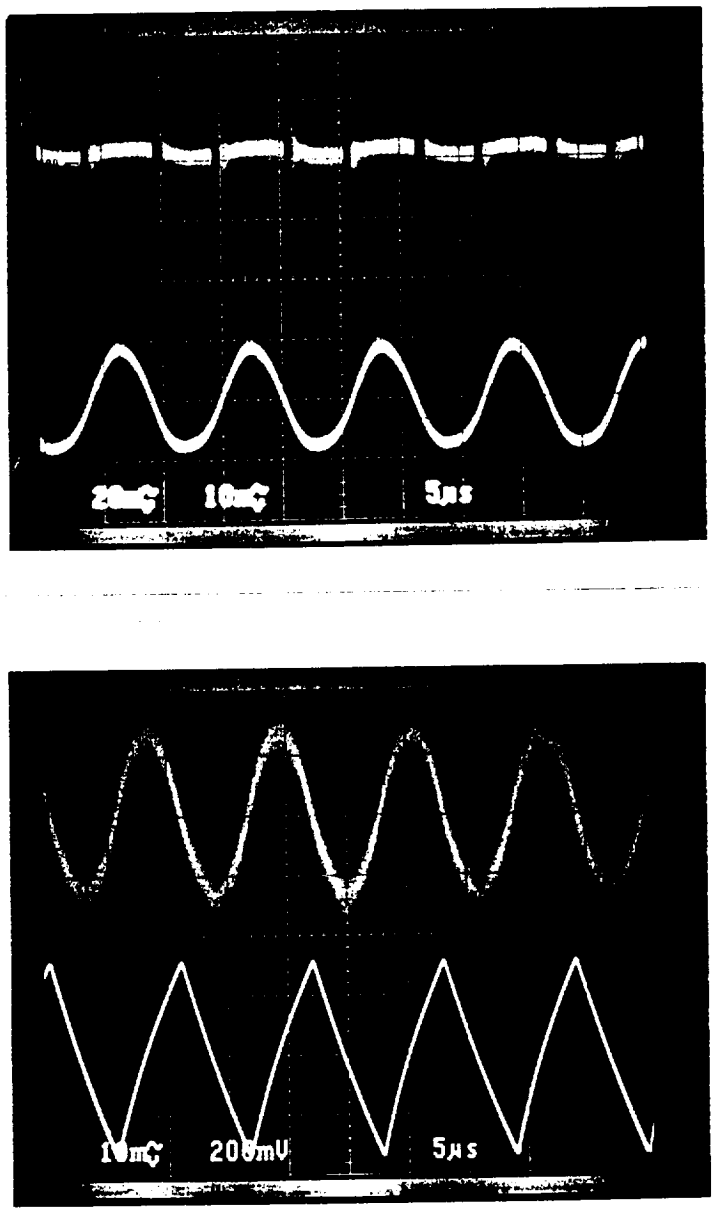


Fig. 4-3. Battery charger efficiency



Bus voltage ripple
20mV/div

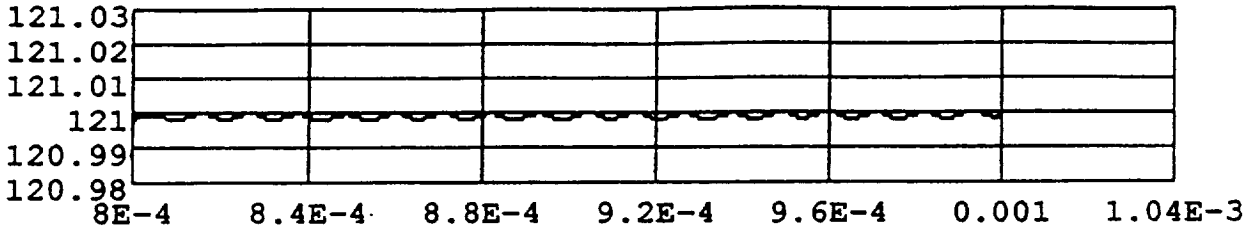
Charger input current
200mA/div

L1 inductor current
2A/div

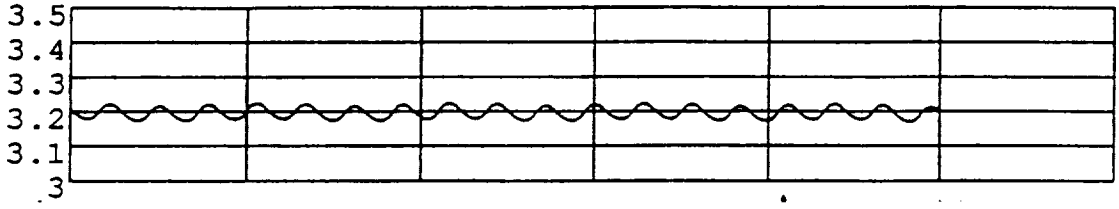
L2 inductor current
100mA/div

Fig. 4-4 Measured Charger Ripple Waveforms

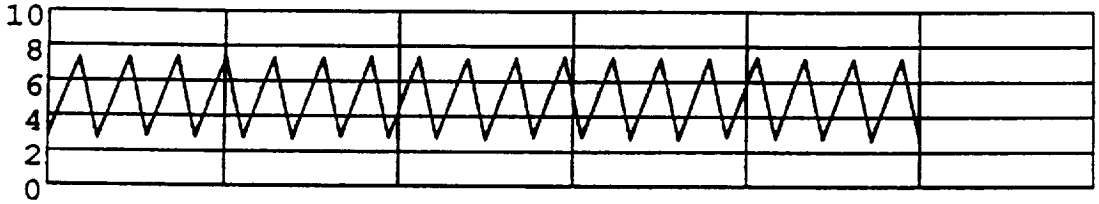
Fig. 4-5. EASY5 simulation of charger ripple waveforms



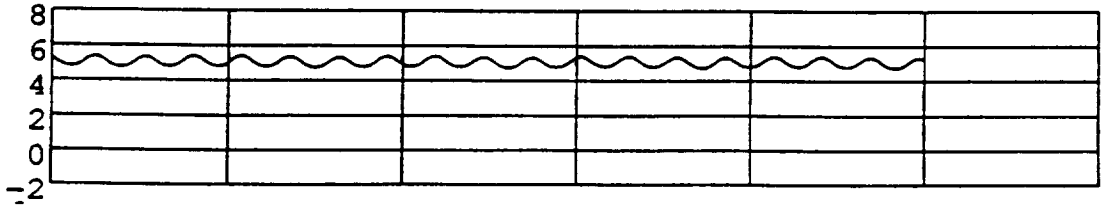
Bus voltage ripple



Charger input current



L1 inductor current



L2 inductor current

4.3 CONTROL SYSTEM MODELLING

4.3.1 Control System Configuration

As shown in Fig. 4-6, the charger has three basic control loops that are ORed together to produce a control signal (v_c). Since each loop has an integrating error amplifier, only one loop is active at a time. The voltage loop regulates the bus voltage during the transition from eclipse to sunlight. The current loop regulates the battery charging current, and the V/T loop controls the final charging of the battery. For each loop, the control signal, v_c , is summed with feedback of i_{L1} , the instantaneous current in L1. The resulting signal, v_r , is compared against a ramp to generate a PWM signal, d, to control the power stage.

4.3.2 Power Stage Modelling

To design the charger control loops, it is necessary to simplify the power stage. The input filter (L_{in} and C_{in}) can safely be deleted, thus eliminating two state variables. Furthermore, the output filter can be accurately represented as a single inductor, L_S , whose value is $L_1 + L_2$. This assumption is valid since $L_1 >> L_2$. These simplifications are essential in deriving workable transfer functions for the charger power stage.

To aid further in the design of the control loops, the PWM switch model [4] is used to characterize the switching of the power stage MOSFETs and rectifiers. As shown in Fig. 4-7, the PWM switch model is inserted into the simplified charger power stage. The model's voltage source depends on the steady-state values of D and the voltage between the active and passive terminals. The current source depends on the DC value of I_{bat} , the current flowing out the common terminal. Since the ESR of the input filter capacitor is so low, the PWM switch parameter r_E is not included. The control signal v_A equals $v_c(1+K_2)$, where K_2 is the gain (R_f / R_i) of the summing amplifier in Fig. 4-6.

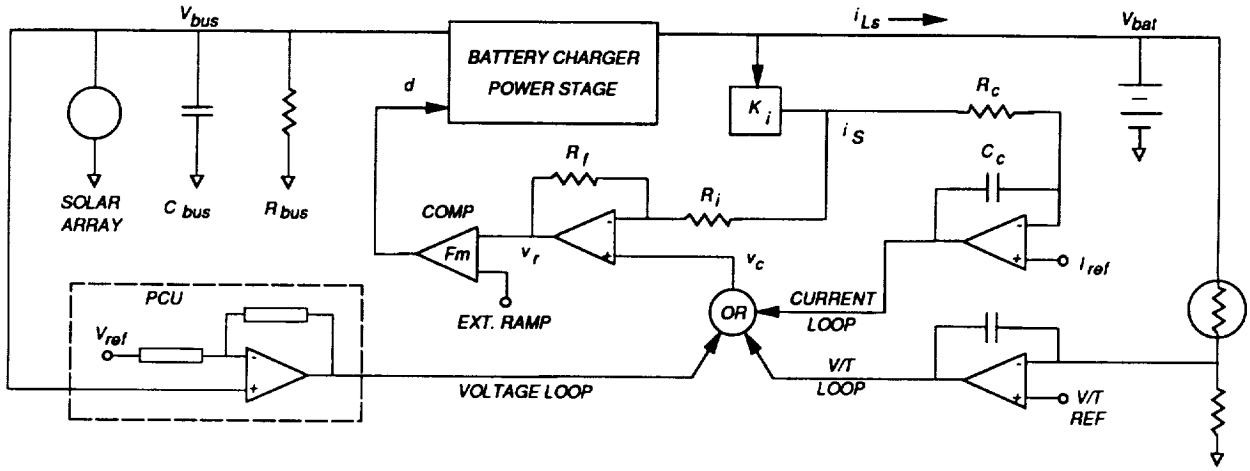


Fig. 4-6. Battery charger control circuit

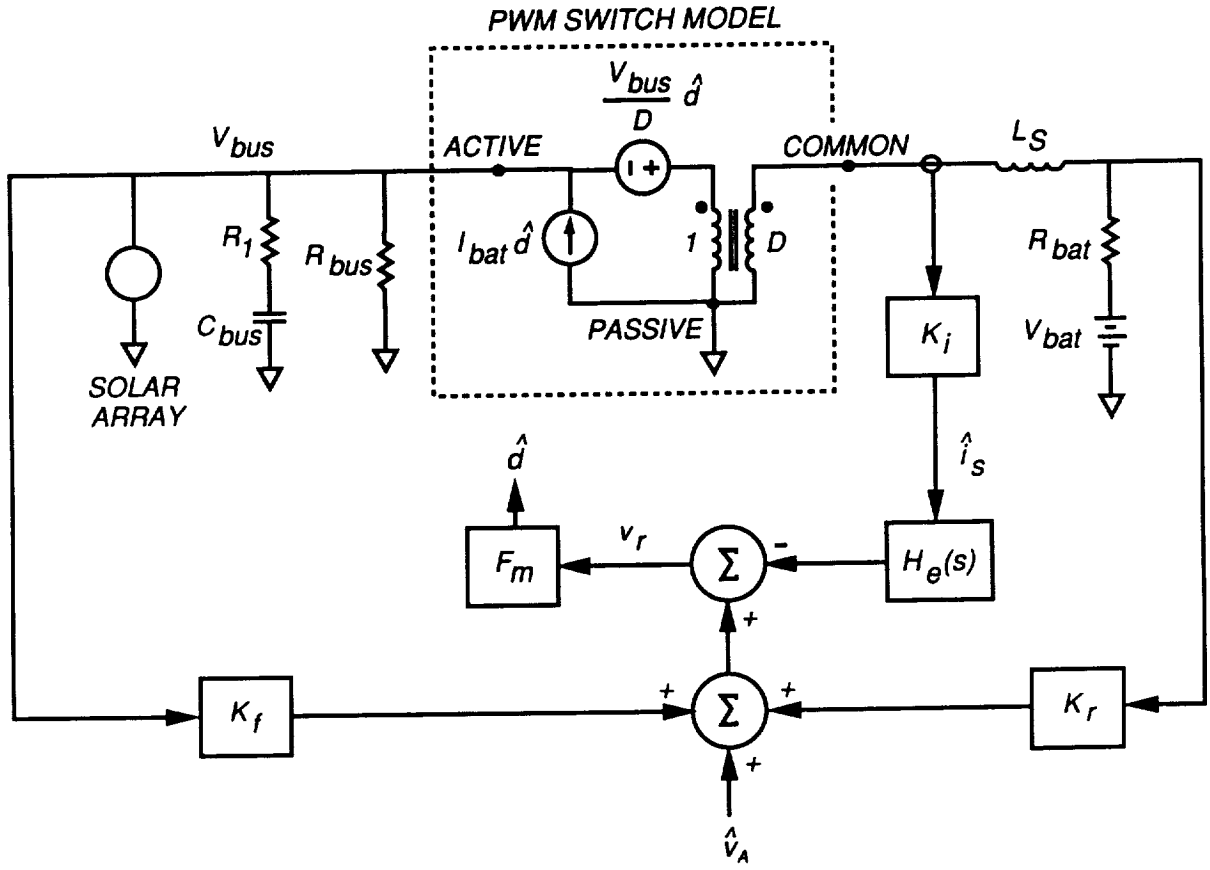


Fig. 4-7. Battery charger control model

4.3.3 Current Mode Control Modelling

Since all three loops use current mode control, it is important to model this control method accurately. The new continuous-time model for current mode control [5] provides a simple and effective method for characterizing this type of sampled-data control. As shown in Fig. 4-7, the sensed current (i_S) is multiplied by the sampling gain $H_e(s)$. This sampling gain can accurately be modelled as a complex pair of right half plane (RHP) zeros at half the switching frequency as given below:

$$H_e(s) = 1 + \frac{s}{\omega_n Q_Z} + \frac{s^2}{\omega_n^2} \quad , \tag{4.8}$$

$$\text{where} \qquad Q_Z = -\frac{2}{\pi} \quad , \quad \text{and} \qquad \omega_n = \pi f \quad .$$

The sampled current is added to the control voltage, v_A , along with feedback of the input and output voltages through the gains k_f and k_r. This sum is multiplied by the comparator gain, F_m , as given below:

$$F_m = \frac{f}{S_N + S_E} \quad , \tag{4.9}$$

where S_N and S_E are the slopes of the sensed on-time current and the external ramp, respectively.

4.4 CURRENT REGULATION MODE

4.4.1 Current Sensing and Control

The primary purpose of the charger is to control the manner in which energy is returned to the battery. Proper design of the charge current regulation circuitry is necessary to ensure that the batteries will be recharged in a manner enabling them to last through the tens of thousands of cycles in their five year life span. In order to properly regulate the charging current, the battery current must be sensed accurately. Of the possible sensing methods, a dual current transformer approach was used in this design. A current transformer (CT) senses the MOSFET drain current, another CT senses the rectifier current, and the two signals are added together. The result is i_S , a replication of the instantaneous current in L_1 . The current sense gain, designated as K_i in Figs. 4-6 and 4-7, is -20 dB. Since the AC portion of i_{L1} flows into the filter capacitor, the actual battery current, i_{L2} , is not directly regulated. However, because the average values of the inductor currents are identical, this method of current sensing enables regulation of the DC current into the battery. The current sensing accuracy is limited by the power stage parasitic capacitance and the CT magnetizing current. The CT*s* and the power stage were carefully designed so that the current sensing error would be less than 1%.

As shown in Fig. 4-6, the sensed current signal, i_S , is fed to an error amplifier where it is subtracted from I_{ref} , the charge current reference signal. As shown in Table 4-1, there are 16 different commanded values of battery charge rates. The 16 different values of I_{ref} are provided by a D/A converter as shown in Fig. 4-8. The error signal, i_S - I_{ref} , is integrated by the amplifier, so the steady-state current regulation error is zero. Since the DC value of the battery current is regulated, this amplifier produces average current mode control. The amplifier gain is selected to provide a high (-36 dB) attenuation of the ripple content of i_S . Therefore, the amplifier output signal, v_c , is essentially pure DC and insensitive to variations in the peak-to-peak amplitude of i_{L1} . The v_c signal is subsequently

added back to the sense signal, i_s , and the resulting waveform is compared against a sawtooth ramp to generate the duty cycle. As detailed in the next section, the addition of i_s to v_c produces the benefits of conventional current mode control.

As the battery is charged at a constant rate, the battery voltage rises until the V/T control circuit is activated. As shown in Fig. 4-9, the operation of the V/T control circuit is very similar to the charge current regulation circuit. The battery voltage is sensed with a voltage divider containing a thermistor to account for the effects of battery temperature. The thermistor is simulated in this charger design with a 5K Ohm potentiometer as shown in Fig. 4-10. To ensure proper charging of the battery under all conditions, there are several V/T reference levels [6] which are shown in Fig. 4-11. The V/T amplifier gradually reduces the current until the battery is fully charged.

RATE	CURRENT (AMPS)	COMMAND DATA			
		S1	S2	S3	S4
1	0.85	0	0	0	0
2	2.33	0	0	0	1
3	3.80	0	0	1	0
4	5.28	0	0	1	1
5	6.76	0	1	0	0
6	8.23	0	1	0	1
7	9.71	0	1	1	0
8	11.1	0	1	1	1
9	12.7	1	0	0	0
10	14.1	1	0	0	1
11	15.6	1	0	1	0
12	17.1	1	0	1	1
13	18.6	1	1	0	0
14	20.0	1	1	0	1
15	21.5	1	1	1	0
16	23.0	1	1	1	1

Table 4-1. Charge current rate selection

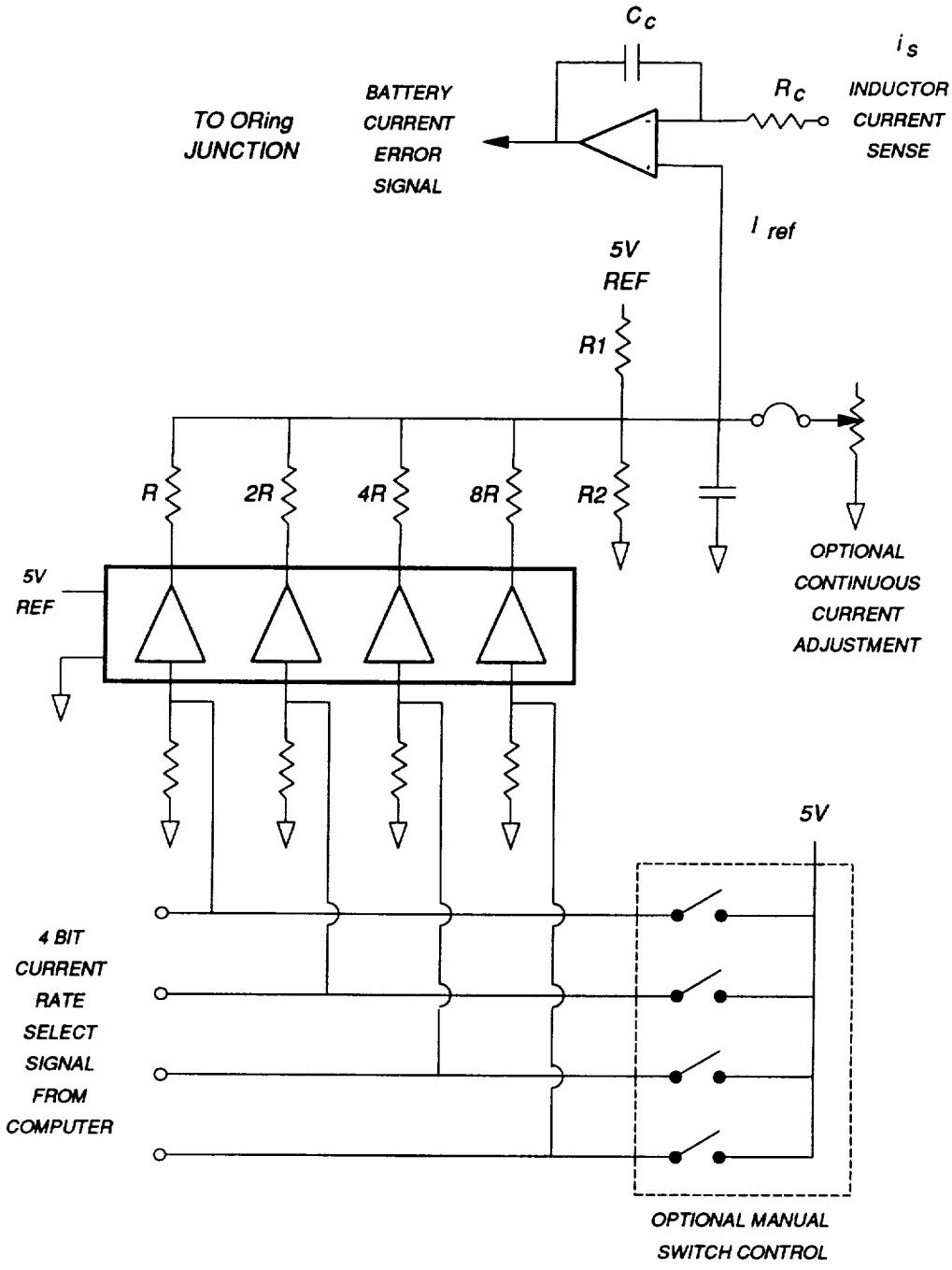


Fig. 4-8. Charge rate selection circuit

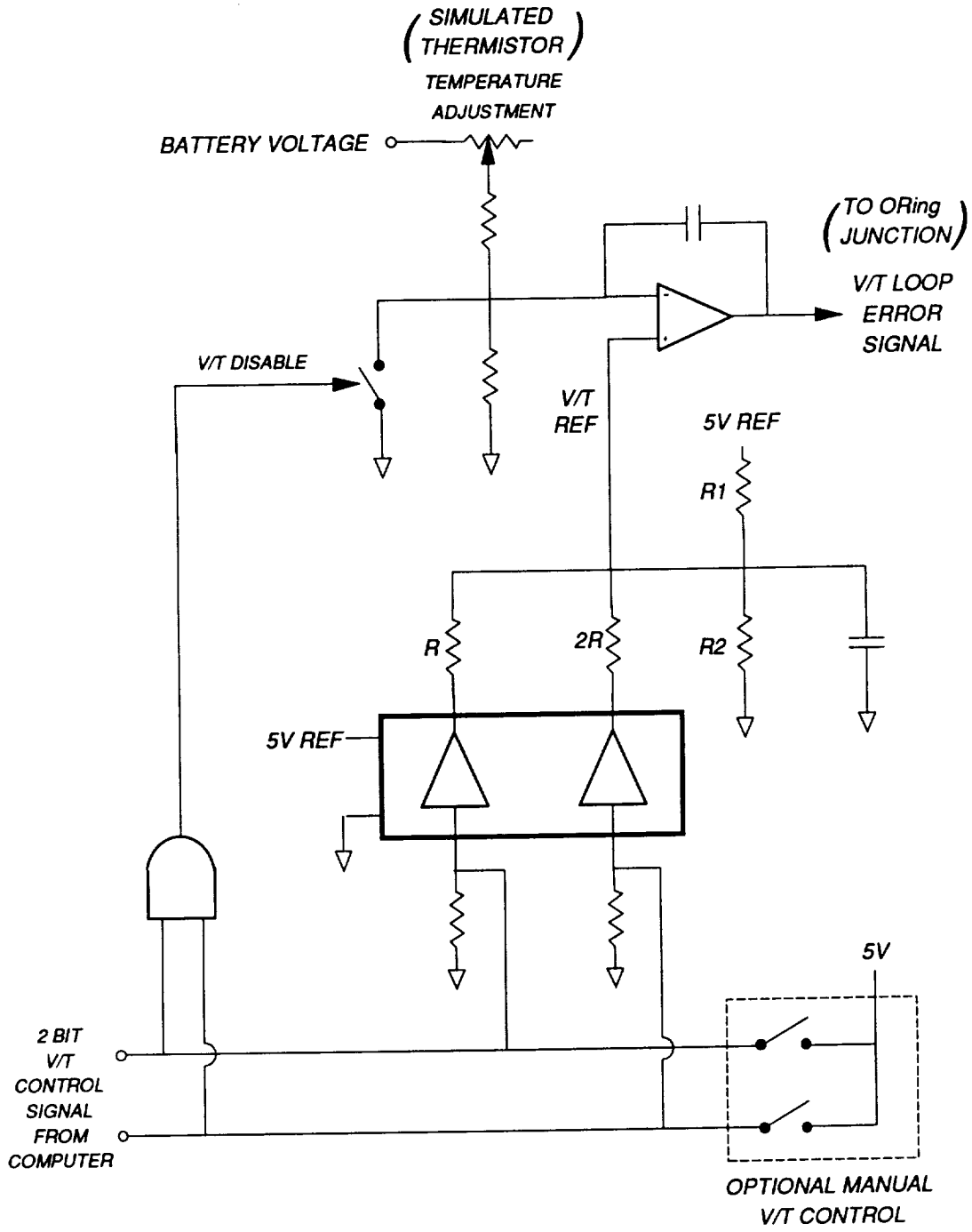


Fig. 4-9. Volt/Temperature control circuit

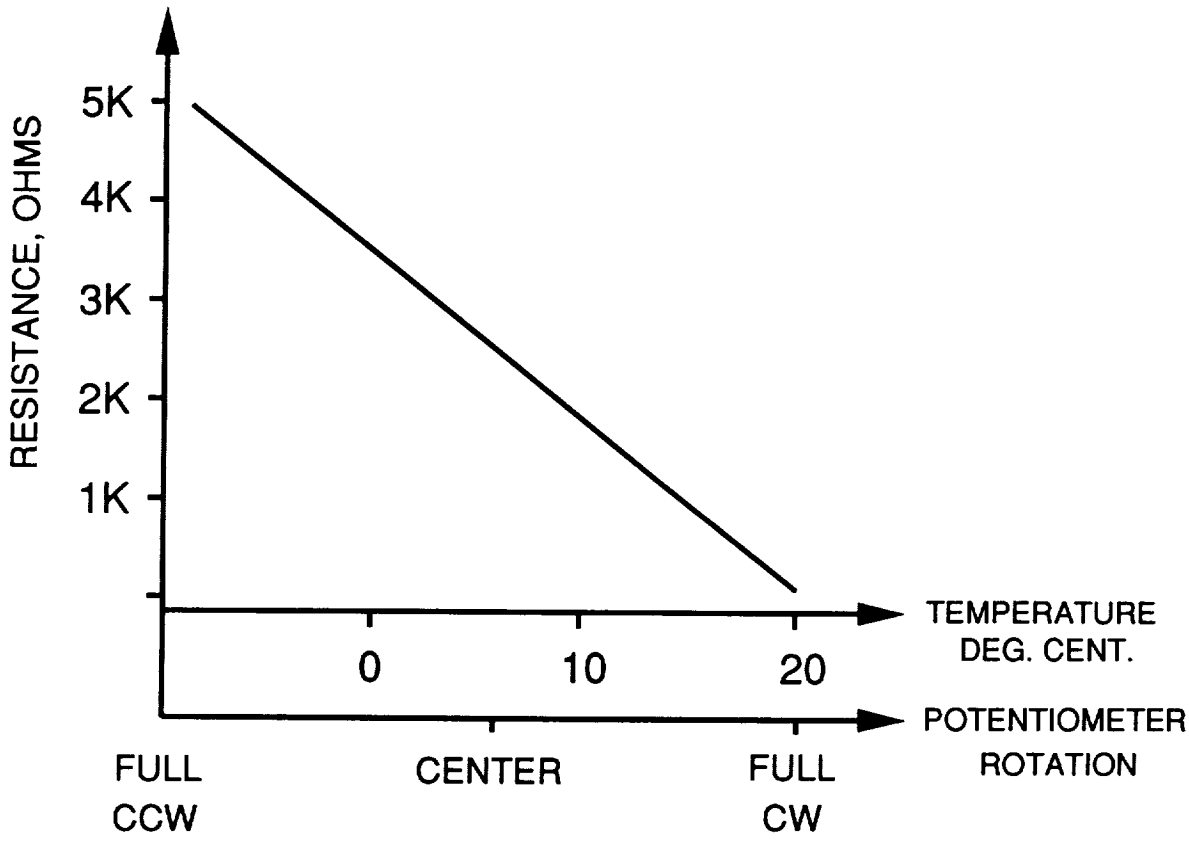


Fig. 4-10. Simulated thermistor

CURVE	S5	S6
1	0	0
2	0	1
3	1	0
V/T DISABLE	1	1

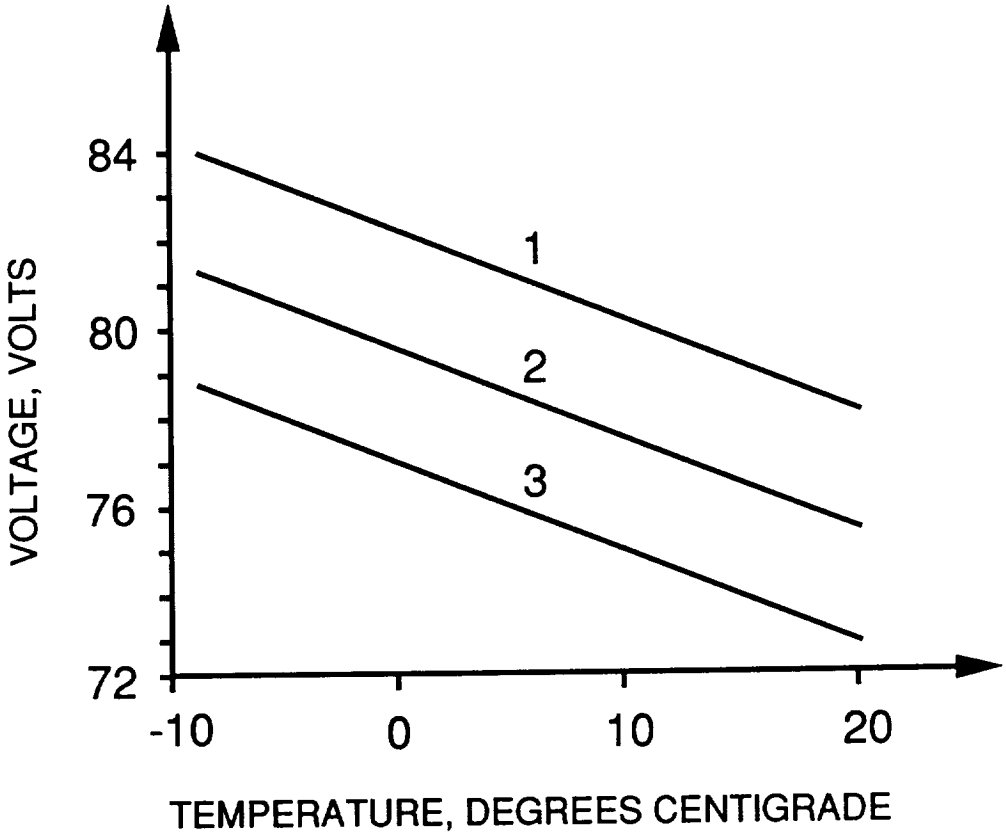


Fig. 4-11. Battery charger V/T curves

4.4.2 Current Loop Design

An important component of the current loop design is the duty cycle-to-inductor current transfer function, designated as F_{di}. Using the charger circuit model in Fig. 4-7, F_{di} is easily derived:

$$F_{di} = \frac{\hat{i}_{Ls}}{\hat{d}} = \frac{V_{bus}}{R_{bat}} \left[\frac{1}{1 + \frac{L_S}{R_{bat}} s} \right] \quad , \tag{4.10}$$

where $L_S = L_1 + L_2$ and R_{bat} is the resistance of the battery, L_1, and L_2. Since R_{bat} is very small, the DC gain of F_{di} is very high (≈60 dB). This transfer function has a single pole located at $s = R_{bat} / L_S$, normally around 500 Hz. Since the resistance of the battery varies widely with its state of charge, this DC gain and pole location are also highly variable.

The design of the current loop is facilitated by the block diagram in Fig. 4-12. This diagram can be simplified by moving the pickoff point of the sampling gain block from i_S to i_{Ls}. The inner loop, T_i, can then be reduced to a block representing the gain from v_A to i_{Ls}. This gain, denoted as G_f, is given below:

$$G_f = \frac{\hat{i}_{Ls}}{\hat{v}_a} = \frac{F_m F_{di}}{1 + F_m F_{di} [K_i H_e(s) K_2]} \quad . \tag{4.11}$$

At frequencies below 10 Khz, G_f can be greatly simplified since $H_e(s)$ is near unity in this region. Furthermore, since F_{di} is so large, the 1 in the denominator of G_f can be neglected. With these simplifications, G_f is reduced to a constant value of $1/K_iK_2$. Herein lies the value of current mode control for this loop: variations in F_{di} do not affect the loop gain. Once G_f is determined, the system loop gain is easily solved:

$$G_{li} = \frac{K_1}{s} (1 + K_2) G_f K_i \quad . \tag{4.12}$$

This loop gain is very simple to compensate due to its first order nature. The loop crossover frequency is determined by K_1, the gain of the integrator, which is $1/R_cC_c$ as shown in Fig. 4-6. A plot

of the measured current loop gain is shown in Fig. 4-13. The current loop gain crosses over at 3 KHz where the phase margin is 83 degrees. The additional phase lag near 10 KHz is due to $H_e(s)$, the sampling gain.

4.4.3 Transient Response

From the design of the current loop, the transient response can be predicted. Since the loop crosses over in the region where $H_e(s)$ is unity, the sampling gain can be neglected in this analysis. The objective is to find the response of i_{Ls} , the battery current, to a unit step in i_{ref} , the charge current reference signal. The response of i_{Ls} is:

$$i_{Ls}(s) = T_c(s)\, i_{ref}(s) \quad , \tag{4.13}$$

$$\text{where} \quad T_c(s) = \frac{G_i}{K_i(1+G_i)} \quad .$$

The time domain response of i_{Ls} (s) is found by taking the Laplace transform of Eq. (4.13), and the result is given below:

$$i_{Ls}(t) = \frac{1}{K_i}(1 - e^{-\alpha t}) \quad , \tag{4.14}$$

$$\text{where} \quad \alpha = \frac{1+K_2}{K_2 R_c C_c} \quad .$$

The battery current response time is shown in Fig. 4-14, where the reference is stepped between two levels. The same operating conditions were simulated with the EASY5 battery charger model, and the results are shown in Fig. 4-15.

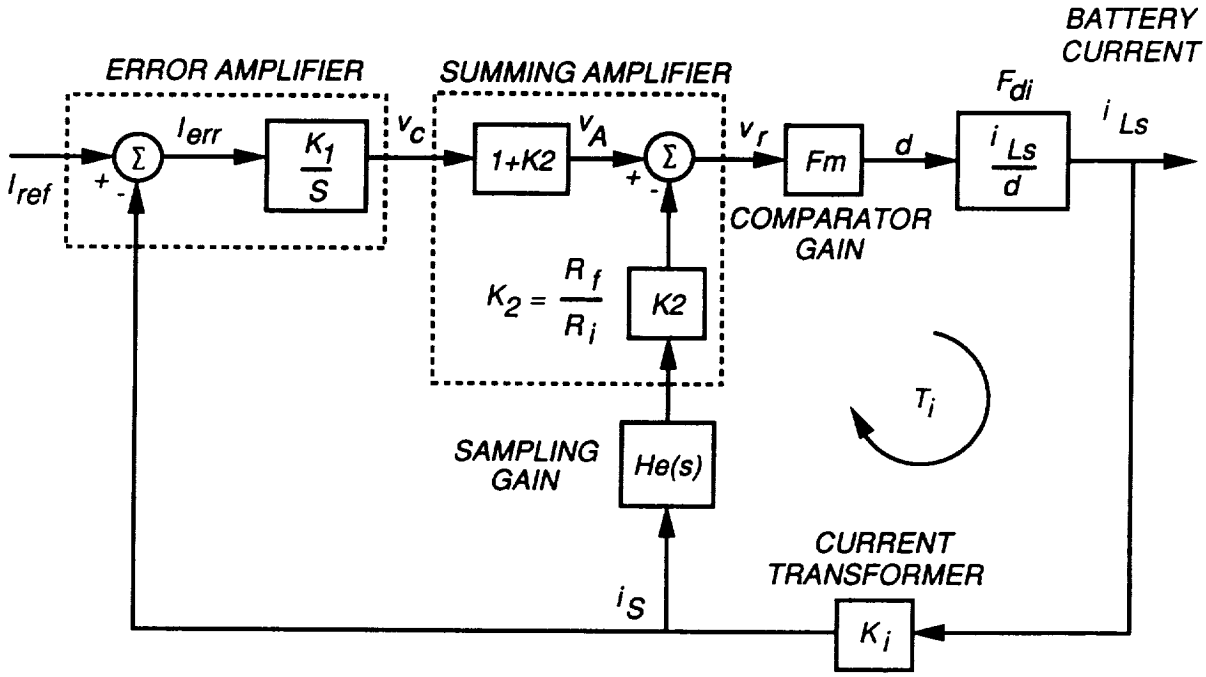


Fig. 4-12. Current regulation control system

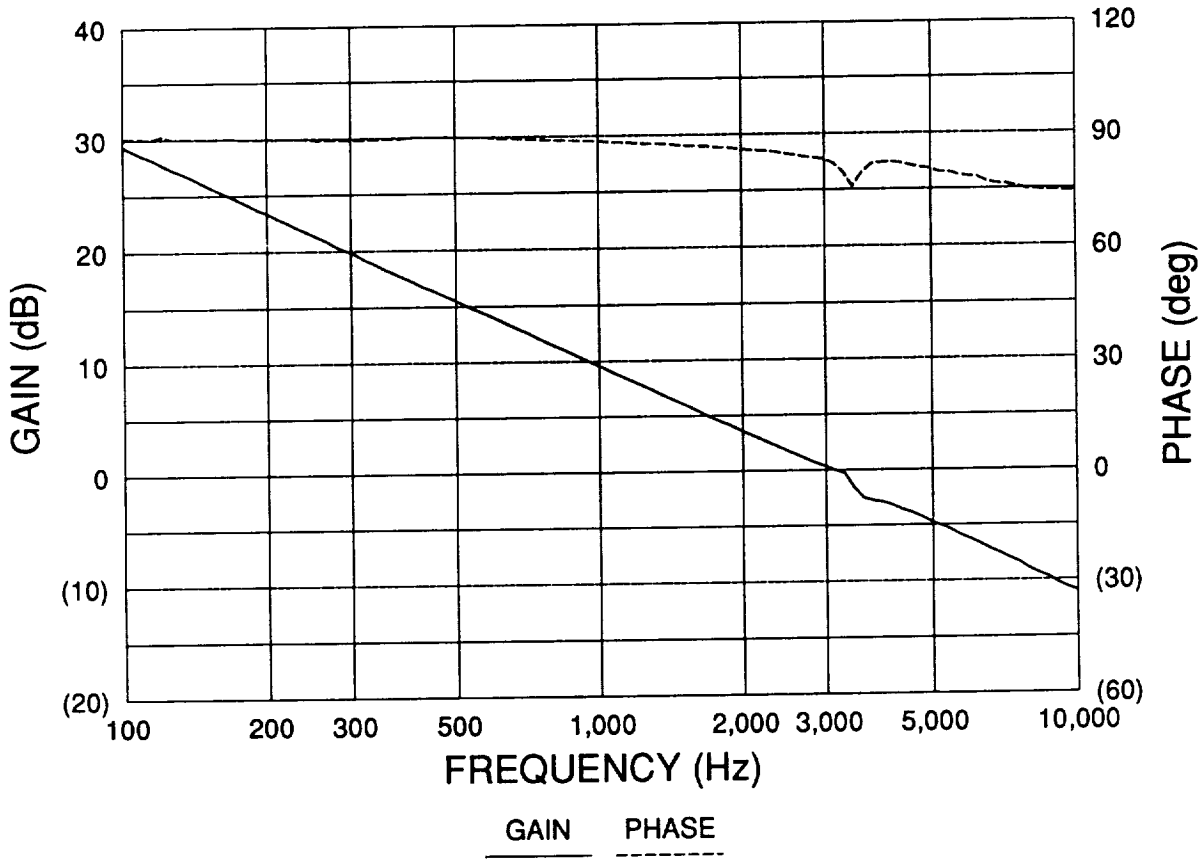
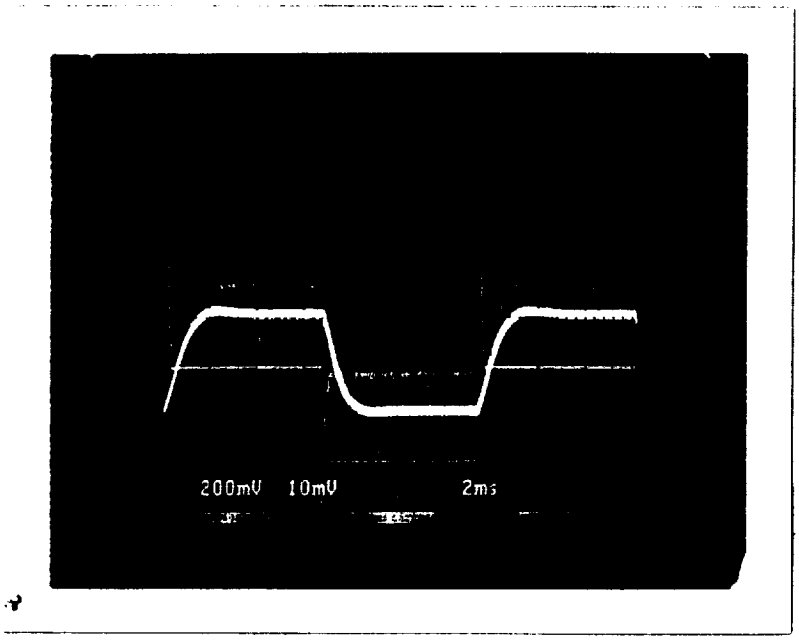


Fig. 4-13. Current loop Bode plot

THE CHARGE CURRENT REFERENCE LEVEL
IS STEPPED BETWEEN TWO LEVELS: 4A AND 8A



L1 CURRENT

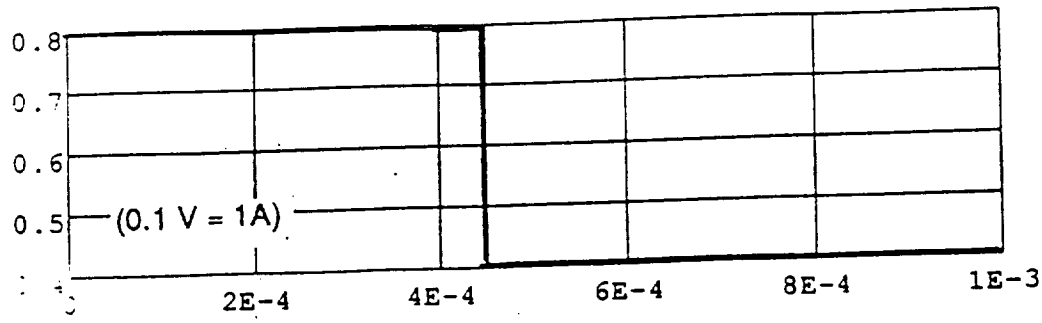
AND

L2 (BATTERY) CURRENT

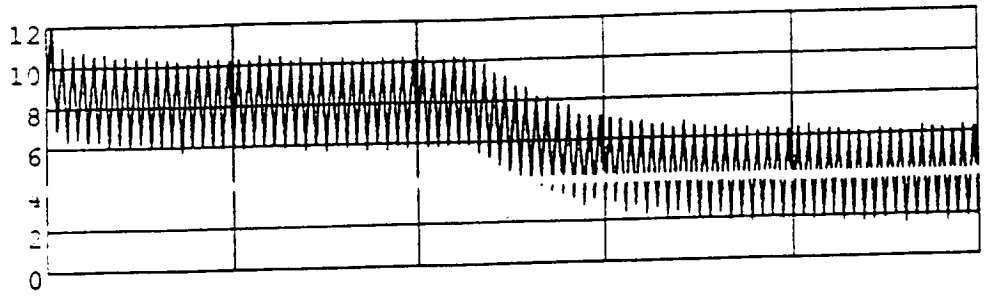
5A/div

Fig. 4-14. Current Loop Step Response

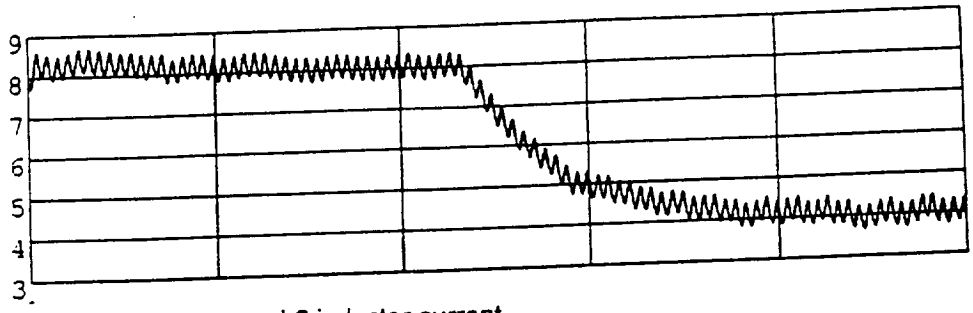
Fig. 4-15. EASY5 simulation of charge current step response



Step change of current reference



L1 inductor current



L2 inductor current

4.5 VOLTAGE REGULATION MODE

4.5.1 Bus Voltage Control

During the transition between eclipse and sunlight, there is a peroid where the solar array has insufficient power to supply the required load and to charge the batteries at the commanded rate. For the Space Platform power system, the battery charger will assume the role of regulating the bus voltage during this post-eclipse transition period. By simply controlling the current drawn from the bus, the charger behaves as a shunt regulator and controls the bus voltage. As the solar array becomes fully illuminated, the charger's current eventually reaches the level required to charge the battery at the constant commanded rate. At this point, the transition from voltage to current regulation is automatically made by the ORing control circuitry within the charger.

During the bus voltage regulation mode, the battery charger regulates its input voltage: hence the charger behaves as a boost converter where the battery voltage is the "input" and the bus voltage is the "output." If the positions of the power stage rectifiers and MOSFETs were interchanged, the charger would indeed look like a conventional boost DC/DC converter. This apparent topology transformation produces a boost converter with negative load current since the direction of current flow is into the battery.

4.5.2 Power Stage Transfer Functions

Using the control model in Fig. 4-7, the key power stage transfer functions are derived for this mode. The open loop control-to-bus voltage transfer function, F_{dv}, is given below:

$$F_{dv} = \frac{\hat{v}_{bus}}{\hat{d}} = -\frac{V_{bus}}{D}\frac{\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{Z2}}\right)}{\Delta(s)} \quad , \tag{4.15}$$

$$\text{where} \quad \omega_{Z1} = \frac{1}{R_1 C_{bus}} \quad , \quad \omega_{Z2} = \frac{V_{bat}}{I_{Ls} L_s} \quad , \quad \text{and}$$

$$\Delta(s) = s^2 \frac{L_s C_{bus}}{D^2} + s\left[\frac{L_s}{D^2 R_{bus}} + \left(\frac{R_{bat}}{D^2} + R_1\right) C_{bus}\right] + 1 \quad .$$

Note that the DC gain of F_{dv} is negative: an increase of the duty cycle produces a decrease of the bus voltage. The zero ω_{Z1} is caused by C_{bus} and R_1, the bus capacitor and its ESR. The other zero, ω_{Z2}, depends on L_s and the DC values of the battery voltage and current. This zero location is clearly highly variable since it depends on I_{Ls}, the battery current. The roots of $\Delta(s)$, the characteristic equation, are normally in the left half plane (LHP). However, since R_{bus} may be negative, under some conditions the s term of $\Delta(s)$ may also be negative, causing a pair of RHP poles [7]. A plot of this transfer function is shown in Fig. 4-16.

The control-to-inductor current transfer function, given by F_{di}, is derived:

$$F_{di} = \frac{\hat{i}_{Ls}}{\hat{d}} = (V_{bus} - D R_{bus} I_{Ls}) \frac{\left[1+\frac{s}{\omega_{Z3}}\right]}{\Delta(s)} \quad , \tag{4.16}$$

$$\text{where} \quad \omega_{Z3} = \frac{V_{bus} - D R_{bus} I_{Ls}}{V_{bus} R_{bus} C_{bus}} \quad .$$

Depending on the operating conditions, the DC gain of F_{di} may be positive or negative. Note that the location of ω_{Z3} may be either in the LHP or RHP, depending on the polarity of the DC gain. A plot of this transfer function is shown in Fig. 4-17.

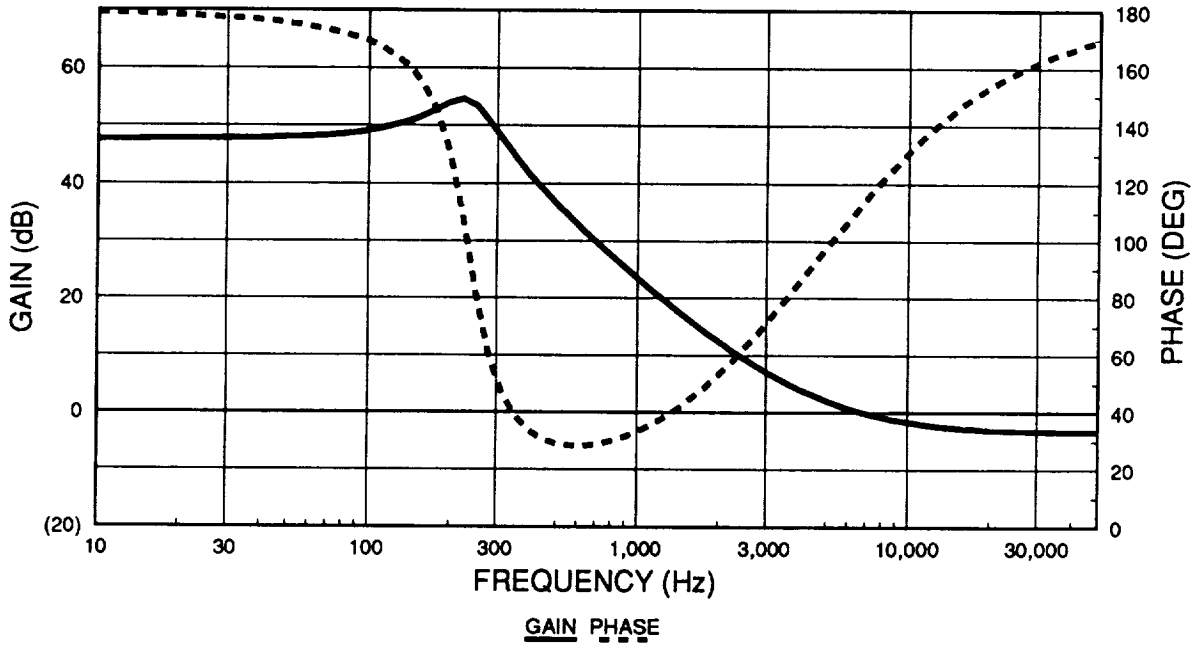


Fig. 4-16. Control-to-bus voltage transfer function

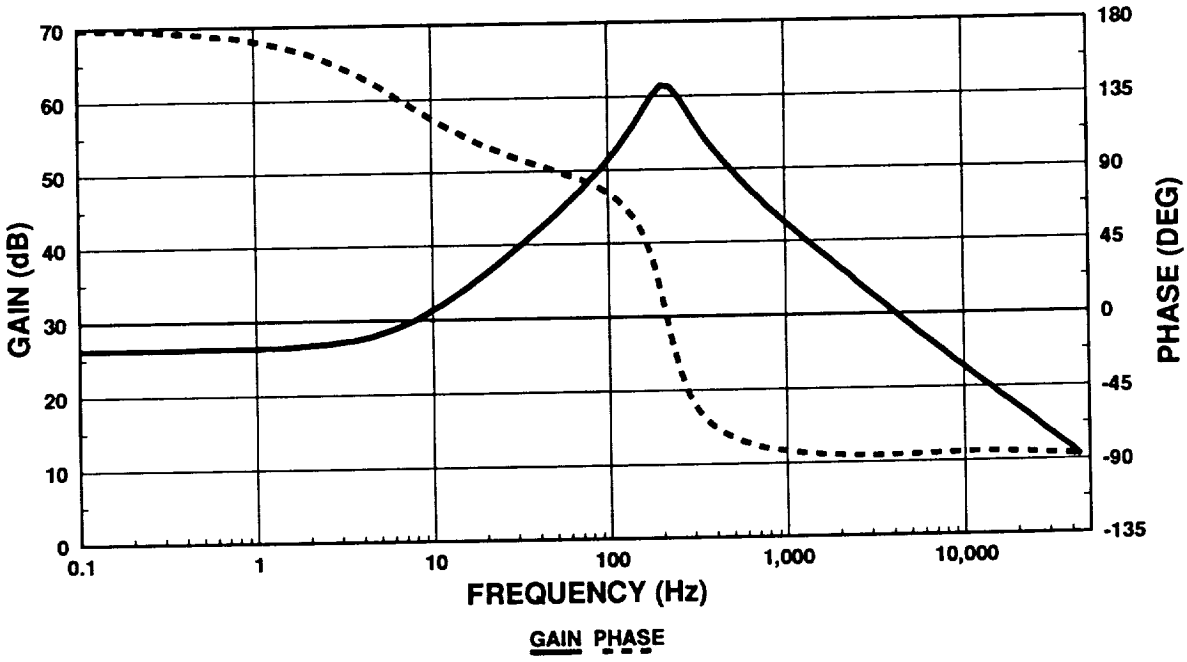


Fig. 4-17. Control-to-inductor current transfer function

4.5.3 Feedback Loop Design

The design of the voltage feedback loop is shown in Fig. 4-18. The system output, the bus voltage, is sensed through the divider ratio K_4 . Since F_{dv} , the control-to-bus voltage transfer function, has a negative DC gain, positive feedback of v_{bus} is necessary to obtain a stable system. The voltage error signal is amplified by the integrating error amplifier. The resulting control signal, v_c , is summed with negative feedback of the inductor current (i_{Ls}). The resulting signal, v_r , is compared against the external ramp to generate the duty cycle (d).

The control loop design begins with T_i , the gain of the current loop. This gain is easily found:

$$T_i = F_m F_{di} K_i H_e(s) K_2 \quad . \tag{4.17}$$

The control-to-bus voltage transfer function, F_v , is solved:

$$F_v = \frac{\hat{v}_{bus}}{\hat{v}_c} = \frac{(1+K_2)F_m F_{dv}}{1+T_i - F_m F_{dv} K_f K_2} \quad . \tag{4.18}$$

As demonstrated in [8], with certain approximations, F_v can be greatly simplified as shown below:

$$F_v = G_x \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\left(1+\frac{s}{\omega_{Z2}}\right)}{\left(1+\frac{s}{\omega_x}\right)\left(1+\frac{s}{\omega_n Q_p}+\frac{s^2}{\omega_n^2}\right)} \quad , \tag{4.19}$$

$$\text{where} \quad G_x = \frac{-F_m V_{bus}}{D(1+G_i)+K_f F_m V_{bus}} \quad ,$$

$$G_i = \frac{\left(\frac{V_{bus}}{R_{bus}} - D I_{Ls}\right)}{D^2} F_m K_i \quad ,$$

$$K_f = -\frac{D K_i}{f L_s}\left(1-\frac{D}{2}\right) \quad ,$$

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)} \quad ,$$

$$\text{with} \quad m_c = 1+\frac{S_E}{S_N} \quad \text{and} \quad D' = 1-D \quad .$$

The dominant pole of F_v is ω_x which, with some approximations, can be shown to be equal to ω_{Z3}, the zero in the control-to-inductor current transfer function (F_{di}). Both ω_x and ω_{Z3} are located at low frequencies (<10 Hz), and both vary directly with the battery current. Under normal conditions, the Space Platform consists largely of constant power loads, so R_{bus} has a negative value. This causes ω_{Z3} to be a RHP zero, which in turn causes ω_x to be a RHP pole. It can be shown through a Nyquist plot that the voltage loop can be stable in the presence of this RHP pole if the loop gain is high enough [8]. The second order polynomial in the characteristic equation for F_v is resonant at half the charger switching frequency. If the external ramp is properly selected, the value of Q_p, the resonant damping factor, will be near unity. In this case, these complex resonant poles will have little effect on the charger dynamic behavior.

The gain of the voltage loop is given by

$$G_{vl} = F_v K_4 \frac{K_5\left(1+\frac{s}{\omega_{z4}}\right)}{s\left(1+\frac{s}{\omega_5}\right)} \quad . \tag{4.20}$$

To compensate the voltage loop, the error amplifier must be properly designed. The compensator pole, ω_5, is set at 9 KHz to attenuate the 90 KHz switching ripple. The DC gain, K_5 , is designed to give a maximum loop gain crossover near 3 KHz so that the bus impedance can be minimized. This crossover frequency must not be pushed out to far since this would decrease the loop attenuation of the 90 KHz switching ripple. Since ω_{Z2}, a zero of F_{di} , is inversely proportional to the battery current, care must be taken to compensate for the movement of this zero. At minimum battery current, ω_{Z2} moves to a high frequency, so the compensating zero, ω_{Z4}, is placed low enough (700 Hz) to provide adequate phase margin. Placement of ω_{Z4} must not be too low since this slows the speed of the voltage loop. A Bode plot of the measured voltage loop gain is shown in Fig. 4-19. The loop crosses over at 2.1 KHz where the phase margin is 81 degrees.

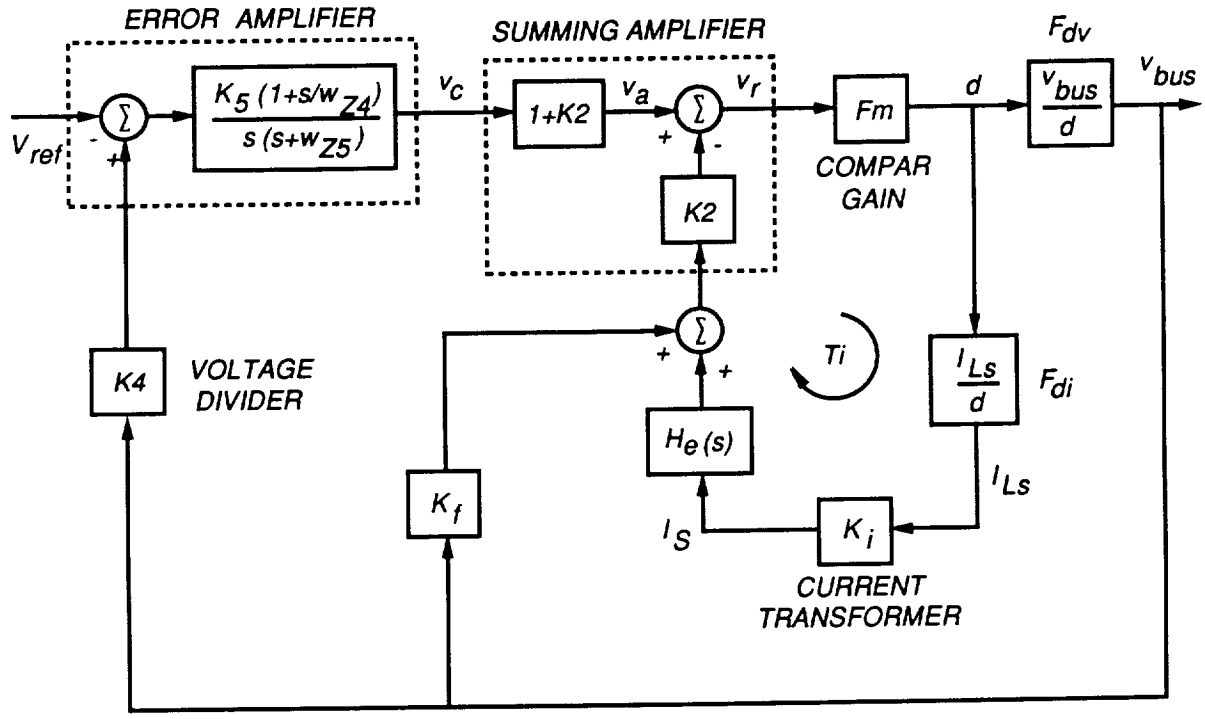


Fig. 4-18. Voltage regulation control system

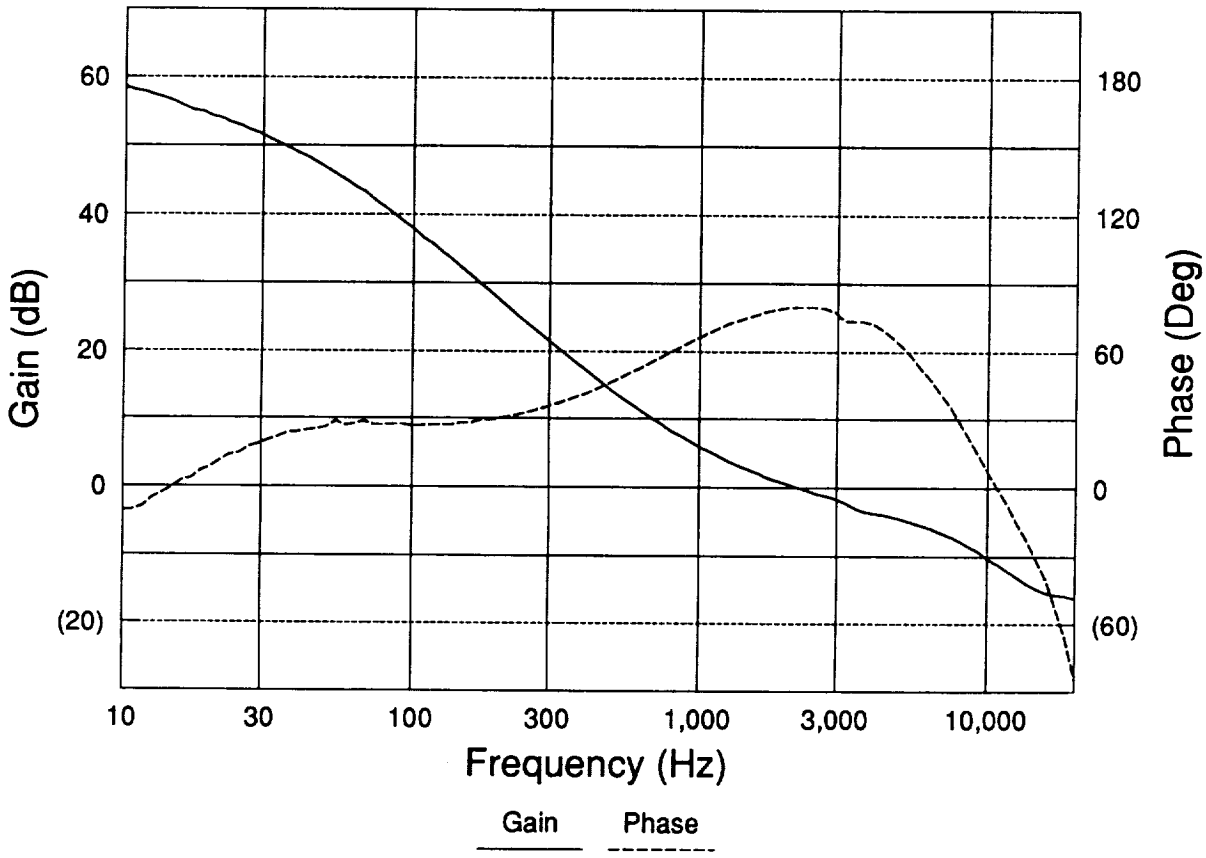


Fig. 4-19. Bode plot of voltage loop

4.5.4 Voltage Loop Performance

To test the transient response of the voltage loop, the bus load current was stepped between two levels. As shown in Fig. 4-20, the bus load current was stepped between 5 and 20 A, and the charger maintained regulation of the bus voltage.

An EASY5 simulation of the charger transient response to a step of the bus load current is shown in Fig. 4-21.

In order to provide a fast transient response with a low overshoot, the charger must have a low output impedance. This is also referred to as the bus impedance since the charger regulates the bus voltage. A measurement of the bus impedance is shown in Fig. 4-22. This impedance is low at lower frequencies because the feedback loop gain is high. In the vicinity of the loop gain crossover point, the impedance reaches a maximum around 60 mOhms. The impedance then falls at a rate determined by the bus capacitance. The impedance then levels off at the value (20 mOhms) of the bus capacitor ESR.

The charger was also tested to determine its level of conducted emissions during the bus voltage regulation mode. The test setup for this measurement is described in Chapter 2. The spectrum of the charger's conducted emissions is shown in Fig. 4-23. The peak current obviously occurs at the fundamental switching frequency (91.3 KHz) of the charger. At this frequency, the bus voltage ripple is found to be 35 mV p-p through the conversion formula presented in Chapter 2. This level is well below the 200 mV p-p bus ripple specification. As can be seen in the spectrum, there are also numerous other peaks in the measurement. These are due to the 17 KHz switching components from the power supply used to simulate the solar array.

THE BUS LOAD CURRENT IS STEPPED BETWEEN TWO LEVELS:

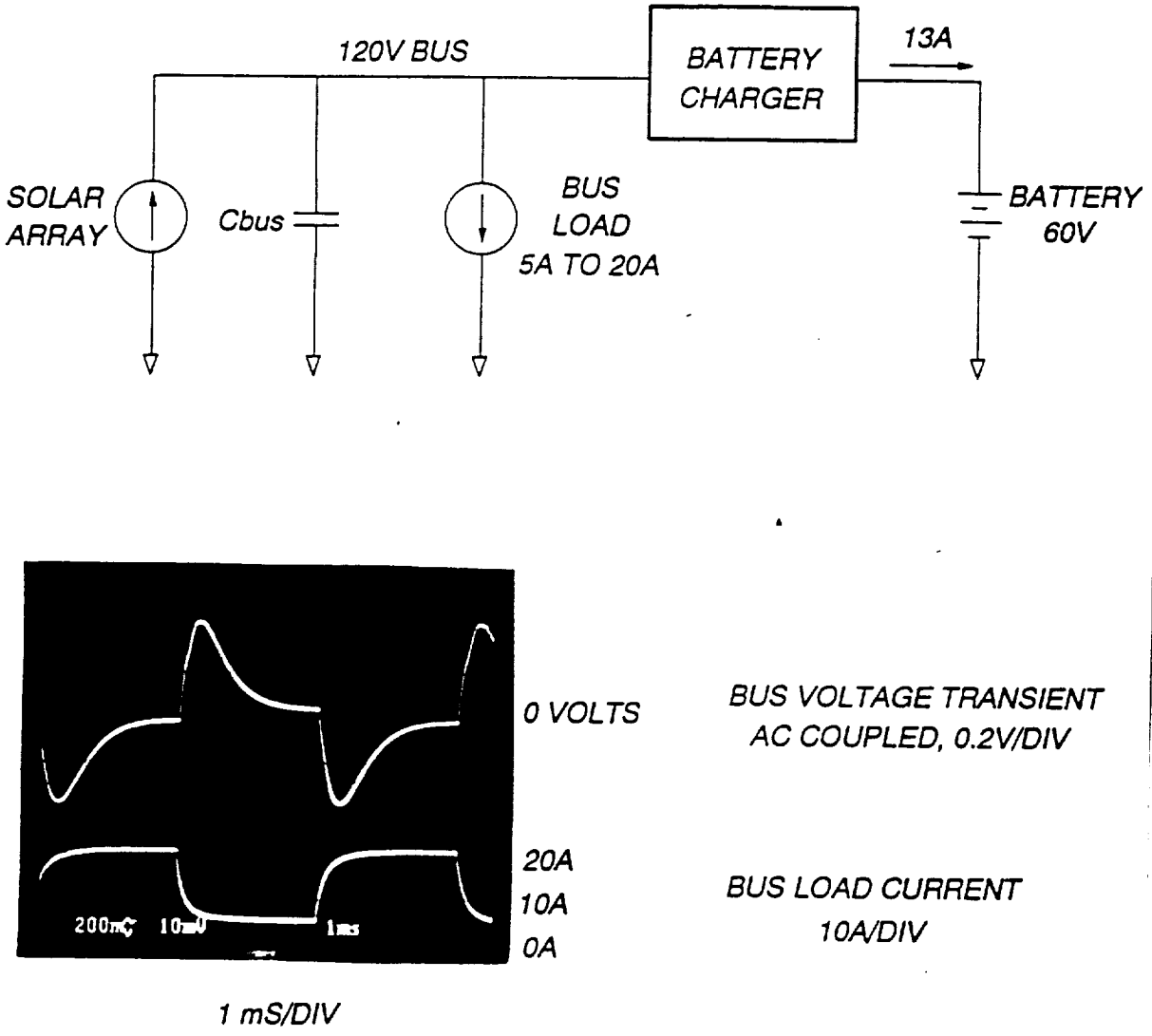
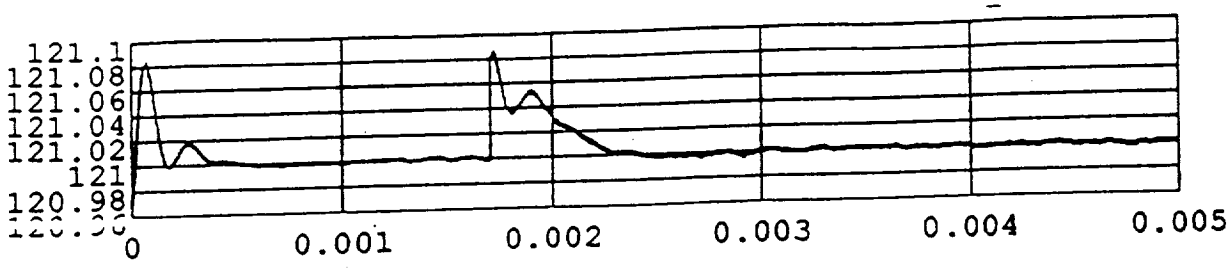
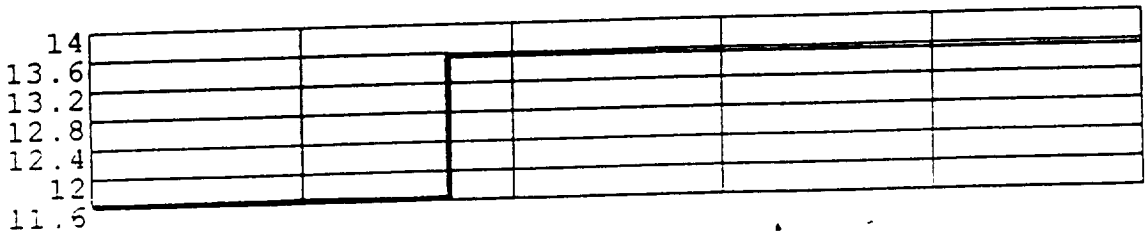


Fig. 4-20 Transient Response of the Voltage Loop

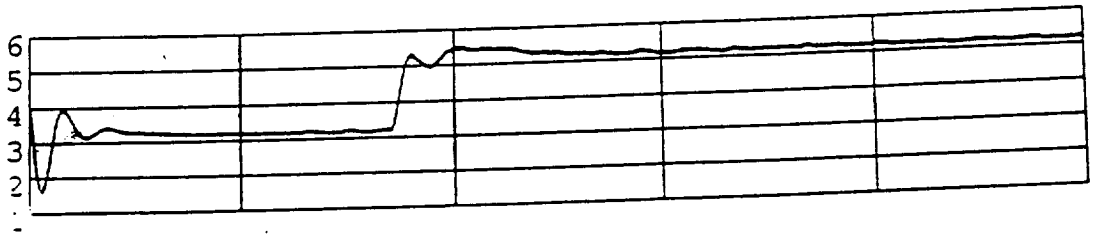
Fig. 4-21 EASY5 simulation of bus load transient in the voltage regulation mode



Bus voltage



Load current



Charger input current

L2 inductor current

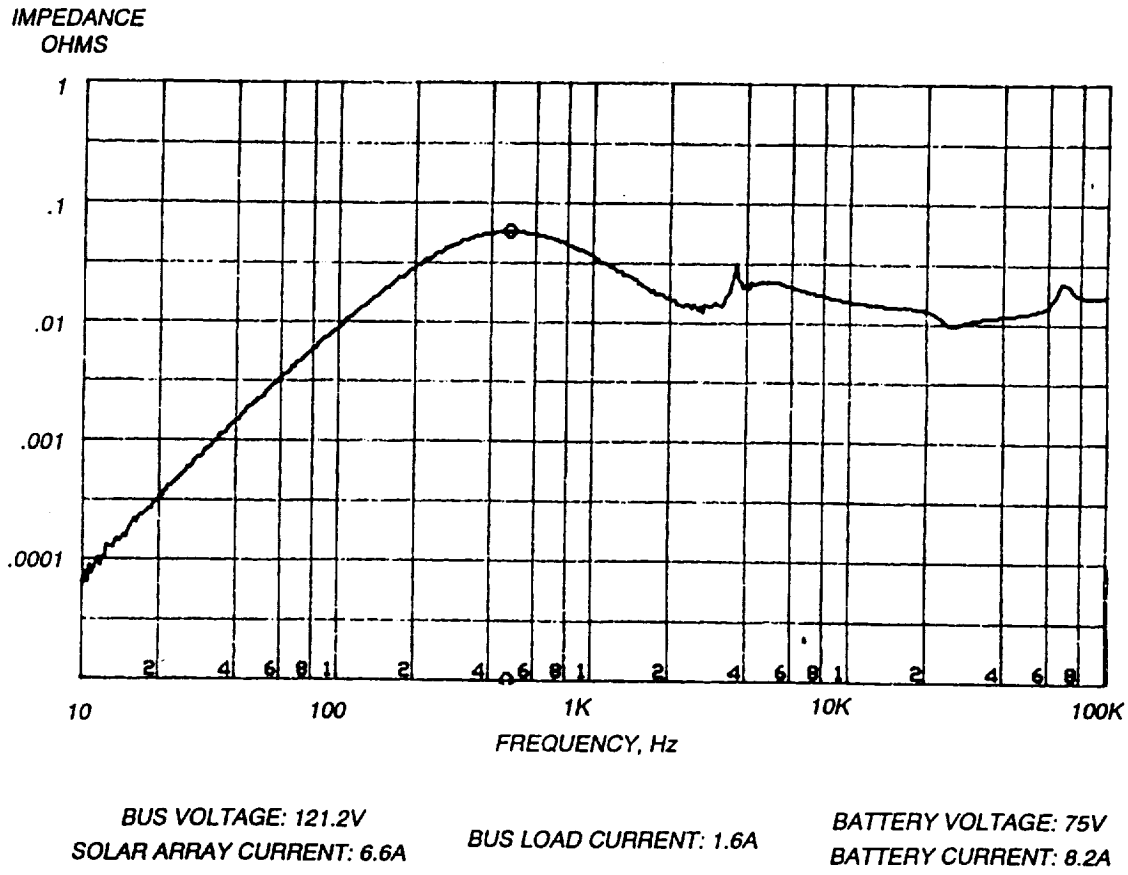


Fig. 4-22 Measurement of Bus Impedance

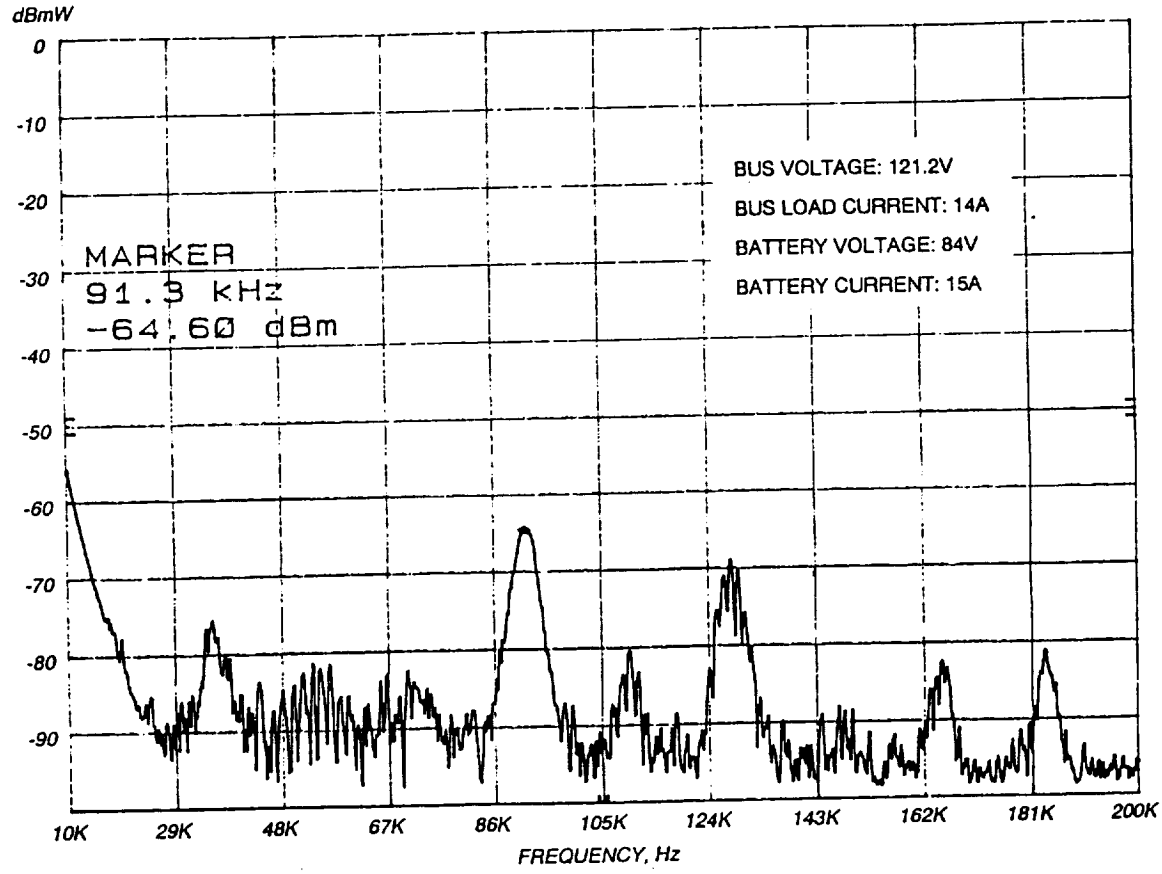


Fig. 4-23 Conducted Emission Measurement of the Charger in the Bus Regulation Mode

4.6 Mode Transition Simulation

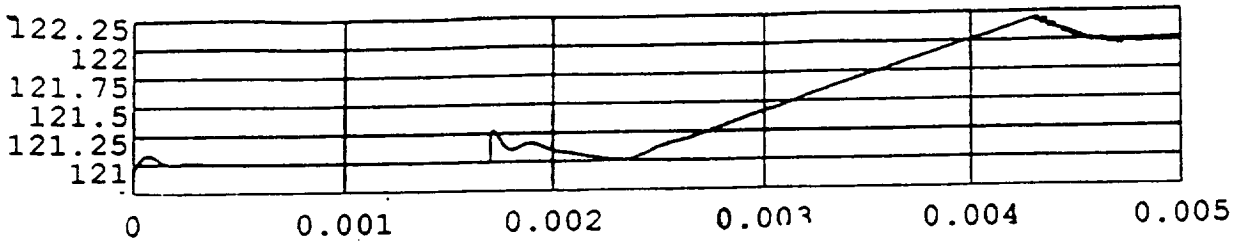
An EASY5 simulation of the transition between voltage and current regulation modes is shown in Fig. 4-24a,b. Initially, the charger is in the bus voltage regulation mode, as can be seen from the control voltages. Whichever of the voltage or the current error signal is the lowest determines the ORed control signal. Since the charger is initially regulating the bus at 121 V, the solar array switching shunt regulator is inactive. Therefore, all the shunt switches are open at the beginning of this simulation. The initial charger input current is 3 A, which is much less than the commanded rate of 8 A.

At time=1.7 mS, the bus load current is stepped from 13.5 A to 7 A. Immediate transients can be seen in all simulated waveforms. In an effort to maintain regulation of the bus voltage, the charger increases its input current to 10.5 A. However, since the commanded battery current rate is 8 A, the charger must make the transition into the current regulation mode. Since the current error control signal is initially saturated high at 4 V, it takes nearly 1 mS for this voltage to fall to the level necessary (2.5 V) to regulate the battery current at 8 A. This time lag is due to the time constant (R_eC_e) of the current error amplifier.

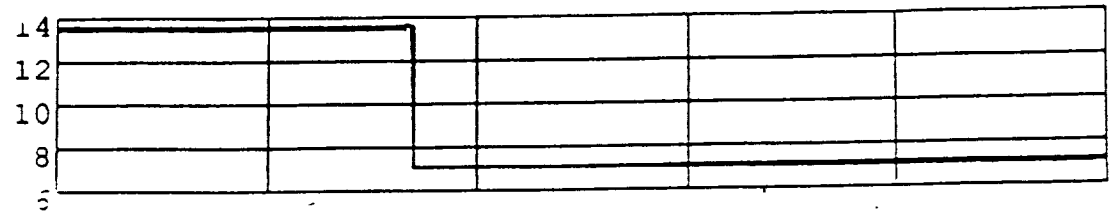
At time=2.3 mS, the current error signal falls below the voltage error signal, so the charger enters the current regulation mode. The ORed control signal follows the current error signal, while the voltage error signal rises up to the +12 V rail of its op-amp. The battery current is then regulated at 8 A for the remainder of the simulation. Since the charger is no longer in the bus regulation mode, the bus voltage rises at a linear rate determined by the values of the bus capacitance and the 6.5 A current step.

At time=4.3 mS, the bus voltage rises to the level where the mode controller (or Power Control Unit, PCU) turns on the solar array switching shunt regulator. After a short delay, the bus voltage is regulated at 122 V by the shunt regulator. The simulation shows that the number of shunt switches is then modulated so that fine regulation of the bus voltage is maintained.

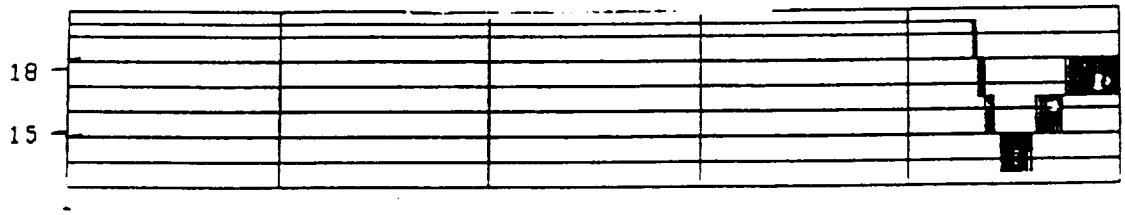
Fig. 4-24a. EASY5 simulation of mode transition



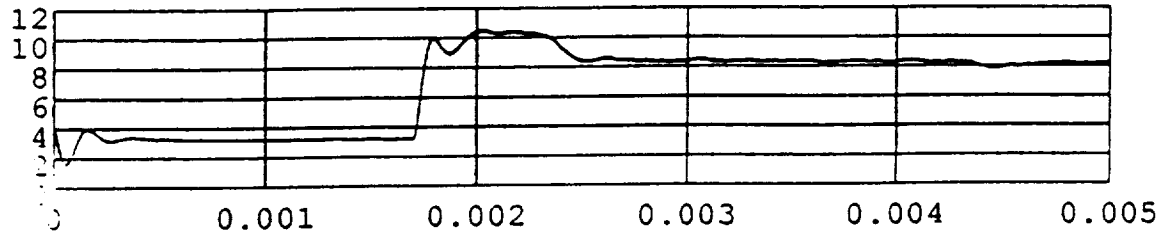
Bus voltage



Load current

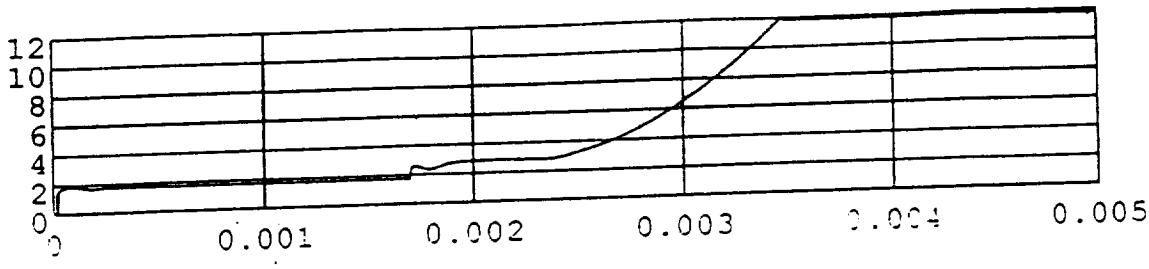


Number of shunt switches open

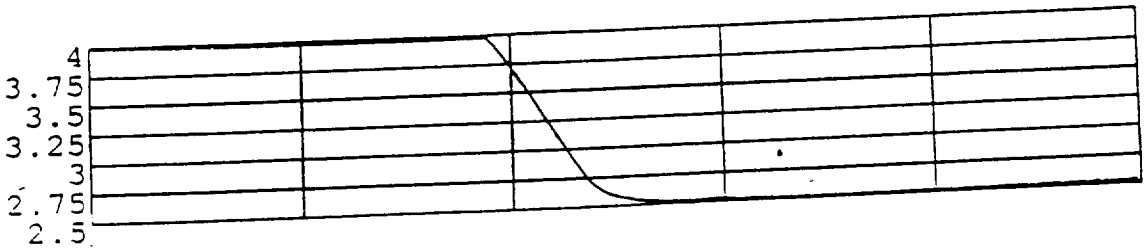


Charger input current

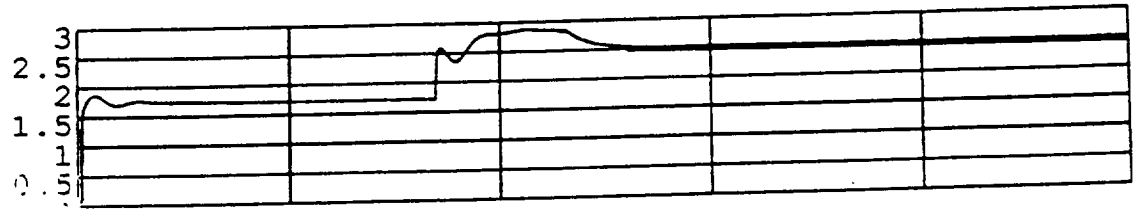
Fig. 4-24b. EASY5 simulation of mode transition



Charger voltage error signal



Charger current error signal



OR'ed control signal

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[3] W. T. McLyman, *Magnetic Core Selection for Transformers and Inductors*, Marcel Dekker, Inc., 1982, pp. 8-16.

[4] V. Vorpérian, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch: Parts I and II," IEEE Trans on Aerospace and Electronic Systems, Vol. 26, No.2, March 1990.

[5] R. Ridley, "A New, Continuous-Time Model for Current-Mode Control," Proceedings of the Power Conversion and Intelligent Motion, Oct. 1989, pp.455-464.

[6] S. Schiffer and E. Pearlman, "Use of V/T Controlled Charging for Nickel Hydrogen Batteries," 1988 IECEC, Vol. 2, pp. 443-446.

[7] Seong J. Kim and Bo H. Cho, "Analysis of Spacecraft Battery Charger Systems," 1990 IECEC, Vol. 1, pp. 365-372.

[8] Seong J. Kim, "Modelling and Analysis of Spacecraft Battery Charger Systems," Ph.D. Dissertation, VPI&SU, April 1991.

5.0 MODE CONTROLLER

The mode controller regulates the bus voltage according to the band structure shown in Fig. 5-1. The dead band between discharge mode and charge mode ensures that the battery charger and discharger never operate simultaneously. In reality, the slopes to the voltage regulation in each of the modes are vertical lines because each of the three controllers contain an pole at the origin.

Bus filter capacitors are included on the mode controller circuit board. The power connection from the mode controller circuit board to the battery ORU is through 20 feet of #10 AWG twisted cable. The error signals for the battery charger and discharger are also sent through 20 feet of cable. Included in this discussion of the mode controller is the circuit design and the theoretical and experimental results, including the effects of the cable.

5.1 CONTROLLER CIRCUIT DESIGN

Fig. 5-2 shows a schematic diagram of the mode control circuit. The output voltage is sensed and compared with the system reference voltage. The difference is amplified so that the gain from bus voltage to amplifier output is unity. The error voltage is divided with a resistor network to yield a boost mode error voltage, charge mode error signal, and a shunt mode error signal. Each of the error voltages are then compensated according to their own dynamics to yield the three error signals.

5.2 THEORETICAL AND EXPERIMENTAL RESULTS

5.2.1 Effects of Cable

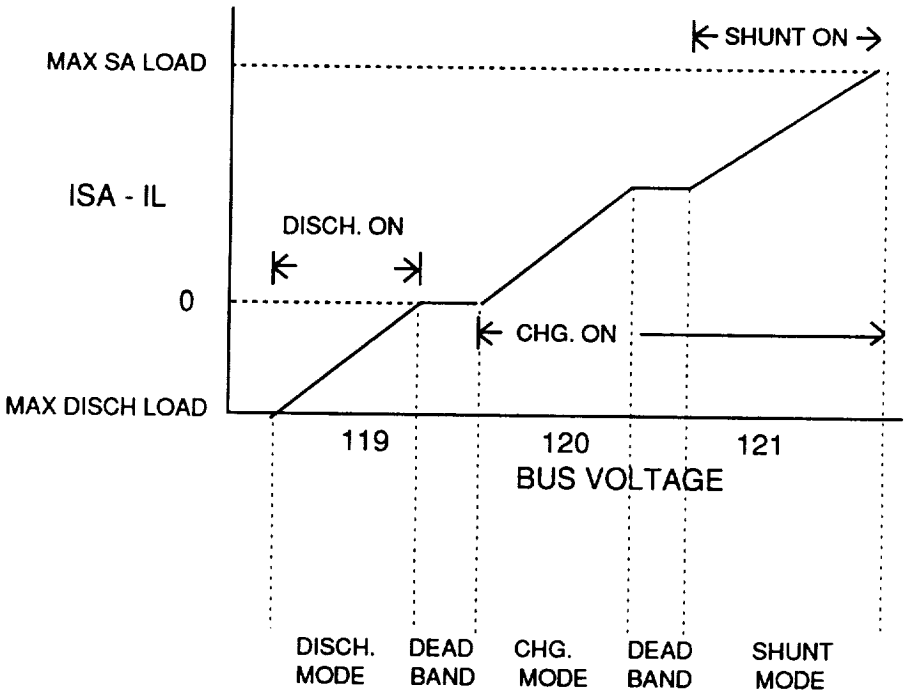


FIG. 5-1 MODE CONTROL BAND STRUCTURE

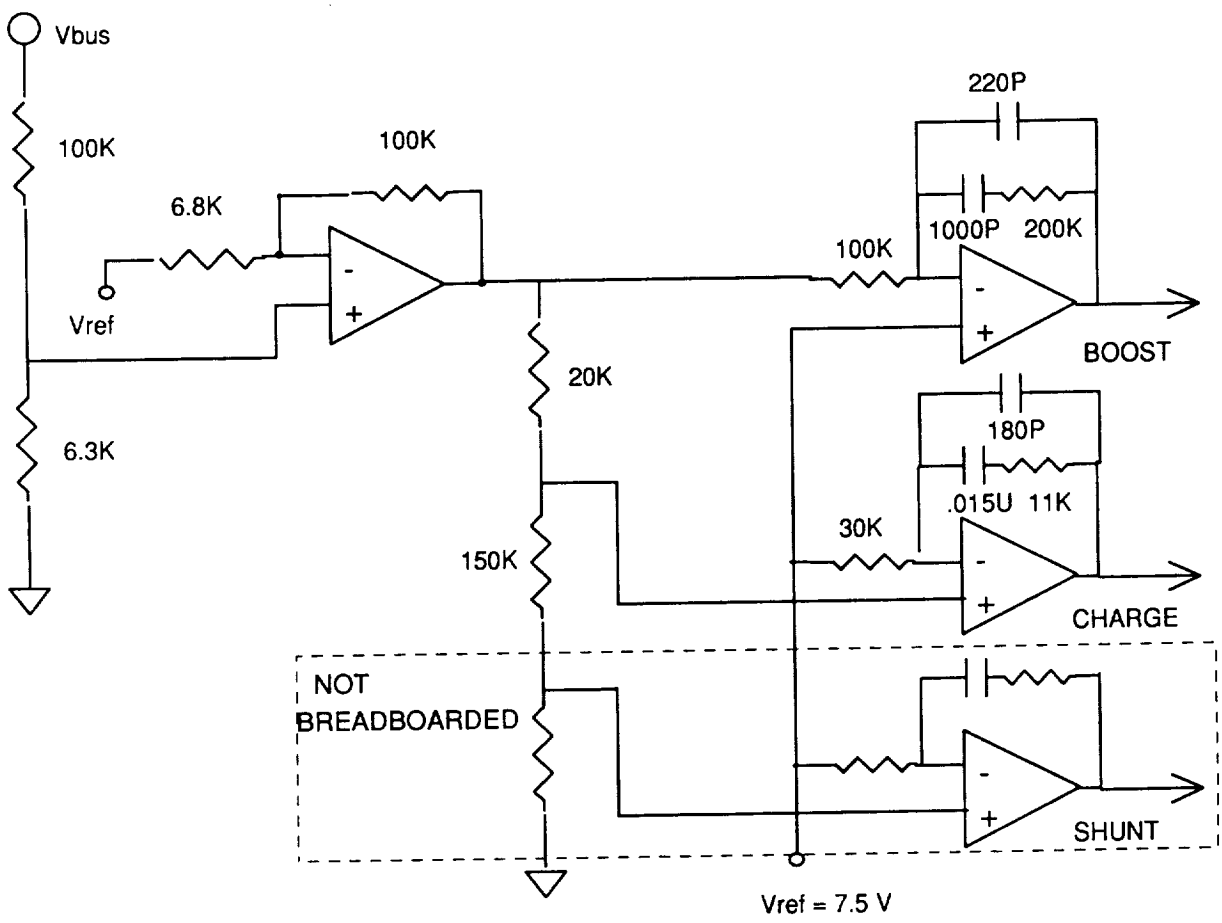


FIG. 5-2 MODE CONTROL CIRCUIT

Fig. 5-3 shows the effects in the four module boost converter loop gain of the twenty feet of cable. The top plot shows the loop gain with the cable. The cross-over frequency is 2.3 kHz with 61 degrees of phase margin and 12 dB of gain margin. The lower plot shows the loop gain after the cable is added. The inductance of the cable resonates with the output capacitance of the boost regulator and introduces some peaking in the loop gain at about 21 kHz. While this has little effect on the cross-over or the phase margin, the gain margin is reduced to slightly greater than 5 dB. Thus the cabling between the battery power ORU and the bus filter can have a detrimental effect on the system stability.

Fig. 5-4 shows the no-load to full-load four module boost converter step transient response. There is only a small difference between this photograph and Fig. 2-19, which shows the transient response without the cable. There is a small additional undershoot when going from full-load to no-load.

5.2.2 Large-Signal Dynamics

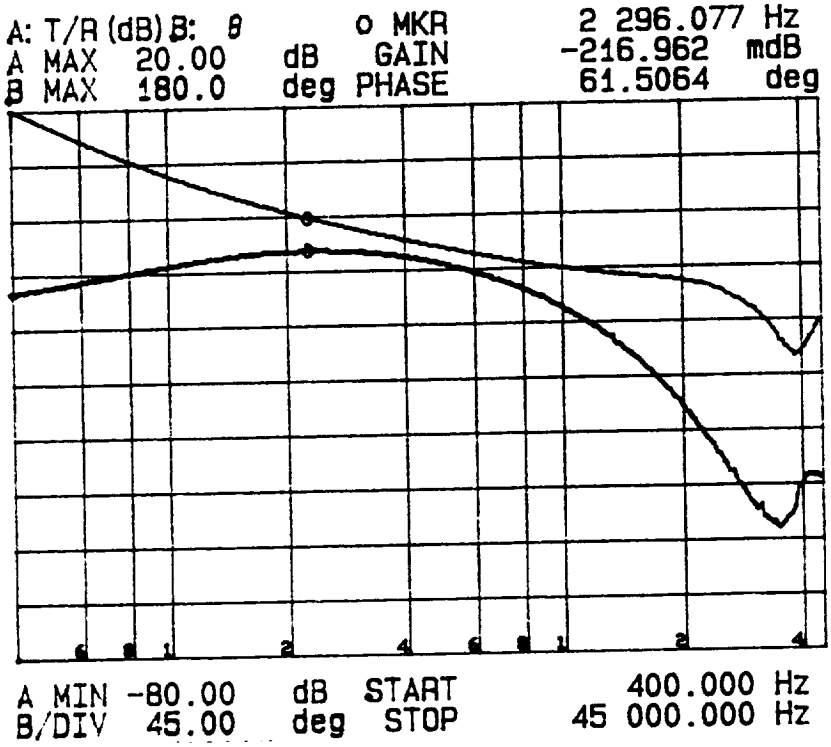
Fig. 5-5 shows a photograph of a large load transient that forces the mode controller to cross between battery charge mode and battery discharge mode. The solar array under these conditions is outputting a constant 8.3 A. The battery charge current select is set for 23 A. The spacecraft load is cycling between approximately 3 A and 12 A. The battery voltage is set to 64 V. The top trace is the bus voltage at 2 V/Div., AC coupled. The next trace shows the battery charger inductor current sense at 1 V/Div. The third trace shows the switch current sense in one of the four module boost converter channels. The lowest trace shows the load current. When the load current is at 12 A, the solar array has inadequate power to supply the load, so the discharger is on, and the charger is off. The bus voltage is regulating at 120 V. When the load steps down to 3 A, the solar array can supply the load. The bus voltage is regulated at 121 V by the battery charger. Note that at no time during the transient are the charger and discharger on simultaneously. There is approximately a 1 V overshoot or undershoot each

FIG. 5-3

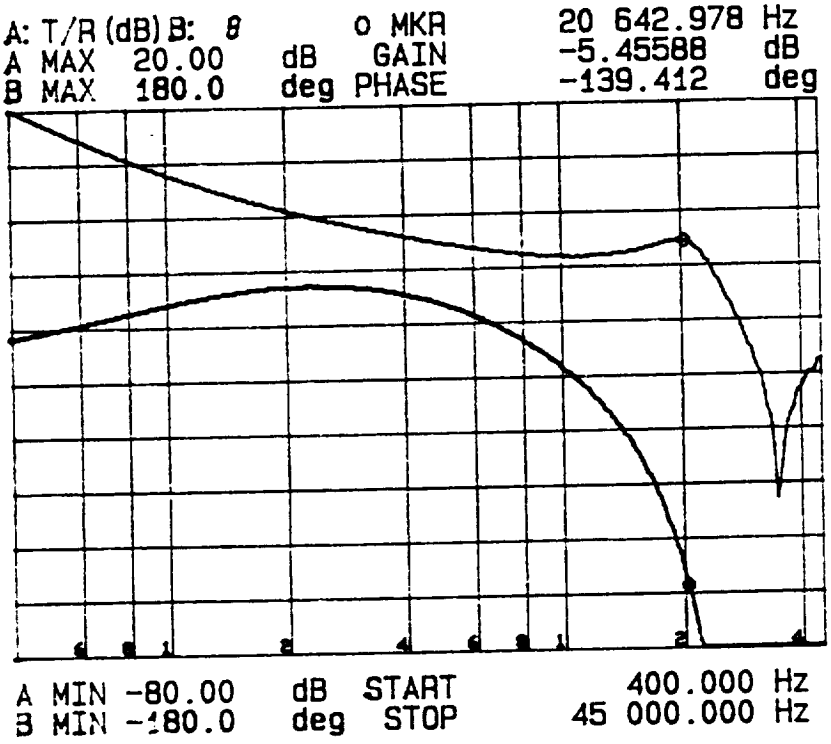
LOOP GAIN COMPARISON WITH AND WITHOUT CABLE

VIN = 64 V, POUT = 1800 W

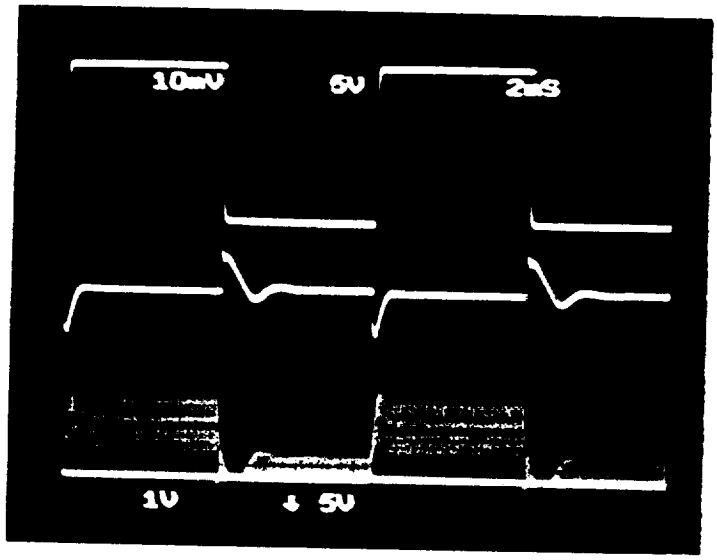
LOOP GAIN WITHOUT CABLE



LOOP GAIN WITH 20' 10 AWG CABLE



Vbatt = 64 V, 1 TO 15 A LOAD STEP



OUTPUT CURRENT 5A/DIV

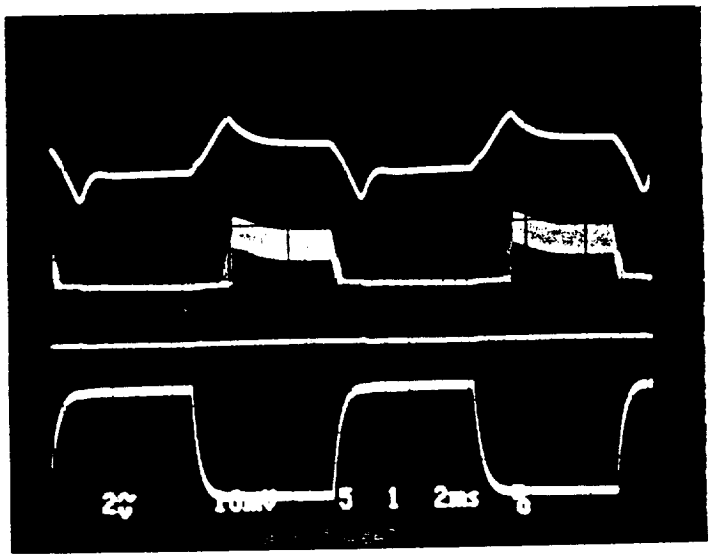
OUTPUT VOLTAGE 1V/DIV

CURRENT SENSE 5V/DIV

2 MS/DIV

FIG. 5-4 LOAD TRANSIENT RESPONSE WITH 20' CABLE

Vbatt = 65 V, 3 A TO 12 A LOAD STEP



VOUT 2V/DIV AC

CHG. ISENSE 1V/DIV.

DISCH. ISENSE 5V/DIV.

OUTPUT CURRENT 5A/DIV.

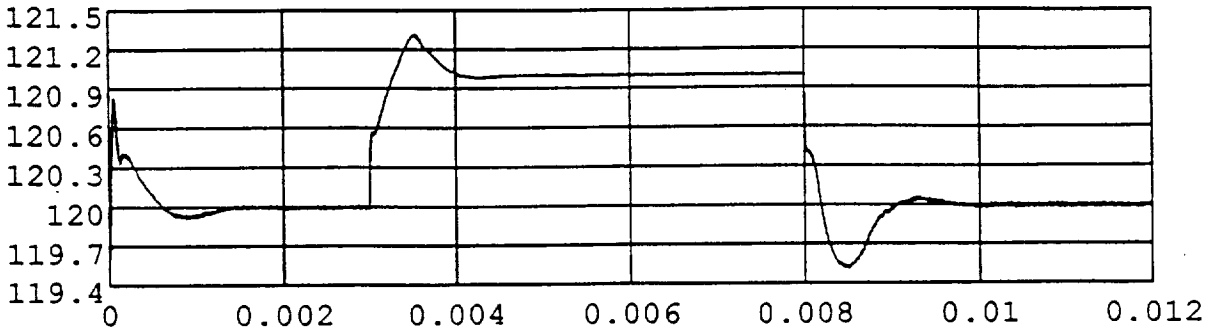
2 mSec/DIV.

FIG. 5-5 CROSS MODE TRANSIENT RESPONSE

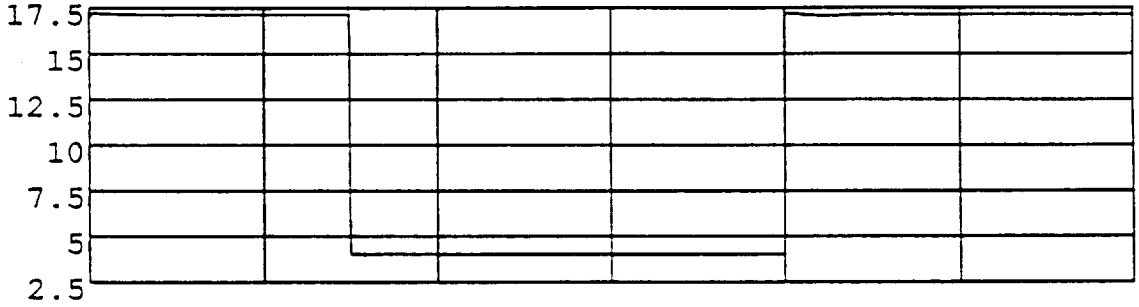
time modes change. The response time is approximately 2 msec. This compares almost precisely with the simulation of the condition shown in Fig. 5-6.

FIG. 5-6

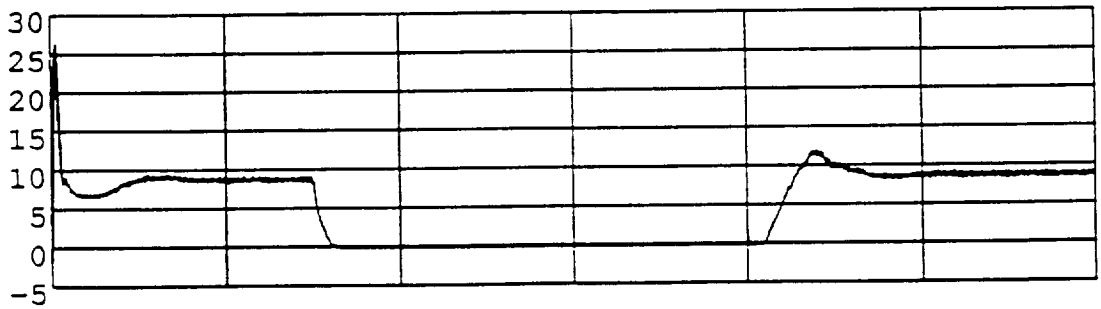
Charger-discharger load cycling test



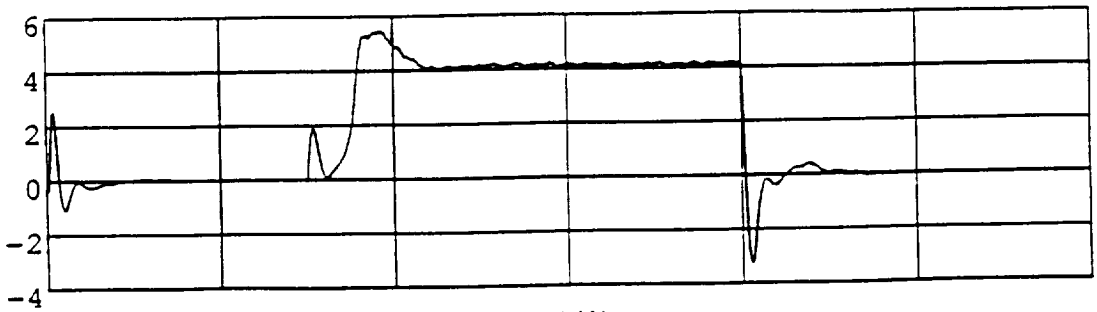
Bus voltage



Load current (A)



Discharger current (A)



Charger current (A)

6.0 OTHER TOPOLOGIES

6.1 BIDIRECTIONAL CHARGER/DISCHARGER

Fig. 6-1 shows a bidirectional battery charger/discharger. This topology was briefly considered for the power ORU. It has the advantage of reusing the power inductor in both charge mode and discharge mode and can potentially result in lighter weight. Since the physical circuitry of the charger and discharger are co-located, it also can result in an even power dissipation over the orbit cycle. However, it also has several disadvantages. There is one additional failure mode in that a failure in the discharger can propagate to the charger. Also, the common inductor must be sized for the worst case mode. In the other mode it is oversized. The is an additional and more subtle problem. The MOSFET body drain diode has a slow reverse recovery. In the past, failures have been induced within the MOSFET by conducting the body diode and following it with a sharp dv/dt. For reliable operation, the body diode should be blocked with a series diode and an additional fast recovery diode placed anti-parallel, as shown in Fig. 6-1. This actually increases the number of semiconductor components when compared against a separate buck charger and boost discharger. It also lowers the efficiency because of the extra series diode drop and extra switching losses. For these reasons, it was decided against using a bidirectional charger/discharger.

6.2 ZERO-RIPPLE CHARGER/DISCHARGER

Fig. 6-2 shows a Zero-Ripple or Two-Inductor buck and boost converter. White [1] and Capel [2] have shown how a topological transformation of normal buck or boost converter can yield beneficial control characteristics. Also, zero input current ripple can conceivably be obtain by coupling the two inductors together. An analysis has shown that these topologies do not offer any weight or efficiency advantage over a conventional buck or boost converter. Also, since the

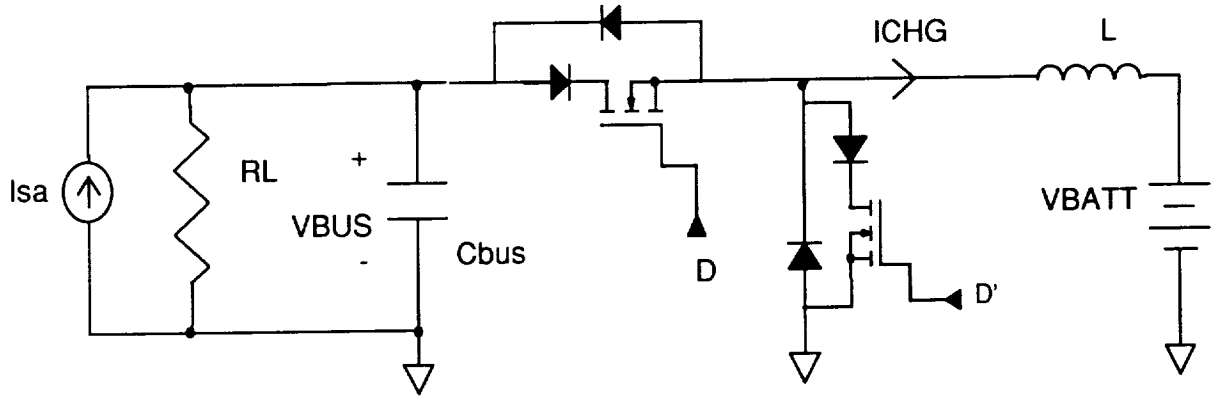
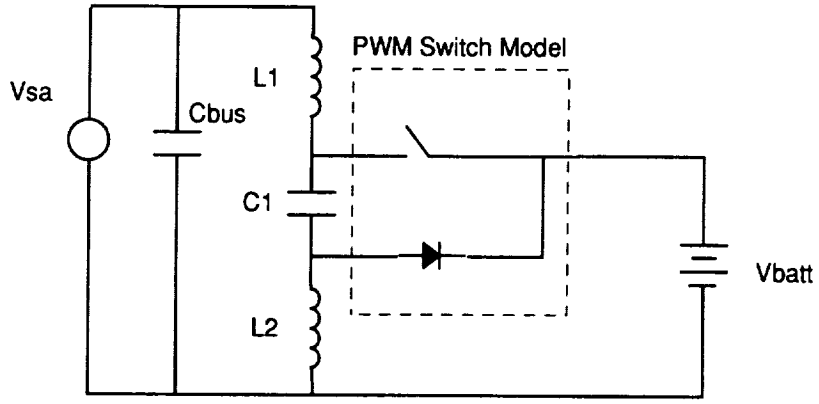


FIG. 6-1 BIDIRECTIONAL CHARGER/DISCHARGER

ZERO RIPPLE BUCK CHARGER



ZERO RIPPLE BOOST DISCHARGER

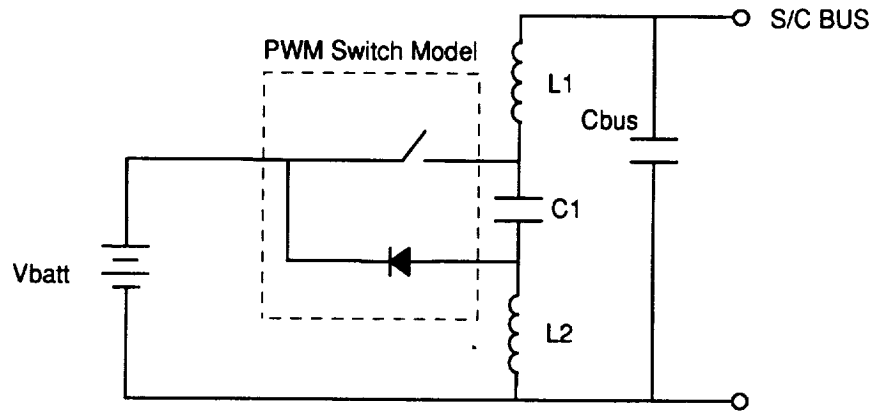


FIG. 6-2 ZERO RIPPLE BUCK AND BOOST CONVERTER

capacitor is floating, one cannot benefit from a multi-module, multi-phase converter. Hence, the internal capacitor is subject to very high RMS current stresses. Sizing the capacitor to meet its ripple current ratings will result in a heavier converter.

The control characteristics can be better, but only if the inductors are not coupled. Since control was not a problem with the charger and discharger, a zero-ripple buck and boost converter were not incorporated for the charger and discharger.

6.3 MULTI-MODULE CHARGER

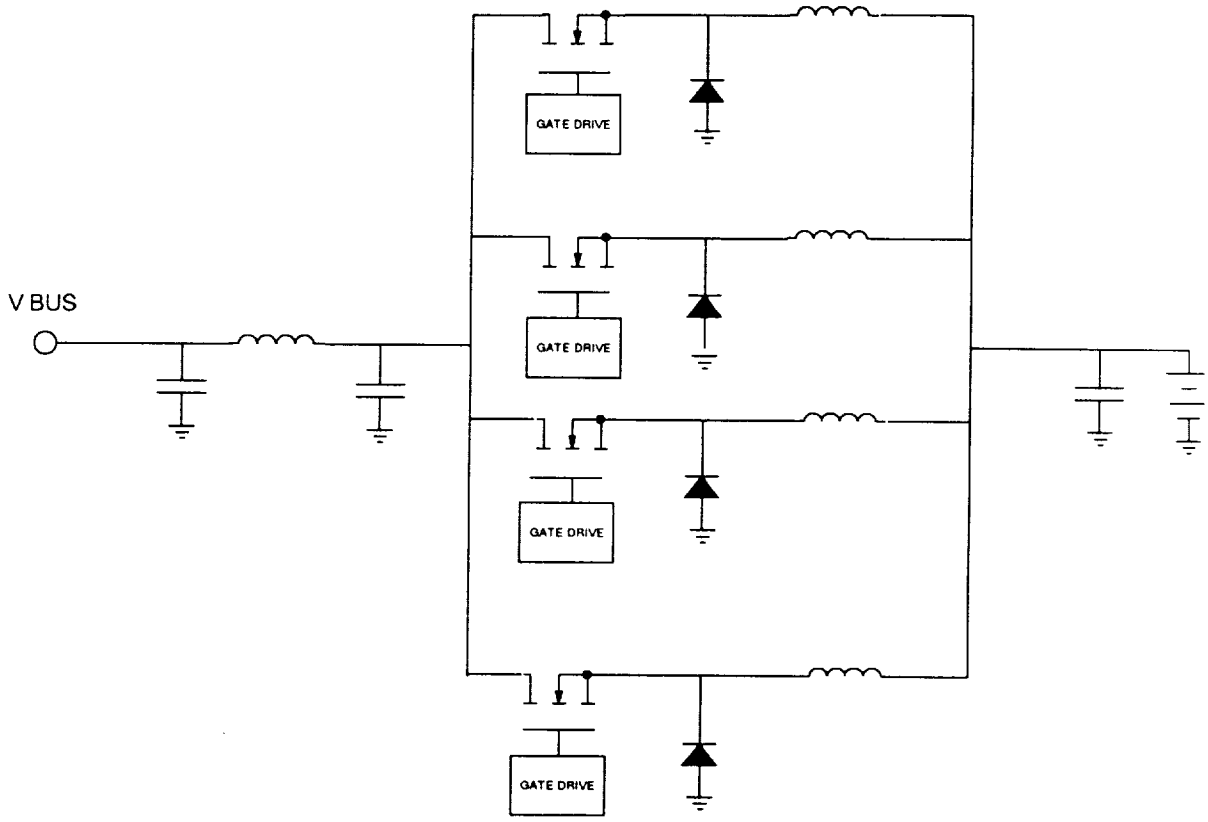
A multi-module battery charger (MMBC) is presently being investigated for the Space Platform power system. The MMBC has potential performance improvements over the single module buck charger. A schematic of the proposed charger is shown in Fig. 6-3. The MMBC power stage will require four power inductors compared to one for the single module. This increase in weight should be offset by reduced input and output filter requirements.

The main feature of the MMBC is the phasing of the modules. In the proposed system, each channel will be 90 degrees out of phase. This reduces input and output current ripple significantly. Another advantage of the multi-phase operation is improved transient response. This occurs since the input and output filter see a ripple frequency four times the switching frequency.

This investigation will be pursued in detail during the next phase of the hardware development contract.

FIG. 6-3

MULTI-MODULE BATTERY CHARGER



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[1] J.L. White and W.J. Muldoon, "Two-Inductor Boost and Buck Converters," IEEE PESC, June, 1987.

[2] A. Capel, H. Spruyt, A. Weinberg, D. O'Sullivan, A. Crausaz, and J.C. Marpinard, "A Versatile Zero Ripple Topology," IEEE PESC, April, 1988.

7. EASY5 COMPONENT AND SYSTEM MODELS

CONTENTS

7.1 INTRODUCTION

This section describes the EASY5 model files developed for the space platform power system hardware. The models have been used to simulate the operation of the power system for this report.

Some simulations have been included in the preceding sections, along with the corresponding hardware description. Additional simulations (which include the solar array shunt switching unit) are presented at the end of this section.

Guidelines are presented for running EASY5 simulations using these models. This section discusses the use of switch states, the integration method to be used (INT MODE), math overflow, and the adjustment of time-step (TINC) needed with abnormal component values.

Finally, brief descriptions are given for error amplifier, converter, and transmission line modeling, followed by small-signal EASY5 models. Most of the small-signal analysis has been carried out in the preceding sections by the use of SPICE simulations. Small-signal EASY5 models are available for the VFPPAT discharger and the charger.

7.2. COMPONENT MODEL FILES

The space power system is divided into a set of invariant ***component*** models which serve as "building blocks." These are basic modules such as filters, error amplifiers, converters, adders, etc. The component model files have a two letter name with the extension MOD:

XX.MOD.

7.3. SUBSYSTEM AND SYSTEM MODEL FILES

The component models are connected as required to form ***subsystem*** models. These represent the charger, mode controller, discharger, shunt, etc., (and various combinations of these up to a full system). The subsystem models include converters, input and output filters, and the control circuits.

The subsystem and system model files also have the extension MOD but are distinguished by using a file name with more than two letters:

XXX.MOD.

7.4. ANALYSIS FILES

A subsystem model can be run with any desired values for the components (R,L,C) or parameters (gain, cutoff frequency, switching period, etc.) by stating the values in the analysis file with the same name, and the extension ANC:

XXX.ANC.

A list of the subsystem models and analysis files is provided in the Appendix. Each subsystem simulation is set up for a specific purpose, such as:

- to observe the steady-state waveforms in one unit (ripple, peak current, or voltage etc.);
- to observe the response to a step change of load (bus voltage regulation);
- to observe the relative response times of the various units during mode transitions (i.e., if compensation and op amp output clamp limits are okay);and
- to observe the entire system behavior with changes in illumination level and load (for example, what units become active for a given load current and illumination level)

The last mentioned test is particularly useful in determining if the mode controller design is successful in maintaining the bus voltage within limits during mode transitions. It is also used to study the transitions that are induced by large step load changes.

The Appendix contains a list of the basic component model descriptions with the EASY5 inputs and outputs for each model.

This modular approach of connecting component models as desired is versatile. In case of changes in the charger, discharger, etc. configurations, the new subsystem models can built up from the same set of basic component models. However, additional component models may be required to suit specific needs.

7.5. SWITCH STATES, NONLINEARITIES, AND INTEGRATION METHODS

The models are set up to provide accurate large-signal behavior of the hardware, including nonlinearities, such as the solar array characteristic, and the saturation of output voltage in error amplifiers.

In order to accomplish this, it is necessary to use switch state representation, wherever appropriate, in the component models. The purpose of the switch states is to allow the use of variable time step integration algorithms, which consume less simulation time.

Switch states are needed to provide a smooth changeover from one set of differential equations to another set. Examples of where this occurs are:

- an inductor current becomes discontinuous instead of reversing, due to the unidirectional nature of the switch,

- an error amplifier output clamps at the saturation (or preset) limit instead of following the linear compensation equations,or
- a PWM comparator output switches from 1 to 0 due to the control voltage crossing the ramp.

Without switch states, it would be necessary to use smaller time steps. The models with switch states work satisfactorily only with variable time step integration methods.

Only variable time step integration algorithms should be used. The **INT MODE = 1** (variable time step BCS Gear) method is found suitable.

7.6. ABNORMAL COMPONENT VALUES, SHORT TIME-CONSTANTS, AND TINC

If abnormal values are chosen for the components, the simulation may fail due to "math overflow" (despite the automatic reduction of step size). An example of what constitutes "abnormal" is given below:

Consider a series resistor-inductor arrangement in a model. With

R = .002 ohm, and

L = 10 uH,

the associated time constant is 5 milliseconds. A time increment (TINC) of 0.4E-7, as used in the analysis files, is more than adequate.

However, if R is changed to 20 ohms, the time constant changes to only 0.5 microseconds. Usually, it is possible to alter component values for both R and L to avoid this. However, if it is necessary to run the simulation with these abnormal values, a suitably small TINC should be used. There will be a corresponding increase in simulation time.

It is noted that the size of the ***time constants*** rather than the components is of concern here.

In case of a math overflow, TINC should be decreased.

In general, a model with very short time constants needs a very small TINC. Short time constants are introduced, for example, by the use of connecting cables.

7.7 CONVERTER MODELING

Figure 7.1 shows the model for a single boost converter (BT.MOD). It will serve to demonstrate the use of switch states. The other models use switch states in the same way. The converter follows one of two sets of equations, depending on whether the switch is open or closed.

If IQ_BT = 1, (switch closed):

$$\frac{di}{dt} = \frac{V_1 - ri}{L}$$

$$i_s = i$$

where

i = inductor current,

i_s = switch current,

L = boost inductor,

r = inductor ESR,

V_1 = input voltage, and

V_o = output voltage.

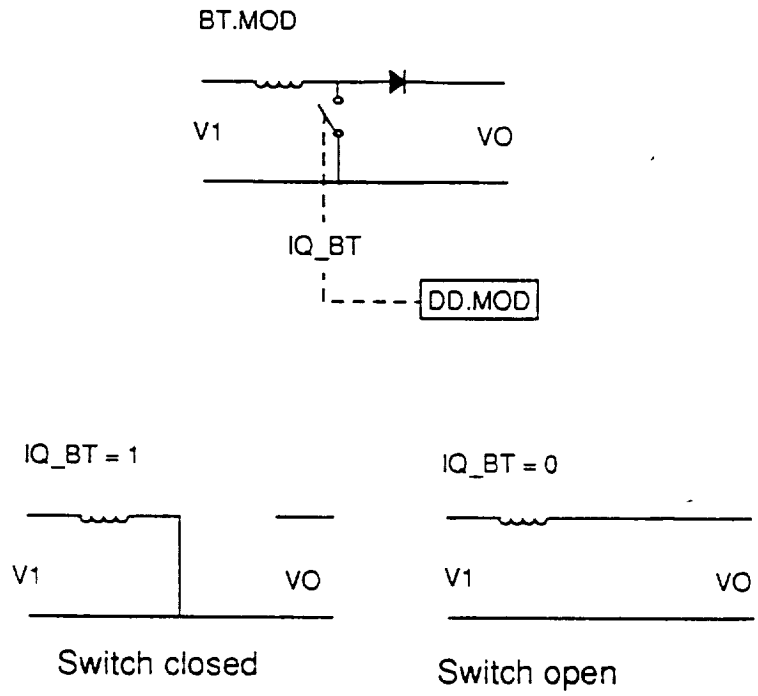


FIG. 7.1 BOOST CONVERTER MODEL

If IQ_BT = 0, (switch open):

$$\frac{di}{dt} = \frac{V_1 - ri - V_O}{L}$$

$$i_s = 0$$

It is necessary to use the switch state IQ_BT to switch from one equation set to the other. In this case, the switch state IQ is obtained from the pulsewidth modulator model (DD.MOD) as SW_DD. It is generated by comparing the control voltage with the ramp (in DD.MOD).

However, it is also necessary to consider that the inductor current cannot reverse because the switch is unidirectional. In order to accomodate this, a third switch state SWLBT is used. This is normally equal to 1, but is set to 0 if the inductor current is zero or less. When SWLBT=0, the inductor current is not allowed to change unless di/dt becomes positive and changes SWLBT back to 1.

7.8 ERROR AMPLIFIER MODELING

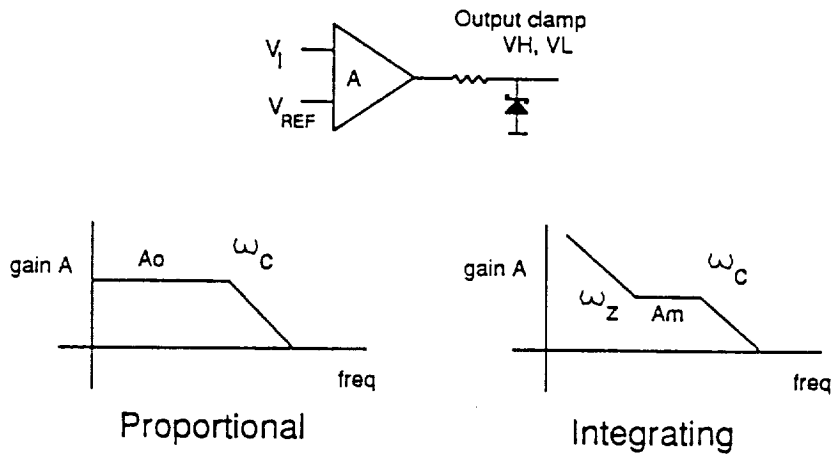
Proportional error amplifiers (Fig 7.2a) have one cutoff frequency and must be modeled with one continuous state. They follow the equation:

$$A = \frac{A_O}{(1 + s/\omega_c)}$$

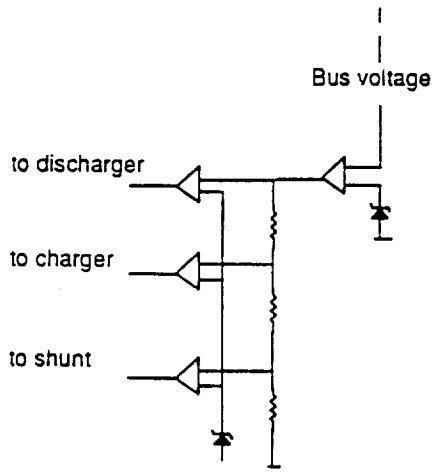
where

A_O = proportional gain, and

ω_c = cutoff frequency.



(a) Error amplifier models



(b) Mode controller model

FIG. 7.2 ERROR AMPLIFIER AND MODE CONTROLLER MODELS

Integrating error amplifiers have two states and must be modeled with two continuous states. They follow the equation:

$$A = \frac{A_m(\omega_z + s)}{(1 + s/\omega_c)}$$

where

A_m = midband gain,

ω_z = zero frequency, and

ω_c = cutoff frequency.

In addition, either type could be inverting or noninverting. This results in four error amplifier types:

EN.MOD = proportional inverting amplifier,

ET.MOD = proportional non-inverting amplifier,

EM.MOD = integrating non-inverting amplifier, and

EI.MOD = integrating inverting amplifier.

Each error amplifier has two inputs, V_I and V_{REF}. The difference voltage is amplified according to the above equations (converted to time domain) to give the output voltage.

Apart from the compensation, it is also necessary to ***clamp*** the output of these amplifiers to some finite voltage. Typically, out of three error amplifiers in the system, two are not in the feedback loop and saturate. In a simulation, this implies the output voltage will rise to abnormal levels and indicate an incorrect time for the error amplifier to enter the active region. This in turn will indicate an incorrect bus voltage as one unit stops regulating and another takes too long to begin regulating.

In the hardware, the error amplifier output is automatically be clamped to the supply voltage (or to any preset clamp voltage).

The output voltage can be clamped by using the upper and lower clamps V_H and V_L in all four error amplifier models. When n particular clamp value is desired, these should be clamped to the supply voltage of + 12 and 0, respectively.

The ***mode controller*** model (Fig. 7.2b) consists of a proportional amplifier cascaded with either of three integrating amplifiers, one each for the shunt, the discharger, and the charger. This arrangement is used in SYSTEM.MOD.

7.9 CONNECTING CABLE MODELING

A transmission line (Fig. 7.3) is a two port network which acts as a sequence of series and parallel resonances as frequency is increased. With the far end open, the impedance is capacitive at low frequencies. As frequency is increased, there is series resonance, followed by reactive impedance, and then parallel resonance (Fig. 7.3a). With the far end shorted, a similar variation is observed, beginning with a reactive impedance.

For a complete representation, this implies an infinite number of time constants of decreasing value. Since time domain simulations require a definite minimum time increment (TINC), complete representation is ruled out.

To arrive at a reasonable lumped equivalent circuit, the impedance of 20 feet of connecting cable used in the hardware was measured (Figs. 7.4, 5). It was observed that the first resonance takes place at a frequency of over 6 MHz. In contrast, the highest frequency of interest is about 180 kHz (four module boost ripple frequency).

The simple lumped circuits of Fig. 7.3b therefore adequately represent the connecting cable in a simulation up to the first resonance frequency. These are capacitive with the the far end open, and inductive with the far end shorted. The L and C parameters for these can be obtained from impedance measurements on the actual cable. The impedances exhibited by the model are compared with the cable impedances in Figs. 7.4 and 7.5.

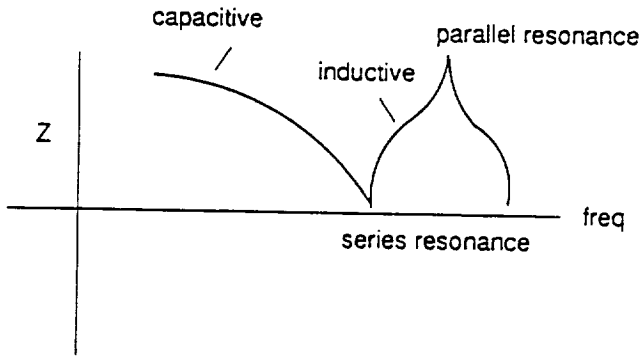
If longer cables are used, the first resonance frequency will be lowered. In that case, it is possible to cascade two or more such models to obtain representation beyond the first resonance frequency.

It is noted that the use of a cable model requires the use of a much smaller time step (TINC) if "math overflow" is to be avoided. This causes a very long simulation time. The cable models should be used only where it is specifically required to observe the effect of the cable.

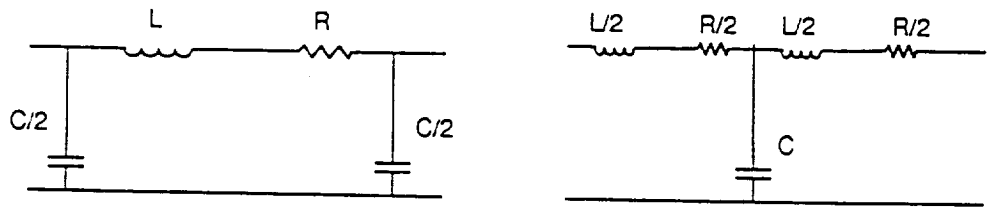
7.10 SMALL-SIGNAL MODELS

Components without switching are inherently linear, and the same model can be used for small-signal analysis and large-signal time domain simulation. Circuits such as input and output filters, connecting cable, etc. fall in this category (Fig. 7.6a).

Components such as converters and PWM comparators follow a different set of differential equations for each position of the switch. These require a separate state-space averaged model for small- signal representation. Converters with current sense feedback require additional control blocks to represent the sampling action of the current sense control (Fig. 7.6c). This form of modeling is discussed in [4].



(a) Impedance of open circuited cable

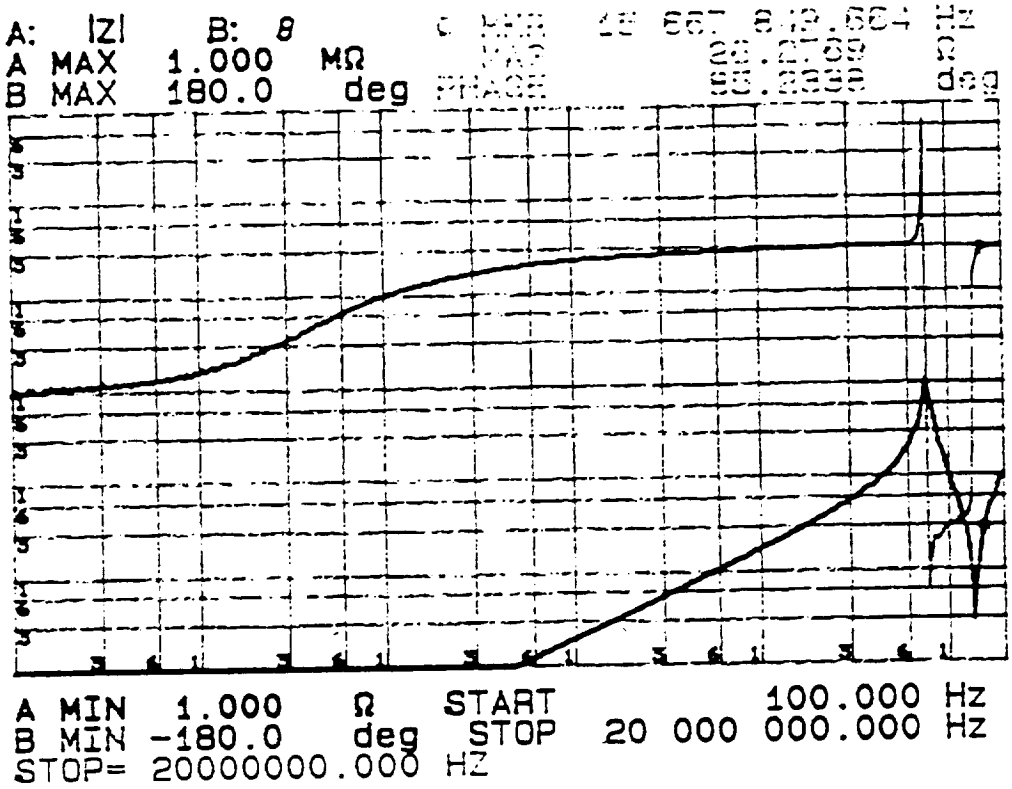


(b) Simplified lumped circuit representations

FIG. 7.3 MODELING OF CONNECTING CABLE

FIG. 7.4 CABLE IMPEDANCES WITH FAR END SHORTED

Measured short circuit impedance of cable



Short circuit impedance of cable model

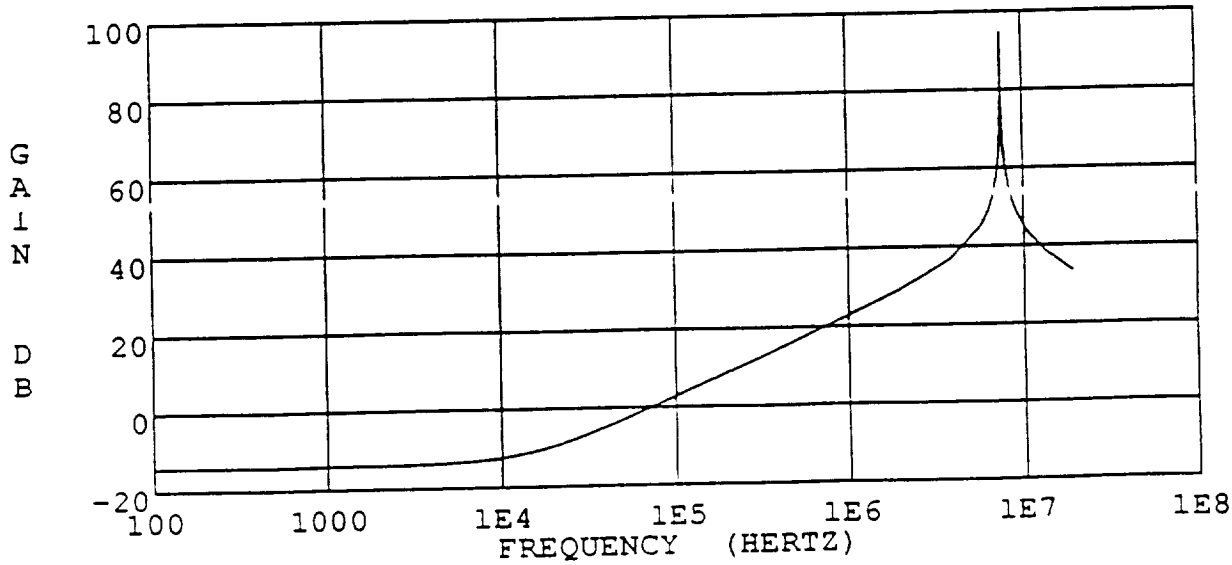
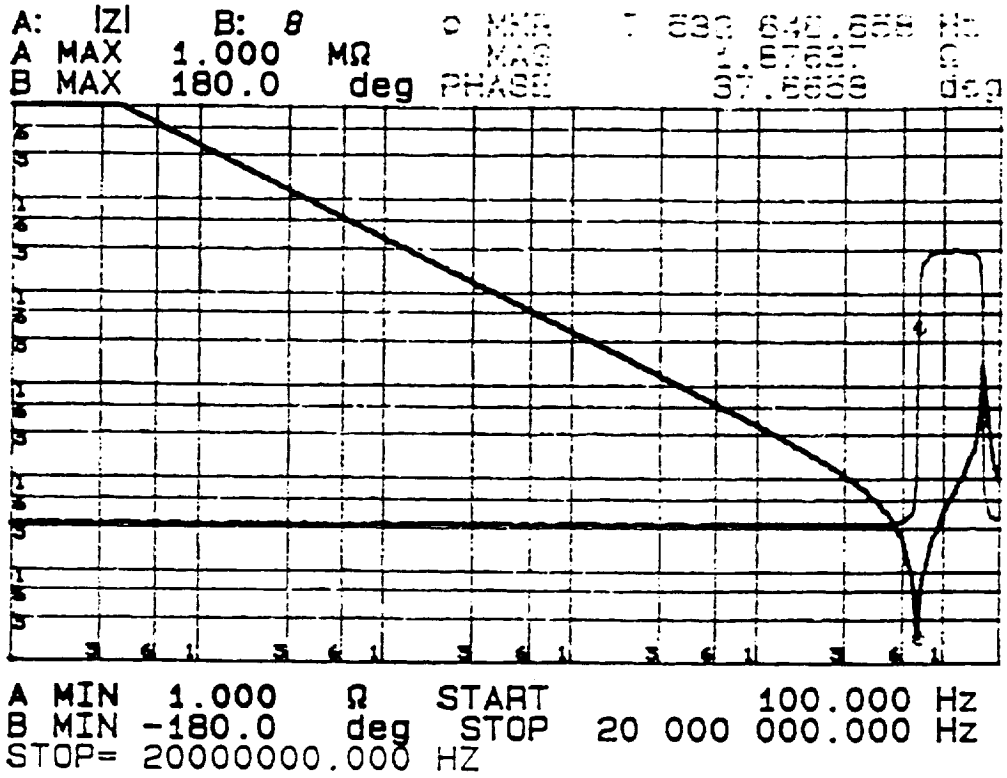
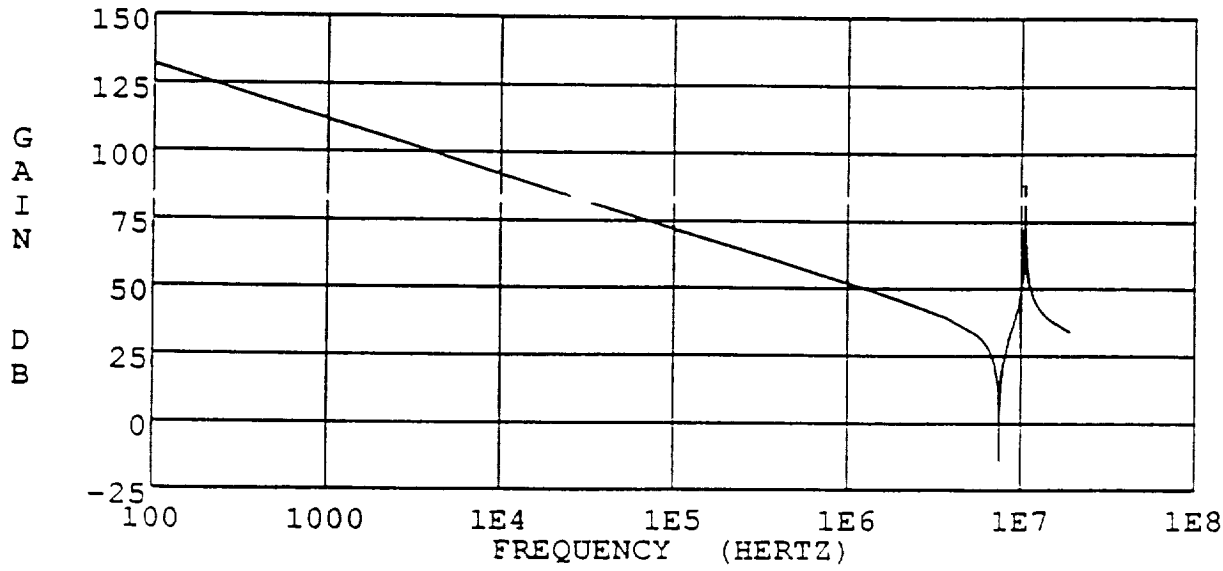


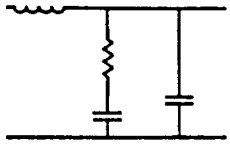
FIG. 7.5 CABLE IMPEDANCES WITH FAR END OPEN

Measured open circuit impedance of cable

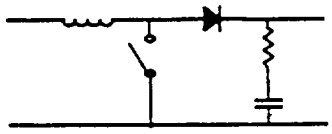


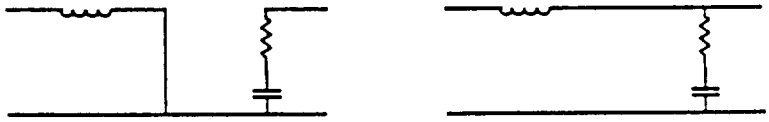
Open circuit impedance of cable model



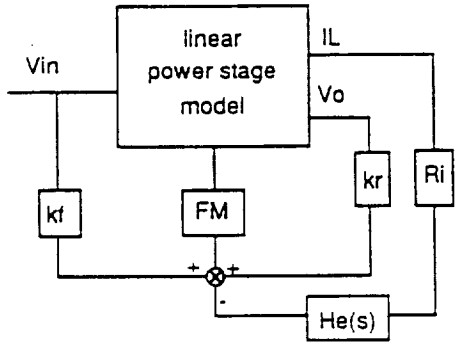


(a) Linear circuit





(b) Switching circuit



(c) Power stage with current sense

FIG. 7.6 SMALL-SIGNAL MODELING

The error amplifier models contain a switch state for clamping the output voltage. This makes them non-linear. The small-signal models for the error amplifiers are essentially the large-signal models with the clamp removed.

7.11 ADDITIONAL SIMULATIONS

Figure 7.7 shows a step load simulation for the shunt switching unit. The load current is cycled from 1.5 A to 15 A. The settling time is about 2 milliseconds, and the peak overshoot/ undershoot is 0.8 V. The peak-to-peak bus voltage ripple is 100 mV for a bus capacitor ESR of 0.04 ohm.

The simulations in Figs. 7.8 and 7.9 demonstrate the operation of the mode controller with changing illumination level.

Figure 7.8 shows the sunlight to eclipse transition. As the illumination level is decreased, the number of open shunt switches increases until the entire array is connected to the bus capacitor. With further decrease in illumination, the array current cannot supply the load, and the bus voltage falls from the shunt regulation level of 122 V. When it reaches the discharger level of 120 V, the discharger turns on and regulates the bus. The bus voltage dip is seen to be 0.4 V. In actuality case, the illumination change will take place more slowly, and the bus voltage dip will be smaller. During this transition, the batteries are charged, and the charger is in trickle charge (current regulation) mode. It does not attempt to regulate the bus.

Figure 7.9 shows the reverse transition from eclipse to sunlight. Initially the bus is regulated by the discharger at 120 V. With increasing illumination level, the discharge current falls to zero, and the bus voltage rises. When it reaches the 121 V regulation level, the charger draws current to regulate the bus. This continues until the charge current

exceeds the current regulation limit. The OR circuit in the charger control then switches the charger to current regulation mode. The bus voltage rises further until it reaches the 122 V level. At this point it is regulated by the shunt.

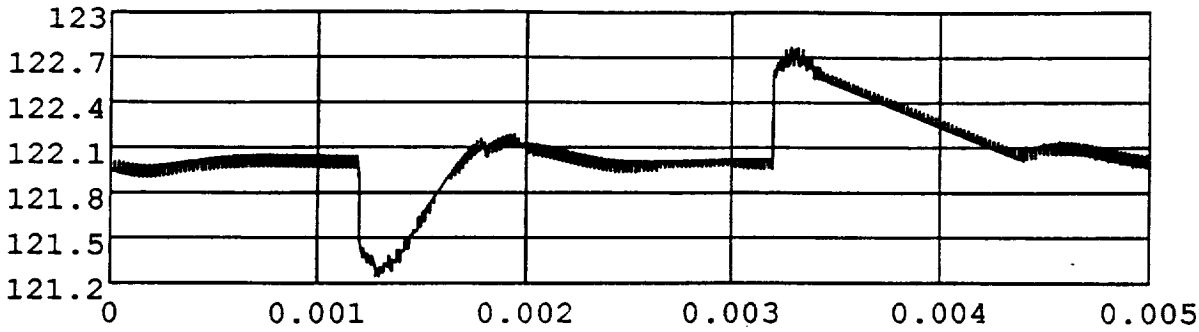
Simulations for mode changes due to ***step load currents*** have been presented in the earlier sections of this report.

Figure 7.10 shows the charger dynamic characteristics using the small- signal model. Figure 7.10a shows the open loop transfer function from the control to the buck inductor current and to the output filter inductor current. Figure 7.10b shows the current loop gain and the closed loop current transfer function (from current reference to inductor current).

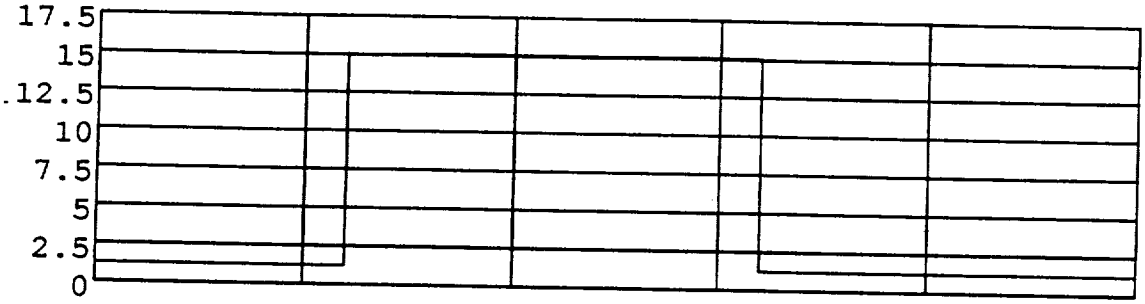
When the charger is regulating the bus, the characteristics are shown in Fig. 7.11. Figure 7.11a indicates the open loop transfer function from the charger control voltage to the bus voltage and the voltage loop gain. The bus impedance with both voltage and current loops closed is shown in Fig. 7.11b.

Figure 7.12 shows similar small-signal characteristics for the VFPPAT discharger.

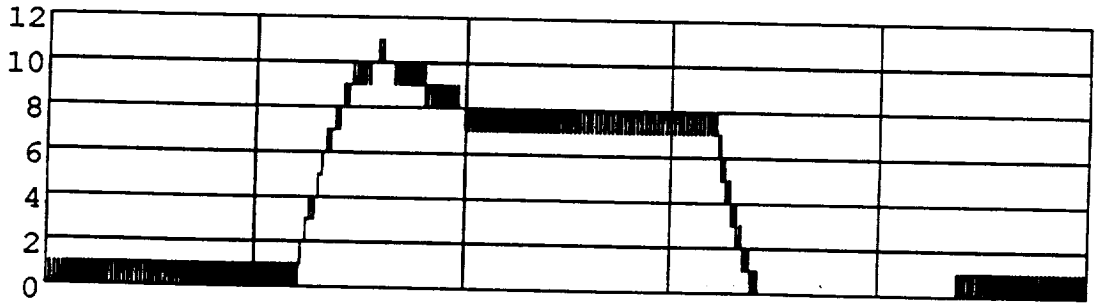
FIG 7.7 BUS REGULATION BY SHUNT SWITCHING UNIT



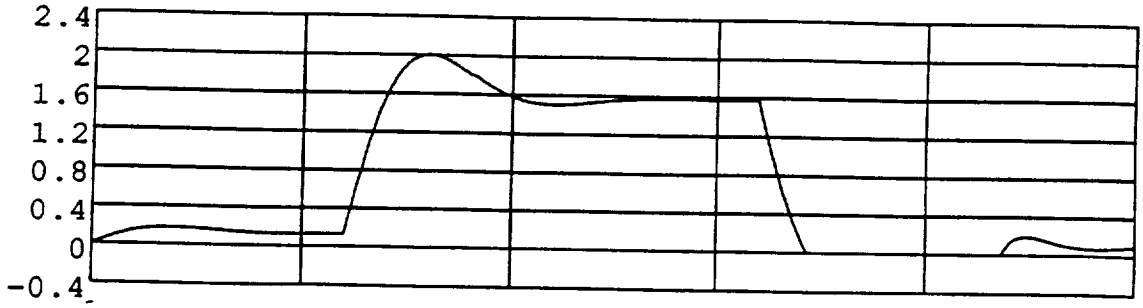
Bus voltage



Load current

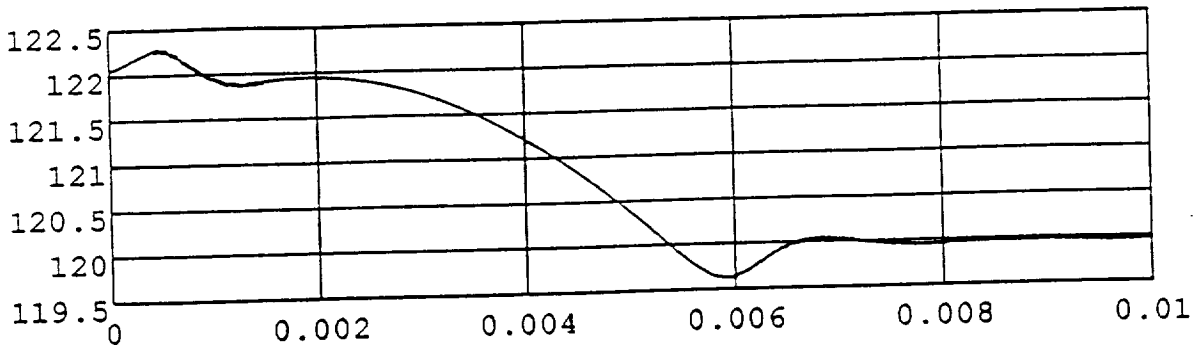


Number of open switches

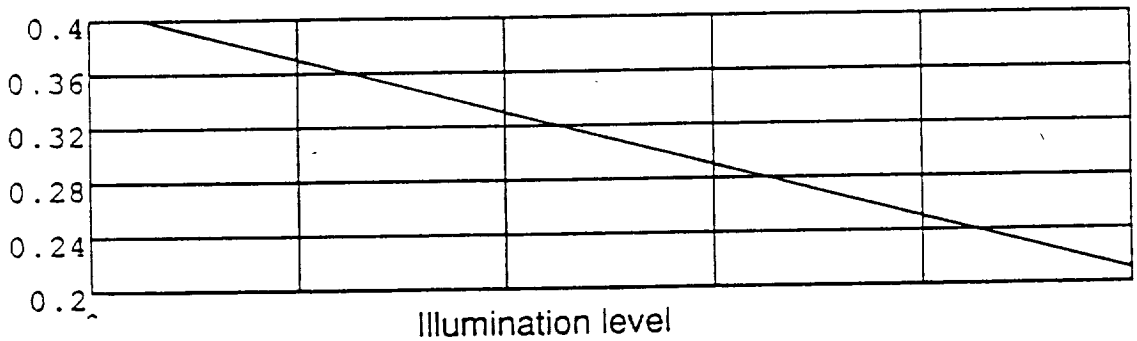


Shunt control voltage

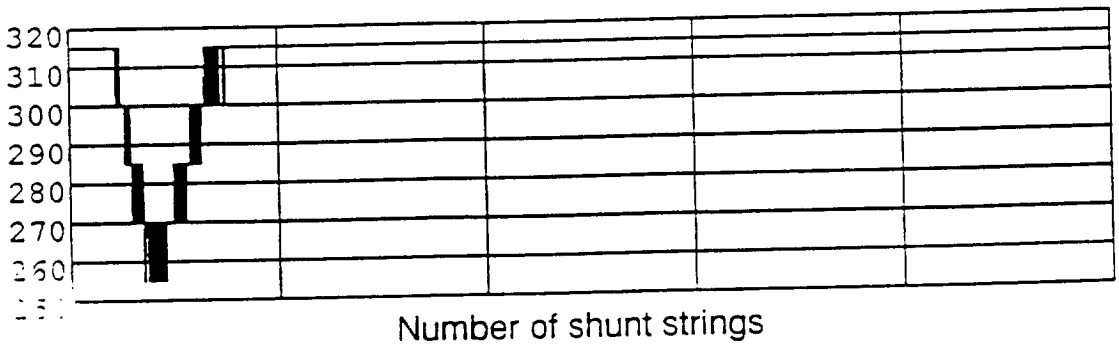
FIG. 7.8 SIMULATION FOR SUNLIGHT TO ECLIPSE TRANSITION



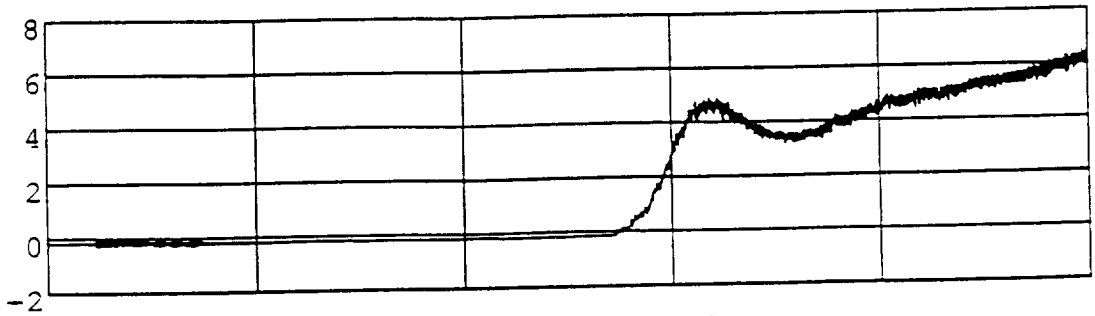
Bus voltage



Illumination level

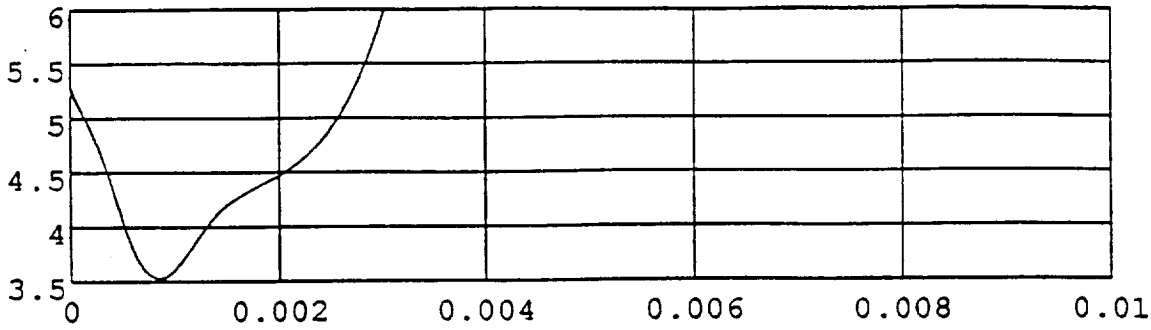


Number of shunt strings

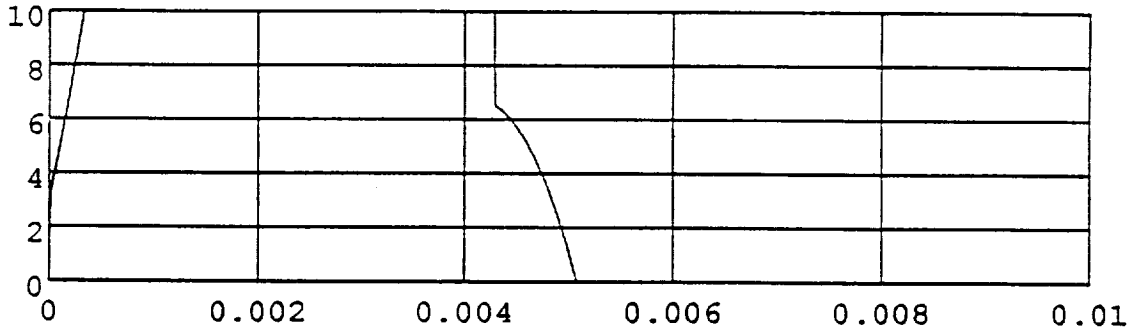


Battery discharge current

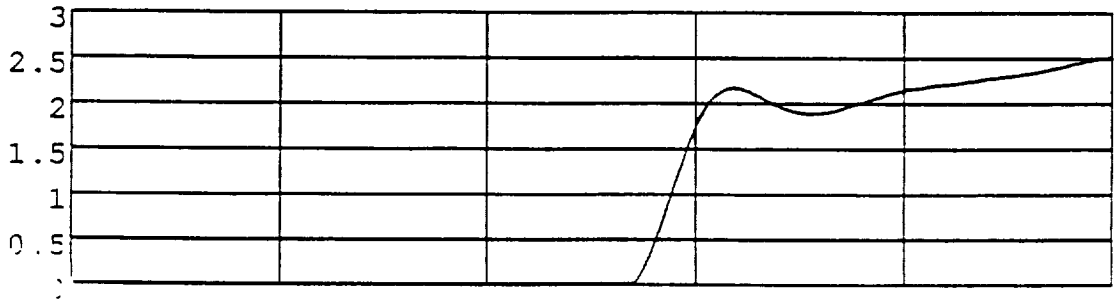
FIG. 7.8 SIMULATION FOR SUNLIGHT TO ECLIPSE TRANSITION (CONTINUED.)



Shunt control voltage

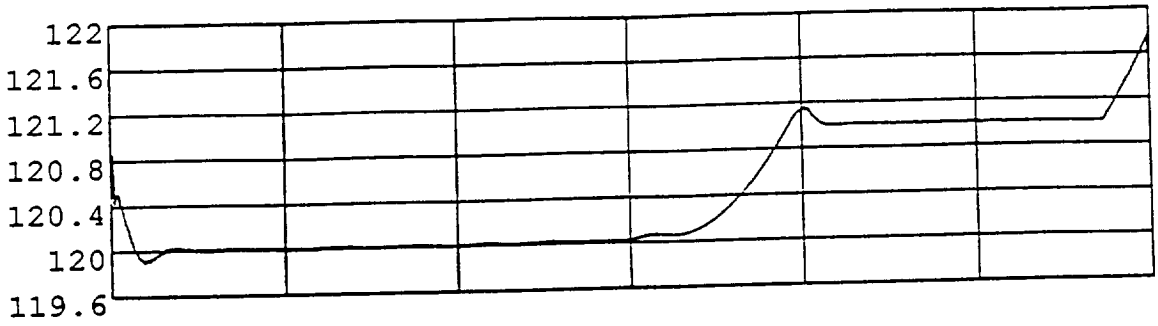


Charger control voltage

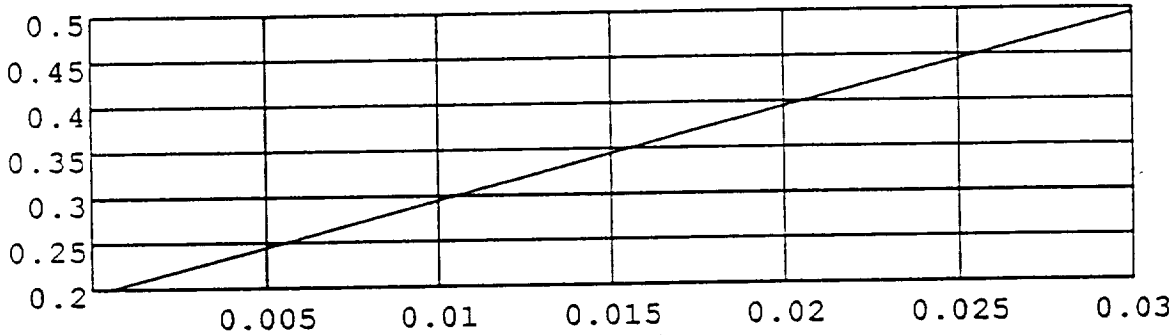


Discharger control voltage

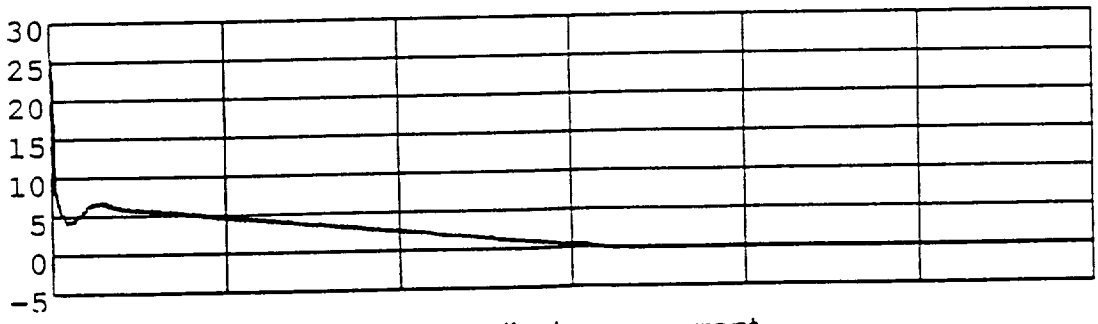
FIG. 7.9 SIMULATION FOR ECLIPSE TO SUNLIGHT TRANSITION



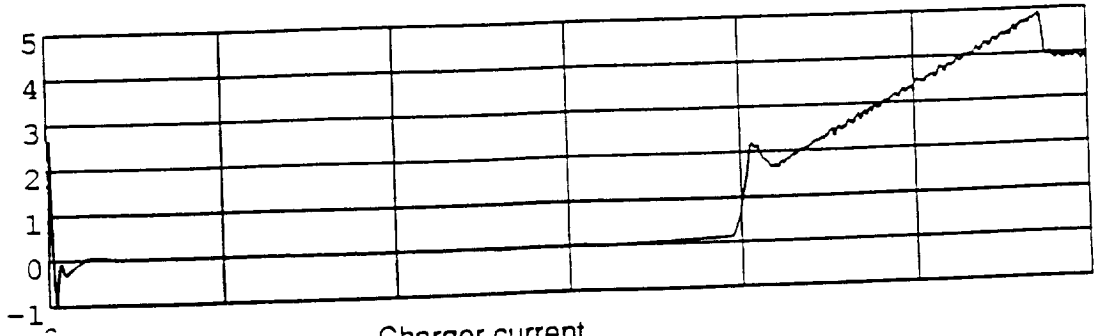
Bus voltage



Illumination level

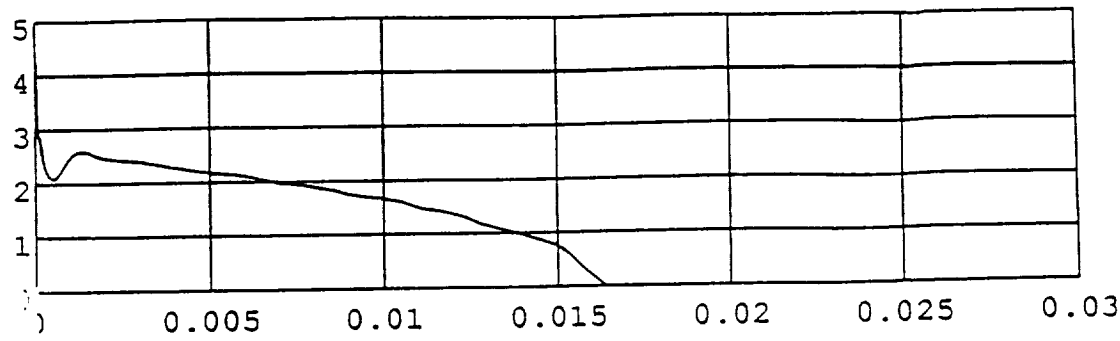


Battery discharge current

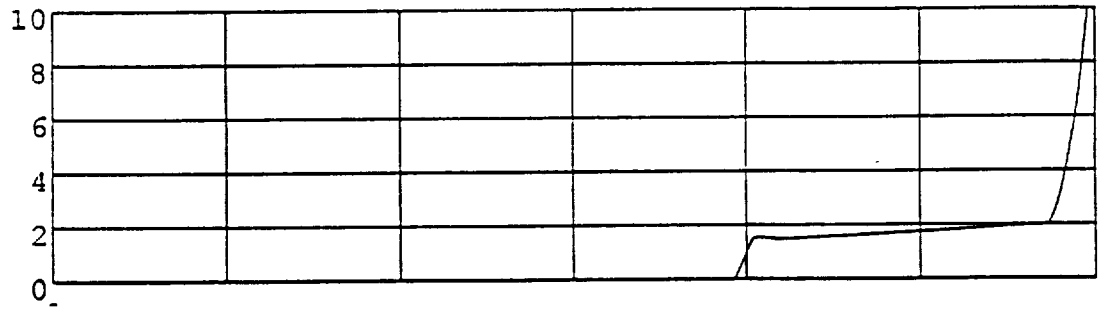


Charger current

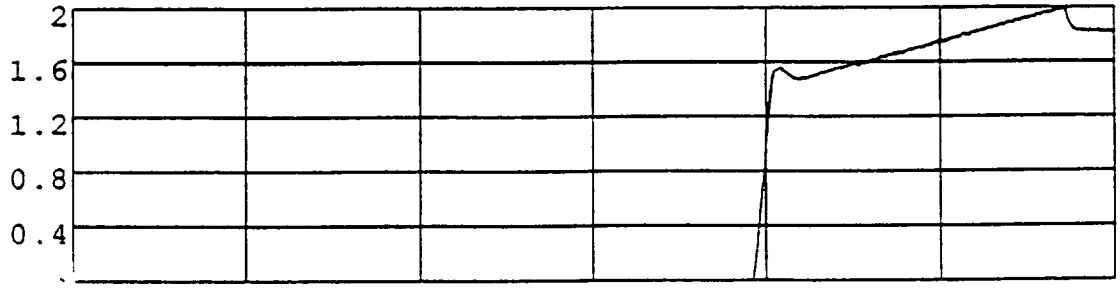
FIG. 7.9 SIMULATION FOR ECLIPSE TO SUNLIGHT TRANSITION (CONTINUED.)



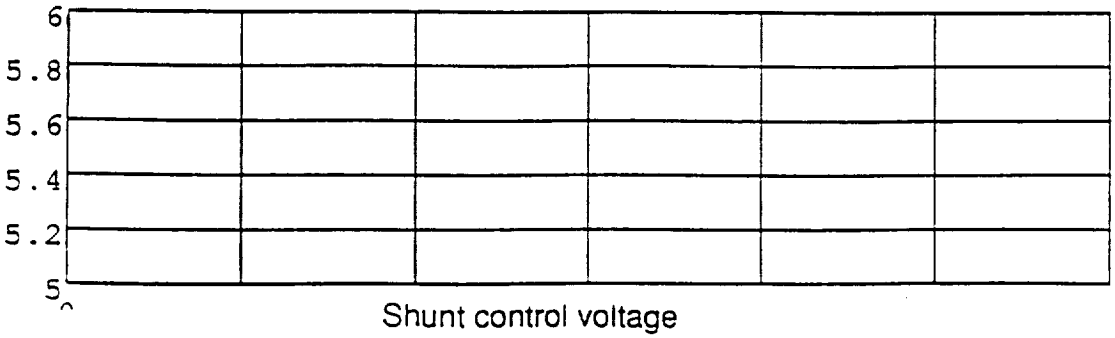
Discharger control voltage



Charger voltage error signal

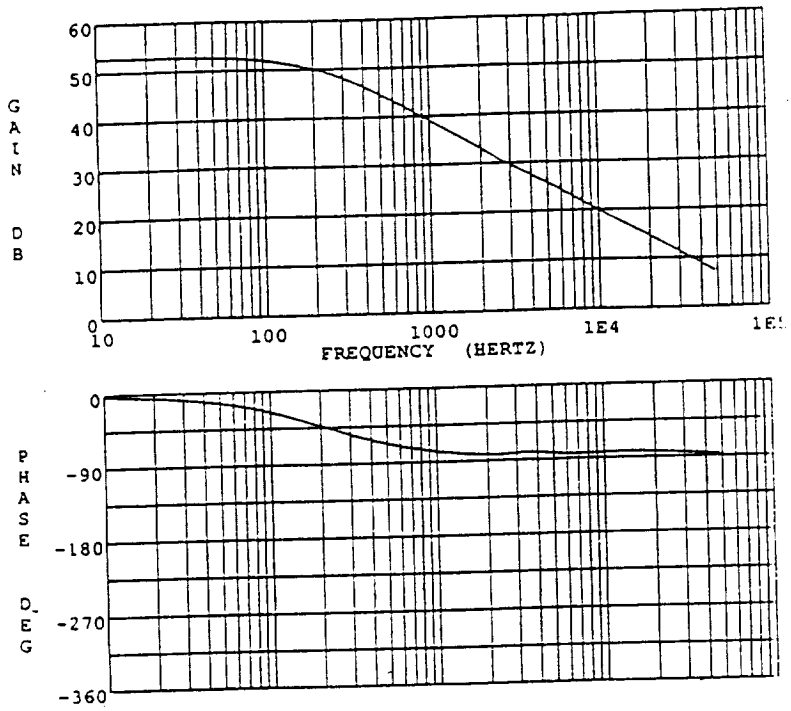


Charger control voltage after ORing

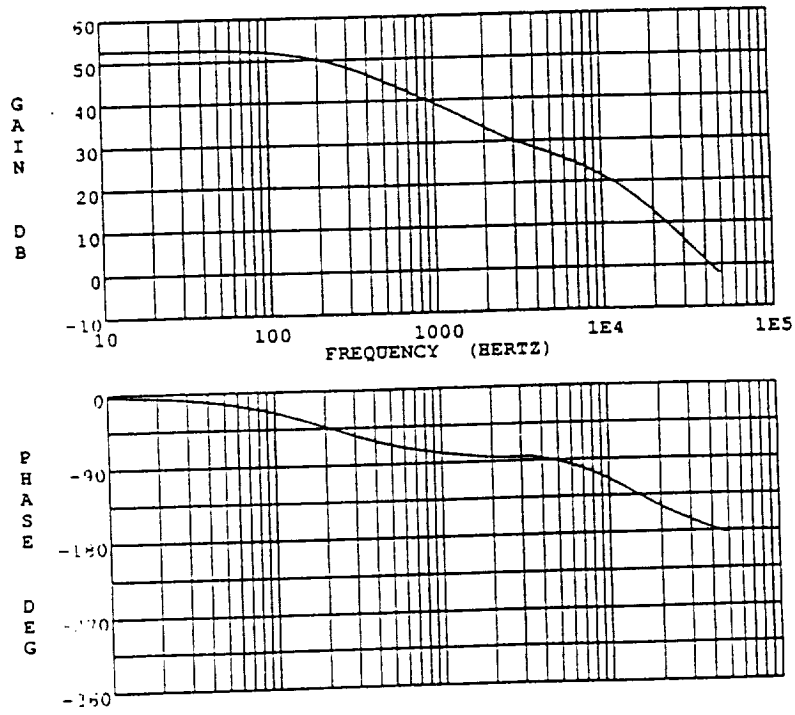


Shunt control voltage

FIG 7.10A CHARGER CURRENT LOOP : OPEN LOOP TRANSFER FUNCTIONS

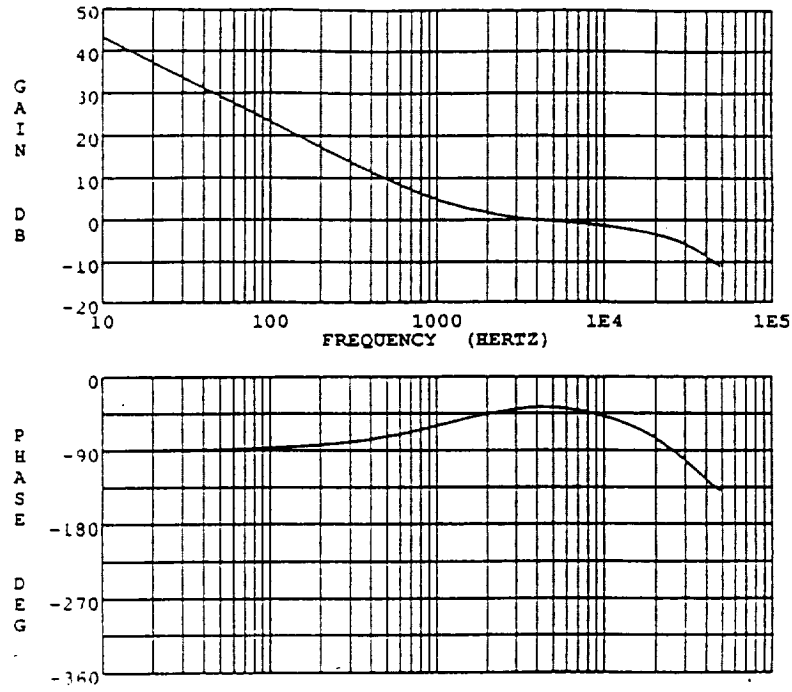


Open loop control to L1 inductor current transfer function

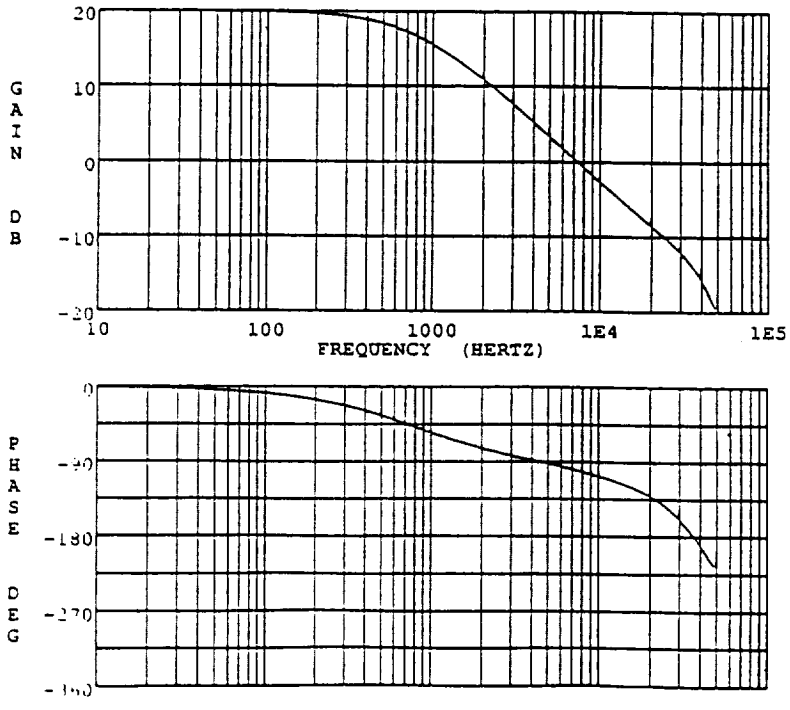


Open loop control to L2 inductor current transfer function

FIG. 7.10B CHARGER CURRENT LOOP : LOOP GAIN AND CLOSED LOOP TRANSFER FUNCTION

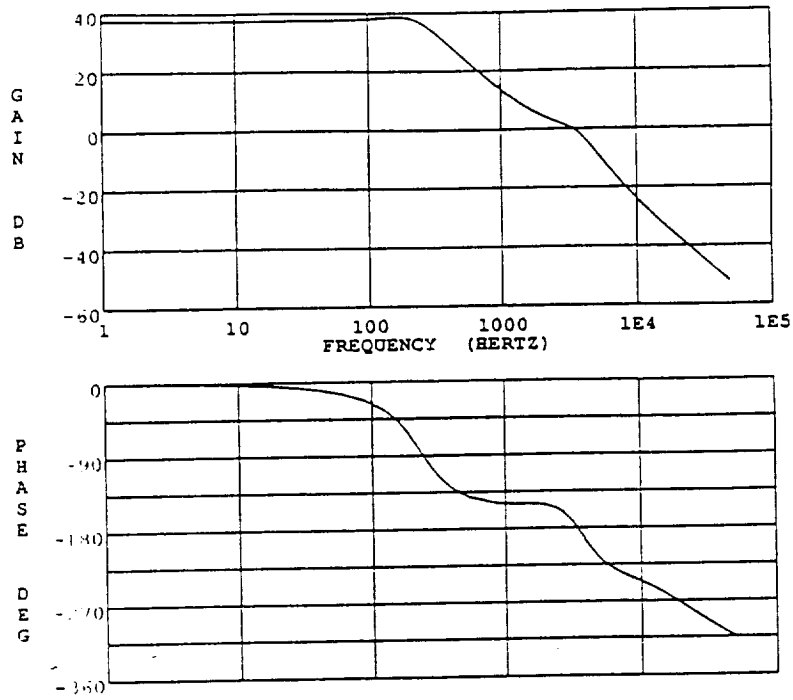


Current loop gain

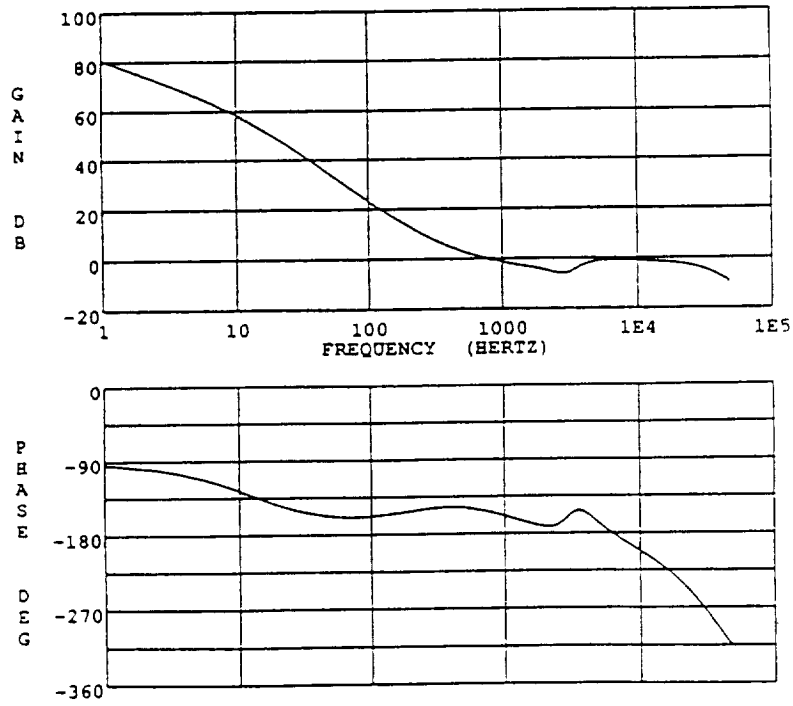


Closed loop IL1/ Iref transfer function

FIG. 7.11A : CHARGER VOLTAGE LOOP

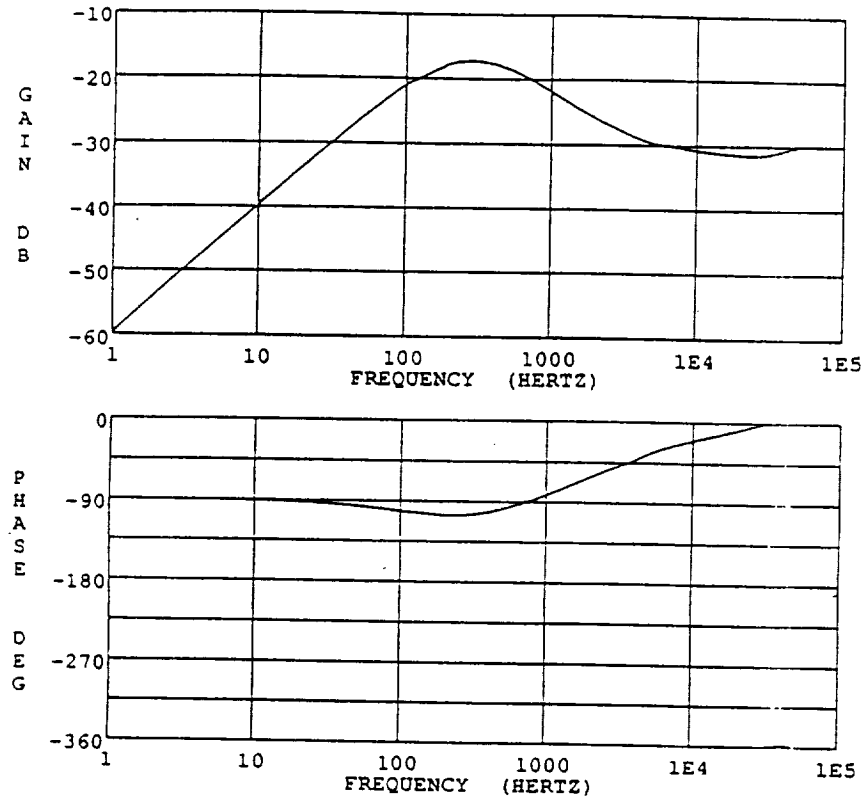


Open loop control to bus voltage transfer function



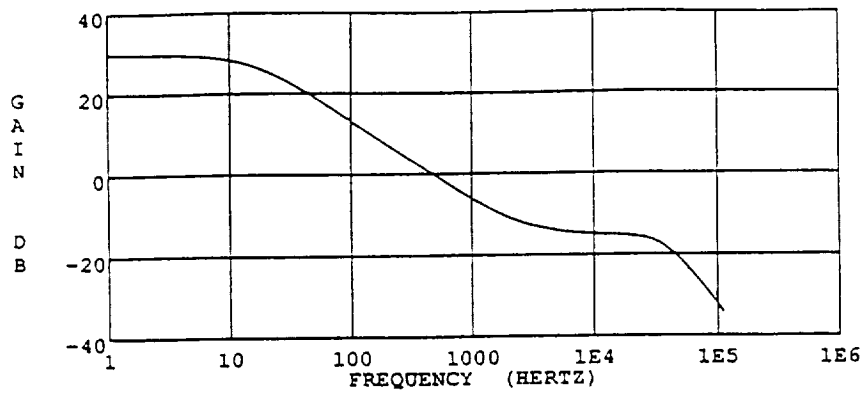
Voltage loop gain

FIG. 7.11B BUS IMPEDANCE WITH CHARGER REGULATION

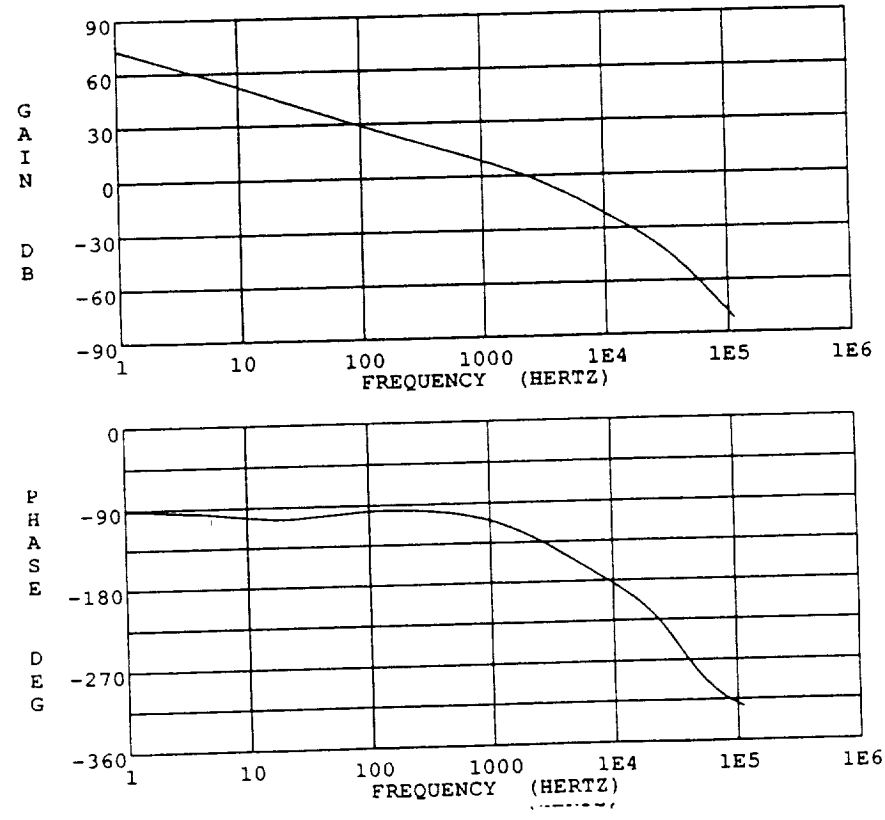


Closed loop bus impedance for charger regulation

FIG. 12 VFPPAT OPEN LOOP TRANSFER FUNCTION AND LOOP GAIN

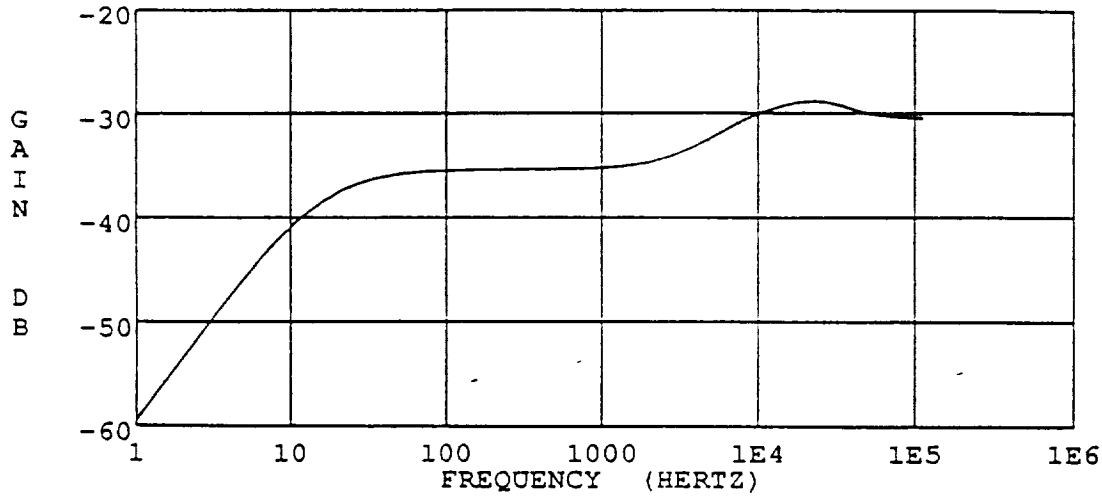


Control to output voltage with current loop closed



Loop gain with both loops closed

FIG. 12 (CONTINUED) VFPPAT BUS IMPEDANCE



Output impedance with both loops closed

References for Chapter 7

1. B. H. Cho and F. C. Lee, "Modeling and Analysis of Spacecraft Power Systems," *IEEE Transactions on Power Electronics, Vol. 3, No. 1, Jan 1988, pp 44-54.*

2. J.R. Lee, B. H. Cho and F.C.Lee, "Modeling and Simulation of Spacecraft Power Systems", *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 24, No. 3, May 1988, pp 295-304.

3. J. R. Lee, S.J. Kim, B. H. Cho and F. C. Lee, "Computer Aided Modeling and Analysis of Power Processing Systems (CAMAPPS) - Phase II," Final Report prepared for NASA/Goddard Space Flight Center, V.P.I and S.U., July, 1989.

4. R.B. Ridley, B.H. Cho and F.C. Lee, "Analysis and Interpretation of Loop Gains of Multi-loop Controlled Switching Regulators," *The Power Electronics Show and Conference*, San Jose, CA, 1986.

8.0 CONCLUSIONS

A detailed design, analysis, and testing of a power system for the space platform has been presented. Two topologies for the battery discharger design, a four module boost converter and a voltage-fed, push-pull autotransformer, have been outlined. Fig. 8-1 shows a comparison of efficiency. At the maximum load condition of 1800 W, the multi-module, multi-phase boost converter is over 97% efficient vs. less than 95% efficient for the autotransformer converter. Also, the efficiency of the the VFPPAT degrades more rapidly with temperature since a high percentage of the loss is due to FET conduction loss. The FET on resistance has a positive temperature coefficient.

The filter weights of the two converters are approximately the same. While the single energy storage inductor of the autotransformer converter is much smaller than the four energy storage inductors of the boost converter, the boost converter does not require an input filter or transformer.

Boost converters are ordinarily much more difficult to control than buck-derived converters due to the presence of a right-half-plane zero and moving poles in the control-to-output transfer function. However, with proper implementation of current-mode control, good dynamic performance was obtained with the four module boost converter with good stability margin. Current-mode control was also necessary in the VFPPAT converter in order to ensure flux balancing on the autotransformer.

A battery charger designed to the Space Platform specifications has also been presented. A high conversion frequency of 90 kHz was selected to minimize the input and output filter weight while maintaining high efficiency. The input filter was designed to attenuate the charger's input current ripple to mainitain the bus voltage ripple within specification during the voltage regulation mode. Four power MOSFETs were paralleled to form the active switch to minimize the conduction losses. The main output filter inductor was designed with a METGLAS cut C-core

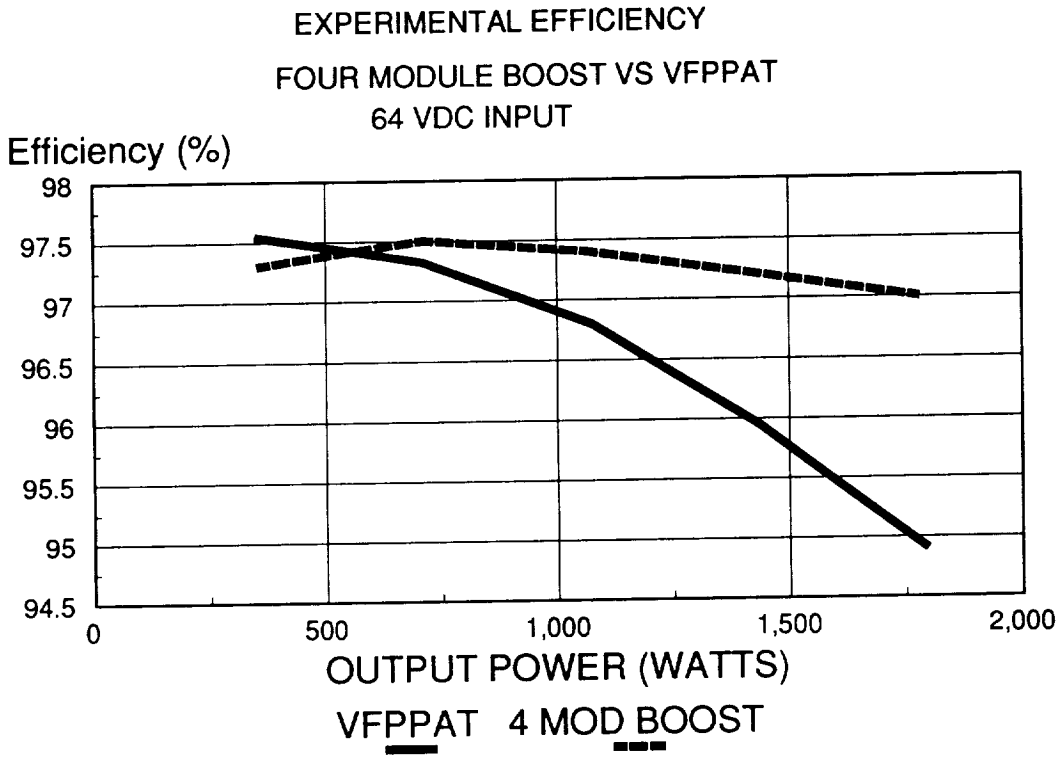


FIG. 8-1 COMPARISON OF FOUR MODULE BOOST AND VFPPAT EFFICIENCY

in order to minimize weight. A secondary output filter was designed to reduce the battery current ripple within specification. The charger design was found to be very layout sensitive. To minimize noise sensitivity, the power stage components were closesly spaced.

The design of the charger control loops was facilitated by use of the PWM switch model and a new, continuous-time model of current-mode control. The charge current regulation loop was designed with average current-mode control so that the battery charging would be accurately controlled under all conditions. Current-mode control ensured stability over a wide range of charge currents. A V/T control loop was designed to limit the maximum charge current as a function of voltage and temperature. The bus voltage regulation loop was designed using current-mode control. The objective was to minimize bus impedance and transient response time while maintaining stability under all operating conditions.

The power system hardware has been modeled using the EASY5 dynamic analysis program. The system has been subdivided into a number of basic modular elements, such as converters, filters, error amplifiers, etc. These are connected together into various subsystem models.

The models have been used to obtain the steady-state waveforms for the charger, discharger, and VFPPAT discharger. Simulations are also used to demonstrate the bus regulation by these units for a step load change.

System level models have been used to show mode transitions, induced by illumination as well as step load changes. These test the operation of the mode controller and show the operation of the charger in the voltage and current regulation modes.

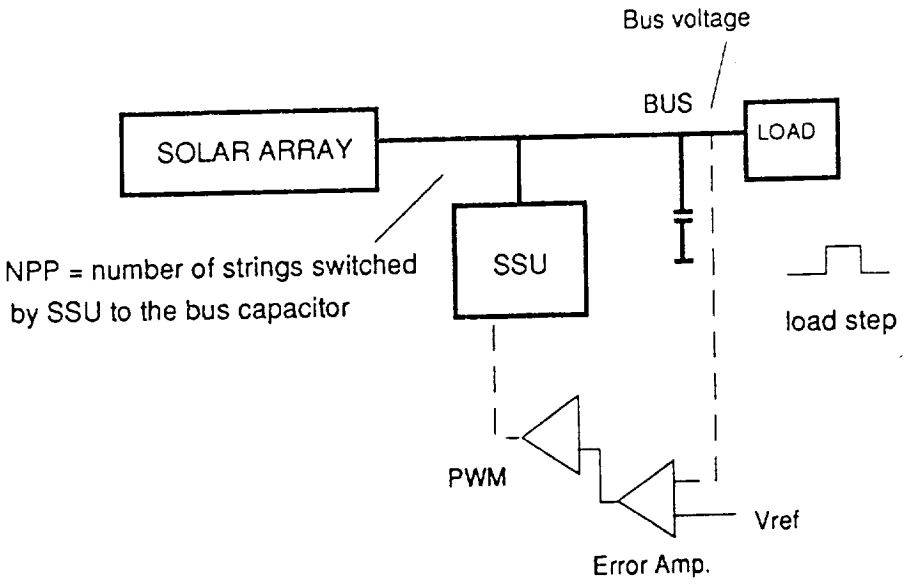
APPENDIX

SUBSYSTEM AND SYSTEM MODELS

SHUNT.MOD	Solar array and shunt switching unit
AUTO.MOD	VFPPAT topology discharger
BOOST.MOD	Four module boost discharger
BOOST2.MOD	Four module boost with connecting cable
CHARGER1.MOD	Charger with closed current loop
CHARGER2.MOD	Charger with SSU to test voltage loop
SYSTEM.MOD	General system model with SSU, mode controller four module boost discharger and buck charger
CHS.MOD	Charger small signal current loop model
CHV.MOD	Charger small signal voltage loop model
ACS2.MOD	VFPPAT small signal (open loop)
ACS3.mod	VFPPAT small signal (closed loop)

SHUNT.MOD

STEP LOAD TEST FOR SSU

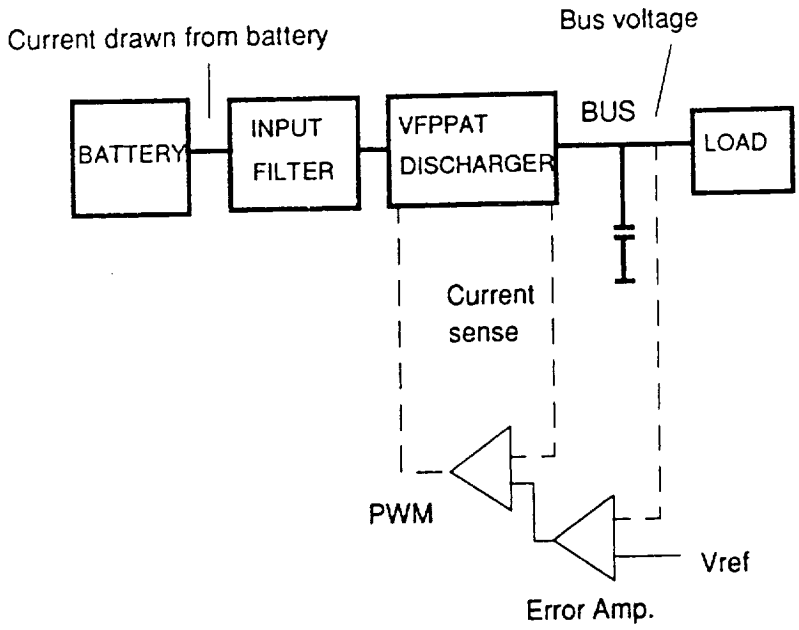


- A load step from 1.2 to 15 A is applied to test bus regulation by the shunt

```
*-------------------------------------------------------
* SHUNT.MOD
* STEP LOAD TEST FOR SSU
*-------------------------------------------------------
MACRO FILE NAME=MACROS
MODEL DESCRIPTION
*-------------------------------------------------------
*SA OUTPUTS :    VB   VC   NPP  VR   NF   D    NPX
*RQ OUTPUTS :    I1
*RX OUTPUTS :    AO
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------
LOCATION= 1 , SA  , INPUTS = RQ(I1=IO),RX(AO=LLM),EI(VO=V
LOCATION= 3 , RQ  , INPUTS = SA(VB=V1)
LOCATION= 5 , RX
LOCATION= 7 , EI  , INPUTS = SA(VB=VI)
*-------------------------------------------------------
END OF MODEL
PRINT
```

AUTO.MOD

TEST FOR BUS REGULATION BY VFPPAT DISCHARGER

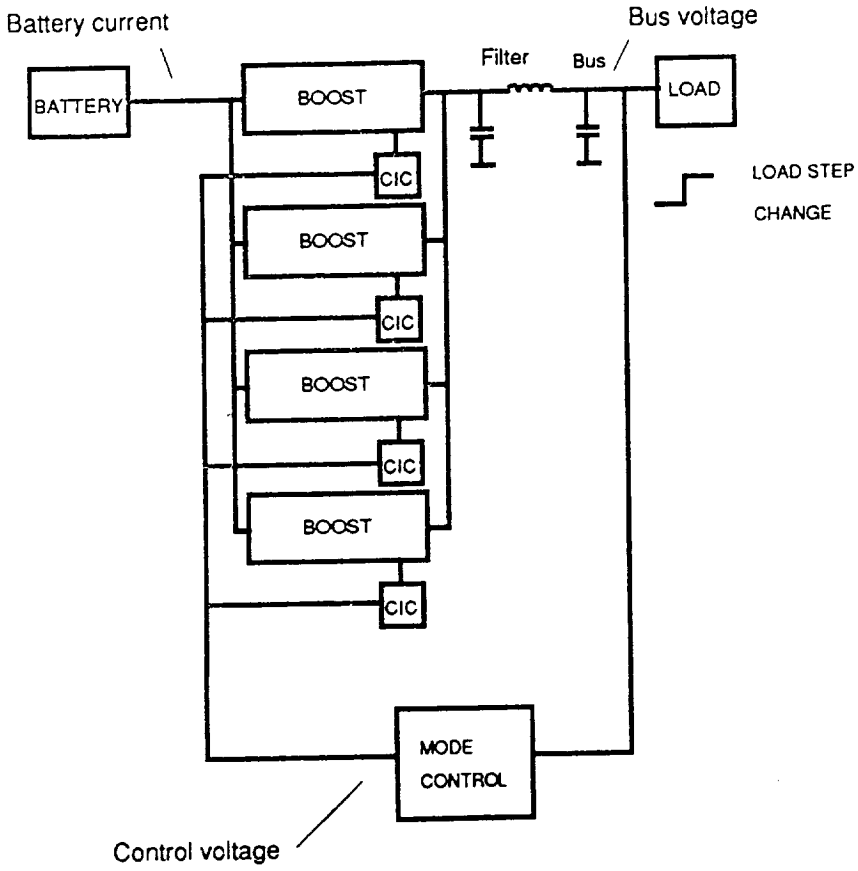


- A load step from 1.2 to 15 A is applied to test bus regulation by the discharger

```
*-------------------------------------------------------
* AUTO.MOD
* VFPPAT LOAD STEP TEST
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
*FD OUTPUTS :    I1   VO   VC1  VC2  I2   IR1  IR2
*AT OUTPUTS :    VB   IL   I1   IS1  IS2  ID1  ID2  IT1
*RQ OUTPUTS :    I1
*DD OUTPUTS :    SW   VR   VCT
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------
LOCATION= 1 , FD  , INPUTS =AT(I1=IO)
LOCATION= 3 , AT  , INPUTS =DD(SW=IQ),FD(VO=V1),RQ(I1=IO)
LOCATION= 5 , RQ  , INPUTS =AT(VB=V1)
LOCATION= 7 , DD  , INPUTS =EI(VO=VC),AT(IS=IL)
LOCATION= 9 , EI  , INPUTS =AT(VB=VI)
*-------------------------------------------------------
END OF MODEL
PRINT
```

BOOST.MOD

STEP LOAD TEST FOR FOUR MODULE BOOST

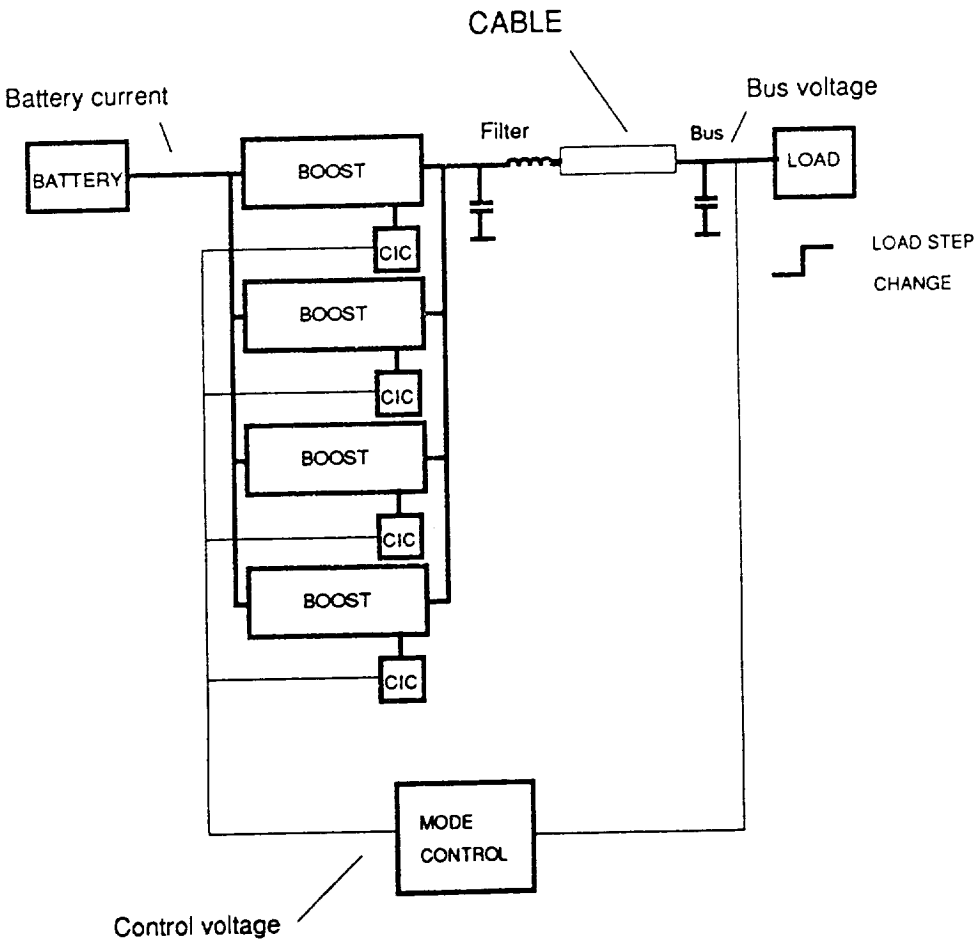


- Bus voltage regulation for 1.2A to 15A load step

```
*-------------------------------------------------------
* BOOST.MOD
* FOUR MODULE BOOST DISCHARGER STEP LOAD TEST
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
*BT OUTPUTS :    IO   IL   IS   SWL
*DD OUTPUTS :    SW   VR   VCT
*BU OUTPUTS :    VO   V1   VC   VC1    IR   IT   ILP  ILS
*RS OUTPUTS :    I1
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------
LOCATION= 1 , BT1 , INPUTS =BU(V1=VO),DD1(SW=IQ)
LOCATION= 3 , BT2 , INPUTS =BU(V1=VO),DD2(SW=IQ)
LOCATION= 5 , BT3 , INPUTS =BU(V1=VO),DD3(SW=IQ)
LOCATION= 7 , BT4 , INPUTS =BU(V1=VO),DD4(SW=IQ)
LOCATION= 9 , DD1 , INPUTS =EI(VO=VC),BT1(IS=IL)
LOCATION=11 , DD2 , INPUTS =EI(VO=VC),BT2(IS=IL)
LOCATION=13 , DD3 , INPUTS =EI(VO=VC),BT3(IS=IL)
LOCATION=15 , DD4 , INPUTS =EI(VO=VC),BT4(IS=IL)
LOCATION=17 , BU,INPUTS =BT1(IO=I1),BT2(IO=I2),BT3(IO=I3)
                  RS(I1=IX)
LOCATION=19 , RS  , INPUTS =BU(VO=V1)
LOCATION=21 , EI  , INPUTS =BU(VO=VI)
LOCATION=22 , AD ,INPUTS=BT1(IL=I1),BT2(IL=I2),BT3(IL=I3)
*-------------------------------------------------------
END OF MODEL
PRINT
```

BOOST2.MOD

BOOST STEP LOAD TEST WITH CONNECTING CABLE

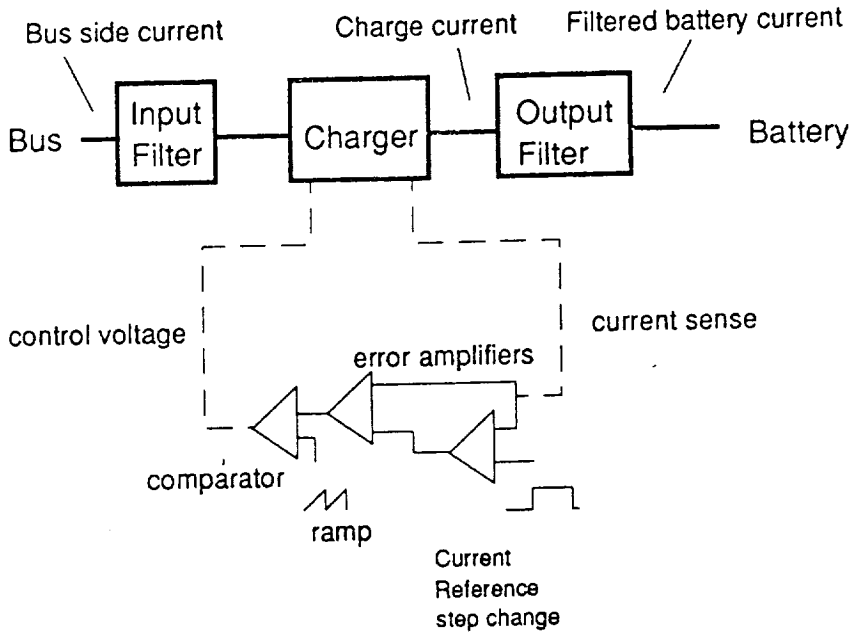


- Bus voltage regulation for 1.2A to 15A
  with a cable connecting the boost to the output capacitor

```
*-------------------------------------------------------
* BOOST2.MOD
* FOUR MODULE BOOST WITH CABLE STEP LOAD TEST
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
*AD OUTPUTS :     IO
*BT OUTPUTS :     IO    IL    IS    SWL
*DD OUTPUTS :     SW    VR    VCT
*BX OUTPUTS :     V1    IX    IXN   VC1   IR    IT    ILP   ILS
*TP OUTPUTS :     V1    VO
*CI OUTPUTS :     I1    VC
*RQ OUTPUTS :     I1
*EI OUTPUTS :     VO    SW    X
*-------------------------------------------------------
LOCATION= 3 , BT1 , INPUTS =BX(V1=VO),DD1(SW=IQ)
LOCATION= 5 , BT2 , INPUTS =BX(V1=VO),DD2(SW=IQ)
LOCATION= 7 , BT3 , INPUTS =BX(V1=VO),DD3(SW=IQ)
LOCATION= 9 , BT4 , INPUTS =BX(V1=VO),DD4(SW=IQ)
LOCATION=11 , DD1 , INPUTS =EI(VO=VC),BT1(IS=IL)
LOCATION=13 , DD2 , INPUTS =EI(VO=VC),BT2(IS=IL)
LOCATION=15 , DD3 , INPUTS =EI(VO=VC),BT3(IS=IL)
LOCATION=17 , DD4 , INPUTS =EI(VO=VC),BT4(IS=IL)
LOCATION=19 , BX  , INPUTS =BT1(IO=I1),BT2(IO=I2),BT3(IO=
                            BT4(IO=I4),TP(V1=VO)
LOCATION=21 , TP  , INPUTS =BX(IXN=I1),CI(I1=IO)
LOCATION=23 , CI  , INPUTS =TP(VO=V1),RQ(I1=IX)
LOCATION=25 , RQ  , INPUTS =TP(VO=V1)
LOCATION=27 , EI  , INPUTS =TP(VO=VI)
LOCATION=28 , AD,INPUTS=BT1(IL=I1),BT2(IL=I2),BT3(IL=I3),
*-------------------------------------------------------
END OF MODEL
PRINT
```

CHARGER1.MOD

CHARGER SIMULATION FOR CURRENT MODE



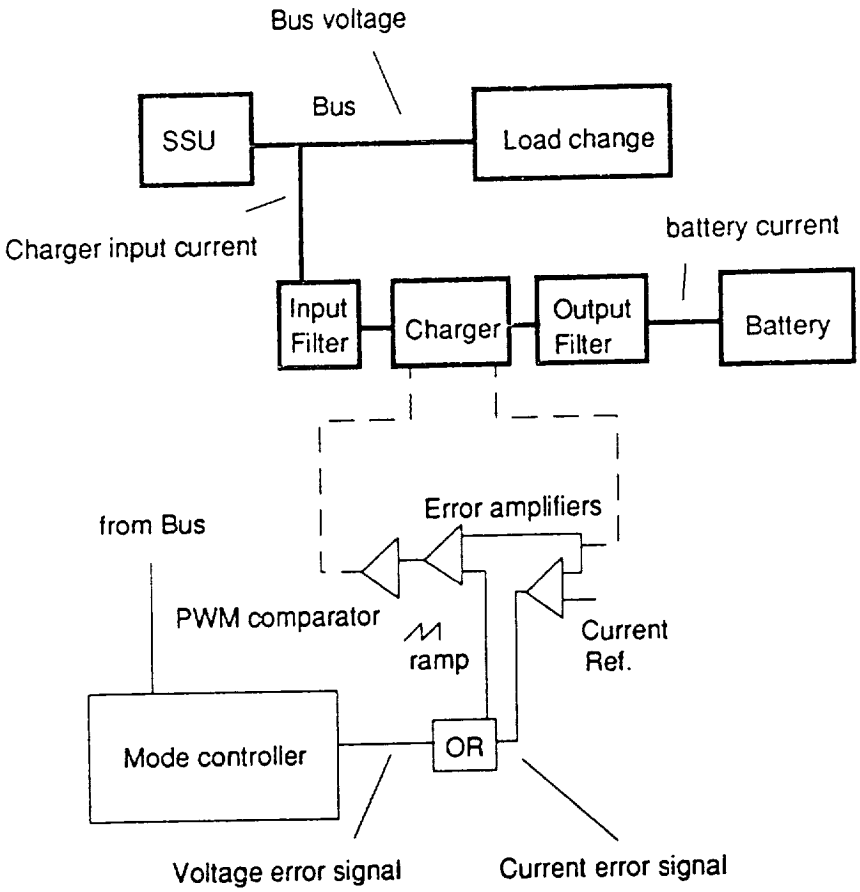
The charger current loop is tested by a step change of current reference from 4 to 8 A

```
*-------------------------------------------------------
* CHARGER1.MOD
* CHARGER WITH CURRENT REF STEP CHANGE
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CH OUTPUTS :    IB   I1   ID   SWL
*FX OUTPUTS :    V1   IB   VC
*PM OUTPUTS :    SW   VR
*EN OUTPUTS :    VO   SW
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------
LOCATION= 1 , FI  , INPUTS =CH(I1=IO)
LOCATION= 3 , CH  , INPUTS =FI(VO=V1),FX(V1=VBB),PM(SW=IQ
LOCATION= 5 , FX  , INPUTS =CH(IB=I1)
LOCATION= 7 , PM  , INPUTS =EN(VO=VC)
LOCATION= 9 , EN  , INPUTS =CH(IB=VI),EI(VO=VRF)
LOCATION=11 , EI  , INPUTS =CH(IB=VI),ST(AO=VRF)
LOCATION=13 , ST
*-------------------------------------------------------
END OF MODEL
PRINT
```

CHARGER2.MOD

CHARGER AND SHUNT SYSTEM SIMULATION

TO TEST CHARGER IN VOLTAGE MODE

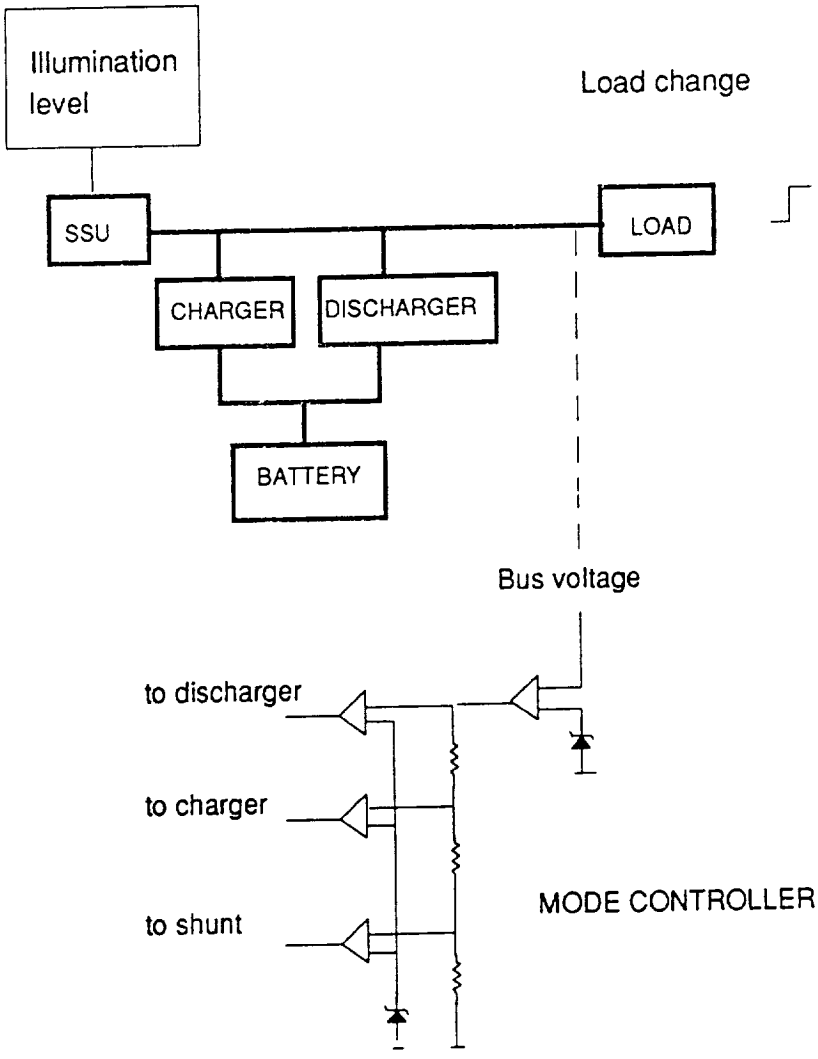


- The illumination level for the array is set at a low value of 0.4.
- A load current step is applied to test the operation of the charger-shunt system

```
*-------------------------------------------------------
* CHARGER2.MOD
* CHARGER VOLTAGE LOOP TEST WITH SSU
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
*SA OUTPUTS :     VB    VC    NPP   VR    NF    D     NPX
*NV OUTPUTS :     AO
*RS OUTPUTS :     I1
*FI OUTPUTS :     VO    I1    IL    VC    VCF   IR    IRF
*CH OUTPUTS :     IB    I1    ID    SWL
*FX OUTPUTS :     V1    IB    VC
*PM OUTPUTS :     SW    VR
*EN OUTPUTS :     VO    SW
*OR OUTPUTS :     VO
*ET OUTPUTS :     VO    SW
*EI OUTPUTS :     VO    SW    X
*EM OUTPUTS :     VO    SW    X
*-------------------------------------------------------
LOCATION= 1 , SA   , INPUTS =NV(AO=IO),EI1(VO=VCA)
LOCATION= 3 , NV   , INPUTS =FI(I1=A1),RS(I1=A2)
LOCATION= 5 , RS   , INPUTS =SA(VB=V1)
LOCATION= 7 , FI   , INPUTS =SA(VB=V1),CH(I1=IO)
LOCATION= 9 , CH   , INPUTS =FI(VO=V1),FX(V1=VBB),PM(SW=IQ
LOCATION=11 , FX   , INPUTS =CH(IB=I1)
LOCATION=13 , PM   , INPUTS =EN(VO=VC)
LOCATION=15 , EN   , INPUTS =CH(IB=VI),OR(VO=VRF)
LOCATION=17 , OR   , INPUTS =EM(VO=V1),EI2(VO=V2)
LOCATION=19 , ET   , INPUTS =SA(VB=VI)
LOCATION=21 , EI1  , INPUTS =ET(VO=VI)
LOCATION=23 , EI2  , INPUTS =CH(IB=VI)
LOCATION=25 , EM   , INPUTS =ET(VO=VI)
*-------------------------------------------------------
END OF MODEL
PRINT
```

SYSTEM.MOD

SYSTEM MODEL FOR GENERAL SIMULATIONS



- The system behavior may be observed by changing the illumination level, or by applying a load step

```
*-------------------------------------------------------
* SYSTEM.MOD
*
* GENERAL SYSTEM MODEL FOR STUDYING EFFECTS OF ILLUMINATI
* LEVEL CHANGE AND STEP LOAD CHANGE
*
* CONTAINS SSU, CHARGER, FOUR MODULE DISCHARGER, MODE CON
* STEP LOAD, AND ILLUMINATION LEVEL GENERATOR
*-------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------
* SSU
LOCATION= 1 , SA   , INPUTS =NV1(AO=IO),RX(AO=LLM),EI1(VO=
LOCATION= 3 , RX
*-------------------------------------------------------
* FOUR MODULE BOOST
*
LOCATION= 5 , BT1  , INPUTS =BX(V1=VO),DD1(SW=IQ)
LOCATION= 7 , BT2  , INPUTS =BX(V1=VO),DD2(SW=IQ)
LOCATION= 9 , BT3  , INPUTS =BX(V1=VO),DD3(SW=IQ)
LOCATION=11 , BT4  , INPUTS =BX(V1=VO),DD4(SW=IQ)
LOCATION=13 , DD1  , INPUTS =EI3(VO=VC),BT1(IS=IL)
LOCATION=15 , DD2  , INPUTS =EI3(VO=VC),BT2(IS=IL)
LOCATION=17 , DD3  , INPUTS =EI3(VO=VC),BT3(IS=IL)
LOCATION=19 , DD4  , INPUTS =EI3(VO=VC),BT4(IS=IL)
LOCATION=21 , BX,  INPUTS =BT1(IO=I1),BT2(IO=I2),BT3(IO=I3
                    SA(VB=VO)
*-------------------------------------------------------
* CHARGER
LOCATION=25 , FI   , INPUTS =SA(VB=V1),CH(I1=IO)
LOCATION=27 , CH   , INPUTS =FI(VO=V1),FX(V1=VBB),PM(SW=IQ
LOCATION=29 , FX   , INPUTS =CH(IB=I1)
*CHARGER CURRENT SENSE AND PWM
LOCATION=31 , OR   , INPUTS =EM(VO=V1),EI2(VO=V2)
LOCATION=33 , PM   , INPUTS =EN(VO=VC)
LOCATION=35 , EN   , INPUTS =CH(IB=VI),OR(VO=VRF)
LOCATION=37 , EI2  , INPUTS =CH(IB=VI)
*-------------------------------------------------------
*MODE CONTROLLER
* 1=SHUNT  2=CHARGER (EM)   3=DISCHARGER
LOCATION=39 , ET   , INPUTS =SA(VB=VI)
LOCATION=41 , EI1  , INPUTS =ET(VO=VI)
LOCATION=43 , EM   , INPUTS =ET(VO=VI)
LOCATION=45 , EI3  , INPUTS =ET(VO=VI)
*-------------------------------------------------------
*LOAD
```

```
LOCATION=47 , NV1  , INPUTS =RQ(I1=A1),NV2(AO=A2)
LOCATION=49 , NV2  , INPUTS =FI(I1=A1),BX(IX=A2)
LOCATION=51 , RQ   , INPUTS =SA(VB=V1)
*-------------------------------------------------------
END OF MODEL
PRINT
```

```
*-------------------------------------------------------------
* CHS.MOD
* SMALL SIGNAL CHARGER ON CURRENT LOOP
*-------------------------------------------------------------
MACRO FILE NAME=MACROS
MODEL DESCRIPTION
*-------------------------------------------------------------
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CS OUTPUTS :    IL   I1   ILS
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
*ES OUTPUTS :    VO   X    VON
*EX OUTPUTS :    VO   VON
* NV IS USED TO MEASURE CURRENT LOOP GAIN
*-------------------------------------------------------------
LOCATION= 1 , FI  , INPUTS =  CS(I1=IO)
LOCATION= 3 , CS  , INPUTS =FI(VO=V1),FX(V1=VO),FC(DH=DH)
LOCATION= 5 , FX  , INPUTS =CS(IL=I1)
LOCATION= 7 , FC  , INPUTS =FI(VO=VI),CS(IL=IL),FX(V1=VO),NV(AO=VC)
LOCATION= 9 , ES  , INPUTS =CS(IL=VI)
LOCATION=11 , EX  , INPUTS =CS(IL=VI),ES(VO=VRF)
LOCATION=13 , NV  , INPUTS =EX(VO=A1)
*-------------------------------------------------------------
END OF MODEL
PRINT
```

```
*-------------------------------------------------------------
* CHV.MOD
* CHARGER SMALL SIGNAL VOLTAGE LOOP WITH CIC
* INCLUDES SMALL SIGNAL SOLAR ARRAY
* NV IS USED TO MEASURE  LOOP GAIN
*-------------------------------------------------------------
MODEL DESCRIPTION
*-------------------------------------------------------------
*PS OUTPUTS :    VO   VC
*CS OUTPUTS :    IL   I1   ILS
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
*NV OUTPUTS :    AO
*ES OUTPUTS :    VO   X    VON
*EX OUTPUTS :    VO   VON
*-------------------------------------------------------------
LOCATION= 1 , PS  , INPUTS =FI(I1=IO)
LOCATION= 3 , CS  , INPUTS =FI(VO=V1),FX(V1=VO),FC(DH=DH)
LOCATION= 5 , FI  , INPUTS =PS(VO=V1),CS(I1=IO)
LOCATION= 7 , FX  , INPUTS =CS(IL=I1)
LOCATION= 9 , FC  , INPUTS =FI(VO=VI),CS(IL=IL),FX(V1=VO),NV(AO=VC)
LOCATION=11 , NV  , INPUTS =EX(VO=A1)
LOCATION=13 , EY  , INPUTS =PS(VO=VI)
LOCATION=15 , EX  , INPUTS =CS(IL=VI),EY(VO=VRF)
*-------------------------------------------------------------
END OF MODEL
PRINT
```

```
*-------------------------------------------------------------
* ACS2.MOD
* VFPPAT SMALL SIGNAL MODEL : LOOP GAIN AND TRANSFER FUNCTIONS
**------------------------------------------------------------
MACRO FILE NAME=MACROS
MODEL DESCRIPTION
*-------------------------------------------------------------
LOCATION= 10 , AS  ,INPUTS = FM(DH=DH)
LOCATION= 15 , ES , INPUTS = AS(VC=VI),
LOCATION= 20 , FM,  INPUTS = TZ(S,2 = VI), AS(VC=VO)
LOCATION= 30 , TZ  ,INPUTS = AS(IL=S,1)
*-------------------------------------------------------------
END OF MODEL
PRINT
```

```
*-------------------------------------------------------------
** ACS3.MOD
* VFPPAT CLOSED LOOP MODEL : BUS IMPEDANCE
**------------------------------------------------------------
MACRO FILE NAME=MACROS
MODEL DESCRIPTION
***-----------------------------------------------------------
LOCATION= 10, AS , INPUTS = FM(DH=DH)
LOCATION= 15, ES , INPUTS = AS(VO=VI)
LOCATION= 20, FM , INPUTS = TZ(S,2=VI), AS(VC=VO), ES(VO=VC)
LOCATION= 30, TZ , INPUTS = AS(IL=S,1)
*-------------------------------------------------------------
END OF MODEL
PRINT
```

ANALYSIS FILES

```
*-------------------------------------------------------------
* SHUNT.ANC
* STEP LOAD TEST FOR SSU
*-------------------------------------------------------------
INITIAL CONDITIONS
*
 VB SA = 122.
 VC SA = 122.
 VO EI = 0
*
*SA OUTPUTS :    VB   VC   NPP  VR   NF   D    NPX
*RQ OUTPUTS :    I1
*RX OUTPUTS :    AO
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
 C1 SA = 10E-6
 C  SA = 2000E-6
 RC SA = .04
 TS SA = 20E-6
 VP SA = 0.2
 NPSSA = 15
 TA SA = 330.
*
*-------------------------------------------------------------
RI RQ  = 100
RF RQ  = 15
TS RQ  = 1200E-6
TP RQ  = 2000E-6
*
*-------------------------------------------------------------
SL RX  = 1
AI RX  = 1
TD RX  = 1
*
*-------------------------------------------------------------
VRFEI  = 7.5
KV EI  = 0.06147
WC EI  = 13000
WZ EI  = 6500
AG EI  = 20
VH EI  = 6
VL EI  = 0
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*-------------------------------------------------------------
DISPLAY1
VB SA
I1 RQ
NPPSA
*-------------------------------------------------------------
DISPLAY2
AO RX
VR SA
VO EI
*-------------------------------------------------------------
*SA OUTPUTS :    VB   VC   NPP  VR   NF   D    NPX
```

```
*RQ OUTPUTS :    I1
*RX OUTPUTS :    AO
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
 TINC = 1E-7
 TMAX = 5000E-6
 OUTRATE = 20
 PRATE = 300
 SIMULATE
```

```
*-------------------------------------------------------------
* AUTO.ANC
* VFPPAT LOAD STEP TEST
*-------------------------------------------------------------
INITIAL CONDITIONS
*
VC1FD = 64
VC2FD = 64
VO FD = 64
I1 FD = 28
I2 FD = 28
*
VB AT = 120
VC AT = 120
IL AT = 15
*
VO EI = 0.75
X  EI = 1
*
*FD OUTPUTS :    I1   VO   VC1  VC2  I2   IR1  IR2
*AT OUTPUTS :    VB   IL   I1   IS1  IS2  ID1  ID2  IT1  IT2  VC   SWL
*RS OUTPUTS :    I1
*DD OUTPUTS :    SW   VR   VCT
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
*
L1 FD  = 10E-6
L2 FD  = 2E-6
R1 FD  = 0.005
R2 FD  = 0.005
C1 FD  = 100E-6
C2 FD  = 20E-6
RC1FD  = 0.6
RC2FD  = 0.005
CX FD  = 1E-6
*
V1 FD = 64
*-------------------------------------------------------------
TS AT  = 12.5E-6
N  AT  = 1.5
L  AT  = 94E-6
C  AT  = 2000E-6
C1 AT  = 20E-6
RC AT  = 0.03
*
*-------------------------------------------------------------
RI RQ  = 100
RF RQ  = 8
TS RQ  = 950E-6
TP RQ  = 2020E-6
*
*-------------------------------------------------------------
ILPDD  = 200
VP DD  = 0.88
TS DD  = 12.5E-6
TD DD  = 0
DMXDD  = .99
XN DD  = 200
XK1DD  = 1
```

```
XK2DD  = 19.5
TX DD  = 1000
*
*---------------------------------------------------------------
VRFEI  = 4
KV EI  = 0.03333
WC EI  = 24460
WZ EI  = 1709
AG EI  = 165
VH EI  = 12
VL EI  = 0
*
*---------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*---------------------------------------------------------------
DISPLAY1
VB AT
I1 RQ
I1 FD
DISPLAY2
VO FD
VO EI
X EI
*FD OUTPUTS :    I1   VO   VC1  VC2  I2   IR1  IR2
*AT OUTPUTS :    VB   IL   I1   IS1  IS2  ID1  ID2  IT1  IT2  VC   SWL
*RS OUTPUTS :    I1
*DD OUTPUTS :    SW   VR   VCT
*EI OUTPUTS :    VO   SW   X
*---------------------------------------------------------------
*---------------------------------------------------------------
TINC = 0.4E-7
TMAX = 6000E-6
OUTRATE = 35
PRATE = 300
SIMULATE
```

```
*-------------------------------------------------------------
* BOOST.ANC
* FOUR MODULE BOOST STEP LOAD TEST
*-------------------------------------------------------------
INITIAL CONDITIONS
IL BT1 = 0.1
IL BT2 = 0.1
IL BT3 = 0.1
IL BT4 = 0.1
*
VC1BU  = 120
VC BU  = 120
VO BU  = 120
V1 BU  = 120
ILPBU  = 4
ILSBU  = 0
*
VO EI  = 1.5
*BT OUTPUTS :    IO   IL   IS   SWL
*DD OUTPUTS :    SW   VR   VCT
*BU OUTPUTS :    VO   V1   VC   VC1   IR   IT   ILP  ILS
*RS OUTPUTS :    I1
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
*
L  BT1 = 75E-6
RL BT1 = 0.01
VI BT1 = 64
*
L  BT2 = 75E-6
RL BT2 = 0.01
VI BT2 = 64
*
L  BT3 = 75E-6
RL BT3 = 0.01
VI BT3 = 64
*
L  BT4 = 75E-6
RL BT4 = 0.01
VI BT4 = 64
*
*-------------------------------------------------------------
ILPDD1 = 50
VP DD1 = 5.88
TS DD1 = 22.22E-6
TD DD1 = 0
DMXDD1 = 0.75
XN DD1 = 100
XK1DD1 = 1
XK2DD1 = 12
TX DD1 = 1000
*
ILPDD2 = 50
VP DD2 = 5.88
TS DD2 = 22.22E-6
TD DD2 = 5.555E-6
DMXDD2 = 0.75
XN DD2 = 100
XK1DD2 = 1
```

```
 XK2DD2 = 12
 TX DD2 = 1000
 *
 ILPDD3 = 50
 VP DD3 = 5.88
 TS DD3 = 22.22E-6
 TD DD3 = 11.11E-6
 DMXDD3 = 0.75
 XN DD3 = 100
 XK1DD3 = 1
 XK2DD3 = 12
 TX DD3 = 1000
 *
 ILPDD4 = 50
 VP DD4 = 5.88
 TS DD4 = 22.22E-6
 TD DD4 = 16.665E-6
 DMXDD4 = 0.75
 XN DD4 = 100
 XK1DD4 = 1
 XK2DD4 = 12
 TX DD4 = 1000
 *
 *---------------------------------------------------------------
 C  BU  = 2000E-6
 RC BU  = 0.03
 C1 BU  = 20E-6
 RC1BU  = .003
 LP BU  = 5E-6
 LS BU  = 0.5E-6
 RS BU  = 0.16
 *
 *---------------------------------------------------------------
 RI RS  = 100
 RF RS  = 8
 TS RS  = 700E-6
 IX RS  = 0
 *
 *---------------------------------------------------------------
 VRFEI  = 7.5
 KV EI  = 0.0625
 WC EI  = 27727
 WZ EI  = 5000
 AG EI  = 26.23
 VH EI  = 12
 VL EI  = 0
 *
 *---------------------------------------------------------------
 PRINTER PLOTS
 ONLINE PLOTS
 INT MODE = 1
 *---------------------------------------------------------------
 DISPLAY1
 * BUS VTG, INPUT CURRENT, LOAD CURRENT
 VO BU
 IO AD
 I1 RS
 DISPLAY2
 * CAP VTG RIPPLE, CT RIP, ERROR AMP
 V1 BU
```

```
IR BU
VO EI
DISPLAY3
* INDUCTOR CURRENTS
IL BT1
IL BT2
IL BT3
IL BT4
*BT OUTPUTS :    IO   IL   IS   SWL
*DD OUTPUTS :    SW   VR   VCT
*BU OUTPUTS :    VO   V1   VC   VC1  IO   IR   IT   ILP  ILS
*RS OUTPUTS :    I1
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 2945E-6
 OUTRATE = 20
 PRATE = 300
 SIMULATE
```

```
*-------------------------------------------------------------
* BOOST2.ANC
* 4 MODULE BOOST WITH CABLE - STEP LOAD TEST
*-------------------------------------------------------------
INITIAL CONDITIONS
*
IL BT1 = 0.1
IL BT2 = 0.1
IL BT3 = 0.1
IL BT4 = 0.1
*
V1 BX  = 120
VC1BX  = 120
ILPBX  = .14
*
VO EI = 1.5
VO TP = 120
V1 TP = 120
*
VC CI = 120
*AD OUTPUTS :    IO
*BT OUTPUTS :    IO   IL   IS   SWL
*DD OUTPUTS :    SW   VR   VCT
*BX OUTPUTS :    V1   IX   IXN  VC1  IR   IT   ILP  ILS
*TP OUTPUTS :    V1   VO
*CB OUTPUTS :    VB   VC
*RQ OUTPUTS :    I1
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
*
*
*-------------------------------------------------------------
L  BT1 = 75E-6
RL BT1 = 0.01
VI BT1 = 64
*
L  BT2 = 75E-6
RL BT2 = 0.01
VI BT2 = 64
*
L  BT3 = 75E-6
RL BT3 = 0.01
VI BT3 = 64
*
L  BT4 = 75E-6
RL BT4 = 0.01
VI BT4 = 64
*
*-------------------------------------------------------------
ILPDD1 = 50
VP DD1 = 5.88
TS DD1 = 22.22E-6
TD DD1 = 0
DMXDD1 = 0.75
XN DD1 = 100
XK1DD1 = 1
XK2DD1 = 12
TX DD1 = 1000
*
```

```
ILPDD2 = 50
VP DD2 = 5.88
TS DD2 = 22.22E-6
TD DD2 = 5.555E-6
DMXDD2 = 0.75
XN DD2 = 100
XK1DD2 = 1
XK2DD2 = 12
TX DD2 = 1000
*
ILPDD3 = 50
VP DD3 = 5.88
TS DD3 = 22.22E-6
TD DD3 = 11.11E-6
DMXDD3 = 0.75
XN DD3 = 100
XK1DD3 = 1
XK2DD3 = 12
TX DD3 = 1000
*
ILPDD4 = 50
VP DD4 = 5.88
TS DD4 = 22.22E-6
TD DD4 = 16.66E-6
DMXDD4 = 0.75
XN DD4 = 100
XK1DD4 = 1
XK2DD4 = 12
TX DD4 = 1000
*
*-------------------------------------------------------------
R  BX  = 600
C1 BX  = 20E-6
RC1BX  = 0.003
LP BX  = 5E-6
LS BX  = 0.5E-6
RS BX  = 0.16
*
*-------------------------------------------------------------
C  TP  = 204E-12
R  TP  = 0.2
L  TP  = 2.2E-6
*
*-------------------------------------------------------------
C  CI  = 2000E-6
RC CI  = 0.03
*
*-------------------------------------------------------------
RI RQ  = 100
RF RQ  = 8
TS RQ  = 600E-6
TP RQ  = 2000E-6
*
*-------------------------------------------------------------
VRFEI  = 7.5
KV EI  = 0.0625
WC EI  = 27727
WZ EI  = 5000
AG EI  = 26.23
VH EI  = 12
```

```
VL EI  = 0
*
*---------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*---------------------------------------------------------------
DISPLAY1
VO TP
V1 BX
I1 RQ
DISPLAY2
V1 BX
VO EI
IR BX
DISPLAY3
IL BT1
IL BT2
IL BT3
IL BT4
SI MANUAL SCALES
DISPLAY4
VO TP,YRANGE,118,122
VO EI,YRANGE,0,12
I1 RQ,YRANGE,0,18
*AD OUTPUTS :    IO
*BT OUTPUTS :    IO   IL   IS   SWL
*DD OUTPUTS :    SW   VR   VCT
*BX OUTPUTS :    V1   IX   IXN  VC1  IR   IT   ILP  ILS
*TP OUTPUTS :    V1   VO
*CB OUTPUTS :    VB   VC
*RQ OUTPUTS :    I1
*EI OUTPUTS :    VO   SW   X
*---------------------------------------------------------------
*---------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 6000E-6
 OUTRATE = 25
  PRATE = 300
 SIMULATE
```

```
*-------------------------------------------------------------
* CHARGER1.ANC
* CURRENT REFERENCE STEP CHANGE TEST FOR CHARGER
*-------------------------------------------------------------
INITIAL CONDITIONS
VO FI = 120
VC FI = 120
VCFFI = 120
IL FI = 1
*
V1 FX = 74
VC FX = 74
IB FX = 4.0
*
IB CH = 4.0
*
VO EN = 1.2
VO EI = 1.5
X  EI = -11
*
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CH OUTPUTS :    IB   I1   ID   SWL
*FX OUTPUTS :    V1   IB   VC
*PM OUTPUTS :    SW   VR
*EN OUTPUTS :    VO   SW
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
*
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = 0.005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 4E-6
*
V1 FI = 120
*-------------------------------------------------------------
L  CH  = 68E-6
RS CH  = 0.006
RM CH  = 0.02
*
*-------------------------------------------------------------
L  FX  = 10E-6
RL FX  = 0.2
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 74
*-------------------------------------------------------------
KV PM  = 1
VP PM  = 1.8
TS PM  = 11.11E-6
DMXPM  = 0.999
*
*-------------------------------------------------------------
KV EN  = 0.1
AG EN  = 1
```

```
WGBEN  = 333333
VH EN  = 12
VL EN  = 0
*
*-------------------------------------------------------------
KV EI  = 0.1
WC EI  = 190000
WZ EI  = 183650
AG EI  = 0.05
VH EI  = 12
VL EI  = 0
*
*-------------------------------------------------------------
AI ST  = 0.4
AF ST  = 0.8
TS ST  = 450E-6
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*-------------------------------------------------------------
DISPLAY1
IB CH
IB FX
AO ST
DISPLAY2
VO EN
VO EI
V1 FX
DISPLAY3
VO FI
IR FI
I1 FI
DISPLAY4,OVERPLOT
VR PM
VO EN
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CH OUTPUTS :    IB   I1   ID   SWL
*FX OUTPUTS :    V1   IB   VC
*PM OUTPUTS :    SW   VR
*EN OUTPUTS :    VO   SW
*EI OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 1000E-6
 OUTRATE = 15
 PRATE =  300
 SIMULATE
```

```
*-------------------------------------------------------------
* CHARGER2.ANC
* CHARGER VOLTAGE LOOP TEST WITH SSU
*
* FILE SET FOR LARGE STEP TRANSITION TO SHUNT AND CHANGEOVER
* OF CHARGER FOR VOLTAGE TO CURRENT MODE. (RF RS = 17)
*
* A SMALLER LOAD STEP RF RS=10.43 DEMONSTRATES CHARGER
* STEP REGULATION W/O CHANGING TO SHUNT
*
*-------------------------------------------------------------
INITIAL CONDITIONS
*
VB SA = 121
VC SA = 121
*
IB CH =6
*
IB FX = 6.5
V1 FX = 75
VC FX = 75
*
VO FI = 121
VC FI = 121
VCFFI = 121
IL FI = 4
*
VO EI1=6
VO EI2=4
VO EM = 1.6
*
*SA OUTPUTS :    VB   VC   NPP  VR   NF   D    NPX
*NV OUTPUTS :    AO
*RS OUTPUTS :    I1
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CH OUTPUTS :    IB   I1   ID   SWL
*FX OUTPUTS :    V1   IB   VC
*PM OUTPUTS :    SW   VR
*EN OUTPUTS :    VO   SW
*OR OUTPUTS :    VO
*ET OUTPUTS :    VO   SW
*EI OUTPUTS :    VO   SW   X
*EM OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
PARAMETER VALUES
*
C1 SA  = 10E-6
C  SA  = 2000E-6
RC SA  = 0.04
TS SA  = 20E-6
VP SA  = 0.2
NPSSA  = 15
TA SA  = 330
*
LLMSA  = 0.4
*-------------------------------------------------------------
KV1NV  = 1
KV2NV  = 1
*
*-------------------------------------------------------------
```

```
RI RS  = 8.89
*RF RS  = 10.43
RF RS  = 17
TS RS  = 1700E-6
IX RS  = 0
*
*---------------------------------------------------------------
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = .005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 4E-6
*
*---------------------------------------------------------------
L  CH  = 68E-6
RS CH  = .006
RM CH  = 0.02
*
*---------------------------------------------------------------
L  FX  = 10E-6
RL FX  = 0.2
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 75
*---------------------------------------------------------------
KV PM  = 1
VP PM  = 1.8
TS PM  = 11.11E-6
DMXPM  = .999
*
*---------------------------------------------------------------
KV EN  = 0.1
AG EN  = 1
WGBEN  = 333333
VH EN  = 12
VL EN  = 0
*
*---------------------------------------------------------------
K1 OR  = 1
K2 OR  = 1
*
*---------------------------------------------------------------
VRFET  = 7.5
KV ET  = .06667
AG ET  = 15
WGBET  = 1E7
VH ET  = 12
VL ET  = 0
*
*---------------------------------------------------------------
VRFEI1 = 7.5
KV EI1 = .789
WC EI1 = 13000
WZ EI1 = 6500
AG EI1 = 8
VH EI1 = 6
```

```
VL EI1 = 0
*
* CHARGER CT SENSE
KV EI2 = 0.1
WC EI2 = 190000
WZ EI2 = 183650
AG EI2 = 0.05
VH EI2 = 4
VL EI2 = 0
* CT REF = 12.8A IS 8A ON BUS SIDE
VRFEI2 = 1.28
*-------------------------------------------------------------
VRFEM  = 7.5
KV EM  = 0.8817
WC EM  = 511111
WZ EM  = 6060
AG EM = 3.3
*AG EM  = 0.658
VH EM  = 12
VL EM  = 0
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*-------------------------------------------------------------
DISPLAY1
VB SA
I1 RS
NPPSA
I1 CH
*
DISPLAY2
IB CH
IB FX
VO FI
IL FI
*
DISPLAY3
VO EI1
VO EM
VO EI2
VO OR
*
*SA OUTPUTS :    VB   VC   NPP  VR   NF   D    NPX
*NV OUTPUTS :    AO
*RS OUTPUTS :    I1
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CH OUTPUTS :    IB   I1   ID   SWL
*FX OUTPUTS :    V1   IB   VC
*PM OUTPUTS :    SW   VR
*EN OUTPUTS :    VO   SW
*OR OUTPUTS :    VO
*ET OUTPUTS :    VO   SW
*EI OUTPUTS :    VO   SW   X
*EM OUTPUTS :    VO   SW   X
*-------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 5000E-6
* OUTRATE = 100
```

```
OUTRATE = 35
 PRATE = 300
 SIMULATE
```

```
*-------------------------------------------------------------
* SYSTEM1.ANC
* SYSTEM MODEL SIMULATION SHOWING
* SUNLIGHT TO ECLIPSE TRANSITION
*-------------------------------------------------------------
INITIAL CONDITIONS
*
*SHUNT
 VB SA = 122.
 VC SA = 122.
*BOOST
*
 VC1BX  = 122
 V1 BX  = 122
 ILPBX  = 0.01
 ILSBX  = 0.01
*
*CHARGER
 IB CH =.01
*
 IB FX = .01
 V1 FX = 75
 VC FX = 75
*
 VO FI = 122
 VC FI = 122
 VCFFI = 122
 IL FI = .01
*
 VO EI2=0
*
*MODE CONTROLLER
 VO EI1 = 5
 VO EM = .01
 VO EI3 = 0
*

*-------------------------------------------------------------
PARAMETER VALUES
*-------------------------------------------------------------
*SHUNT
*
 C1 SA = 10E-6
 C  SA = 2000E-6
 RC SA = .04
 TS SA = 20E-6
 VP SA = 0.2
 NPSSA = 15
 TA SA = 330.
*
*ILLUMINATION LEVEL
*
 SL RX  = -20
 AI RX  = 0.4
 TD RX  = 500E-6
*
*-------------------------------------------------------------
*BOOST
*
L  BT1 = 75E-6
```

```
RL BT1 = 0.01
VI BT1 = 75
*
L  BT2 = 75E-6
RL BT2 = 0.01
VI BT2 = 75
*
L  BT3 = 75E-6
RL BT3 = 0.01
VI BT3 = 75
*
L  BT4 = 75E-6
RL BT4 = 0.01
VI BT4 = 75
*
ILPDD1 = 50
VP DD1 = 5.88
TS DD1 = 22.22E-6
TD DD1 = 0
DMXDD1 = 0.75
XN DD1 = 100
XK1DD1 = 1
XK2DD1 = 12
TX DD1 = 1000
*
ILPDD2 = 50
VP DD2 = 5.88
TS DD2 = 22.22E-6
TD DD2 = 5.555E-6
DMXDD2 = 0.75
XN DD2 = 100
XK1DD2 = 1
XK2DD2 = 12
TX DD2 = 1000
*
ILPDD3 = 50
VP DD3 = 5.88
TS DD3 = 22.22E-6
TD DD3 = 11.11E-6
DMXDD3 = 0.75
XN DD3 = 100
XK1DD3 = 1
XK2DD3 = 12
TX DD3 = 1000
*
ILPDD4 = 50
VP DD4 = 5.88
TS DD4 = 22.22E-6
TD DD4 = 16.665E-6
DMXDD4 = 0.75
XN DD4 = 100
XK1DD4 = 1
XK2DD4 = 12
TX DD4 = 1000
*
R  BX  = 600
C1 BX  = 20E-6
RC1BX  = .003
LP BX  = 5E-6
LS BX  = 0.5E-6
```

```
RS BX  = 0.16
*
*-------------------------------------------------------------
*CHARGER
*
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = .005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 4E-6
*
L  CH  = 68E-6
RS CH  = .006
RM CH  = 0.02
*
L  FX  = 10E-6
RL FX  = 0.2
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 75
*
KV PM  = 1
VP PM  = 1.8
TS PM  = 11.11E-6
DMXPM  = .999
*
KV EN  = 0.1
AG EN  = 1
WGBEN  = 333333
VH EN  = 12
VL EN  = 0
*
K1 OR  = 1
K2 OR  = 1
*
KV EI2 = 0.1
WC EI2 = 190000
WZ EI2 = 183650
AG EI2 = 0.05
VH EI2 = 4
VL EI2 = 0
*
* CT REF = 12.8A IS 8A ON BUS SIDE
* VRFEI2 = 1.28
 VRFEI2 = 0.6
*
*-------------------------------------------------------------
*LOAD
*
KV1NV1 = 1
KV2NV1 = 1
KV1NV2 = 1
KV2NV2 = 1
*
RI RQ  = 8
RF RQ  = 8
```

```
TS RQ  = 1
TP RQ  = 1
*
*---------------------------------------------------------------
*MODE CONTROLLER
*
VRFET  = 7.5
KV ET  = .06667
AG ET  = 15
WGBET  = 1E7
VH ET  = 12
VL ET  = 0
*
VRFEI1 = 7.5
KV EI1 = 0.7894
WC EI1 = 13000
WZ EI1 = 6500
AG EI1 = 2
VH EI1 = 6
VL EI1 = 0
*
VRFEM  = 7.5
KV EM  = 0.8817
WC EM  = 511111
WZ EM  = 6060
AG EM = 3.3
VH EM  = 10
VL EM  = 0
*
VRFEI3 = 7.5
KV EI3 = 1
WC EI3 = 27727
WZ EI3 = 5000
AG EI3 = 1.639
VH EI3 = 6
VL EI3 = 0
*
*---------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*---------------------------------------------------------------
* BUS VOLTAGE, ILLUM. LEVEL, STRINGS
DISPLAY1
VB SA
AO RX
NPPSA
*-------------------------------------------------------
* OP AMP OUTPUTS
DISPLAY2
VO EI1
VO EM
VO EI3
*-------------------------------------------------------
* LOAD CURRENT, DISCHARGER BUS CT, BATT CT
DISPLAY3
I1 RQ
IXNBX
VO OR
*---------------------------------------------------------------
```

```
* ONE BOOST IL, CHARGER BUS CT, CHARGER BAT CT
DISPLAY4
IL BT1
IL FI
IB FX
*
*-------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 0.03
*TMAX = 1000E-6
 OUTRATE = 290
*OUTRATE  = 20
 PRATE = 300
 SIMULATE
```

```
*---------------------------------------------------------------
* SYSTEM2.ANC
* SYSTEM MODEL SIMULATION SHOWING
* ECLIPSE TO SUNLIGHT TRANSITION
*---------------------------------------------------------------
INITIAL CONDITIONS
*
*SHUNT
 VB SA = 120.
 VC SA = 120.
*BOOST
*
 VC1BX  = 120
 V1 BX  = 120
 ILPBX  = 15
 ILSBX  = 0.01
*
*CHARGER
 IB CH =.01
*
 IB FX = .01
 V1 FX = 75
 VC FX = 75
*
 VO FI = 120
 VC FI = 120
 VCFFI = 120
 IL FI = .01
*
 VO EI2=0
*
*MODE CONTROLLER
 VO EI1 = 5
 VO EM = .01
 VO EI3 = 4.0
*

*---------------------------------------------------------------
PARAMETER VALUES
*---------------------------------------------------------------
*SHUNT
*
 C1 SA = 10E-6
 C  SA = 2000E-6
 RC SA = .04
 TS SA = 20E-6
 VP SA = 0.2
 NPSSA = 15
 TA SA = 330.
*
*ILLUMINATION LEVEL
*
 SL RX  = 10
 AI RX  = 0.2
 TD RX  = 500E-6
*
*---------------------------------------------------------------
*BOOST
*
L  BT1 = 75E-6
```

```
RL BT1 = 0.01
VI BT1 = 75
*
L  BT2 = 75E-6
RL BT2 = 0.01
VI BT2 = 75
*
L  BT3 = 75E-6
RL BT3 = 0.01
VI BT3 = 75
*
L  BT4 = 75E-6
RL BT4 = 0.01
VI BT4 = 75
*
ILPDD1 = 50
VP DD1 = 5.88
TS DD1 = 22.22E-6
TD DD1 = 0
DMXDD1 = 0.75
XN DD1 = 100
XK1DD1 = 1
XK2DD1 = 12
TX DD1 = 1000
*
ILPDD2 = 50
VP DD2 = 5.88
TS DD2 = 22.22E-6
TD DD2 = 5.555E-6
DMXDD2 = 0.75
XN DD2 = 100
XK1DD2 = 1
XK2DD2 = 12
TX DD2 = 1000
*
ILPDD3 = 50
VP DD3 = 5.88
TS DD3 = 22.22E-6
TD DD3 = 11.11E-6
DMXDD3 = 0.75
XN DD3 = 100
XK1DD3 = 1
XK2DD3 = 12
TX DD3 = 1000
*
ILPDD4 = 50
VP DD4 = 5.88
TS DD4 = 22.22E-6
TD DD4 = 16.665E-6
DMXDD4 = 0.75
XN DD4 = 100
XK1DD4 = 1
XK2DD4 = 12
TX DD4 = 1000
*
R  BX  = 600
C1 BX  = 20E-6
RC1BX  = .003
LP BX  = 5E-6
LS BX  = 0.5E-6
```

```
RS BX  = 0.16
*
*-------------------------------------------------------------
*CHARGER
*
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = .005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 4E-6
*
L  CH  = 68E-6
RS CH  = .006
RM CH  = 0.02
*
L  FX  = 10E-6
RL FX  = 0.2
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 75
*
KV PM  = 1
VP PM  = 1.8
TS PM  = 11.11E-6
DMXPM  = .999
*
KV EN  = 0.1
AG EN  = 1
WGBEN  = 333333
VH EN  = 12
VL EN  = 0
*
K1 OR  = 1
K2 OR  = 1
*
KV EI2 = 0.1
WC EI2 = 190000
WZ EI2 = 183650
AG EI2 = 0.05
VH EI2 = 4
VL EI2 = 0
*
* CT REF = 12.8A IS 8A ON BUS SIDE
* VRFEI2 = 1.28
 VRFEI2 = 0
*
*-------------------------------------------------------------
*LOAD
*
KV1NV1 = 1
KV2NV1 = 1
KV1NV2 = 1
KV2NV2 = 1
*
RI RQ  = 8
RF RQ  = 8
```

```
TS RQ  = 1
TP RQ  = 1
*
*-------------------------------------------------------------
*MODE CONTROLLER
*
VRFET  = 7.5
KV ET  = .06667
AG ET  = 15
WGBET  = 1E7
VH ET  = 12
VL ET  = 0
*
VRFEI1 = 7.5
KV EI1 = 0.7894
WC EI1 = 13000
WZ EI1 = 6500
AG EI1 = 2
VH EI1 = 6
VL EI1 = 0
*
VRFEM  = 7.5
KV EM  = 0.8817
WC EM  = 511111
WZ EM  = 6060
AG EM = 3.3
VH EM  = 10
VL EM  = 0
*
VRFEI3 = 7.5
KV EI3 = 1
WC EI3 = 27727
WZ EI3 = 5000
AG EI3 = 1.639
VH EI3 = 6
VL EI3 = 0
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
INT MODE = 1
*-------------------------------------------------------------
* BUS VOLTAGE, ILLUM. LEVEL, STRINGS
DISPLAY1
VB SA
AO RX
NPPSA
*-----------------------------------------------------------
* OP AMP OUTPUTS
DISPLAY2
VO EI1
VO EM
VO EI3
*-----------------------------------------------------------
* LOAD CURRENT, DISCHARGER BUS CT, BATT CT
DISPLAY3
I1 RQ
IXNBX
VO OR
*-------------------------------------------------------------
```

```
* ONE BOOST IL, CHARGER BUS CT, CHARGER BAT CT
DISPLAY4
IL BT1
IL FI
IB FX
*
*---------------------------------------------------------------
 TINC = 0.4E-7
 TMAX = 0.01
*TMAX = 1000E-6
 OUTRATE = 100
*OUTRATE  = 20
 PRATE = 300
 SIMULATE
```

```
*-------------------------------------------------------------
* CHS.ANC
* SMALL SIGNAL CHARGER ON CURRENT LOOP
*-------------------------------------------------------------
INITIAL CONDITIONS
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CS OUTPUTS :    IL   I1   ILS
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
*ES OUTPUTS :    VO   X    VON
*EX OUTPUTS :    VO   VON
*-------------------------------------------------------------
PARAMETER VALUES
*
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = 0.005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 4E-6
*
V1 FI  = 120
*-------------------------------------------------------------
L  CS  = 68E-6
RL CS  = .01
D  CS  = 0.616
V1SCS  = 120
VOSCS  = 74
*
*-------------------------------------------------------------
L  FX  = 10E-6
RL FX  = 0.1
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 74
*-------------------------------------------------------------
RI FC  = 0.1
TS FC  = 1.111E-5
L  FC  = 68E-6
VP FC  = 1.8
DI FC  = 4.5
D  FC  = 0.616
KHEFC  = 1.
KINFC = 1.
KOTFC = 1.
*
*-------------------------------------------------------------
KV ES  = 0.1
WC ES  = 190000
WZ ES  = 183650
AG ES  = 0.05
*
VRFES  = 0
*-------------------------------------------------------------
AG EX  = 1
WC EX  = 333333
KV EX  = 0.1
```

```
*
*-------------------------------------------------------------
KV1NV  = 1
KV2NV  = 0
A2 NV  = 0
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
*-------------------------------------------------------------
TF MANUAL SCALE
FREQ MIN = 6.3
FREQ MAX = 3E5
*-------------------------------------------------------------
TITLE = IL1/IRF WITH CURRENT LOOP CLOSED
TF INPUT = VRFES
TF OUTPUT = IL CS
TRANSFER FUNCTION
*-------------------------------------------------------------
PARAMETER VALUES
KV1NV = 0
KV2NV = 1
TITLE = CURRENT LOOP GAIN
TF INPUT =  A2 NV
TF OUTPUT = VONEX
TRANSFER FUNCTION
*-------------------------------------------------------------
*
PARAMETER VALUES
KINFC = 0
KOTFC = 0
KHEFC = 0
TF INPUT = AO NV
TF OUTPUT = IL CS
TITLE = OPEN LOOP CONTROL TO L1 INDUCTOR CURRENT
TRANSFER FUNCTION
**------------------------------------------------------------
TF INPUT = AO NV
TF OUTPUT = IB FX
TITLE = OPEN LOOP CONTROL TO L2 INDUCTOR CURRENT
TRANSFER FUNCTION
*-------------------------------------------------------------
NO STATES
TF INPUT = VRFES
INT CONTROLS, VO ES = 1, X  ES = 1
TF OUTPUT = VO ES
TITLE = INTEGRATING COMPENSATOR RESPONSE
TRANSFER FUNCTION
*-------------------------------------------------------------
NO STATES
TF INPUT = VO ES
INT CONTROLS, VO EX = 1
TF OUTPUT = VO EX
TITLE = PROPORTIONAL COMPENSATOR RESPONSE
TRANSFER FUNCTION
*-------------------------------------------------------------
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CS OUTPUTS :    IL   I1   ILS
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
```

```
*---------------------------------------------------------------
* CHV.ANC
* CHARGER SMALL SIGNAL VOLTAGE LOOP WITH CIC
*---------------------------------------------------------------
INITIAL CONDITIONS
*PS OUTPUTS :    VO   VC
*CS OUTPUTS :    IL   I1   ILS
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
*NV OUTPUTS :    AO
*EY OUTPUTS :    VO   X    VON
*EX OUTPUTS :    VO   VON
*---------------------------------------------------------------
PARAMETER VALUES
*
IA PS  = 2.86
C  PS  = 2000E-6
RC PS  = 0.03
C1 PS  = 1E-6
RD PS  = 10
*
IX PS  = 0
*---------------------------------------------------------------
L  CS  = 68E-6
RL CS  = 0.01
D  CS  = 0.616
V1SCS  = 120
VOSCS  = 74
*
*---------------------------------------------------------------
L  FI  = 10E-6
RL FI  = 0.005
C  FI  = 40E-6
RC FI  = 0.005
CF FI  = 200E-6
RCFFI  = 0.2
C1 FI  = 1E-6
*
*---------------------------------------------------------------
L  FX  = 10E-6
RL FX  = 0.1
C  FX  = 20E-6
RC FX  = 1
C1 FX  = 1E-6
*
VBBFX  = 74
*---------------------------------------------------------------
*
RI FC  = 0.1
TS FC  = 1.111E-5
L  FC  = 68E-6
VP FC  = 1.8
DI FC  = 4.5
D  FC  = 0.616
KHEFC  = 1.
KINFC  = 1.
KOTFC  = 1.
*
*---------------------------------------------------------------
```

```
KV1NV  = 1
KV2NV  = 0
*
A2 NV  = 0
*-------------------------------------------------------------
KV EY  = 0.1
WC EY  = 511111
WZ EY  = 4000
WZ2EY  = 6000
AG EY  = 5
*
VRFEY  = 7.5
*-------------------------------------------------------------
AG EX  = 1
WC EX  = 333333
KV EX  = 0.1
*
*-------------------------------------------------------------
PRINTER PLOTS
ONLINE PLOTS
*-------------------------------------------------------------
TF MANUAL SCALE
FREQ MIN = 6.3
FREQ MAX = 3E5
*-------------------------------------------------------------
TITLE = CLOSED LOOP BUS IMPEDANCE
TF INPUT =  IX PS
TF OUTPUT = VO PS
TRANSFER FUNCTION
*-------------------------------------------------------------
PARAMETER VALUES
KV1NV = 0
TITLE = LOOP GAIN
TF INPUT =  AO NV
TF OUTPUT = VO EX
TRANSFER FUNCTION
*-------------------------------------------------------------
NO STATES
TF INPUT = VRFEY
INT CONTROLS, X2 EY = 1, X1 EY = 1
TF OUTPUT = VO EY
TITLE = VOLTAGE COMPENSATOR RESPONSE
TRANSFER FUNCTION
*-------------------------------------------------------------
PARAMETER VALUES
KINFC = 0
KOTFC = 0
KHEFC = 0
ALL STATES
TF INPUT = AO NV
TF OUTPUT = VONPS
TITLE = OPEN LOOP CONTROL TO BUS VOLTAGE
TRANSFER FUNCTION
*FI OUTPUTS :    VO   I1   IL   VC   VCF  IR   IRF
*CS OUTPUTS :    IL   I1   ILS
*FX OUTPUTS :    V1   IB   VC
*FC OUTPUTS :    DH   X1   X2
*ES OUTPUTS :    VO   X    VON
*EX OUTPUTS :    VO   VON
*-------------------------------------------------------------
```

```
*ACS2.ANC
*VFPPAT SMALL SIGNAL MODEL : TRANSFER FUNCTIONS, LOOP GAIN
*
PARAMETER VALUES
*
KV ES = 0.1
IRFES = 12
WC ES = 2E4
AG ES = 60
WZ ES = 150
*
L  AS = 94E-6
RL AS = .01
C  AS = 2000E-6
RC AS = 0.03
R  AS = 8
N  AS = 1.5
D  AS = 0.4
V1SAS = 75
IOSAS = 15
RI AS = 0.17
*
RI FM = 0.17
* 3.5 X 0.17A PER 0.4 TS = 119000
SN FM = 119000
* 1V/1.25E-5
* ALSO 2V=160000        1.5V = 120000
SE FM = 80000
*SE FM = 0
TS FM = 1.25E-5
XL FM = 94E-6
*
* ZO TZ = 1
*Z1 TZ = -6.25E-6
*Z2 TZ = 1.583E-11
ZO TZ = 1E14
Z1 TZ = -6.25E8
Z2 TZ = 1583
P1 TZ = 2E7
PO TZ = 1E14
*
ONLINE PLOTS
TF MANUAL SCALE
FREQ MIN = 6.3
FREQ MAX = 0.7E6
*
ALL STATES
TF INPUT = VC FM
TF OUTPUT = VO AS
TITLE = VO/VC WITH CURRENT LOOP CLOSED
TRANSFER FUNCTION
*
NO STATES
TF INPUT = VC AS
TF OUTPUT = VO ES
INT CONTROLS
X  ES = 1
VO ES = 1
TITLE = COMPENSATOR
TRANSFER FUNCTION
```

```
*
TF INPUT = VC FM
TF OUTPUT =VONES
TITLE = LOOP GAIN
TRANSFER FUNCTION
```

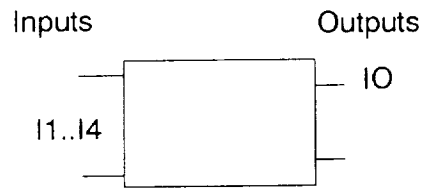
```
* ACS3.ANC
* VFPPAT SMALL SIGNAL : CLOASED LOOP BUS IMPEDANCE
*
PARAMETER VALUES
*
*
KV ES = 0.1
IRFES = 12
WC ES = 2E4
AG ES = 100
WZ ES = 100
*
L  AS = 94E-6
RL AS = .01
C  AS = 2000E-6
RC AS = 0.03
R  AS = 8
N  AS = 1.5
D  AS = 0.4
V1SAS = 75
IOSAS = 15
RI AS = 0.17
*
RI FM = 0.17
* 3.5 X 0.17A PER 0.4 TS = 119000
SN FM = 119000
* 1V/1.25E-5
* ALSO 2V=160000          1.5V = 120000
SE FM = 80000
*SE FM = 0
TS FM = 1.25E-5
XL FM = 94E-6
*
* ZO TZ = 1
*Z1 TZ = -6.25E-6
*Z2 TZ = 1.583E-11
Z0 TZ = 1E14
Z1 TZ = -6.25E8
Z2 TZ = 1583
P1 TZ = 2E7
P0 TZ = 1E14
*
ONLINE PLOTS
TF MANUAL SCALE
FREQ MIN = 6.3
FREQ MAX = 0.7E6
*
*
ALL STATES
TF INPUT = IO AS
TF OUTPUT = VO AS
TITLE =  OUTPUT IMPEDANCE WITH BOTH LOOPS CLOSED
TRANSFER FUNCTION
```

COMPONENT MODELS

AD	adder for four quantities
AT	voltage fed push pull autotransformer discharger
BT	single boost module
BU	adder and output filter for four module boost
BX	adder and output filter without bus capacitor
CH	charger buck converter
CI	bus capacitor
DD	PWM comparator with current sense
EI	inverting integrating compensator with clamps
EM	noninverting integrating compensator with clamps
EN	inverting proportional compensator with clamps
ET	noninverting proportional compensator with clamps
FD	input filter for VFPPAT
FI	input filter for charger
FX	output filter for charger
NV	adder/inverter for twoquantities
OR	OR gate to select lesser of two values
PM	PWM comparator with max duty ratio limit
RX	general slope generator (for illumination level)
RQ	pulsed resistive load step change
RS	resistive load step change
SA	solar array, SSU, and bus capacitor
ST	step generator
TP	lumped model for connecting cable

AD.MOD

Adder for four quantities



OUTPUTS

Units

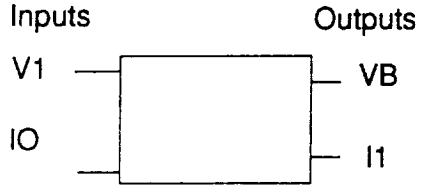
IO	output	

INPUTS

I1 I2 I3 I4	four inputs	

AT.MOD

Voltage fed push-pull autotransformer topology



OUTPUTS

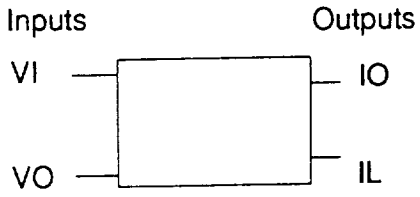
		Units
VB	bus voltage	V
IL	inductor current	A
I1	input current	A
IS1..IS2	switch currents	A
ID1..ID2	diode currents	A
IT1..IT2	winding currents	A
VC	bus capacitor state	V
SWL	inductor discontinuity switch state	-
IS	sum of switch currents for sensing	A

INPUTS

IQ	switch signal	-
V1	battery voltage	V
IO	load current	A
TS	secondary side switching period	sec
N	turns ratio	-
L	filter inductor	H
C	bus capacitor	F
C1	aux capacitor	F
RC	bus capacitor ESR	ohm

BT.MOD

Single boost converter module



OUTPUTS

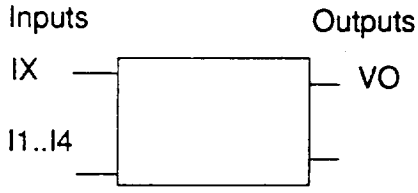
		Units
IO	output current	A
IL	inductor current	A
IS	switch current	A
SWL	inductor discontinuity switch state	-

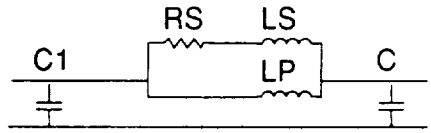
INPUTS

VO	output voltage	V
IQ	switch state signal	-
L	inductor	H
RL	inductor ESR	ohm

BU.MOD

Adder and output filter for four module boost





OUTPUTS

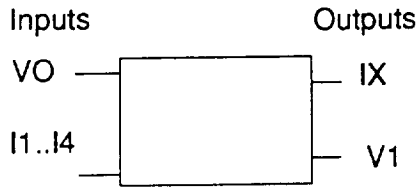
		Units
VO	bus voltage	V
V1	input voltage	BV
VC	bus capacitor state	V
VC1	input capacitor state	V
1R	ripple current in C1	A
1T	sum of four input currents	A
1LP	inductor current in LP	A
ILS	inductor current in LS	A

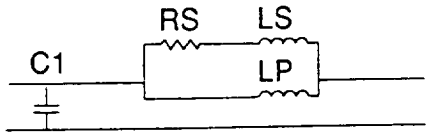
INPUTS

I1..I4	currents from 4 boost modules	A
IX	load current	A
C	bus capacitor	F
RC	bus capacitor ESR	ohm
C1	input capacitor	F
RC1	input capacitor ESR	ohm
LP	main inductor	H
LS	shunt inductor	H
RS	damping resistor	ohm

BX.MOD

Variant of BU.MOD without bus capacitor





OUTPUTS

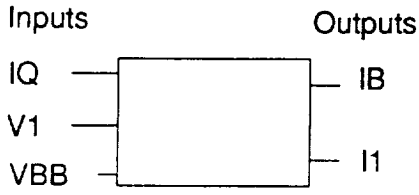
		Units
IX	load current	A
IXN	negative of IX	A
V1	input voltage	V
VC1	input capacitor state	V
IR	current ripple in C1	A
IT	sum of boost diode currents	A
ILP	current in inductor LP	A
ILS	current in LS-RS branch	A

INPUTS

I1..I4	currents from four boost modules	A
VO	bus voltage	V
R	load resistor	ohm
C1	filter capacitor	F
RC1	filter capacitor ESR	ohm
LP	filter inductor	H
LS	damping inductor	H
RS	damping resistor	ohm

CH.MOD

Buck charger converter



OUTPUTS

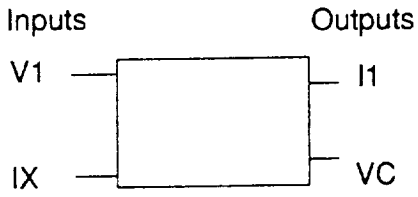
		Units
IB	Inductor current	A
I1	Input current	A
ID	Diode current	A
SWL	Inductor discontinuity switch state	-

INPUTS

V1	input voltage	V
VBB	load voltage	V
IQ	switch state	-
L	inductor	H
RS	inductor series resistance	ohm
RM	mosfet (switch) on resistance	ohm

CI.MOD

Bus capacitor and ESR



OUTPUTS

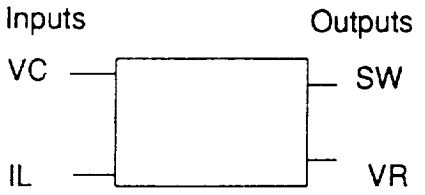
		Units
I1	input current	A
VC	capacitor voltage (state)	V

INPUTS

V1	input voltage	V
IX	load current	A
RC	Bus capacitor ESR	ohm
C	Bus capacitor	F

DD.MOD

PWM modulator with current sense



OUTPUTS

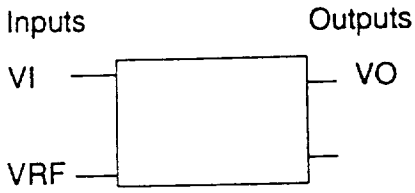
		Units
SW	switch signal	-
VCT	total voltage compared with ramp	V
VR	ramp with phase shift	V

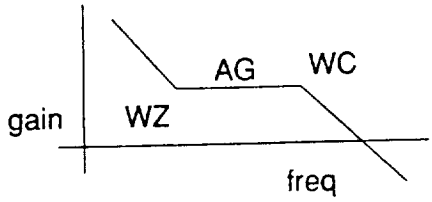
INPUTS

VC	voltage error signal	V
IL	sensed inductor current	A
XN	current transformer turns ratio	-
XK1	voltage gain	-
XK2	current gain (including current sense R)	R
ILP	peak current limit	A
DMX	max. duty ratio limit	-
TD	delay for ramp phase shift	sec
TS	period for internal ramp	sec
VP	peak amplitude of internal ramp	V
TX	simulation time at which switching ceases	sec

EI.MOD

Inverting integrator error amplifier with output clamps





OUTPUTS

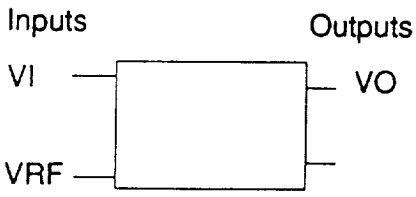
		Units
VO	output voltage	V
SW	saturation state	-
X	auxiliary state	V

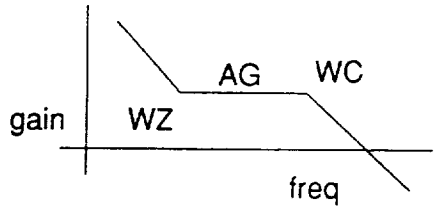
INPUTS

VI	input voltage	V
VRF	reference input	V
KV	factor for VI	-
AG	midband gain	-
WC	cutoff frequency	rad/s
VH	upper clamp for output voltage	V
VL	lower clamp for output voltage	V
WZ	zero frequency	rad/s

EM.MOD

Noninverting integrator error amplifier with output clamps





OUTPUTS

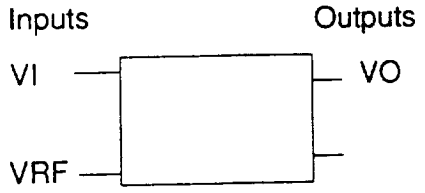
		Units
VO	output voltage	V
SW	saturation state	-
X	auxiliary state	V

INPUTS

VI	input voltage	V
VRF	reference input	V
KV	factor for VI	-
AG	midband gain	-
WC	cutoff frequency	rad/s
VH	upper clamp for output voltage	V
VL	lower clamp for output voltage	V
WZ	zero frequency	rad/s

EN.MOD

Inverting proportional error amplifier with output clamps



OUTPUTS

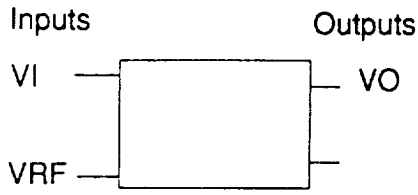
		Units
VO	output voltage	V
SW	saturation state	-

INPUTS

VI	input voltage	V
VRF	reference input	V
KV	factor for VI	-
AG	proportional gain	-
WGB	gain-bandwidth product of op-amp	rad/s
VH	upper clamp for output voltage	V
VL	lower clamp for output voltage	V

ET.MOD

Noninverting proportional error amplifier with output clamps



OUTPUTS

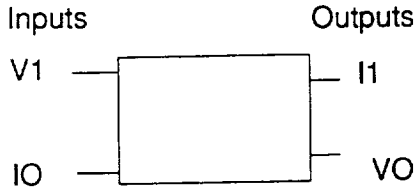
		Units
VO	output voltage	V
SW	saturation state	-

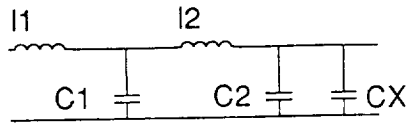
INPUTS

VI	input voltage	V
VRF	reference input	V
KV	factor for VI	-
AG	proportional gain	-
WGB	gain-bandwidth product of op-amp	rad/s
VH	upper clamp for output voltage	V
VL	lower clamp for output voltage	V

FD.MOD

Input filter for VFPPAT discharger





OUTPUTS

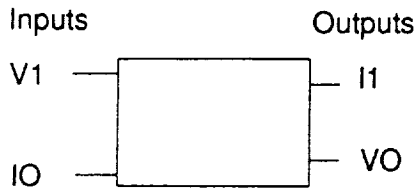
		Units
VO	output voltage	V
I1	input current	A
I2	L2 current	A
VC1	C1 voltage	V
VC2	C2 voltage	V
IR1	ripple current in C1	A
IR2	ripple current in C2	A

INPUTS

V1	input voltage	V
IO	output current	A
L1	series inductor	H
L2	series inductor	H
R1	L1 parasitic ESR	ohm
R2	L2 parasitic ESR	ohm
C1	parallel capacitor	F
C2	parallel capacitor	F
RC1	ESR for C1	ohm
RC2	ESR for C2	ohm
CX	aux capacitor for EASY5	F

FI.MOD

Input filter for charger



OUTPUTS

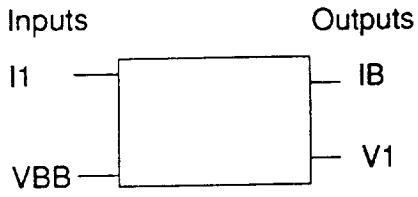
		Units
VO	output voltage	V
I1	input current	A
IL	inductor current	A
VC	capacitor state	V
VCF	damping capacitor voltage	V
IR	ripple current in filter capacitor	A
IRF	ripple current in damping capacitor	A

INPUTS

V1	input voltage	V
IO	output current to charger	A
L	series inductor	H
RL	series inductor ESR	ohm
C	filter capacitor	F
RC	filter capacitor ESR	ohm
CF	damping capacitor	F
RCF	damping resistor	ohm
C1	aux capacitor for EASY5	F

FX.MOD

Output filter for charger



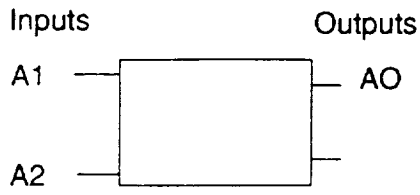
OUTPUTS		Units
IB	battery current	A
V1	input capacitor voltage	V
VC	capacitor voltage (state)	V

INPUTS

I1	input current from charger	A
VBB	battery voltage	V
L	filter inductor	H
C	filter capacitor	F
RC	filter capacitor ESR	ohm
C1	aux capacitor for EASY5	F

NV.MOD

Adder/inverter for two quantities



$$AO = K1*A1 + K2*A2$$

OUTPUTS

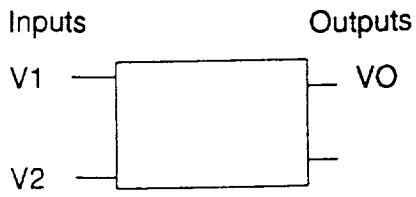
		Units
AO	output	

INPUTS

A1	first input	
A2	second input	
KV1	multiplier for A1	
KV2	multiplier for A2	

OR.MOD

OR gate to choose lesser of two values



OUTPUTS

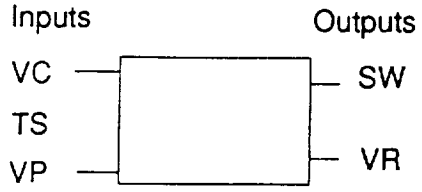
		Units
VO	output	

INPUTS

V1	first input	
V2	second input	
K1	multiplier for A1	
K2	multiplier for A2	

PM.MOD

PWM comparator with max. duty ratio limit



OUTPUTS

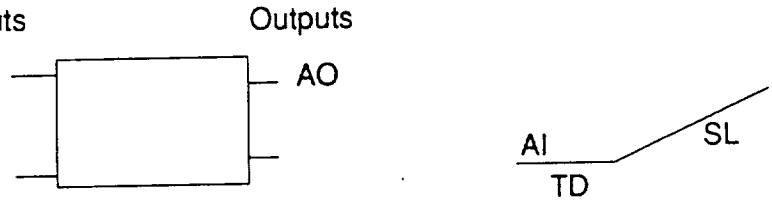
		Units
SW	switch state for charger	-
VR	PWM ramp	V

INPUTS

VC	control voltage	V
KV	multiplier for VC	-
DMX	maximum duty ratio limit	-
TS	period for internal ramp	sec
TP	amplitude of internal ramp	V

RX.MOD

General slope generator with delay



OUTPUTS

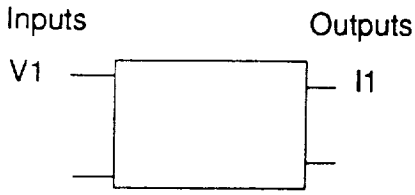
		Units
AO	output	

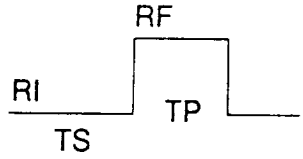
INPUTS

AI	initial value	
SL	slope	1/sec
TD	time for which value remains at AI	sec

RQ.MOD

Pulsed resistive load change





OUTPUTS

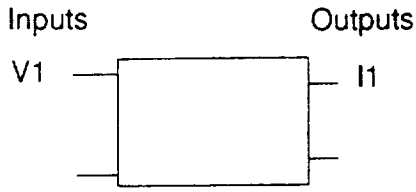
		Units
I1	current drawn by load	A

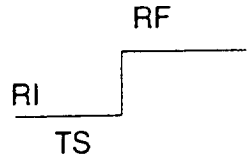
INPUTS

V1	voltage applied to load	V
RI	initial load resistance	ohm
RF	pulsed value of load resistance	ohm
TS	time after which value is pulsed	sec
TP	pulse duration	sec

RS.MOD

Step resistive load change





OUTPUTS

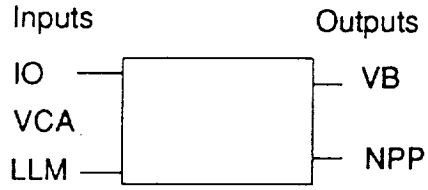
		Units
I1	current drawn by load	A

INPUTS

V1	voltage applied to load	V
RI	initial load resistance	ohm
RF	final load resistance	ohm
TS	time after which step is applied	sec

SA.MOD

Solar array, shunt switching unit and bus capacitor



OUTPUTS

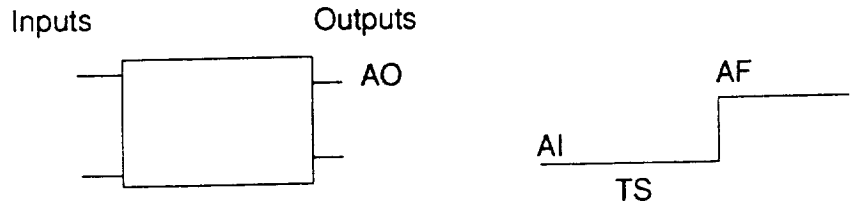
		Units
VB	bus voltage	V
NPP	number of strings connected to load	-
VR	ramp waveform	V
VC	bus capacitor state	V
D	PWM state (1=connected to bus)	-
NPX	number of switches (NPP/NPS)	-
NF	number of switches open	-

INPUTS

IO	load current	A
LLM	illumination level	-
VCA	control voltage	V
C	bus capacitor	F
RC	bus capacitor ESR	ohm
C1	aux capacitor for EASY5	f
NPS	strings per switch	-
VP	PWM ramp amplitude	v
TS	PWM switching period	sec
TA	ambient temperature	deg K

ST.MOD

Step generator



OUTPUTS

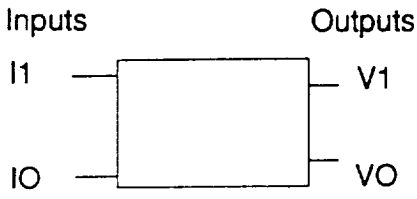
		Units
AO	output	

INPUTS

AI	initial value	
AF	final value	
TS	time at which value changes	sec

TP.MOD

Connecting cable model



OUTPUTS

		Units
V1	input voltage	V
VO	output voltage	V

INPUTS

I1	input current	A
I2	output current	A
C	half of cable capacitance	F
R	cable resistance	ohm
L	cable inductance	H

```
DEFINE MACRO = AD
************************************************************
*
* ADDER      IO = I1 + I2 + I3 + I4
* USED TO SUM INPUT CURRENTS FOR 4 MODULE BOOST
*
************************************************************
MACRO INPUTS = I1       I2
               I3       I4
************************************************************
MACRO OUTPUTS =  IO
* AO = OUTPUT
************************************************************
MACRO CODE
MACRO STOP SORT
C
      IO AD-- = I1 AD-- + I2 AD-- + I3 AD-- + I4 AD--
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, AD
END OF MODEL
PRINT
```

```
*************************************************************
*
* VOLTAGE FED PUSH PULL WITH TAPPED AUTOTRANSFORMER
* ALTERNATE DISCHARGER TOPOLOGY (VFPPAT)
*
*************************************************************
DEFINE MACRO = AT
*
MACRO INPUTS =   N        C1       V1
                 L        RC       IO
                 C        IQ       TS
*
* IQ1, IQ2 ARE SWITCH SIGNALS 1=ON
* C, C1 = BUS CAP
* IO = LOAD CURRENT STEP
* TS = SECONDARY SIDE PERIOD
*************************************************************
MACRO OUTPUTS =  VB       I1       IT1      ID2
                 VC       IS1      IT2      SWL
                 IL       IS2      ID1      IS
*
* VB = BUS VOLTAGE
* VC = BUS CAP STATE
* I1 = INPUT CURRENT DRAWN FROM BATTERY
* IL = INDUCTOR STATE
* ID = DIODE
* IS = SWITCH   IS=SUM OF IS1 AND IS2
* IT = WINDING CURRENTS
* SWL = SWITCH STATE FOR INDUCTOR (PREVENTS REVERSE CURRENT)
*************************************************************
MACRO CODE
MACRO STOP SORT
C
C CLOCK FOR 2*TS
C
C T VARIES FROM 0 TO 2
C
      TS = 2*TS AT--
      T = (TIME + TS)/TS
      T = T - IDINT(T)
      T = 2*T
C
      XN = N  AT--
C
      IF( T .LT. 1 .AND. IQ .GT. 0.5) THEN
         VD = (XN + 1.)*V1 AT--
         IS1AT-- = XN * IL AT--
         IS2AT-- = 0
         IT1AT-- = IS1AT--
         IT2AT-- = IL AT--
         I1 AT-- = (XN + 1 )*IL AT--
         ID1AT-- = 0
         ID2AT-- = IL AT--
      ELSEIF( T .GE. 1 .AND. IQ .GT. 0.5) THEN
         VD = (XN + 1.)*V1 AT--
         IS1AT-- = 0
         IS2AT-- = XN * IL AT--
         IT1AT-- = IL AT--
         IT2AT-- = IS2AT--
         I1 AT-- = (XN + 1 )*IL AT--
```

```
         ID1AT-- = IL AT--
         ID2AT-- = 0
      ELSE
         VD = V1 AT--
         IS1AT-- = 0
         IS2AT-- = 0
         IT1AT-- = IL AT-- /2
         IT2AT-- = IL AT-- /2
         I1 AT-- = IL AT--
         ID1AT-- = IL AT--/2
         ID2AT-- = IL AT--/2
      ENDIF
C
      IS AT-- = IS1AT-- + IS2AT--
C
C CLAMP INDUCTOR CURRENT POSITIVE
C
      DIL = VD - VB AT--
      IF (SWLAT-- .EQ. 0) THEN
         SWLDOT=0
         IF(DIL .GT. 0) SWLDOT=1
      ELSE
         SWLDOT=1
         IF(IL AT-- .LE. 0 .AND. DIL .LT. 0) SWLDOT=0
      ENDIF
C
C DERIVATIVES
C
      XRC = (VB AT-- - VC AT--)/RC AT--
      DC1 = (IL AT-- - XRC - IO AT--)/C1 AT--
C
MACRO SWITCH, SWLAT-- = SWLDOT
C
MACRO DERIVATIVE, VB AT-- = DC1
MACRO DERIVATIVE, VC AT-- = XRC/C  AT--
MACRO DERIVATIVE, IL AT-- = SWLDOT*DIL/L  AT--
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, AT
END OF MODEL
PRINT
```

```
*-------------------------------------------------------
*
* SINGLE BOOST CONVERTER MODULE
*
*-------------------------------------------------------
DEFINE MACRO = BT
*-------------------------------------------------------
MACRO INPUTS = IQ
               L       RL
               VI      VO
* IQ = SIGNAL FROM COMPARATOR DD
*      1 INDUCTOR CONNECTED TO GROUND
*      0 IL FLOWS TO LOAD
* VI = INPUT VOLTAGE (BATTERY)
* VO = OUTPUT VOLTAGE (FROM EXTERNAL COMMON CAPACITOR)
* L  = INDUCTOR
* RL = INDUCTOR SERIES PARASITIC RESISTANCE
*-------------------------------------------------------
MACRO OUTPUTS =  IO       IL
                 IS       SWL
* IL  = INDUCTOR CURRENT DRAWN FROM BATTERY  (A STATE)
* IO  = CURRENT FED TO OUTPUT CAP (NOT A STATE !)
* IS  = SWITCH CURRENT
* SWL = INDUCTOR DISCONTINUITY SWITCH STATE
*-------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
      XIL = IL BT--
      V1  = VI BT--
      RL  = RL BT--
C
C  INDUCTOR CONNECTED TO GROUND
C
      IF (IQ BT-- .GT. 0.5) THEN
         IS BT-- = IL BT--
         IO BT-- = 0.
         DIL = (V1 - RL*XIL )/ L  BT--
      ELSE
C
C  INDUCTOR CONNECTED TO LOAD
C
         IS BT-- = 0.
         IO BT-- = IL BT--
         DIL = (V1 - XIL*RL - VO BT--)/L  BT--
      ENDIF
C
C  IL (AND THEREFORE IO) IS ALWAYS POSITIVE
C
      IF (SWLBT-- .EQ. 0) THEN
        SWLDOT=0
        IF (DIL .GT. 0) SWLDOT=1
      ELSE
        SWLDOT=1
        IF (XIL .LE. 0 .AND. DIL .LT. 0 ) SWLDOT=0
      ENDIF
C
C     IF (XIL .LE. 0 .AND. DIL .LT. 0 ) DIL = 0.
C
MACRO SWITCH,     SWLBT-- = SWLDOT
```

```
MACRO DERIVATIVE, IL BT-- = DIL*SWLDOT
C
MACRO RESUME SORT
END OF MACRO
*-------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, BT
END OF MODEL
PRINT
```

```
*-------------------------------------------------------
*
* ADDER, OUTPUT FILTER AND BUS CAP FOR MULTI-MODULE BOOST
* BU.MOD
*
*-------------------------------------------------------
DEFINE MACRO = BU
*-------------------------------------------------------
MACRO INPUTS =  I1     I2     I3     I4
                IX
                RC     C      C1     RC1
                RS     LS     LP
* I1...I4 = INPUT CURRENTS FROM 4 BOOST MODULES
* IX LOAD CURRENT APPLIED EXTERNALLY
* C = BUS CAPACITOR
* RC = BUS CAPACITOR ESR
* C1 = PRIMARY CAPACITOR
* RC1 = PRIMARY CAPACITOR ESR
* RS, LS, LP = FILTER INDUCTOR COMPONENTS
*-------------------------------------------------------
MACRO OUTPUTS =  V1     VO
                 ILS    ILP    VC1   VC
                 IT     IR
*
* VOLTAGE (STATES)
* VO BUS VOLTAGE
* V1 BOOST SIDE VOLTAGE
* VC BUS CAP STATE
* VC1 PRIMARY CAP STATE
*
* IT TOTAL BOOST SIDE CURRENT (DIODES)
* IR INPUT CAPACITOR CURRENT RIPPLE
* ILS, ILP = INDUCTOR STATES
*-------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
C  ADDER
C
      IT BU-- = I1 BU--  + I2 BU-- + I3 BU-- + I4 BU--
C
C  AUX CAPS
C
      C2 = 0.05 * C1 BU--
      CB = 0.05 * C  BU--
C
C  RIPPLE CURRENT
C
      IR BU-- = (V1 BU-- - VC1BU--)/RC1BU--
      XRC     = (VO BU-- - VC BU--)/RC BU--
C
C  DIFFERENTIAL EQUATIONS
C
      DLS = (V1 BU-- - VO BU-- - RS BU--*ILSBU-- )/LS BU--
      DLP = (V1 BU-- - VO BU-- )/LP BU--
      DVC = XRC/C  BU--
      DV1 = (IT BU-- - IR BU-- - ILPBU-- - ILSBU-- )/C2
      DC1 = IR BU-- /C1 BU--
      DVO = (ILPBU-- + ILSBU-- -XRC -IX BU--)/CB
C
```

```
MACRO DERIVATIVE, ILSBU-- = DLS
MACRO DERIVATIVE, ILPBU-- = DLP
MACRO DERIVATIVE, VC BU-- = DVC
MACRO DERIVATIVE, V1 BU-- = DV1
MACRO DERIVATIVE, VC1BU-- = DC1
MACRO DERIVATIVE, VO BU-- = DVO
C
MACRO RESUME SORT
END OF MACRO
*-------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, BU
END OF MODEL
PRINT
```

```
*-------------------------------------------------------
*
* ADDER, OUTPUT FILTER, LOAD  FOR MULTI-MODULE BOOST
* BX.MOD
*
* VARIANT OF BU.MOD WITHOUT BUS CAPACITOR BUT WITH LOAD
* VO IS A MODEL INPUT !!
*-------------------------------------------------------
MACRO FILE NAME = MACROS
DEFINE MACRO = BX
MACRO INPUTS =  I1     I2     I3     I4
                VO     R
                C1     RC1
                RS     LS     LP
* I1...I4 = INPUT CURRENTS FROM 4 BOOST MODULES
* * VO VOLTAGE APPLIED EXTERNALLY * *
* R = MAIN LOAD RESISTOR
* C1 = PRIMARY CAPACITOR
* RC1 = PRIMARY CAPACITOR ESR
* RS, LS, LP = FILTER INDUCTOR COMPONENTS
*-------------------------------------------------------
MACRO OUTPUTS =  V1     IX     IXN
                 ILS    ILP    VC1
                 IT     IR
*
* IX CURRENT DRAWN INTO UNIT
* IXN -VE OF IX
* V1 BOOST SIDE VOLTAGE (STATE)
* VC1 PRIMARY CAP STATE
*
* IT TOTAL BOOST SIDE CURRENT
* IR INPUT CAPACITOR CURRENT RIPPLE
* ILS, ILP = INDUCTOR STATES
*-------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
C  ADDER
C
      IT BX-- = I1 BX--  + I2 BX-- + I3 BX-- + I4 BX--
C
      C2 = 0.05 * C1 BX--
C
C  CURRENT DRAWN INTO UNIT (THIS IS NOT LOAD CURRENT)
C
      IX BX-- =  VO BX--/R  BX-- - ILSBX-- - ILPBX--
      IXNBX-- =  - IX BX--
C
C  RIPPLE CURRENT
C
      IR BX-- = (V1 BX-- - VC1BX--)/RC1BX--
C
C  DIFFERENTIAL EQUATIONS
C
      DLS = (V1 BX-- - VO BX-- - RS BX--*ILSBX-- )/LS BX--
      DLP = (V1 BX-- - VO BX-- )/LP BX--
      DV1 = (IT BX-- - IR BX-- - ILPBX-- - ILSBX-- )/C2
      DC1 = IR BX-- /C1 BX--
C
MACRO DERIVATIVE, ILSBX-- = DLS
```

```
MACRO DERIVATIVE, ILPBX-- = DLP
MACRO DERIVATIVE, V1 BX-- = DV1
MACRO DERIVATIVE, VC1BX-- = DC1
C
MACRO RESUME SORT
END OF MACRO
*-------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, BX
END OF MODEL
PRINT
```

```
*-------------------------------------------------------
*
* CHARGER BUCK CONVERTER
*
* CH.MOD
*-------------------------------------------------------
DEFINE MACRO =   CH
*-------------------------------------------------------
MACRO INPUTS =   V1      VBB      IQ
                 L       RS       RM
*
* V1  = INPUT VOLTAGE (FROM FILTER)
* VBB = BATTERY OR LOAD SIDE VOLTAGE
* IQ  = SWITCH.  1=CONN. TO INPUT   0=FREEWHEELS
* RS  = SERIES RESISTANCE IN BATTERY CHARGING PATH
* RM  = MOSFET ON RESISTANCE
*-------------------------------------------------------
MACRO OUTPUTS =  IB      I1      ID       SWL
*
* IB = BATTERY CHARGE CURRENT (INDUCTOR STATE)
* I1 = INPUT CURRENT FROM FILTER
* ID = DIODE CURRENT
* SWL = INDUCTOR STATE 1=FORWARD CURRENT 0=REV CURRENT BLOCKED
*
*-------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
      V1  = V1 CH--
      VBB = VBBCH--
      XL  = L  CH--
      XIB = IB CH--
C
      RS = RS CH--
      RM = RM CH--
C
      IF (IQ CH-- .GT. 0.5 ) THEN
         I1 CH-- = IB CH--
         DIB = V1 - IB CH--*(RM+RS) - VBB
         ID CH-- = 0
      ELSE
         DIB = - IB CH-- * RS - VBB
         ID CH-- = IB CH--
         I1 CH-- = 0
      ENDIF
C
C CLAMP INDUCTOR CURRENT POSITIVE
C
C     IF (XIB .LE. 0 .AND. DIB .LT. 0 ) DIB = 0
      IF (SWLCH-- .EQ. 0) THEN
         SWLDOT = 0
         IF (DIB .GT. 0 ) SWLDOT = 1
      ELSE
         SWLDOT = 1
         IF( XIB .LE. 0 .AND. DIB .LT. 0 ) SWLDOT=0
      ENDIF
C
MACRO SWITCH,     SWLCH-- = SWLDOT
MACRO DERIVATIVE, IB CH-- = SWLDOT*DIB/XL
C
```

```
MACRO RESUME SORT
END OF MACRO
*-------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, CH
END OF MODEL
PRINT
```

```
*************************************************************
*
* BUS CAPACITOR
* TO BE USED WITH PI MODEL FOR CABLE
*
*************************************************************
DEFINE MACRO = CI
*************************************************************
MACRO INPUTS = C        IX
               RC       V1
* C  = BUS CAPACITOR
* RC = ESR
* V1 = BUS VOLTAGE
* IX = LOAD CURRENT OUT OF CAPACITOR
*************************************************************
MACRO OUTPUTS =  I1
                 VC
* I1 = INPUT CURRENT
* VC = BUS CAPACITOR STATE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      C  = C  CI--
      RC = RC CI--
      VO = V1 CI--
      VC = VC CI--
C
      XRC = (VO - VC)/RC
      I1 CI-- = XRC + IX CI--
C
MACRO DERIVATIVE, VC CI-- = XRC/C
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, CI
END OF MODEL
PRINT
```

```
*-------------------------------------------------------
*
* PWM MODULATOR FOR TWO-LOOP FEEDBACK WITH CURRENT SENSE
* INCLUDES CURRENT SENSE GAIN
*
*-------------------------------------------------------
MACRO FILE NAME = MACROS
DEFINE MACRO = DD
*-------------------------------------------------------
MACRO INPUTS = VC          IL          ILP
               VP          TS          TD          DMX
               XN          XK1         XK2         TX
* IL = INDUCTOR CURRENT
* ILP = INDUCTOR PEAK CURRENT LIMIT
* VC = CONTROL VOLTAGE FROM VOLTAGE ERROR AMPLIFIER
* VP = PEAK OF AUXILIARY RAMP
* TS = SWITCHING PERIOD FOR RAMP
* TD = DELAY FOR PHASE SHIFTED RAMP (SPECIFY LESS THAN TS !)
* TX = TIME AT WHICH SWITCHING IS DISABLED (TO TEST EFFECT OF
*      MODULE FAILURE)
* XN = TURNS RATIO OF CURRENT PICKUP TRANSFORMER (1:XN)
* XK1= VOLTAGE GAIN CONSTANT
* XK2= CURRENT GAIN CONSTANT
* DMX= MAX D LIMIT (SPECIFY GREATER THAN 0.2 !)
*-------------------------------------------------------
MACRO OUTPUTS =  SW        VR       VCT
* SW  = 1 OVER DURATION D.TS   SW = 0 OVER DURATION D'.TS
* VR  = AUXILIARY RAMP
* VCT = TOTAL CONTROL VTG BEING COMPARED WITH RAMP
*-------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
C GENERATION OF RAMP VR WITH DELAY TD AND PEAK VP
C
C T INCREASES FROM 0 TO 1 OVER PERIOD TS
C
      TS = TS DD--
      TD = TD DD--
      T = (TIME + TS )/TS
      T = T - IDINT(T)
      X = TD/TS
      T = T - X + 1E-9
      IF (T .LT. 0) T = T + 1.
C
      VP = VP DD--
      VR = T*VP
      VR DD-- = VR
C
C ERROR VOLTAGE AND CURRENT SIGNAL
C
      VI = - IL DD--/XN DD--
      VCT = XK1DD-- *VC DD-- + XK2DD-- *VI
      VCTDD-- = VCT
C
C COMPARATOR : THIS ALLOWS ONLY ONE ON/OFF OPERATION PER CYCLE
C
      DMAX = DMXDD--
      XILP = ILPDD--
      XIL  = IL DD--
```

```
      IF (SW DD-- .EQ. 1) THEN
         SWDOT = 1
         IF (VR .GE. VCT) SWDOT = 0
         IF (T  .GT. DMAX ) SWDOT=0
         IF (XIL .GT. XILP  ) SWDOT=0
         IF (TIME .GT. TX DD--) SWDOT=0
      ELSE
         SWDOT = 0
C         IF ( T .LT. 0.1 .AND. XIL .LE. XILP ) SWDOT=1
       IF (T .LT. 0.1 .AND. XIL .LE. XILP .AND. VR .LT. VCT)SWDOT=1
      ENDIF
C
MACRO SWITCH, SW DD-- = SWDOT
C
MACRO RESUME SORT
END OF MACRO
*-----------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, DD
END OF MODEL
PRINT
```

```
*************************************************************
*
* INVERTING INTEGRATOR ERROR AMPLIFIER WITH CLAMPS
* EI.MOD
*
*************************************************************
DEFINE MACRO = EI
*************************************************************
MACRO INPUTS = VI       VRF
               AG       WC       WZ      KV
               VH       VL
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR BY WHICH VI IS REDUCED (INPUT POT. DIVIDER)
* VRF = REFERENCE VOLTAGE
* VH  = CLAMP ON UPPER LIMIT OF VO
* VL  = CLAMP ON LOWER LIMIT OF VO
* WC  = CUTOFF FREQUENCY
* WZ  = ZERO FREQUENCY
* AG  = MIDBAND GAIN
*************************************************************
MACRO OUTPUTS =  VO
                 SW
                 X
*
* VO = OUTPUT VOLTAGE
* SW = SWITCH STATE OF OP-AMP (0=LINEAR, -1,+1, = SATURATED)
* X  = AUXILIARY STATE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      DV = VRFEI--  - KV EI-- * VI EI--
      WC = WC EI--
      WZ = WZ EI--
      AG = AG EI--
      VH  = VH EI--
      VL  = VL EI--
      VO  = VO EI--
C
      GK = AG * WC
      DXS = 0.0
      DXN = GK*(WZ - WC)*DV - X  EI-- * WC
      DVN = GK*DV + X  EI--
C
      IF (SW EI-- .EQ. 1) THEN
          SWDOT = 1
          IF (DV .LE. 0 ) SWDOT = 0
      ELSEIF (SW EI-- .EQ. -1) THEN
          SWDOT = -1
          IF (DV .GE. 0 ) SWDOT=0
      ELSE
          SWDOT = 0
          IF (VO .GT. VH .AND. DV .GT. 0) SWDOT = 1
          IF (VO .LT. VL .AND. DV .LT. 0) SWDOT = -1
      ENDIF
C
MACRO SWITCH, SW EI-- = SWDOT
C
      IF (SW EI-- .EQ. 1) THEN
         DVO = DXS
```

```
         DX  = DXS
      ELSEIF (SW EI-- .EQ. -1) THEN
         DVO = DXS
         DX  = DXS
      ELSE
         DVO = DVN
         DX  = DXN
      ENDIF
C
MACRO DERIVATIVE, X  EI-- = DX
MACRO DERIVATIVE, VO EI-- = DVO
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, EI
END OF MODEL
PRINT
```

```
*************************************************************
*
* NON INVERTING INTEGRATOR ERROR AMPLIFIER WITH CLAMPS
* EM.MOD
*
*************************************************************
DEFINE MACRO = EM
*************************************************************
MACRO INPUTS = VI       VRF
               AG       WC       WZ      KV
               VH       VL
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR BY WHICH VI IS REDUCED (INPUT POT. DIVIDER)
* VRF = REFERENCE VOLTAGE
* VH  = CLAMP ON UPPER LIMIT OF VO
* VL  = CLAMP ON LOWER LIMIT OF VO
* WC  = CUTOFF FREQUENCY
* WZ  = ZERO FREQUENCY
* AG  = MIDBAND GAIN
*************************************************************
MACRO OUTPUTS =  VO
                 SW
                 X
*
* VO = OUTPUT VOLTAGE
* SW = SWITCH STATE OF OP-AMP (0=LINEAR, -1,+1, = SATURATED)
* X  = AUXILIARY STATE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      DV = - VRFEM--  + KV EM-- * VI EM--
      WC = WC EM--
      WZ = WZ EM--
      AG = AG EM--
      VH  = VH EM--
      VL  = VL EM--
      VO  = VO EM--
C
      GK = AG * WC
      DXS = 0.0
      DXN = GK*(WZ - WC)*DV - X  EM-- * WC
      DVN = GK*DV + X  EM--
C
      IF (SW EM-- .EQ. 1) THEN
          SWDOT = 1
          IF (DV .LE. 0 ) SWDOT = 0
      ELSEIF (SW EM-- .EQ. -1) THEN
          SWDOT = -1
          IF (DV .GE. 0 ) SWDOT=0
      ELSE
          SWDOT = 0
          IF (VO .GT. VH .AND. DV .GT. 0) SWDOT = 1
          IF (VO .LT. VL .AND. DV .LT. 0) SWDOT = -1
      ENDIF
C
MACRO SWITCH, SW EM-- = SWDOT
C
      IF (SW EM-- .EQ. 1) THEN
         DVO = DXS
```

```
         DX  = DXS
      ELSEIF (SW EM-- .EQ. -1) THEN
         DVO = DXS
         DX  = DXS
      ELSE
         DVO = DVN
         DX  = DXN
      ENDIF
C
MACRO DERIVATIVE, X  EM-- = DX
MACRO DERIVATIVE, VO EM-- = DVO
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, EM
END OF MODEL
PRINT
```

```
*************************************************************
*
* INVERTING PROPORTIONAL ERROR AMPLIFIER   EN.MOD
* (INVERTING VERSION OF ET.MOD)
*
*************************************************************
DEFINE MACRO = EN
*************************************************************
MACRO INPUTS = VI       VRF     KV
               AG       WGB
               VH       VL
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR FOR VI (INPUT POT. DIVIDER)
* VRF = REFERENCE VOLTAGE
* VH  = CLAMP ON UPPER LIMIT OF VO
* VL  = CLAMP ON LOWER LIMIT OF VO
* WGB = GAIN-BANDWIDTH PRODUCT OF OP-AMP
* AG  = PROPORTIONAL GAIN
*************************************************************
MACRO OUTPUTS =  VO
                 SW
*
* VO = OUTPUT VOLTAGE
* SW = SWITCH STATE OF OP-AMP (0=LINEAR, þ1=SATURATED)
*************************************************************
MACRO CODE
MACRO STOP SORT
C
C  ERROR VOLTAGE AND CONTROL VOLTAGE CLAMP LIMITS
C
      DV = VRFEN-- - KV EN-- *VI EN--
      VH  = VH EN--
      VL  = VL EN--
      VO = VO EN--
      AG = AG EN--
C
      WC = WGBEN--/AG
      DXS = 0.0
      DXN = WC*AG*DV - VO*WC
C
      IF (SW EN-- .EQ. 1) THEN
          SWDOT = 1
          IF (DV .LE. 0 ) SWDOT = 0
      ELSEIF (SW EN-- .EQ. -1) THEN
          SWDOT = -1
          IF (DV .GE. 0 ) SWDOT=0
      ELSE
          SWDOT = 0
          IF (VO .GT. VH .AND. DV .GT. 0) SWDOT = 1
          IF (VO .LT. VL .AND. DV .LT. 0) SWDOT = -1
      ENDIF
C
MACRO SWITCH, SW EN-- = SWDOT
C
      IF (SW EN-- .EQ. 1) THEN
         DVO = DXS
      ELSEIF (SW EN-- .EQ. -1) THEN
         DVO = DXS
      ELSE
         DVO = DXN
```

```
      ENDIF
C
MACRO DERIVATIVE, VO EN-- = DVO
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, EN
END OF MODEL
PRINT
```

```
*************************************************************
*
* NON INVERTING PROPORTIONAL ERROR AMPLIFIER   ET.MOD
*
*************************************************************
DEFINE MACRO = ET
*************************************************************
MACRO INPUTS = VI       VRF      KV
               AG       WGB
               VH       VL
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR FOR VI (INPUT POT. DIVIDER)
* VRF = REFERENCE VOLTAGE
* VH  = CLAMP ON UPPER LIMIT OF VO
* VL  = CLAMP ON LOWER LIMIT OF VO
* WGB = GAIN BANDWIDTH PRODUCT OF OP AMP
* AG  = PROPORTIONAL GAIN
*************************************************************
MACRO OUTPUTS =  VO
                 SW
*
* VO = OUTPUT VOLTAGE
* SW = SWITCH STATE OF OP-AMP (0=LINEAR, þ1=SATURATED)
*************************************************************
MACRO CODE
MACRO STOP SORT
C
C  ERROR VOLTAGE AND CONTROL VOLTAGE CLAMP LIMITS
C
      DV = VI ET--* KV ET--   -  VRFET--
      VH  = VH ET--
      VL  = VL ET--
      VO = VO ET--
      AG = AG ET--
      WC = WGBET--/AG
C
      DXS = 0.0
      DXN = WC*AG*DV - VO*WC
C
      IF (SW ET-- .EQ. 1) THEN
          SWDOT = 1
          IF (DV .LE. 0 ) SWDOT = 0
      ELSEIF (SW ET-- .EQ. -1) THEN
          SWDOT = -1
          IF (DV .GE. 0 ) SWDOT=0
      ELSE
          SWDOT = 0
          IF (VO .GT. VH .AND. DV .GT. 0) SWDOT = 1
          IF (VO .LT. VL .AND. DV .LT. 0) SWDOT = -1
      ENDIF
C
MACRO SWITCH, SW ET-- = SWDOT
C
      IF (SW ET-- .EQ. 1) THEN
         DVO = DXS
      ELSEIF (SW ET-- .EQ. -1) THEN
         DVO = DXS
      ELSE
         DVO = DXN
      ENDIF
```

```
C
MACRO DERIVATIVE, VO ET-- = DVO
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, ET
END OF MODEL
PRINT
```

```
************************************************************
*
* INPUT TWO STAGE FILTER FOR VFPPAT DISCHARGER
*
************************************************************
DEFINE MACRO = FD
MACRO INPUTS = V1       IO
               L1       L2       C1      C2       CX
               R1       R2       RC1     RC2
* V1  = INPUT VOLTAGE (BUS)
* IO  = OUTPUT CURRENT (DRAWN BY DISCHARGER)
* L1, L2  = FILTER INDUCTORS
* R1, R2  = FILTER INDUCTOR ESR'S
* C1, C2  = FILTER CAPACITORS
* RC1, RC2  = FILTER CAPACITOR ESR'S
* CX  = AUX OUTPUT CAP TO GET STATE
************************************************************
MACRO OUTPUTS =  I1       I2      VC1     VC2      VO
                 IR1      IR2
*
* I1  = INPUT CURRENT (L1 INDUCTOR STATE)
* VO  = OUTPUT VOLTAGE (CX STATE)
* VC1, VC2  = FILTER CAP STATES
* I2  = 2ND INDUCTOR CURRENT STATE
* IR1 = RIPPLE CURRENT IST FILTER CAP
* IR2 = RIPPLE CURRENT 2ND FILTER CAP
************************************************************
MACRO CODE
MACRO STOP SORT
C
      XL1 = L1 FD--
      XL2 = L2 FD--
      R1  = R1 FD--
      R2  = R2 FD--
      CX  = CX FD--
      C1  = C1 FD--
      C2  = C2 FD--
      RC1 = RC1FD--
      RC2 = RC2FD--
      XIO = IO FD--
      V1  = V1 FD--
C
      XI1 = I1 FD--
      XI2 = I2 FD--
      VC1 = VC1FD--
      VC2 = VC2FD--
      VO  = VO FD--
C
C RIPPLE CURRENTS
C
      XRF1 = XI1 - XI2
      XRF2 = (VO - VC2)/RC2
      XRX  = XI2 - XIO - XRF2
      VM   = VC1 + XRF1*R1
C
MACRO DERIVATIVE, I1 FD-- = (V1 - VM - R1*XI1)/XL1
MACRO DERIVATIVE, I2 FD-- = (VM - VO - R2*XI2)/XL2
MACRO DERIVATIVE, VC1FD-- = XRF1/C1
MACRO DERIVATIVE, VC2FD-- = XRF2/C2
MACRO DERIVATIVE, VO FD-- = XRX/CX
```

```
C
MACRO RESUME SORT
END OF MACRO
*****************************************************************
MODEL DESCRIPTION
LOCATION = 20, FD
END OF MODEL
PRINT
```

```
************************************************************
*
* INPUT L C FILTER FOR BUCK CHARGER
*
************************************************************
DEFINE MACRO = FI
MACRO INPUTS = V1       IO
               L        C        CF      C1
               RL       RC       RCF
* V1  = INPUT VOLTAGE (BUS)
* IO  = LOAD CURRENT (DRAWN BY CHARGER)
* L   = INDUCTOR
* RL  = INDUCTOR ESR
* C   = FILTER CAPACITOR
* RC  = FILTER CAPACITOR ESR
* CF  = DAMPING CAPACITOR
* RCF = DAMPING CAPACITOR  RESISTOR (ESR)
* C1  = SMALL AUX CAP FOR EASY5 PURPOSES
************************************************************
MACRO OUTPUTS =  IL       VO      VC      VCF
                 I1       IR      IRF
*
* IL  = SERIES INDUCTOR CURRENT, STATE
* VO  = FILTER CAPACITOR VOLTAGE (INPUT TO CHARGER), STATE
* VC  = MAIN FIL. CAPACITOR VOLTAGE, STATE
* VCF = DAMPING FIL. CAPACITOR VOLTAGE, STATE
* IR  = RIPPLE CURRENT IN MAIN FILTER CAP ESR (NOT A STATE)
* IRF = RIPPLE CURRENT IN MAIN FILTER CAP ESR (NOT A STATE)
************************************************************
MACRO CODE
MACRO STOP SORT
C
      RC  = RC FI--
      RCF = RCFFI--
      RL  = RL FI--
      XL  = L  FI--
      C   = C  FI--
      C1  = C1 FI--
      CF  = CF FI--
C
      XIL = IL FI--
      VC  = VC FI--
      VO  = VO FI--
      VCF = VCFFI--
C
      XIO = IO FI--
      V1  = V1 FI--
C
C RIPPLE CURRENTS
C
      IR FI-- = (VO FI-- - VC FI--)/RC
      IRFFI-- = (VO FI-- - VCFFI--)/RCF
      XIR  = IR FI--
      XIRF = IRFFI--
C
C INPUT CURRENT
C
      I1 FI-- = IL FI--
C
MACRO DERIVATIVE, IL FI-- = (V1 - - XIL*RL - VO FI-- )/XL
```

```
MACRO DERIVATIVE, VCFFI-- = XIRF/CF
MACRO DERIVATIVE, VO FI-- = (IL FI-- - XIO - XIR - XIRF) /C1
MACRO DERIVATIVE, VC FI-- = XIR/C
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, FI
END OF MODEL
PRINT
```

```
************************************************************
*
* PULSED RESISTIVE LOAD CHANGE
*
************************************************************
DEFINE MACRO = RQ
************************************************************
MACRO INPUTS = RI        TS       V1
               RF        TP
* RI = INITIAL RESISTANCE
* RF = PULSED RESISTANCE
* TS = TIME AT WHICH STEP IS APPLIED
* TP = DURATION FOR WHICH IT REMAINS AT RF
* V1 = APPLIED VOLTAGE
************************************************************
MACRO OUTPUTS =  I1
* I1 = CURRENT DRAWN
************************************************************
MACRO CODE
MACRO STOP SORT
C
      TS = TS RQ--
      TX = TS RQ-- + TP RQ--
C
      IF (TIME .LT. TS .OR. TIME .GT. TX ) THEN
         R = RI RQ--
      ELSE
         R = RF RQ--
      ENDIF
C
      I1 RQ-- = V1 RQ--/R
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, RQ
END OF MODEL
PRINT
```

```
*************************************************************
*
* OUTPUT FILTER FOR CHARGER
*
*************************************************************
DEFINE MACRO = FX
MACRO INPUTS = I1      VBB
               C1      RC      L       C       RL
* I1 = INDUCTOR CURRENT FROM CHARGER
* VBB= BATTERY VOLTAGE
* L  = FILTER (SECOND) INDUCTOR
* C  = INPUT FILTER CAPACITOR
* C1 = AUX CAP FOR C
* RL = RESISTOR IN SERIES WITH BATTERY
* RC = CAPACITOR ESR
*************************************************************
MACRO OUTPUTS =  V1
                 IB
                 VC
* IB = FILTERED BATTERY CURRENT
* IB = FILTERED BATTERY CURRENT
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      V1  = V1 FX--
      XIB = IB FX--
      XL  = L  FX--
      C   = C  FX--
      XIN = I1 FX--
      VBB = VBBFX--
      C1  = C1 FX--
      RC  = RC FX--
      RL  = RL FX--
      XRC = (V1 - VC FX--)/RC
C
MACRO DERIVATIVE, VC FX-- = XRC/C
MACRO DERIVATIVE, IB FX-- = (V1 - VBB - XIB*RL )/XL
MACRO DERIVATIVE, V1 FX-- = (XIN - XIB -XRC)/C1
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, FX
END OF MODEL
PRINT
```

```
************************************************************
*
* ADDER / INVERTER FOR TWO QUANTITIES  AO = KV1.A1 + KV2.A2
*
************************************************************
DEFINE MACRO = NV
MACRO INPUTS = A1       A2
               KV1      KV2

* A'S = INPUTS
* KV = SET TO -1  FOR INVERSION
************************************************************
MACRO OUTPUTS =  AO
* AO = OUTPUT
************************************************************
MACRO CODE
MACRO STOP SORT
C
      AO NV-- = KV1NV-- * A1 NV-- + KV2NV-- * A2 NV--
C
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, NV
END OF MODEL
PRINT
```

```
*****************************************************************
*
* OR GATE TO SELECT LESSR OF TWO VALUES
* OR'S K1*V1 WITH K2*V2
*
*****************************************************************
DEFINE MACRO = OR
*****************************************************************
MACRO INPUTS = V1    K1
               V2    K2
* V1, V2 = INPUTS
* K'S = MULTIPLIERS FOR V1 AND V2
*****************************************************************
MACRO OUTPUTS =  VO
* VO = OUTPUT
*****************************************************************
MACRO CODE
MACRO STOP SORT
C
      V1 = K1 OR-- * V1 OR--
      V2 = K2 OR-- * V2 OR--
      IF (V1 .LT. V2 ) THEN
         VO OR-- = V1
      ELSE
         VO OR-- = V2
      ENDIF
C
MACRO RESUME SORT
END OF MACRO
*****************************************************************
MODEL DESCRIPTION
LOCATION = 20, OR
END OF MODEL
PRINT
```

```
*---------------------------------------------------------
*
* PWM COMPARATOR WITH MAX DUTY RATIO LIMIT - NO CURRENT SENSE
* BUILT IN RAMP
*
*---------------------------------------------------------
DEFINE MACRO = PM
*---------------------------------------------------------
MACRO INPUTS = VC          TS        DMX
               VP          KV
* VC = CONTROL VOLTAGE FROM VOLTAGE ERROR AMPLIFIER
* VP = PEAK OF AUXILIARY RAMP
* TS = SWITCHING PERIOD FOR RAMP
* DMX= MAX D LIMIT
* KV = KV*VC IS USED (USE KV TO INVERT SIGN OF VC WHEREVER REQD)
*      RAMP VR IS ALWAYS POSITIVE
*---------------------------------------------------------
MACRO OUTPUTS =  SW
                 VR
* SW  = 1 OVER DURATION D.TS     (KV*VC > RAMP)
*     = 0 OVER DURATION D'.TS    (KV*VC < RAMP)
* VR  = RAMP
*---------------------------------------------------------
MACRO CODE
MACRO STOP SORT
C
C GENERATION OF RAMP
C
C T INCREASES FROM 0 TO 1 OVER TS
C
      TS = TS PM--
      TD = 0
      T = (TIME + TS )/TS
      T = T - IDINT(T)
      X = TD/TS
      T = T - X + 1E-9
      IF (T .LT. 0) T = T + 1.
C
      VP = VP PM--
      VR = T*VP
      VR PM-- = VR
C
C ERROR VOLTAGE VCT
C
      VCT = KV PM-- * VC PM--
C
C COMPARATOR : THIS ALLOWS ONLY ONE ON/OFF OPERATION PER CYCLE
C
      DMAX = DMXPM--
      IF (SW PM-- .EQ. 1) THEN
         SWDOT = 1
         IF (VR .GE. VCT) SWDOT = 0
         IF (T  .GT. DMAX ) SWDOT=0
      ELSE
         SWDOT = 0
         IF (T .LT. 0.1 .AND. VR .LT. VCT) SWDOT=1
      ENDIF
C
MACRO SWITCH, SW PM-- = SWDOT
C
```

```
MACRO RESUME SORT
END OF MACRO
*-------------------------------------------------------
MODEL DESCRIPTION
LOCATION = 20, PM
END OF MODEL
PRINT
```

```
DEFINE MACRO = RX
*************************************************************
*
* GENERAL SLOPE GENERATOR
*
*************************************************************
MACRO INPUTS = TD
               AI
               SL
* AI = INITIAL VALUE
* TD = TIME AT WHICH SLOPE IS APPLIED
* SL = SLOPE (+VE FOR INCREASE)
*************************************************************
MACRO OUTPUTS =  AO
* OUTPUT
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      IF (TIME .LT. TD RX--) THEN
         AO RX-- = AI RX--
      ELSE
         AO RX-- = AI RX-- + SL RX--*(TIME - TD RX--)
      ENDIF
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, RX
END OF MODEL
PRINT
```

```
*************************************************************
*
* PULSED RESISTIVE LOAD CHANGE
*
*************************************************************
DEFINE MACRO = RQ
*************************************************************
MACRO INPUTS = RI        TS       V1
               RF        TP
* RI = INITIAL RESISTANCE
* RF = PULSED RESISTANCE
* TS = TIME AT WHICH STEP IS APPLIED
* TP = DURATION FOR WHICH IT REMAINS AT RF
* V1 = APPLIED VOLTAGE
*************************************************************
MACRO OUTPUTS =  I1
* I1 = CURRENT DRAWN
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      TS = TS RQ--
      TX = TS RQ-- + TP RQ--
C
      IF (TIME .LT. TS .OR. TIME .GT. TX ) THEN
         R = RI RQ--
      ELSE
         R = RF RQ--
      ENDIF
C
      I1 RQ-- = V1 RQ--/R
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, RQ
END OF MODEL
PRINT
```

```
*************************************************************
*
* RESISTIVE LOAD STEP CHANGE WITH OPTIONAL CURRENT STEP
*
*************************************************************
DEFINE MACRO = RS
*************************************************************
MACRO INPUTS = RI
               RF
               IX
               V1
               TS
* BOTH IX AND R CHANGE AT TIME TS
*    INITIALLY,      IX=0    R = RI
*    AFTER TIME TS,  IX=IX   R = RF
* V1 = VOLTAGE APPLIED TO LOAD
*
* THIS CAN BE USED TO APPLY EITHER IX OR R STEP BY SUITABLY
*  CHOOSING RI, RF, AND IX
*
* PROVIDE VOLTAGE FEED AT INPUT
*************************************************************
MACRO OUTPUTS =  I1
* I1 = CURRENT DRAWN BY R
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      IF (TIME .LT. TS RS--) THEN
         XI = 0
         R  = RI RS--
      ELSE
         XI = IX RS--
         R  = RF RS--
      ENDIF
C
      I1 RS-- = V1 RS--/R   + XI
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, RS
END OF MODEL
PRINT
```

```
************************************************************
*
* SOLAR ARRAY, SHUNT SWITCHING UNIT AND BUS CAPACITOR
*
************************************************************
DEFINE MACRO = SA
MACRO INPUTS = IO       LLM     VCA
               C1       C       RC
               TS       VP
               NPS      TA
* IO  = OUTPUT CURRENT
* C1  = AUX CAP
* C   = BUS CAP
* RC  = BUS CAP ESR
* LLM = ILLUMINATION LEVEL
* TS  = TIME AT WHICH STEP IS APPLIED
* VP  = RAMP AMPLITUDE
* VCA = CONTROL VOLTAGE
* NPS = STRINGS PER SET (CONNECTED TO ONE SWITCH)
* TA  = ACTUAL TEMPERATURE OF ARRAY IN DEG K
************************************************************
MACRO OUTPUTS =  VB        VC
                 NPP
                 VR
                 NF        D
                 NPX
* VB = BUS VOLTAGE
* VC = BUS CAPACITOR STATE
* VR = RAMP WAVEFORM
* NPP= NUMBER OF PARALLEL STRINGS (PWM + FIXED)
* NPX= NPP/NPS (AS SETS)
* NF = STEADILY SWITCHED PART OF NPP (FIXED)
* D  = 1    IF PWM SET IS CONNECTED TO BUS
************************************************************
MACRO CODE
MACRO STOP SORT
C
C SOLAR ARRAY PARAMETERS
C
      XIG = .14115
      RS  = .42
      RP  = 250.
      XIO = 4.1869E-11
      XKO = 39.8
C
C TOTAL CELLS IN SERIES AND TOTAL NO. OF STRINGS IN ARRAY
C
      XNS = 318.
      XNP = 315.
C
C ALL PARAMETERS ARE FOR ONE SOLAR CELL
C
C XIG = LIGHT GENERATED CURRENT AT TN FOR LLM=1
C RS  = SERIES RESISTANCE
C RP  = SHUNT RESISTANCE
C XIO = REVERSE SATURATION CURRENT OF SOLAR ARRAY DIODE
C XKO = q/AkT (CONSTANT)    T=301 K
C
C ILLUMINATION CHANGE
C
```

```
      XIG = XIG * LLMSA--
C
C TEMPERATURE CHANGE OF VB TO TN
C
      VBC = VB SA-- /XNS
      FC = 8E-5
      FV = -2E-3
      TN = 301.
      DT = TA SA--  - TN
      VBC = VBC - (FV + FC*RS )*DT
C
C GIVEN V, TO FIND THE CURRENT PER CELL X1 -----------------
C
      V = VBC
      X1 = 1.1* XIG
         DO +++4 J=1,30
         F1 = V + X1*RS
         EX = DEXP( XKO*F1 )
         F = X1 - XIG + XIO*EX + F1/RP
         DF = 1. + RS/RP + XIO*EX*XKO
         X1P = X1
         X1 = X1 - F/DF
         IF (DABS(X1P - X1) .LT. 1E-4) GOTO +++5
+++4     CONTINUE
C ---------------------------------------------------------
+++5  CONTINUE
C
C TEMPERATURE CHANGE OF X1 TO TA
C
      X1 = X1 + FC * DT
C
C RAMP GENERATION
C
      TS = TS SA--
      T = (TIME + TS)/TS
      T = T - IDINT(T)
      VR = VP SA-- *T
      VR SA-- = VR
C
C COMPARATOR
C
C GENERATION OF D
C
      VCA = VCASA--
      VP = VP SA--
C
      IF (VCA .LE. 0) THEN
         NF SA-- = 0
         D  SA-- = 0.
         GOTO +++9
      ENDIF
C
      NF = IDINT(VCA/VP)
      VCE = VCA - NF * VP
      NF SA-- = NF
C
      IF (T .LT. 0.1 ) D  SA-- = 1
      IF (VCE .LT. VR .AND. D  SA-- .GT. 0.5 ) D  SA-- = 0
C
+++9  CONTINUE
```

```
C
C  NPP AND TOTAL CURRENT
C
      NPPSA-- = NF SA--*NPSSA--    + NPSSA-- * D  SA--
      IF (NPPSA-- .GE.  XNP) NPPSA-- = XNP
      NPXSA-- = NPPSA--/NPSSA--
      XI = NPPSA-- *X1
C
C DIFFERENTIAL EQUATIONS ---------------------------------
C
      XIC = (VB SA-- - VC SA--)/RC SA--
C
MACRO DERIVATIVE, VB SA-- = (XI - IO SA-- - XIC)/C1 SA--
MACRO DERIVATIVE, VC SA-- = XIC/C  SA--
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, SA
END OF MODEL
PRINT
```

```
************************************************************
*
* STEP GENERATOR
*
************************************************************
DEFINE MACRO = ST
MACRO INPUTS = AI
               AF
               TS
* AI = INITIAL VALUE
* AF = FINAL   VALUE
* TS = TIME AT WHICH STEP IS APPLIED
************************************************************
MACRO OUTPUTS =  AO
* OUTPUT
************************************************************
MACRO CODE
MACRO STOP SORT
C
      IF (TIME .LT. TS ST--) THEN
         AO ST-- = AI ST--
      ELSE
         AO ST-- = AF ST--
      ENDIF
C
C
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, ST
END OF MODEL
PRINT
```

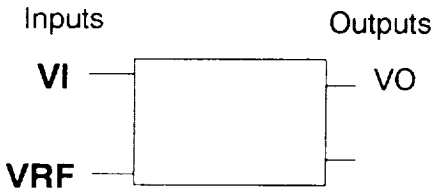
```
************************************************************
*
* LUMPED PI MODEL FOR CABLE     --L-R---
*                               C      C
*                               --------
************************************************************
DEFINE MACRO = TP
************************************************************
MACRO INPUTS = L       I1
               C       IO
               R
* L  = INDUCTANCE PER SEGMENT
* C  = SHUNT CAPACITOR
* R  = RESISTANCE PER SEGMENT
* I1 = INPUT CURRENT
* IO = OUTPUT CURRENT
************************************************************
MACRO OUTPUTS =  V1        VO       IL
*
* V1 = INPUT VOLTAGE
* VO = OUTPUT VOLTAGE
* IL = SERIES L STATE
************************************************************
MACRO CODE
MACRO STOP SORT
C
      C  = C  TP--
      XL = L  TP--
      R  = R  TP--
C
      DV1 = I1 TP-- - IL TP--
      DVO = IL TP-- - IO TP--
      DIL = V1 TP-- - VO TP-- - R* IL TP--
C
MACRO DERIVATIVE, V1 TP-- = DV1/C
MACRO DERIVATIVE, VO TP-- = DVO/C
MACRO DERIVATIVE, IL TP-- = DIL/XL
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, TP
END OF MODEL
PRINT
```

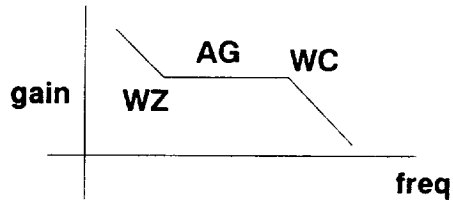
SMALL SIGNAL COMPONENT MODELS

ES	Small signal error amplifier (2 states)
EY	2 pole 2 zero compensator
EX	Small signal proportional compensator
FC	Small signal PWM modulator with cic (charger)
FM	Small signal PWM modulator for VFPPAT
CS	Small signal charger
PS	Small signal solar array and bus capacitor
AS	Small signal VFPPAT discharger

ES.MOD

Small signal error amplifier (2 states)





OUTPUTS

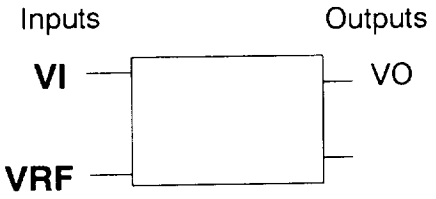
		Units
VO	Output voltage	
VON	Output voltage inverted	
X	Aux state	

INPUTS

VI	Input voltage	
VRF	Reference voltage	
AG	Midband gain	
WC	Cutoff frequency	rad/s
WZ	Zero freuency	rad/s
KV	Input voltage multiplier	

EY.MOD

Small signal 2 pole 2 zero compensator



OUTPUTS

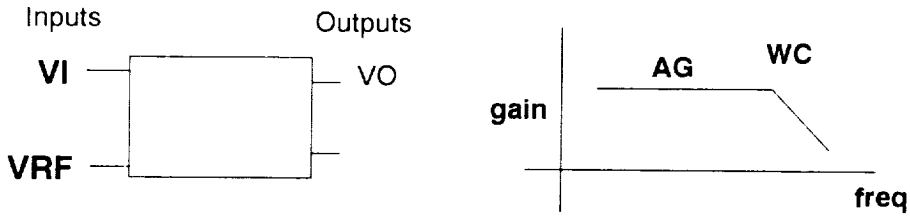
		Units
VO	Output voltage	
VON	Output voltage inverted	
X1	Aux state	
X2	Aux state	

INPUTS

VI	Input voltage	
VRF	Reference voltage	
AG	Midband gain	
WC	Cutoff frequency	rad/s
WZ	Zero freuency	rad/s
KV	Input voltage multiplier	
WZ2	Additional zero frequency	rad/s

EX.MOD

Small signal proportional error amplifier (1 state)



OUTPUTS

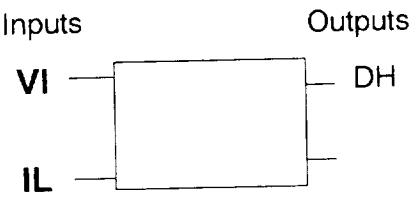
		Units
VO	Output voltage	
VON	Output voltage inverted	

INPUTS

VI	Input voltage	
VRF	Reference voltage	
AG	Proportional gain	
WC	Cutoff frequency	rad/s
KV	Input voltage multiplier	

FC.MOD

Small signal cic PWM modulator for charger



OUTPUTS

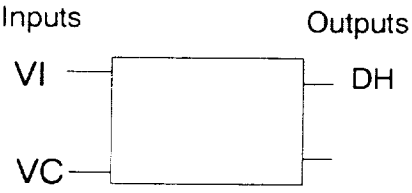
		Units
DH	Output duty ratio (AC)	
X1	Aux state	
X2	Aux state	

INPUTS

VI	Input side voltage (AC)	V
IL	Inductor current (AC)	A
VC	Control voltage (AC)	V
VO	Output side voltage (AC)	V
D	DC duty ratio	-
RI	Current sense gain	ohm
TS	Switching period of aux ramp	sec
L	Inductor	H
VP	External ramp amplitude	V
DI	Peak to peak inductor current	A
KIN		
KOT	factors to be set to 1	
KHE		

FM.MOD

Small signal cic PWM modulator for VFPPAT



OUTPUTS

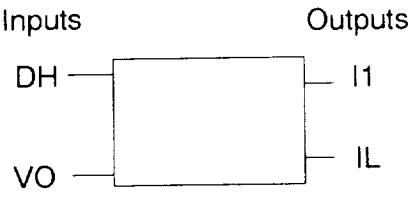
		Units
DH	Output duty ratio (AC)	

INPUTS

VI	Input side voltage (AC)	V
VC	Control voltage	V
SN	On slope of inductor current	V/sec
SE	Slope of external ramp	V/sec
TS	Period of external ramp	sec
VO	Output voltage	V
RI	Current sense gain	ohm
XL	Inductor	H

CS.MOD

Small signal charger model

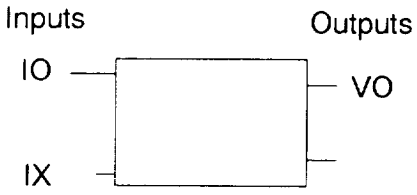


OUTPUTS		Units
I1	Input current (AC)	A
IL	Inductor current (AC)	A

INPUTS		
VO	Output voltage (AC)	V
V1	Input voltage (AC)	V
L	Inductor	H
RL	Inductor ESR	ohm
DH	AC duty ratio	-
V1S	DC input voltage	V
VOS	DC output voltage	V
D	DC duty ratio	-

PS.MOD

Small signal solar array and bus capacitor



OUTPUTS

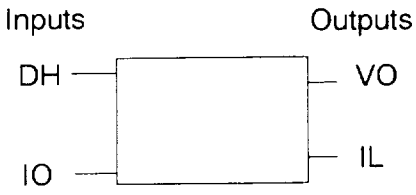
		Units
VO	Bus voltage (AC)	V
VON	Bus voltage (inverted)	v
VC	Bus capacitor state	v
	(inverted voltage is only to obtain bus impedance plots)	

INPUTS

IO	Outgoing load current	A
IA	Array DC photocurrent	A
IX	Incoming load current	A
C	Bus capacitor	F
RC	Bus capacitor ESR	ohm
C1	Aux capacitor	F
RD	Array dynamic resistance	ohm

AS.MOD

Small signal VFPPAT discharger



OUTPUTS

		Units
VO	Output voltage (AC)	V
VC	Capacitor state (output voltage)	V
IL	Inductor current (AC)	A
I1	Input current (AC)	A
IS	Sensed inductor current (AC)	V

INPUTS

V1	Input voltage	V
IO	Load current	A
DH	AC duty ratio	-
V1S	DC Input voltage	V
IOS	DC load current	A
D	DC duty ratio	-
RC	Capacitor ESR	ohm
C	Bus capacitor	F
L	Inductor	H
RL	Inductor ESR	ohm
R	Load resistor	ohm
N	VFPPAT turns parameter	-
RI	current sense gain	ohm

```
*************************************************************
*
* SMALL SIGNAL INVERTING INTEGRATOR ERROR AMPLIFIER
* ES.MOD
*
* CLAMPS REMOVED FROM EI.MOD
* NO SWITCH STATES
*************************************************************
DEFINE MACRO = ES
*************************************************************
MACRO INPUTS = VI
               AG      WC      WZ      KV
               VRF
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR BY WHICH VI IS REDUCED (INPUT POT. DIVIDER)
* WC  = CUTOFF FREQUENCY
* WZ  = ZERO FREQUENCY
* AG  = MIDBAND GAIN
* VRF = +VE INPUT VOLTAGE
*************************************************************
MACRO OUTPUTS =  VO
                 X
                 VON
*
* VO = OUTPUT VOLTAGE
* VON= NEGATIVE OF OUTPUT VOLTAGE
* X  = AUXILIARY STATE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      DV  = -KV ES-- * VI ES-- + VRFES--
      WC = WC ES--
      WZ = WZ ES--
      AG = AG ES--
      VO = VO ES--
      VONES-- = -VO ES--
C
      GK = AG * WC
      DXN = GK*(WZ - WC)*DV - X  ES-- * WC
      DVN = GK*DV + X  ES--
C
MACRO DERIVATIVE, X  ES-- = DXN
MACRO DERIVATIVE, VO ES-- = DVN
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, ES
END OF MODEL
PRINT
```

```
*************************************************************
*
* SMALL SIGNAL INVERTING INTEGRATOR ERROR AMPLIFIER
* EY.MOD
*
*************************************************************
DEFINE MACRO = EY
*************************************************************
MACRO INPUTS = VI
               AG      WC      WZ      KV
               WZ2     VRF
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR BY WHICH VI IS REDUCED (INPUT POT. DIVIDER)
* WC  = CUTOFF FREQUENCY
* WZ  = ZERO FREQUENCY
* AG  = MIDBAND GAIN
* VRF = +VE INPUT VOLTAGE
* WZ2 = ADDITIONAL ZERO
*************************************************************
MACRO OUTPUTS =  VO
                 X1      X2
                 VON
*
* VO = OUTPUT VOLTAGE
* VON= NEGATIVE OF OUTPUT VOLTAGE
* X  = AUXILIARY STATE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      DV  = -KV EY-- * VI EY-- + VRFEY--
      WC = WC EY--
      WZ = WZ EY--
      AG = AG EY--
C
      V1 = DV
C
      PO = 0
      P1 = WC
      AGX = AG * WC
      ZO = AGX * WZ
      Z1 = AGX*(1 + WZ/WZ2EY--)
      Z2 = AGX/WZ2EY--
C
      VO EY-- = X2 EY-- + Z2*V1
      VONEY-- = - VO EY--
C
MACRO DERIVATIVE, X1 EY-- = ZO*V1 - PO*VO EY--
MACRO DERIVATIVE, X2 EY-- = X1 EY-- + Z1*V1 - P1*VO EY--
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, EY
END OF MODEL
PRINT
```

```
*************************************************************
*
* SMALL SIGNAL PROPORTIONAL ERROR AMPLIFIER
* EX.MOD
*
* CLAMPS REMOVED FROM ET.MOD
* NO SWITCH STATES
*************************************************************
DEFINE MACRO = EX
*************************************************************
MACRO INPUTS = VI
               AG       WC      KV
               VRF
* VI  = INPUT (VOLTAGE BEING REGULATED)
* KV  = FACTOR BY WHICH VI IS REDUCED (INPUT POT. DIVIDER)
* WC  = CUTOFF FREQUENCY
* AG  = PROPORTIONAL  GAIN
* VRF = +VE INPUT VOLTAGE
*************************************************************
MACRO OUTPUTS =  VO
                 VON
*
* VO = OUTPUT VOLTAGE
* VON= NEGATIVE OF OUTPUT VOLTAGE
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      DV  = -KV EX-- * VI EX-- + VRFEX--
      WC = WC EX--
      AG = AG EX--
      VO = VO EX--
      VONEX-- = -VO EX--
C
      DVO = WC*AG*DV - VO*WC
C
MACRO DERIVATIVE, VO EX-- = DVO
C
MACRO RESUME SORT
END OF MACRO
*************************************************************
MODEL DESCRIPTION
LOCATION = 20, EX
END OF MODEL
PRINT
```

```
DEFINE MACRO = FC
************************************************************
*
* SMALL SIGNAL CIC PWM MODULATOR FOR CHARGER
*
************************************************************
MACRO INPUTS = VI          IL
               VC          VO          D
               RI          TS          L
               VP          DI
               KIN         KOT         KHE
*
* VI = SMALL SIGNAL INPUT VOLTAGE
* VC = SMALL SIGNAL CONTROL VOLTAGE
* IL = SMALL SIGNAL INDUCTOR CURRENT (NOT REDUCED BY RSENSE !)
* VO = SMALL SIGNAL OUTPUT VOLTAGE
*
* DI = PEAK TO PEAK CURRENT
* VP = AMPLITUDE OF EXTERNAL RAMP
*
* TS  = SWITCHING TIME PERIOD
* RI  = EFFECTIVE RSENSE/TURNS RATIO
* D   = DC DUTY RATIO OF CHARGER
* L   = CHARGER INDUCTOR
* KIN KHE AND KOT ARE TO DISABLE KF AND KR FEEDBACKS
************************************************************
MACRO OUTPUTS =  DH
                 X1        X2
* DH = SMALL SIGNAL DUTY RATIO
* X1, X2 = AUX STATES
************************************************************
MACRO CODE
MACRO STOP SORT
C
C HE(S) GENERATION
C
      PI = 3.14159265
      QZ = -2./PI
      WN = PI/TS FC--
C
      B = WN*WN
      A = WN*QZ
      C = 10*WN
      D = 15*WN
C
      ZO = C*D
      Z1 = C*D/A
      Z2 = C*D/B
      P1 = C + D
      PO = C*D
C
      VIN = RI FC-- * IL FC--
      VOT = X2 FC-- + Z2*VIN
C
C FEEDBACK AND FEEDFORWARD BLOCK CONSTANTS, KF, KR
C
      DD  = D  FC--
      XL  = L  FC--
      TS  = TS FC--
      RI  = RI FC--
```

```
C
      XKF = - DD*TS*RI*(1. - DD/2.)/XL
      XKR = TS*RI/(2.*XL)
C
      VI  = KINFC-- *VI FC--
      VO  = KOTFC-- *VO FC--
      VOTX = KHEFC-- * VOT
      DH FC-- = XKF * VI  + XKR * VO  - VOTX + VC FC--
      FMI = DI FC-- * RI FC--/DD + VP FC--
      DH FC-- = DH FC-- / FMI
C
MACRO DERIVATIVE, X1 FC-- = ZO*VIN - PO*VOT
MACRO DERIVATIVE, X2 FC-- = X1 FC-- + Z1*VIN - P1*VOT
C
MACRO RESUME SORT
END OF MACRO
*****************************************************************
MODEL DESCRIPTION
LOCATION = 20, FC
END OF MODEL
PRINT
```

```
MACRO FILE NAME = MACROS
DEFINE MACRO = FM
************************************************************
*
* STEP GENERATOR
*
************************************************************
MACRO INPUTS = VI
               VC
               SN
               SE
               TS
               VO
               RI
               XL
************************************************************
MACRO OUTPUTS =  DH
* OUTPUT
************************************************************
MACRO CODE
MACRO STOP SORT
C
      RK = TS FM-- *RI FM-- /(2*XL FM--)
      VX = VO FM-- *RK +VC FM-- - VI FM-- *RI FM--
      XX = (SN FM-- + SE FM-- )*TS FM--
      DH FM-- = VX/XX
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, FM
END OF MODEL
PRINT
```

```
DEFINE MACRO = CS
************************************************************
*
* SMALL SIGNAL CHARGER MODEL
*
* ADD FT.MOD FOR INPUT FILTER
* ADD FX.MOD FOR OUTPUT FILTER
*
************************************************************
MACRO INPUTS = VO       V1
               L        RL       DH
               V1S      VOS      D
* VO = OUTPUT VOLTAGE (AC)
* V1 = INPUT VOLTAGE FROM FILTER (AC)
* V1S, VOS = DC VALUES
* L  = BUCK INDUCTOR
* RL = INDUCTOR ESR
* DH = AC DUTY RATIO
* D  = DC DUTY RATIO
************************************************************
MACRO OUTPUTS =  I1       IL
                 ILS
*
* I1 = CURRENT DRAWN FROM FILTER (AC)
* IL = BATTERY CHARGING CURRENT (STATE) (AC)
* ILS= DC SOLUTION BATTERY CHARGING CURRENT
************************************************************
MACRO CODE
MACRO STOP SORT
C
      XL = L  CS--
      R  = RL CS--
      D  = D  CS--
      DH = DH CS--
C
      A1 = -R/XL
      AM1 = 0
C
      B1 = D/XL
      B2 = -1/XL
      BM1 = 1/XL
      BM2 = 0
C
      C1 = D
      CM1 = 1
C
C  DC SOLUTION
C
      V1S = V1SCS--
      VOS = VOSCS--
C
      BU = B1*V1S + B2* VOS
      XIS = -BU/A1
      ILSCS-- = XIS
C
C  CONTROL MATRIX
C
      P = BM1*V1S + BM2*VOS
      Q = CM1*XIS
C
```

```
C  OUTPUT EQUATION
C
      XIL = IL CS--
      V1  = V1 CS--
      VO  = VO CS--
      I1 CS-- = C1*XIL + Q*DH
C
MACRO DERIVATIVE, IL CS-- = A1*XIL + B1*V1 + B2*VO + P*DH
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, CS
END OF MODEL
PRINT
```

```
MACRO FILE NAME = MACROS
DEFINE MACRO = PS
************************************************************
*
* SMALL SIGNAL ARRAY AND BUS CAP
*
************************************************************
MACRO INPUTS = IO
               IX
               C
               RC
               C1
               IA
               RD
* IA = ARRAY DC CURRENT
* C  = BUS CAPACITOR
* C1 = AUX CAPACITOR
* IO = CURRENT DRAWN FROM ARRAY
* RC = BUS CAP ESR
* RD = ARRAY DYNAMIC RESISTANCE
************************************************************
MACRO OUTPUTS =  VO       VC
                 VON
* VON = -VE VO (ONLY TO PLOT VO/VC TRANSFER FUNCTIONS)
* VO = OUTPUT VOLTAGE (STATE)
* VC = MAIN BUS CAP STATE
************************************************************
MACRO CODE
MACRO STOP SORT
C
      XIO = IO PS--
      RC  = RC PS--
      RD  = RD PS--
      XIA = IA PS--
      C   = C  PS--
      C1  = C1 PS--
C
      VO  = VO PS--
      VC  = VC PS--
C
      XRD = VO/RD
      XRC = (VO - VC)/RC
      VONPS-- = -VO PS--
C
      DVO = XIA - XIO - XRC - XRD + IX PS--
C
MACRO DERIVATIVE, VO PS-- = DVO/C1
MACRO DERIVATIVE, VC PS-- = XRC/C
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, PS
END OF MODEL
PRINT
```

```
DEFINE MACRO = AS
*
*************************************************************
*
* SMALL SIGNAL MODEL FOR VFPPAT DISCHARGER
*
*************************************************************
MACRO INPUTS = V1      IO      DH
               V1S     IOS     D
               RC      C       L       RL      R
               N       RI
* V1 = INPUT VOLTAGE (AC)
* IO = LOAD CURRENT (AC)
* DH = (AC) DUTY RATIO
* D  = DC DUTY RATIO
*
* V1S , IOS = DC VALUES OF BATTERY VOLTAGE AND EXTRA LOAD CURRENT
*
* RL = INDUCTOR ESR : R = LOAD
*************************************************************
MACRO OUTPUTS =  IL      VC
                 VO      I1
                 VOS     ILS
                 IS
* STATES
*  IL = INDUCTOR CURRENT (AC)
*  VC = OUTPUT VOLTAGE (AC)
* OUTPUTS
*  VO = OUTPUT VOLTAGE (AC)
*  I1 = INPUT CURRENT (AC)
* STEADY STATE SOLUTION
*  VOS = OUTPUT CAP VOLTAGE (DC)
*  ILS = INDUCTOR CURRENT (DC)
*************************************************************
MACRO CODE
MACRO STOP SORT
C
      R  = R  AS--
      RC = RC AS--
      RCC= 1 + RC/R
      XL = L  AS--
      RL = RL AS--
      C  = C  AS--
C
      D  = D  AS--
      DD = 1 - D
      XN1 = (N  AS-- + 1)
C
C    MATRICES A, B, C, E
C
C    A  = A1.D + A2.DD
C    AM = A1 - A2        NO D'S !!
C
      A11 = -(RL + RC/RCC)/XL
      A12 = -1/(XL*RCC)
      A21 = 1/(C*RCC)
      A22 = -1/( C*(R+RC) )
C
      AM11 = 0
      AM12 = 0
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      AM21 = 0
      AM22 = 0
C
      B11 = D*XN1/XL + DD/XL
      B12 = RC/(XL*RCC)
      B21 = 0
      B22 = 1/(C*RCC)
C
      BM11 = (XN1-1)/XL
      BM12 = 0
      BM21 = 0
      BM22 = 0
C
      C11 = RC/RCC
      C12 = 1/RCC
      C21 = D*XN1 + DD
      C22 = 0
C
      CM11 = 0
      CM12 = 0
      CM21 = XN1-1
      CM22 = 0
C
      E11 = 0
      E12 = -RC/RCC
      E21 = 0
      E22 = 0
C
      EM11 = 0
      EM12 = 0
      EM21 = 0
      EM22 = 0
C
C  STEADY STATE SOLUTION
C
      U1S = V1SAS--
      U2S = IOSAS--
C
C     X = -AINV.B.U
C
      BU1 = B11*U1S + B12*U2S
      BU2 = B21*U1S + B22*U2S
C
      DEL  = A11*A22 - A21*A12
      AI11 =  A22/DEL
      AI12 = -A12/DEL
      AI21 = -A21/DEL
      AI22 =  A11/DEL
      XIS  = -AI11*BU1 - AI12*BU2
      VCS  = -AI21*BU1 - AI22*BU2
      VOSAS-- = VCS
      ILSAS-- = XIS
C
C  CONTROL MATRICES
C
C     P = (A1 - A2).X + (B1 - B2).U
C     Q = (C1 - C2).X + (E1 - E2).U
C
      P1 = AM11*XIS +AM12*VCS +BM11*U1S +BM12*U2S
      P2 = AM21*XIS +AM22*VCS +BM21*U1S +BM22*U2S
```

```
C
      Q1 = CM11*XIS +CM12*VCS +EM11*U1S +EM12*U2S
      Q2 = CM21*XIS +CM22*VCS +EM21*U1S +EM22*U2S
C
C  OUTPUT EQUATION
C
      XIL = IL AS--
      IS AS-- = RI AS-- * IL AS--
      XIO = IO AS--
      VC  = VC AS--
      V1  = V1 AS--
      DH  = DH AS--
      VO AS-- = C11*XIL  + C12*VC   + E11*V1 + E12*XIO + Q1*DH
      I1 AS-- = C21*XIL  + C22*VC   + E21*V1 + E22*XIO + Q2*DH
C
MACRO DERIVATIVE, IL AS-- = A11*XIL +A12*VC +B11*V1 +B12*XIO +P1*DH
MACRO DERIVATIVE, VC AS-- = A21*XIL +A22*VC +B21*V1 +B22*XIO +P2*DH
C
MACRO RESUME SORT
END OF MACRO
************************************************************
MODEL DESCRIPTION
LOCATION = 20, AS
END OF MODEL
PRINT
```