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# Ka-Band MMIC Microstrip Array for High Rate Communications

R.Q. Lee and C.A. Raquet  
*Lewis Research Center  
Cleveland, Ohio*

and

J.B. Tolleson and S.M. Sanzgiri  
*Texas Instruments Incorporated  
McKinney, Texas*

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(NASA-TM-104500) KA-BAND MMIC MICROSTRIP  
ARRAY FOR HIGH RATE COMMUNICATIONS (NASA)  
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Unclass  
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Excitation of the patches is via aperture coupling which offers wider bandwidth and greatly simplifies the interconnect problem particularly for large arrays. One drawback of aperture feeding is back radiation which could cause serious inter-circuit coupling. To reduce back radiation, the apertures are shielded from the remaining RF distribution circuits. The choice of cavity-backed patch element offers two advantages. Surface wave modes will be suppressed with the patches placed in metal cavities. Also, the thick cavity plate will provide good structural support and serve as a heat sink for the MMIC devices.

To demonstrate the aperture coupled feeding technique, an aperture coupled rectangular patch antenna has been fabricated and tested. The antenna geometry is shown in Fig. 2(a), and results for the gain and radiation patterns are shown in Fig. 2(b) to (d). The antenna has a gain of over 5 dB at 29.3 GHz, and exhibits symmetrical E and H-plane patterns.

In array design, mutual coupling is a major concern because it can cause blindness or total reflection of RF power at the antenna input terminal. Mutual coupling for a  $4 \times 4$  subarray with circular cavity-backed patch elements has been measured, and is plotted in Fig. 3. Results indicate that the mutual coupling between adjacent elements is below 30 dB. Figure 4 shows the element mismatch versus scan angles for arrays with cavity-backed patch elements and arrays with elements fabricated on a continuous substrate. In comparison with arrays of continuous substrates, the array with cavity-backed elements has smaller element mismatch, and exhibits no blindness over a  $30^\circ$  scan.

The active beamforming network layer as shown in Fig. 1(b) is made up of MMIC devices and a microstrip power divider network. For ease of device characterization and replacement, MMIC devices are mounted on individual carrier plates with each carrier plate containing two phase shifters and two amplifiers. Wilkinson power dividers are used for RF power distribution, and are connected to the carrier plates via wire or ribbon bonding. To provide direct conductive cooling of the devices, the carrier plates are soldered to the base plate with the MMIC amplifiers located adjacent to the side walls of the subarray housing. The RF input to the beamforming network is realized using a coaxial probe to stripline/microstrip transition. The stripline is matched to the microstrip through a coplanar waveguide matching section. To satisfy the specified EIRP requirement, an external amplifier driver stage is also inserted at the input port.

Breadboard testing of Wilkinson power dividers and a two-channel carrier plate assembly have been successfully completed. Results for the 2:1 power divider indicate over 14 dB return loss and 18 dB isolation. Tests on the carrier plate were conducted using amplifiers from previous NASA mask set and 50- $\Omega$  lines in place of the phase shifters. Effects of the wall and lid on the operational stability of the carrier plate assembly were also evaluated. Results from these tests indicate low coupling levels and more than 15 dB isolation between adjacent channels.

The baseline designs of the amplifier and the phase shifter are shown in Fig. 5(a) to (b) respectively. The three stage amplifier chip design was based on amplifier developed under a previous NASA Lewis contract (NAS3-24239), which demonstrated over 90 mW output power with over 45 percent efficiency at around 31 GHz. For this application, minor reoptimization is required to operate the amplifier at around 29.3 GHz. The phase shifter has 4-bit phase settings using pin diodes as switching elements. The baseline design was derived from a 35 GHz MMIC originally developed under Army LABCOM contract NO. DAALo1-88-C-0860). Measured results for the phase shifter are shown in Fig. 6(a) to (c). These results indicate that the phase for each bit is linear over a broad frequency range (25 GHz to 35 GHz), and is very close to the design value at 30 GHz. The 4-bit phase shifter also exhibits an excellent insertion loss of about 6 dB and a return loss of less than 12 dB at 29.3 GHz. The input impedance of the phase shifter is approximately 50  $\Omega$  for each bit of the phase settings as indicated in Fig. 6(c).

The preliminary design of the dc/logic distribution layer is shown in Fig. 1(c). In addition to providing the capability for individually setting the state of the 4-bit phase shifters, the logic circuit must meet other requirements. The design was developed to provide sufficient isolation of control lines to prevent possible RF leakage from affecting the performance of other devices, and to have the minimum number of signal lines reducing the number of hermetic feedthroughs required. Taking into consideration the two-compartment subarray housing geometry, the proposed design utilizes two dc/logic circuit boards. Each board controls eight phase shifters and eight amplifiers, and is placed above the power divider network to allow easy access to the carrier plates. The dc and logic signals are transmitted through four hermetic feedthroughs located at each side of the subarray housing. The logic control of each element is through a central controller. To simplify routing and minimize RF transmission line crossovers, two custom ASIC chips are used

to control the MMIC devices with each ASIC chip controlling one half of the subarray. The input data word to the ASIC chip is 48 bit in length. Thirty-two bits are needed to set the phase shifter bits, and 8 bits are reserved for on/off control of the amplifiers. The remaining 8 bits serve as an enable control to allow a selectable third (0 volt) bias state for each phase shifter. Since the unbiased diodes in the phase shifter have a predicted 10 dB/bit input/output rejection, the phase shifter could be used as a 40 dB RF switch to selectively turn off elements. This low current switching technique offers advantages of simpler dc/Logic board assembly and eliminates the risk associated with transient related amplifier failures.

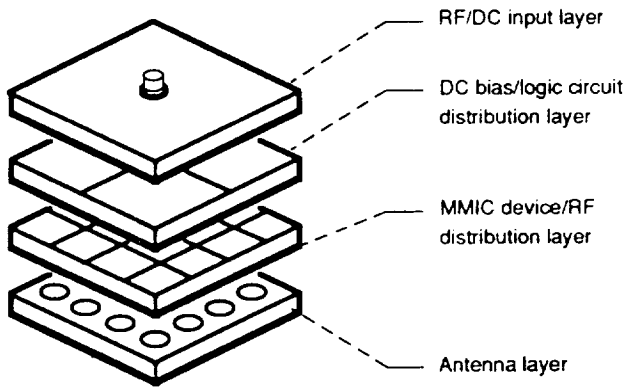
Conclusion

The baseline architecture and integration approach of a 4x4 MMIC microstrip subarray has been described.

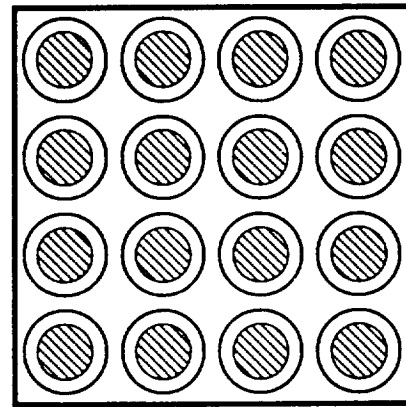
The proposed design was constrained to using currently available Ka-band MMIC devices and to a 'tile' configuration geometry. As a consequence, innovative integration and fabrication techniques are required to address the problems of spatial constraints, interconnections and heat removal. The subarray is modular in design, and thus, can be combined to form large arrays as required for candidate SEI antenna systems. Many of the key subarray components have been breadboarded and tested. Based on the successful results to date, the subarray is expected to demonstrate a major advance in MMIC insertion technology enabling future SEI and other space communications applications.

Reference

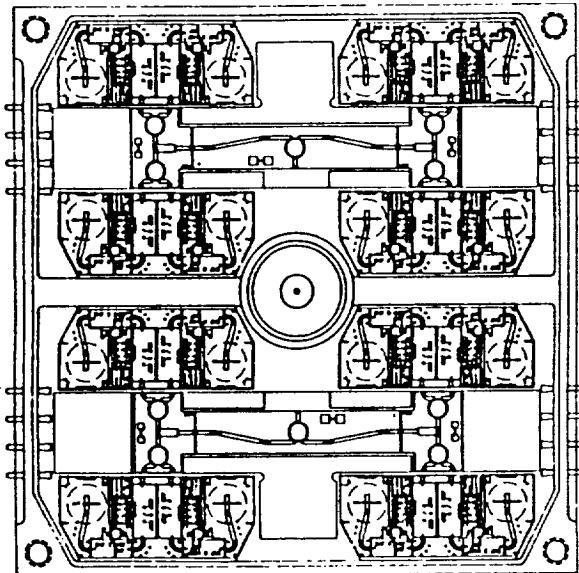
1. D. S. Ponchak, J. E. Zuzek, W. A. Whyte, Jr., R. L. Spence, P. Y. Sohn, "A Technology Assessment of Alternative Communication Systems for the Space Exploration Initiative," NASA TM-103243.



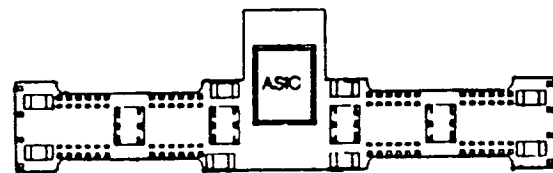
Multilayer tile construction



(a) Antenna elements.



(b) Beamforming network.



(c) dc/logic distribution network.

Figure 1.—Baseline design for the Ka-band MMIC microstrip subarray.

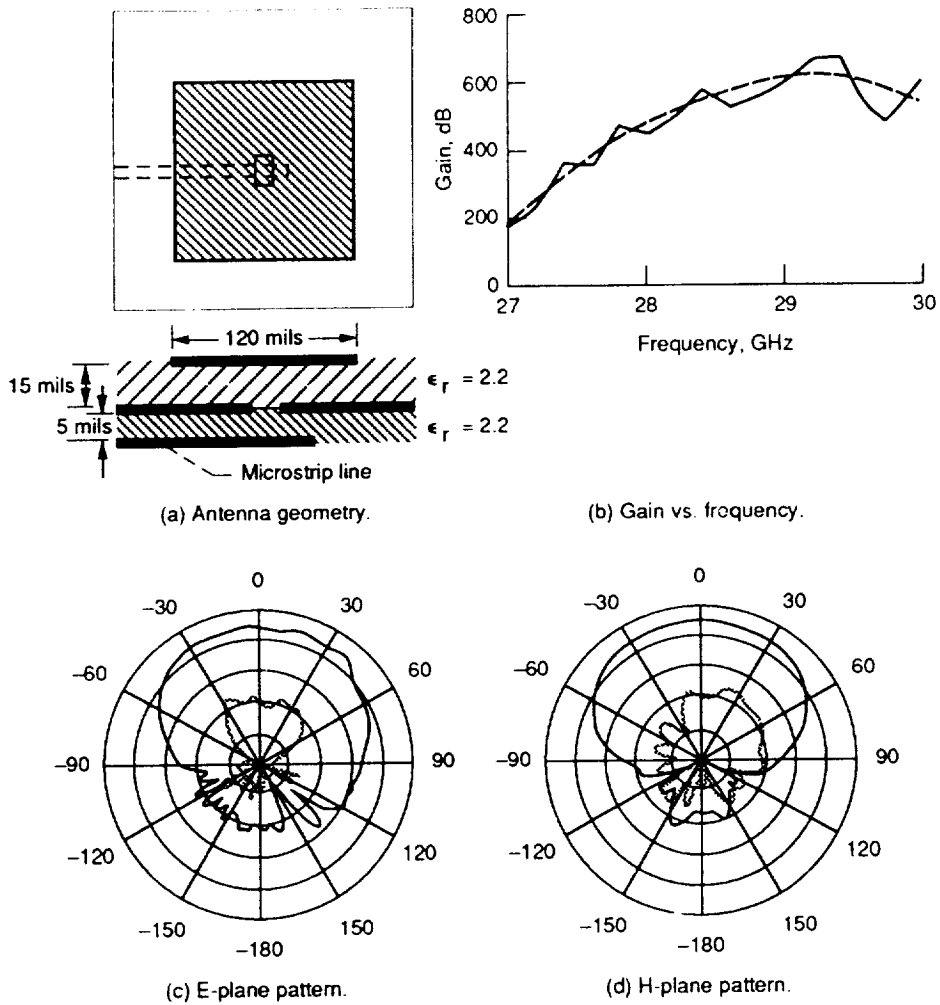


Figure 2.—Aperture coupled patch element.

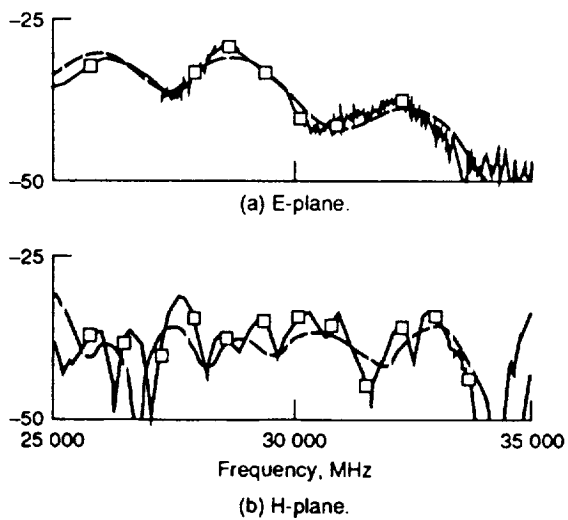


Figure 3.—Measured mutual coupling of a 4x4 sub-array with cavity backed patch elements.

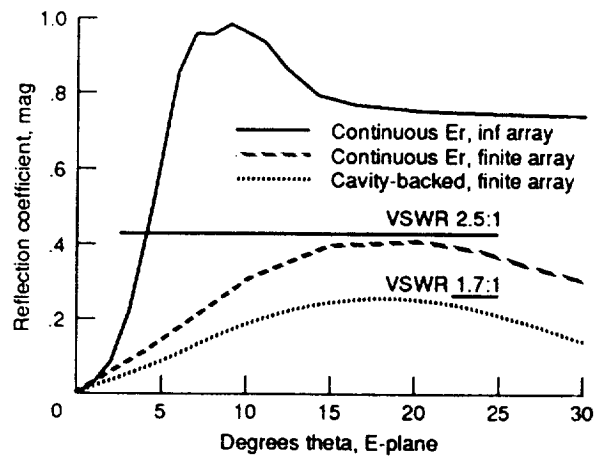
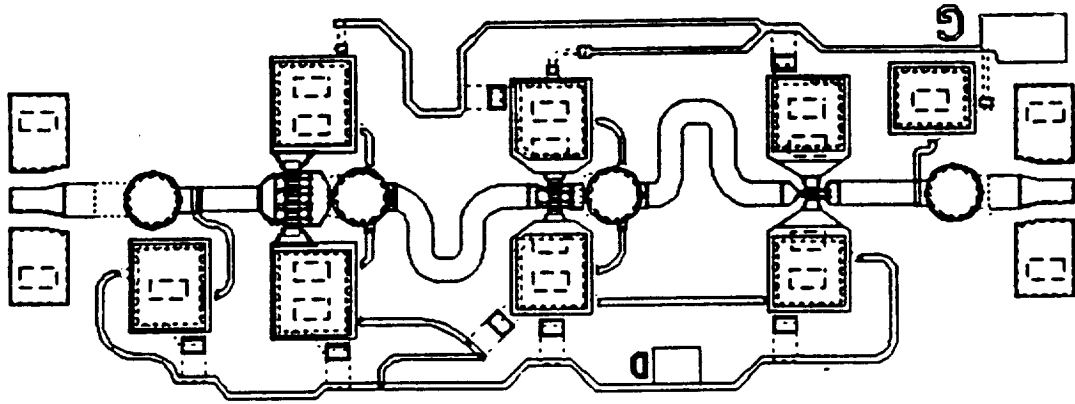
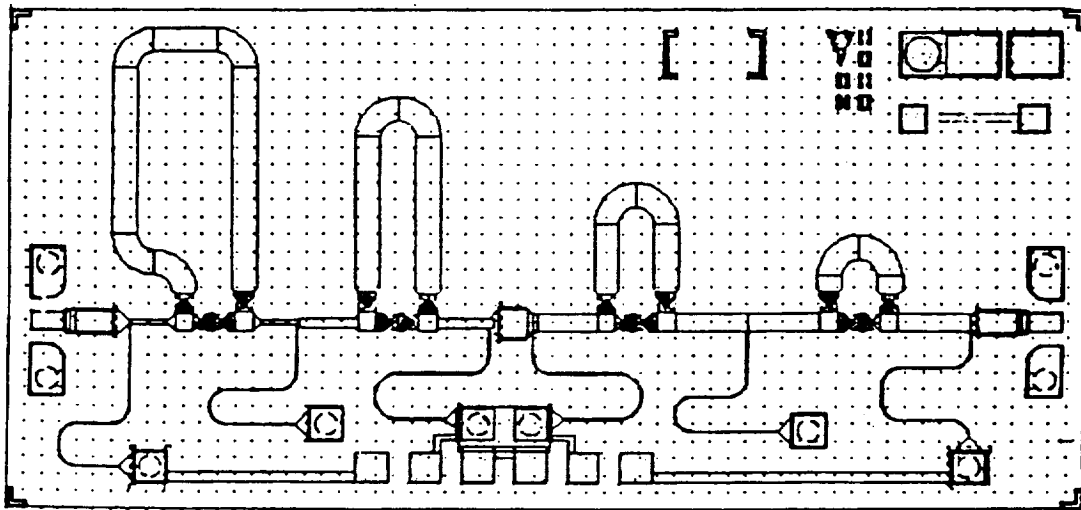


Figure 4.—Element mismatch versus scan angle (matched at broadside).

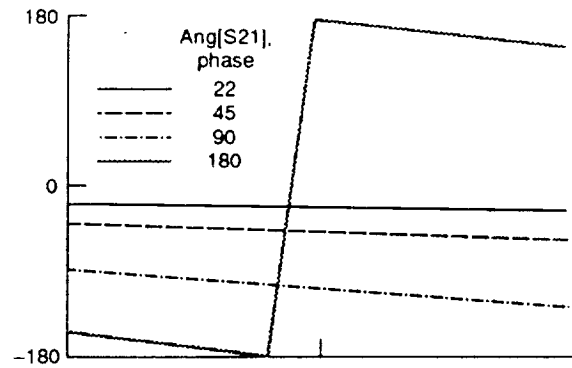


(a) Amplifier.

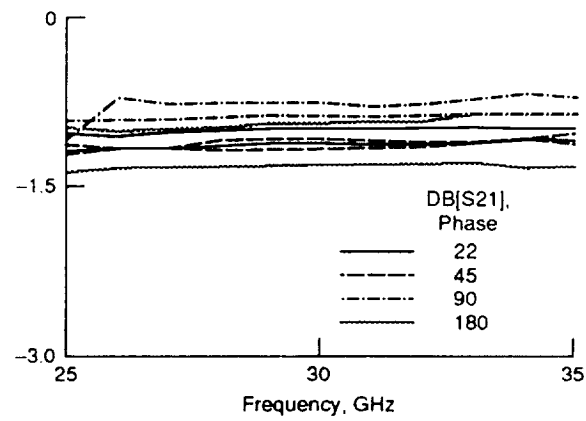


(b) Phase shifter.

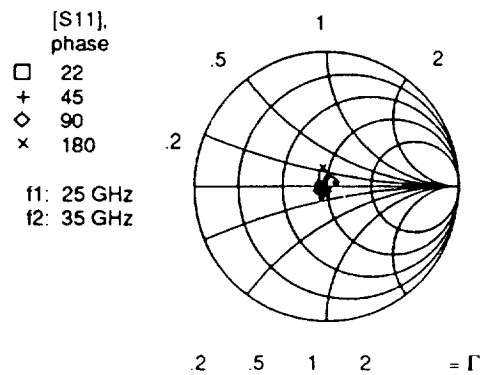
Figure 5.—MMIC device design layout.



(a) Phase vs. frequency.



(b) Insertion loss vs. frequency.



(c) Input impedance vs. frequency for each phase bit.

Figure 6.—Test data for the phase shifter.





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## Report Documentation Page

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16. Abstract In a recent technology assessment of alternative communication systems for the space exploration initiative (SEI), Ka-band (18-40 GHz) communication technology has been identified to meet the mission requirements of telecommunication, navigation and information management. Compared to the lower frequency bands, Ka-band antennas offer higher gain and broader bandwidths, and thus, are more suitable for high data rate communications. Over the years, NASA has played an important role in MMIC phased array technology development, and currently, has an ongoing contract with Texas Instruments (TI) to develop a modular Ka-band MMIC microstrip subarray (NAS3-25718). The TI contract emphasizes MMIC integration technology development and stipulates using existing MMIC devices to minimize the array development cost. The objective of this paper is to present array component technologies and integration techniques used to construct the subarray modules.					
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