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# TUNNEL JUNCTIONS FOR InP-on-Si SOLAR CELLS [1]

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We have succeeded in growing, by metalorganic chemical vapor deposition, a tunnel junction which makes possible an ohmic back contact in an n-on-p InP solar cell on a silicon substrate. The junction between heavily doped layers of p-type InGaAs and n-type InP shows resistance low enough not to affect the performance of these cells. InP solar cells made on n-type Si substrates with this structure were measured with an efficiency of 9.9% (AM0, 1- sun). Controls using p-type GaAs substrates showed no significant difference in cell performance, indicating that the resistance associated with the tunnel junction is less than about 0.1 ohm-cm$^2$.

## INTRODUCTION

Growth of InP solar cells on silicon substrates is one promising approach to achieving the high efficiency and radiation resistance of InP solar cells (refs. 1,2) without the high cost of InP wafers. Research into InP on Si has been motivated by the favorable results achieved with GaAs cells on silicon substrates (refs. 3-6). Dislocation densities as low as 2 x $10^6$ cm$^{-2}$ (ref. 4) and efficiencies over 18% AM0 have been reported (ref. 5). Since a recent theoretical study (ref. 7) projected achievable efficiencies of 18% with InP if dislocation density of $10^6$ cm$^{-2}$ or less could be achieved, these results make InP on silicon solar cells a promising avenue of research.

Considerable progress has been made in the related area of InP growth on GaAs substrates. In reference 8 a cell with 13.7% efficiency at one sun and 19% at concentration is reported on a GaAs substrate.

However, growth of n-on-p InP cells on silicon substrates has proved difficult because the first III-V layer grown on the silicon is always n-type; this makes an ohmic contact to the back of the cell problematic. (ref. 9) In previous work, researchers have circumvented this problem by using a p-on-n cell structure (ref. 10), by arranging to contact the base from the front of the structure, or by providing current paths outside of the active area of the cell (ref. 9). The p-on-n cells currently have somewhat lower efficiency than n-on-p, and the other techniques limit the size of the cells and detract from the available active area, which is expected to complicate the assembly of practical arrays.

The use of a tunnel junction between the substrate and the cell has been proposed as a solution to this difficulty (ref. 9). Here we report success in using such a tunnel junction, leading to InP-on-Si efficiencies of 9.8% AM0.

## THEORY

The tunnel junction consists of two heavily-doped semiconductor layers of opposite types. The doping in each layer must be degenerate (Fermi level outside of the band gap), and the width of the depletion region must be narrow enough for quantum-mechanical tunneling to occur across the triangular barrier formed by the depletion

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region (fig. 1). Under these conditions, electrons can tunnel between states in the valence band of the n-type material and states of the same energy in the conduction band of the p-type material.

Specifically, as shown in references 11 and 12, the effective conductance of the tunnel junction is given roughly by:

$$S = \frac{q^2}{4\pi^3\hbar^2 W}(2mE_g)^{1/2} \exp\left[-\frac{4W}{3}\frac{(2mE_g)^{1/2}}{\hbar}\frac{E_g}{qV_b}\right] \quad (1)$$

where W, the depletion width, is given by:

$$W = \left[\frac{2\varepsilon E_g(N_A+N_D)}{q^2 N_A N_D}\right]^{1/2} \quad (2)$$

In these equations, $S$ is the tunnel junction conductance (which has the units of A/cm$^2$V), $q$ the elementary charge, $E_g$ the band gap energy, $V_b$ the built-in voltage (slightly larger than $E_g$), $m$ the effective mass of electron (the tunneling current for holes is generally less than that for electrons), $\hbar$ (Plank's constant h/2$\pi$, $\varepsilon$ the dielectric permittivity (12.2$\varepsilon_0$ for InP), and $N_A$ and $N_D$ the dopant concentrations.

In practice, useful values of current density for solar cells require W to be less than 20 nm, which in turn means that the doping density in each of the two regions must be approximately $10^{19}$ or greater. From experience with the materials involved and from the results of reference 13, we concluded that the most appropriate choice for the tunnel junction was a combination of p-type $In_{0.53}Ga_{0.47}As$ and n-type InP, since doping levels of this order can easily be achieved in those materials, and the combination has a good lattice match. Figure 2 shows the calculated tunneling resistance for this combination as a function of the doping densities.

## EXPERIMENT

Figure 3 shows the experimental structure used in this work. All the layers described here were grown by metalorganic chemical vapor deposition. On a an n-type silicon substrate, a layer of GaAs is grown, following procedures developed earlier (ref. 14). Then a layer of $In_xGa_{1-x}As$ is grown, with a graded composition varying from close to x=0 to x=0.53, which is the lattice-matched composition to InP. All these layers are n-type. After the graded layer, a thin layer of n+ InP is deposited, followed by a thin layer of p+ $In_{0.53}Ga_{0.47}As$ to form the tunnel junction. Measurements indicated a dopant density of about 1.2 x $10^{19}$ cm$^{-3}$ in the p-type layer and 3 x $10^{19}$ cm$^{-3}$ in the n-type layer. This is followed by the solar cell structure, which consists of a p+ BSF, p-type base, thin n+ emitter, and n-type $In_{0.53}Ga_{0.47}As$ cap. (The solar cell structure is described in more detail in reference 1.)

Control cells were made using a p-type GaAs substrate with a graded layer which was similar but p-type. The same cell structure was used for the controls, but no tunnel junction.

The material was characterized by transmission electron microscopy and photoluminescence decay as well as solar cell measurements.

After the growth of the structure was complete, solar cells were made using established metallization, etching, and antireflection coating procedures (ref. 1,2). Solar cell areas were 1.00 and 0.25 cm$^2$. The efficiency of the cells was measured under a Spectrolab X25 solar simulator at AM0 intensity, calibrated with a GaAs reference cell. Internal quantum efficiency and dark I-V characteristics were also measured, and the series resistance extracted.

## RESULTS

TEM examination of InP films grown uncer the same conditions revealed a defect density in the range of $10^8$ $cm^{-2}$. This is only slightly lower than that measured on InP films grown on GaAs or silicon without such a graded layer, and considerably more than reported in reference 8. Figure 4 shows a cross-sectional TEM image of the graded layer; it can be seen that the distribution of defects in the graded layer is uneven. Further work on graded layers is in progress. Photoluminescence decay measurements showed lifetime of 0.7 ns.

Results of the solar cell efficiency measurements are given in table I. It is interesting to note that the results of wafer #2 are essentially equivalent to those of wafer #3, the GaAs control. This indicates that the low efficiency is due primarily to the high defect density, and not to the formation of a barrier at the back surface.

Figure 5 shows the measured I-V characteristics for representative 1.00 $cm^2$ cells from wafers 2 and 3. The similarity of the curves shows that the use of the silicon substrate has not resulted in additional series resistance. The total series resistance, obtained from dark I-V and $V_{oc}$-$I_{sc}$ curves, is 1.17 ohms for an 0.25 $cm^2$ cell on the silicon substrate (#2), and 1.16 ohms for a similar control cell (#3).

## CONCLUSIONS

We have made n-on-p InP solar cells on silicon substrates using a tunnel junction to make ohmic contact to the back of the cell. Measurements indicate that the tunnel junction has a resistance which is negligible, at least for one-sun applications (less than 0.1 ohm-$cm^2$).

This result, in addition to yielding the highest InP-on-Si solar cell efficiency so far published, is important because it indicates that InP structures of either polarity can be grown on silicon substrates without suffering a penalty due to the back contact. Using this technique, we expect that any efficiency which can be achieved in InP with GaAs substrates can be duplicated with silicon substrates.

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Table I. Solar Cell Results.
(AM0, 25°C)

| Wafer # | Substrate Structure | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | Fill Factor | Efficiency (%) |
|---|---|---|---|---|---|
| 2 (avg.) | n-GaAs/n-Si | 679 | 27.24 | 0.710 | 9.6 |
| 2 (std.) | | 2 | 0.43 | 0.009 | 0.2 |
| 2 (best) | | 682 | 28.07 | 0.706 | 9.9 |
| 3 (avg.) | p-GaAs | 689 | 26.62 | 0.706 | 9.4 |
| 3 (std.) | | 3 | 0.41 | 0.022 | 0.3 |
| 3 (best) | | 689 | 27.66 | 0.699 | 9.7 |

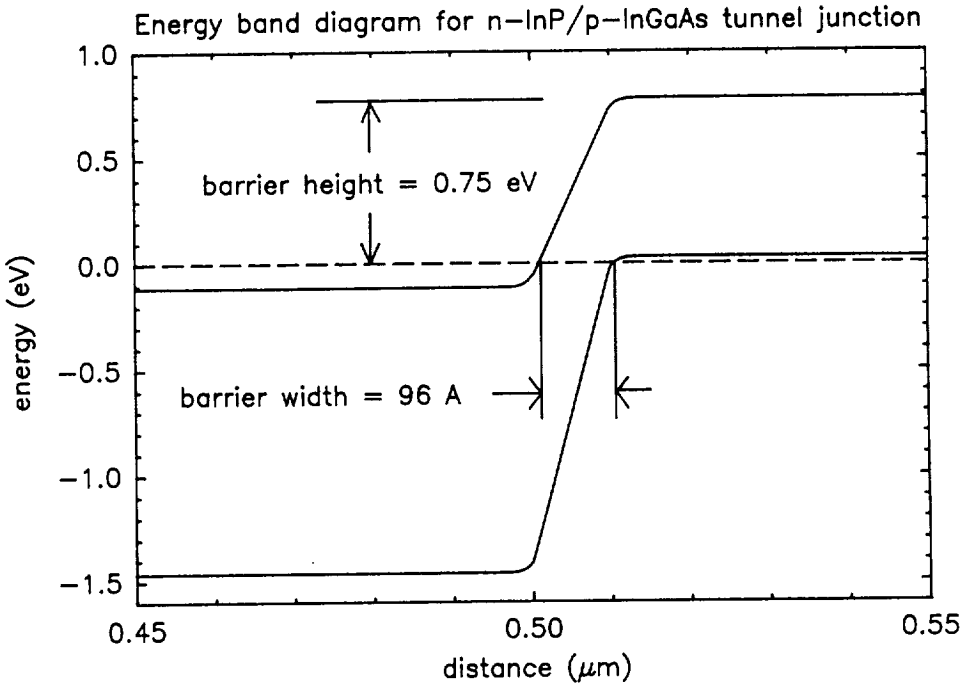


Figure 1. Band diagram of an n-InP/p-InGaAs tunnel junction. Tunneling takes place between filled states in the valence band of the n-type material and empty states of the same energy in the p-type material.

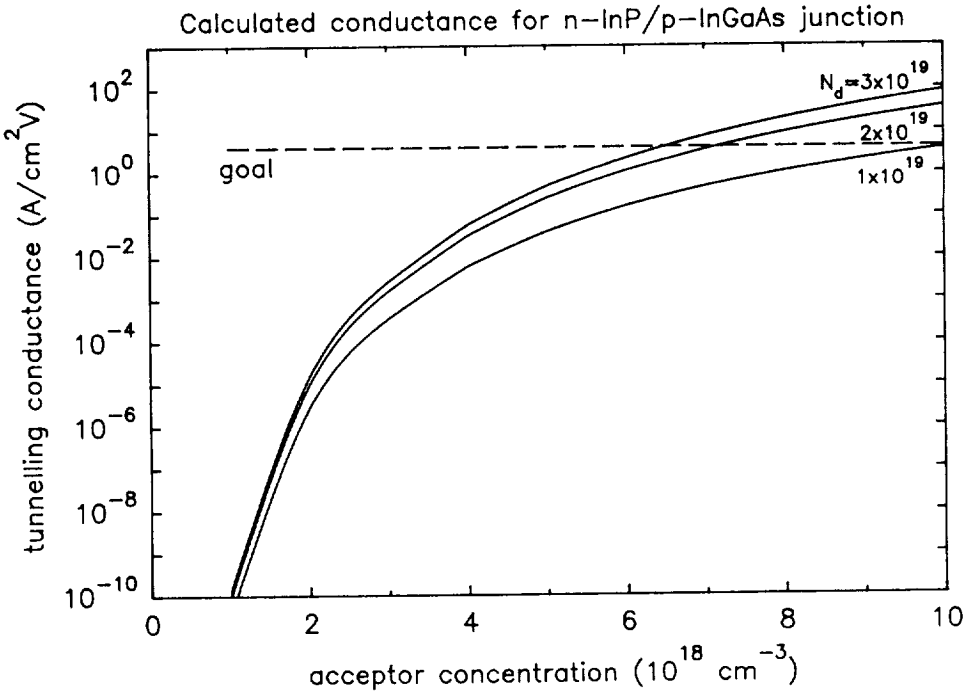


Figure 2. Calculated resistance of the tunnel junction as a function of the doping densities (note log scale).

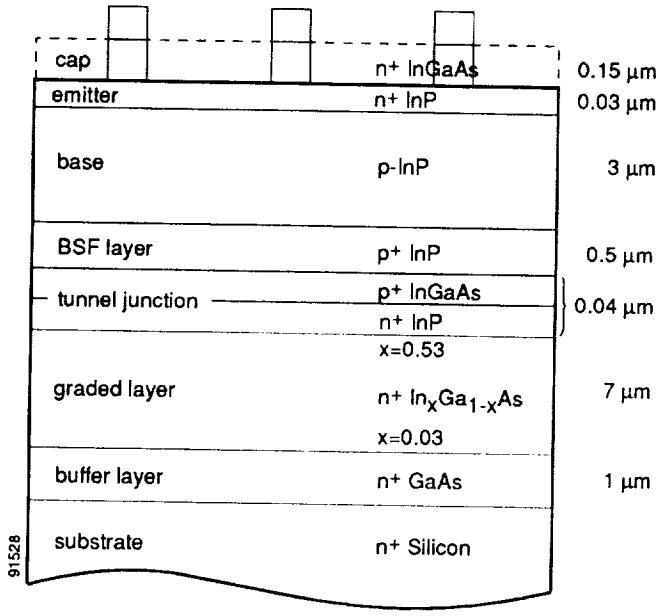


Figure 3. Cell structure used in this work. The graded InGaAs layer reduces the defect density and the tunnel junction provides an ohmic interconnection between the p-InP layer and the substrate.

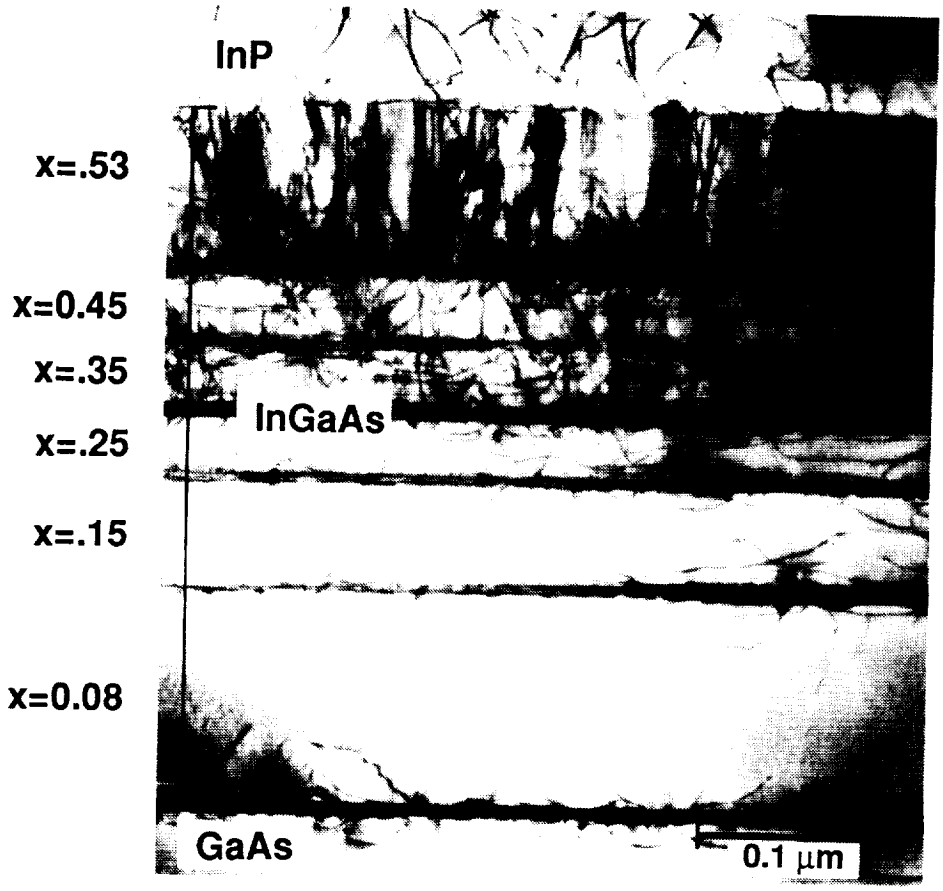


Figure 4. Cross-sectional TEM image of the cell structure. High defect density results from lattice mismatch at the intermediate interfaces.

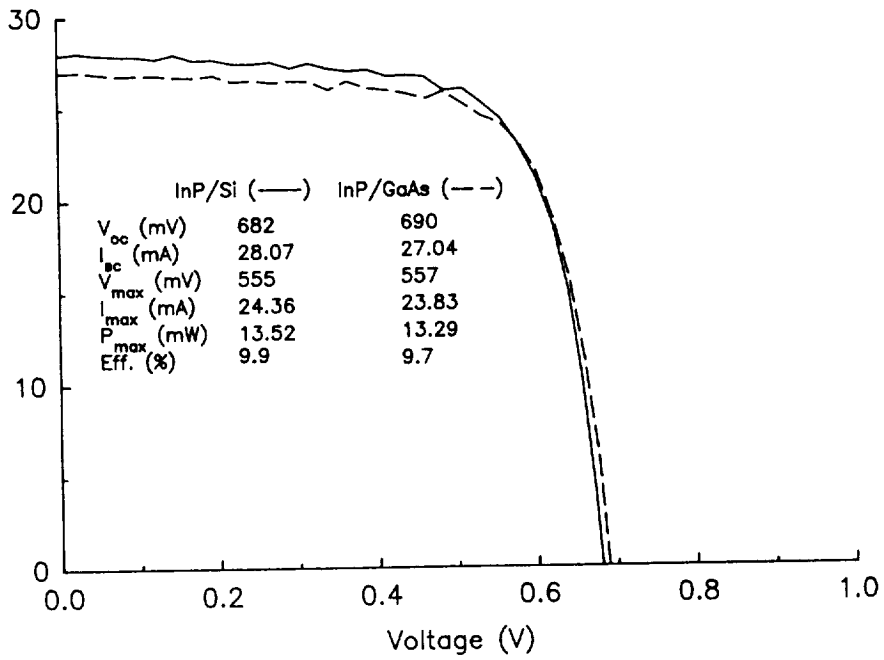


Figure 5. I-V characteristics of an InP-on-Si cell and an InP-on- GaAs control. The cells on silicon substrates show slightly lower voltages but higher currents than the controls.