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RECENT ADVANCES IN GaAs/Ge SOLAR CELLS

C. L. Chu, P. A. Iles
Applied Solar Energy Corporation
City of Industry, CA

W. Patterson
MANTECH Directorate
Wright Laboratories, Ohio

1.0 BACKGROUND

GaAs solar cells have several advantages for space use including high efficiency, radiation resistance and lower power fall-off at elevated operating temperatures. In the latter part of the 1980's, GaAs cells delivering 50 KW of space power were manufactured at ASEC.

By growing the GaAs cell on a Ge substrate, the advantages of GaAs cells can be retained and the higher mechanical strength of the Ge makes larger, thinner GaAs cells possible.

To conform to immediate user requirements, ASEC modified GaAs growth conditions to eliminate the additional PV output at the GaAs/Ge interface. GaAs cells on inactive Ge substrates have demonstrated efficiencies over 20% (AMO), for areas up to 6 x 6 cm^2, and cell thicknesses down to 3.5 mils (lower thicknesses are possible). Those cells had all the other advantages of GaAs/GaAs cells.

An unexpected bonus was the much reduced degradation observed after exposure to high reverse currents, thus increasing survivability of partially shadowed panels in space applications.

2.0 MANUFACTURING TECHNOLOGY

To demonstrate acceptable cell manufacturing technology, the major areas in cell manufacture were analyzed and developed, and effectively combined. Also the cells were successfully assembled on current lightweight arrays. The main areas of effort are discussed next.

2.1 Ge Substrates

We continued to specify square substrates (4.5 x 4.5 cm^2), 8 mils thick. Because of the inactive Ge design, we could relax the electrical requirements, specifying only the crystallographic and surface quality. We evaluated three Ge suppliers, who used either Czochralski or Horizontal Bridgman techniques to grow the Ge crystals. Table 1 shows the results of those tests.

Table 1 Comparison of Ge Substrates

Ge Ingot Growth	Vendor	Wafer Size (cm^2 - mil)	Elec. Yield (≥17%)	Process Lot
Czochralski	Laser Diode Eagle Picher	4.5x4.5--3.5 4.5x4.5--3.5	96.2% 95.2%	M111 M84,M86
Horizontal Bridgman	Crystal Specialties	4.5x4.5--3.5	82.6%	M79 M81 M82

Note: The mechanical yield of the 4.5 x 4.5 cm^2 thin cell is around >70%. The results of 6.0 x 6.0 cm^2 thin cells are also close.

Low dislocation density or lineage were not serious requirements. Some crystals contained "linear defects" and these defects often caused cracking because they etched perpendically during the thinning process and the resultant thin Ge layer was more easily cracked. Figure 1 shows some of these defects. These defects were problems even when substrates as thin as 5 mils were thinned. We are working with the Ge suppliers to eliminate these defects.

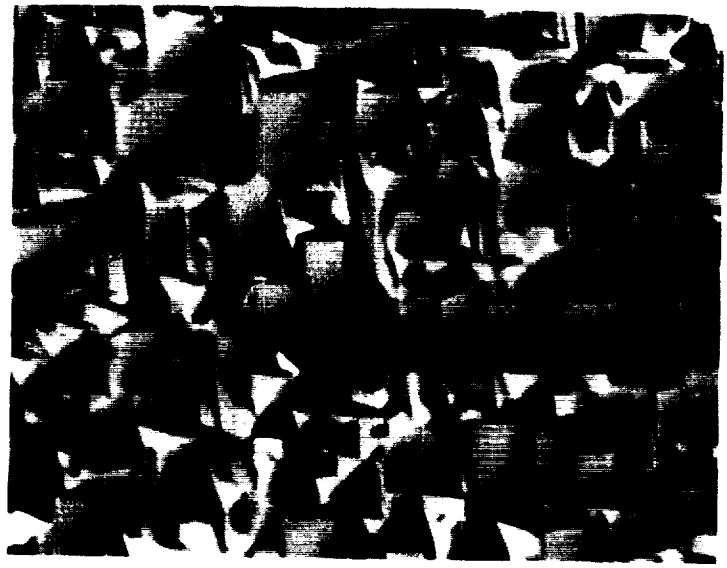

Figure 1 Linear defect (revealed in Ge Substrate Thinning) (X400)

2.2 MOCVD Growth

All our layers were grown on one of five production reactors operating continuously. The overall MOCVD growth conditions have been optimized and generally give high electrical yields. In a few runs, poor surface morphology or unwanted impurities can lead to reduced electrical performance. For runs with very poor morphology, repolishing the wafers for re-use is cost-effective, and can provide good cells with reasonable yields.

To show the effectiveness of the process, we present Figure 2 which shows electrical yields for 40 successive runs. These cells were 8 cm^2 area, 8 mils thick, but similar results were obtained for thin, larger area cells.

Lot #	Voc (mV)	Isc (mA)	Eff (%) @ 825 mV 4x2 cm	Projected Eff (%) at Pmax 2x4 cm
1	1008.0	246.5	17.6	18.7
2	1008.0	248.5	17.9	19.0
3	1005.0	245.8	17.5	18.6
4	1007.0	247.3	17.5	18.6
5	1012.0	245.3	17.8	18.9
6	1009.0	245.5	17.7	18.8
7	1002.0	245.1	17.4	18.5
8	1007.0	248.8	17.8	18.9
9	1005.0	246.6	17.7	18.8
10	1008.0	244.0	17.5	18.6
11	1008.0	246.5	17.8	18.9
12	1006.0	249.0	17.6	18.7
13	1006.0	244.3	17.6	18.7
14	1009.0	245.0	17.8	18.9
15	1010.0	246.7	17.8	18.9
16	992.0	246.7	17.2	18.3
17	992.0	246.7	17.2	18.3
18	1005.0	246.9	17.6	18.7
19	1007.0	247.4	17.7	18.8
20	998.0	248.2	17.6	18.7
21	1013.7	246.1	17.2	18.3
22	995.7	246.5	17.2	18.3
23	1002.0	243.3	17.3	18.4
24	1001.0	248.2	17.4	18.5
25	999.0	245.0	17.2	18.3
26	1004.0	244.4	17.6	18.7
27	1010.0	245.8	17.8	19.0
28	1006.0	244.8	17.4	18.5
29	1006.0	247.9	17.6	18.7
30	1009.0	244.7	17.6	18.7
31	1009.0	246.1	17.8	18.9
32	1008.0	246.1	17.7	18.9
33	1009.0	244.5	17.6	18.7
34	998.0	248.2	17.3	18.4
35	1013.0	247.6	18.0	19.2
36	1009.0	248.5	17.8	18.9
37	1012.0	248.7	18.1	19.2
38	1008.0	246.7	17.8	19.0
39	1009.0	241.7	17.5	18.6
40	1012.0	247.9	18.1	19.2
Average	1006.3	246.4	17.6	18.7

Figure 2 **Lot Average Data for GaAs/Gei Solar Cells (8 cm^2) at AMO Condition, 28 Deg. C for 40 Consecutive Lots, 1991**

2.3 Cell Processing

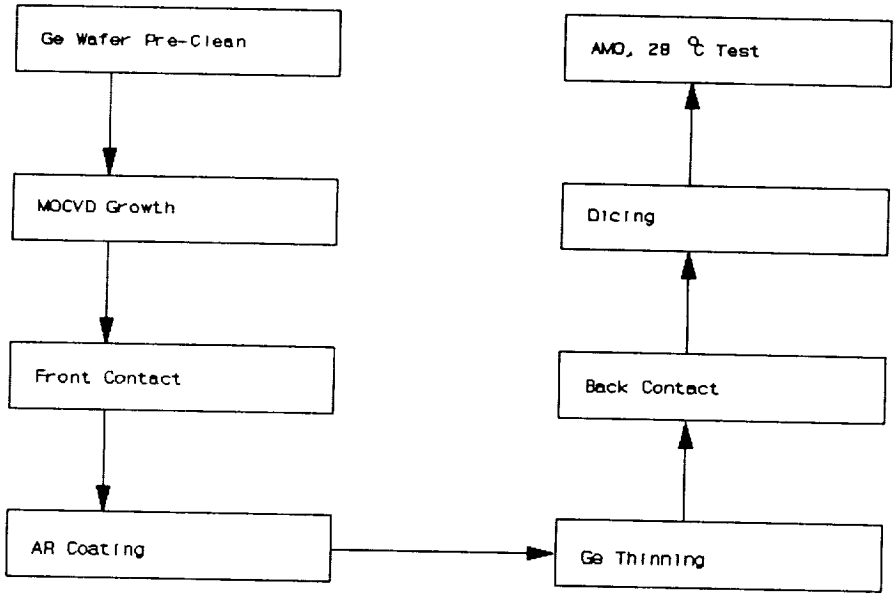

Figure 3 Flow Chart of GaAs/Ge Thin Cell Process

We have adapted standard production processes to apply front surface contacts and Al coatings to the grown layers. We have slightly modified the processing sequence and methods along with the testing to reduce breakage in the thinning process.

2.4 Thinning the Ge Substrates

A protective layer is applied to the front surface, and the Ge substrate is thinned (from 8 to <4 mils) by wet-etching. We are continuing evaluation of dry etching and other wet processes to see if the preferential attack on linear defects is reduced.

3.0 CELL PERFORMANCE

3.1 Electrical Output

For cells up to 6 x 6 cm^2, 3.5 mils thick, efficiencies over 20% have been obtained.

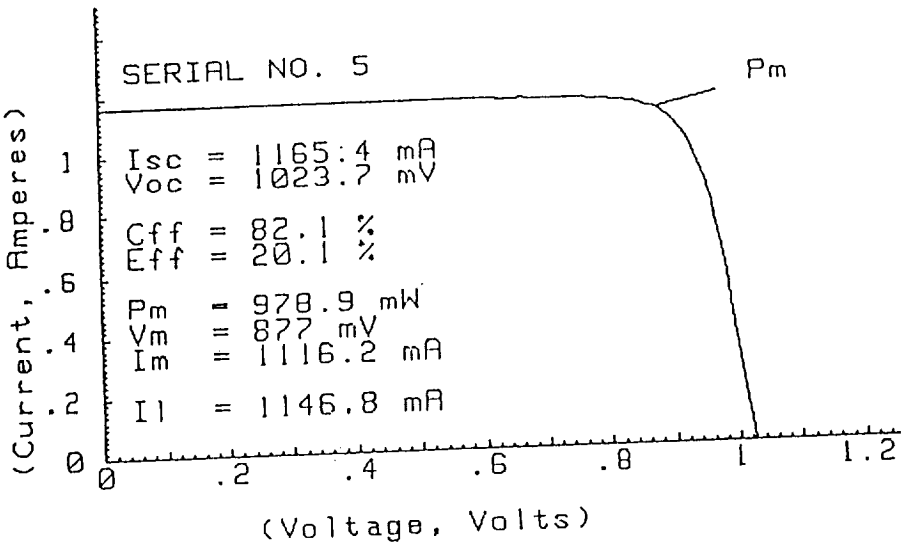

Figure 4 I-V Curve 6 x 6 cm² Thin Cell

Average lot efficiencies have exceeded 18% (4 x 4 cm², 3.5 mil thick).

Table 2 Electrical Testing Results of GaAs/Ge 4 x 4 cm² Thin Cells

Description: GAAS/GE THIN 4X4 M155
Test: Baseline
Lot number: M155
Load Voltage: .825
Date: 4 Dec 1990
Time: 11:48:23

Cell #	Voc mV	Isc mA	IL mA	Vm mV	Im mA	Pm mW	Cff %	Eff %
1	1016	495	485	882	466	411	81.7	19.0
2	1012	495	480	866	464	402	80.2	18.6
3	1010	488	475	867	460	399	80.9	18.4
4	1011	495	452	846	440	372	74.4	17.2
5	1010	496	486	877	470	412	82.3	19.0
6	1011	492	460	862	434	374	75.2	17.3
7	1012	495	482	874	465	406	81.1	18.8
8	1010	499	488	870	473	412	81.7	19.0
9	1018	492	482	871	467	407	81.2	18.8
10	1019	501	491	874	476	416	81.5	19.2
11	1004	497	485	867	470	407	81.7	18.8
12	1012	490	475	868	460	399	80.5	18.4
13	1016	499	489	875	474	415	81.8	19.2
14	1011	495	476	861	462	398	79.5	18.4
15	1016	505	495	871	480	418	81.5	19.3
16	1009	496	405	855	394	337	67.3	15.6
17	1014	501	493	873	478	417	82.1	19.3
18	980	494	482	871	466	406	83.8	18.8
19	1016	505	493	869	477	415	80.8	19.2
20	1015	505	496	873	480	419	81.8	19.4
21	1013	496	478	857	464	398	79.1	18.4
22	1011	504	489	867	474	411	80.7	19.0
23	1016	499	488	871	474	413	81.4	19.1
24	1013	500	490	872	475	414	81.8	19.1
25	1014	495	484	875	469	410	81.8	18.9
26	1003	494	355	843	347	293	59.0	13.5
27	1012	493	483	876	465	407	81.6	18.8
28	1018	498	487	875	470	411	81.1	19.0
29	1013	504	488	863	473	408	80.0	18.8
30	1015	497	486	876	470	412	81.6	19.0
31	1014	497	486	872	470	410	81.3	18.9
32	1014	496	484	877	466	409	81.3	18.9
33	1015	507	496	868	481	418	81.1	19.3
34	1011	497	486	875	469	410	81.7	18.9
35	1005	490	479	862	465	401	81.4	18.5
36	1017	507	497	877	480	421	81.6	19.4
37	1015	497	486	874	471	412	81.6	19.0
38	1014	495	471	862	455	392	78.1	18.1
Average	1012	497	479	869	463	402	79.9	18.6
Standard Dev	6	5	26	8	25	24	4.5	1.1

The cell efficiency has been retained when cells are mounted on panels (see 3.6).

3.2 Temperature Coefficients, Radiation Resistance

Similar values to those requested for GaAs/GaAs cells are obtained.

3.3 Contact Pull Strength

High pull strengths and satisfactory bonding onto arrays were obtained for thin cells using both soldered and welded interconnects with only slight adjustment in normal bonding schedules.

Table 3 Pull Strength of GaAs/Ge Cells

No. of Joints	Interconnected Area (mil^2)	Pull Strength (Gram)	
		Front	Back
34	Soldered Joints 35 x 75	1173	--
55		758	--
43		--	1130
11	Welded Joints 50 x 75	464	--
54		--	810
10	25 x 45	358	--

The efficiency of the cells used for the test is 17% - 18%.

3.4 Resistance to Reverse Current Stressing

After exposure to reverse currents 20 to 30% above the Isc (AMO) value, the degradation of GaAs/Ge cells was very low, a significant improvement over results obtained for GaAs/GaAs cells.

3.5 Contact Modifications

3.5.1 Coplanar Back Contacts

To adapt to flexible array interconnections, 6 x 6 cm, 8 mil cells with coplanar contacts (wraparound or wrapthrough) have been made with efficiencies up to 18%. Present work is directed at improved consistency in the process sequence.

3.5.2 High Temperature Stability

We have modified the contact structure to withstand exposure to high temperatures. With minimum process modification (addition of a barrier layer), cells can withstand exposure to 500-550°C. With additional process steps, we have shown the feasibility of no degradation (from 18%) after 600°C for 5 minutes and less than 5% degradation after heating at 600°C for 30 minutes. Present work is aimed at simplification of structures and processes to increase the yields of cells which are stable after high temperature exposure.

3.6 Panel Performance

These large area, thin GaAs/Ge cells have been successfully assembled on lightweight rigid panels. Panels 1 ft x 1 ft, containing forty-nine 4 x 4 cm^2 cells were made with both welded and soldered interconnects. The panel efficiencies were 17.7%.

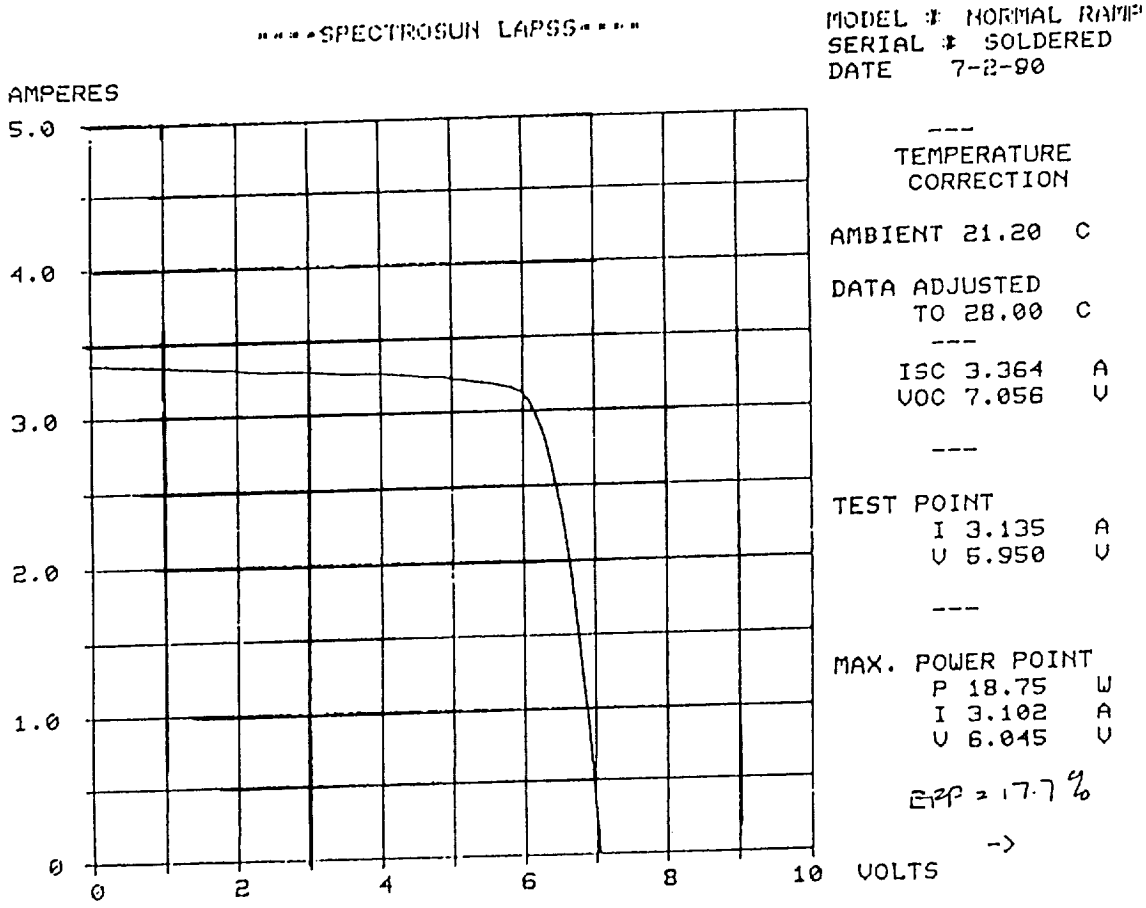

Figure 5 I-V Curve of Soldered 4 x 4 cm^2, Thin Cell Panel (7P, 7S)

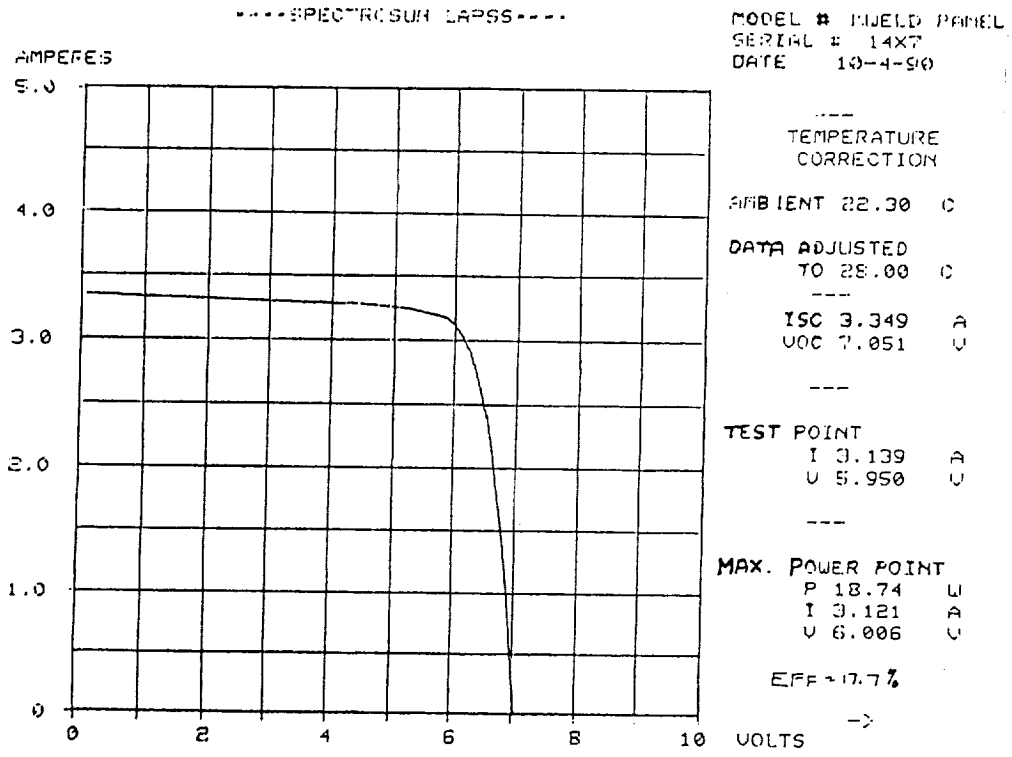

Figure 6 I-V Curve of Welded 2 x 2 cm² Thin Cell Panel (7P, 7S)

A small panel (2S, 2P 4 x 4 cm² cells) had efficiency 19.4%.

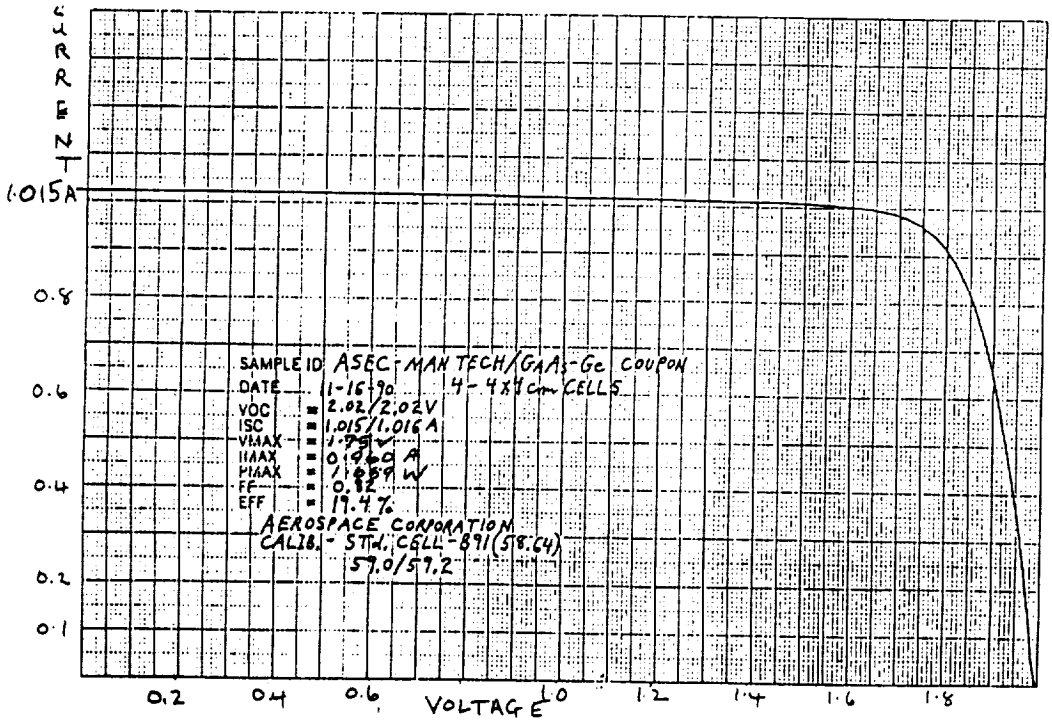

Figure 7 I-V Curve of 4 x 4 cm², Thin Cell Coupon (2P, 2S) After 5,000 Thermal Cycles

A small panel (3S, 3P, 6 x 6 cm^2 cells) had efficiency 18.8%

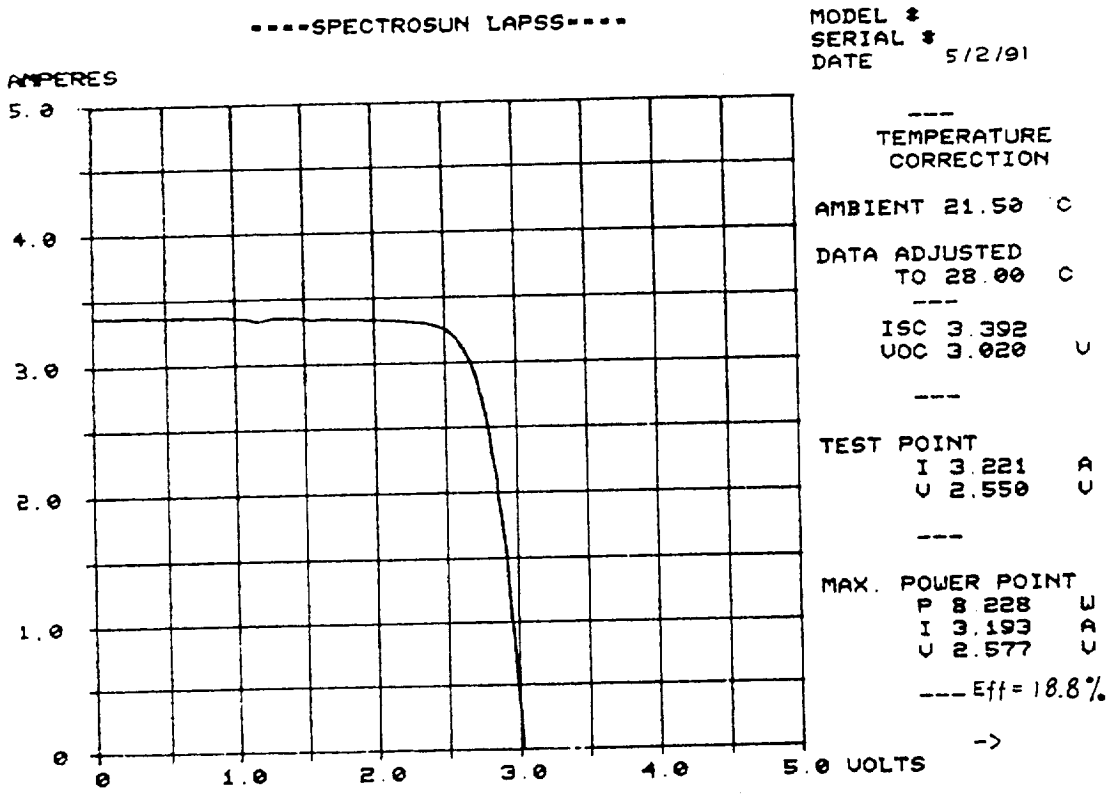

Figure 8 I-V Curve of 6 x 6 cm^2 Thin Cells (3S, 3 P Panel)

These panels have withstood standard space qualification testing conditions.

Other users have successfully mounted these thin, large area cells on lightweight flexible cells as well as other lightweight rigid panels.

3.7 Costs

Although costs depend on cell specification and quantities, we have demonstrated that the reduced material costs and higher mechanical yields have resulted in a significant reduction in costs of GaAs cells grown on Ge substrates.

4.0 CONCLUSIONS

We have demonstrated the advantages of using Ge substrates for supplying large area, lightweight, highly efficient GaAs cells. These cells and panels made from them, have passed typical qualification tests. These results have provided the foundation for firm estimates of controlled yields and lower costs for high production rates, and have helped to increase the demand for these cells for a variety of space missions, both military and commercial.

Acknowledgment

Part of this work reported was suggested by the MANTECH Directorate of the Air Force.