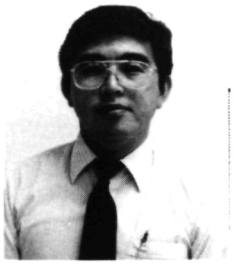


Masaki Togai, Ph.D.

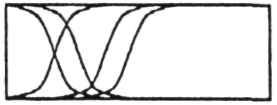
Togai InfraLogic, Inc.
Westlake Village,
California

Dr. Togai received his M.S. and Ph.D. degrees in electrical engineering in 1977 and 1982, respectively, from Duke University. He is president and chief executive officer of Tagai InfraLogic, Inc. Dr. Togai has spent the last 10 years leading fuzzy logic development groups at Duke University, AT&T Bell Laboratories, and Rockwell International. He is best known in the industry for developing the world's first fuzzy microchip for real-time approximate reasoning. He is a member of the board of directors of the North American Fuzzy Information Processing Society (NAFIPS), a member of the American Association of Artificial Intelligence, IEEE, International Fuzzy Systems Association (IFSA), and Sigma xi. In addition, Dr. Togai is the editor-in-chief of the Japan Artificial Intelligence Newsletter; and is an associate editor for the Information Sciences, and the Journal of Approximate Reasoning. He is an author of two books: "Intelligent Robotic Systems", and "Approximate Reasoning in Expert Systems". He has authored and coauthored more than 30 papers.

FUZZY AND NEURAL NET PROCESSOR AND ITS PROGRAMMING ENVIRONMENT

Abstract

The fuzzy logic inference processor (FLIP) is a slave processor designed to speed rule evaluation in high-speed, real-time oriented expert systems. It interfaces easily as a slave processor to standard microprocessors and microcontrollers, and is capable of operating without intervention from the host system. The FLIP device is capable of inferencing using two distinct paradigms: fuzzy and neural. The fuzzy paradigm grades the observation values as to their degree of support of the premise, then weighs and merges conclusions based upon the degree of support each premise receives. The neural paradigm weighs each of the inputs, sums all of the weighted inputs, then applies a transfer function to derive the output. Any combination of these paradigms may be included in a knowledge base. The software system to support the development of fuzzy logic system or neural net descriptions for the FLIP is also under development. This user friendly software interfaces FLIP for evaluation of fuzzy and neural systems, allowing considerable flexibility in developing rules and rule evaluations with capacity for trace and truth maintenance. Use of symbolic representation and "human definitions" greatly simplifies the job of knowledge acquisition.



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SOFTWARE ENVIRONMENT

Software developed in ANSI Standard C

Graphical interface developed in Microsoft Windows ™

- Uniform graphical interface
- Screen-cut & text/graphics for documentation
- DOS executive provided

Graphical environment provides ease of knowledge acquisition

- Schematic representation of networks

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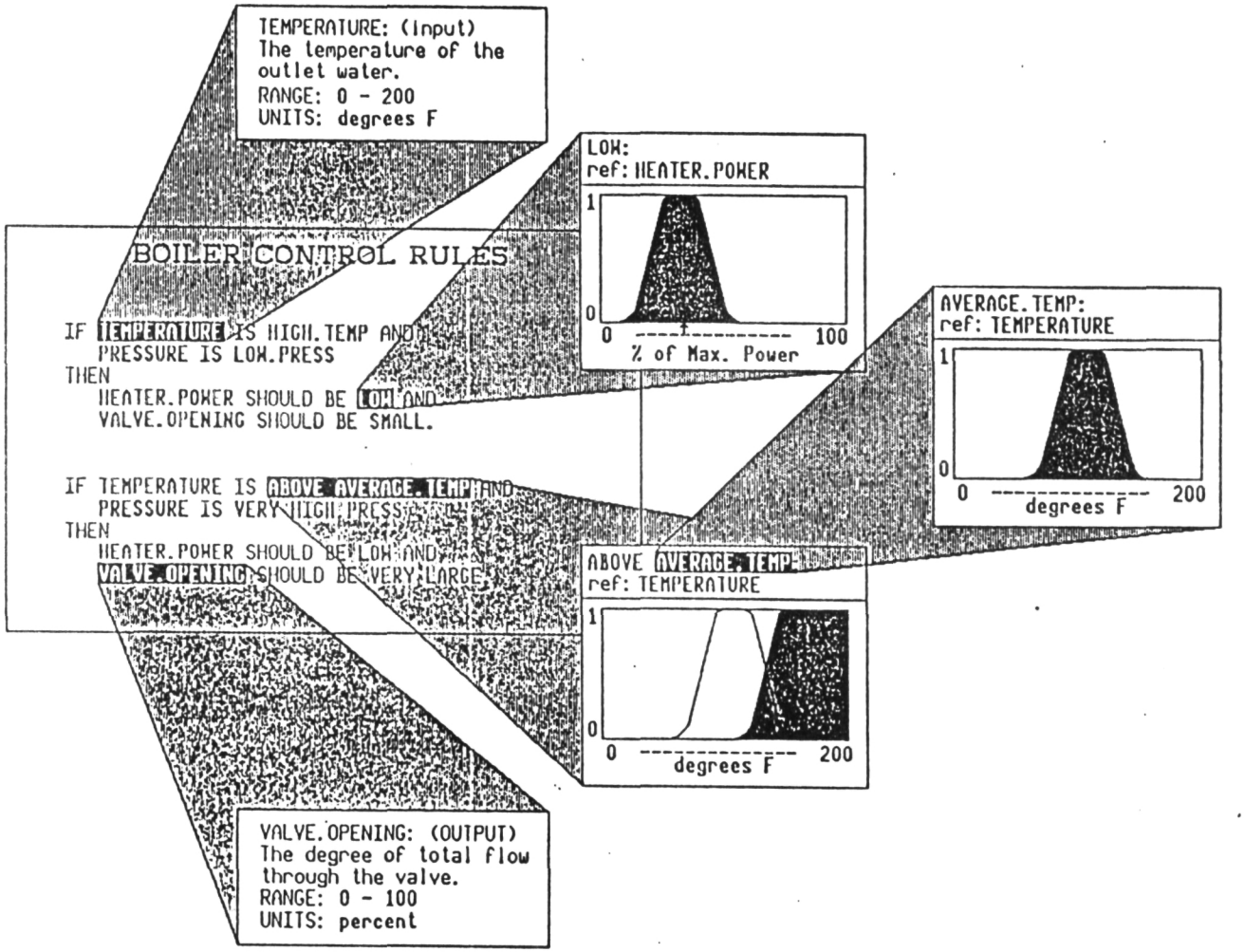
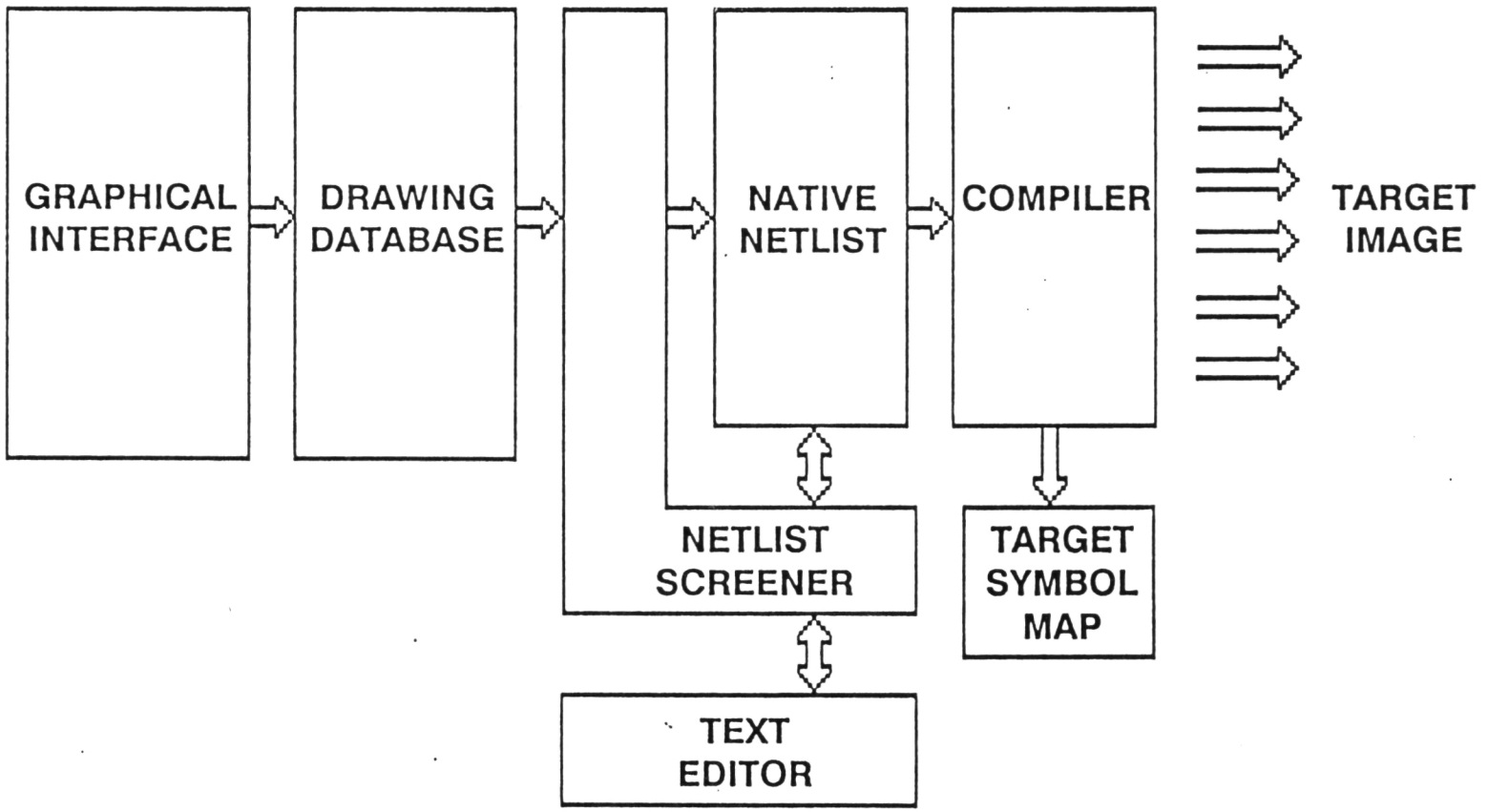
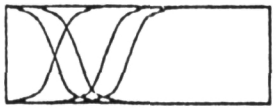


HYPERTEXT CONCEPT



TIL SOFTWARE ENVIRONMENT



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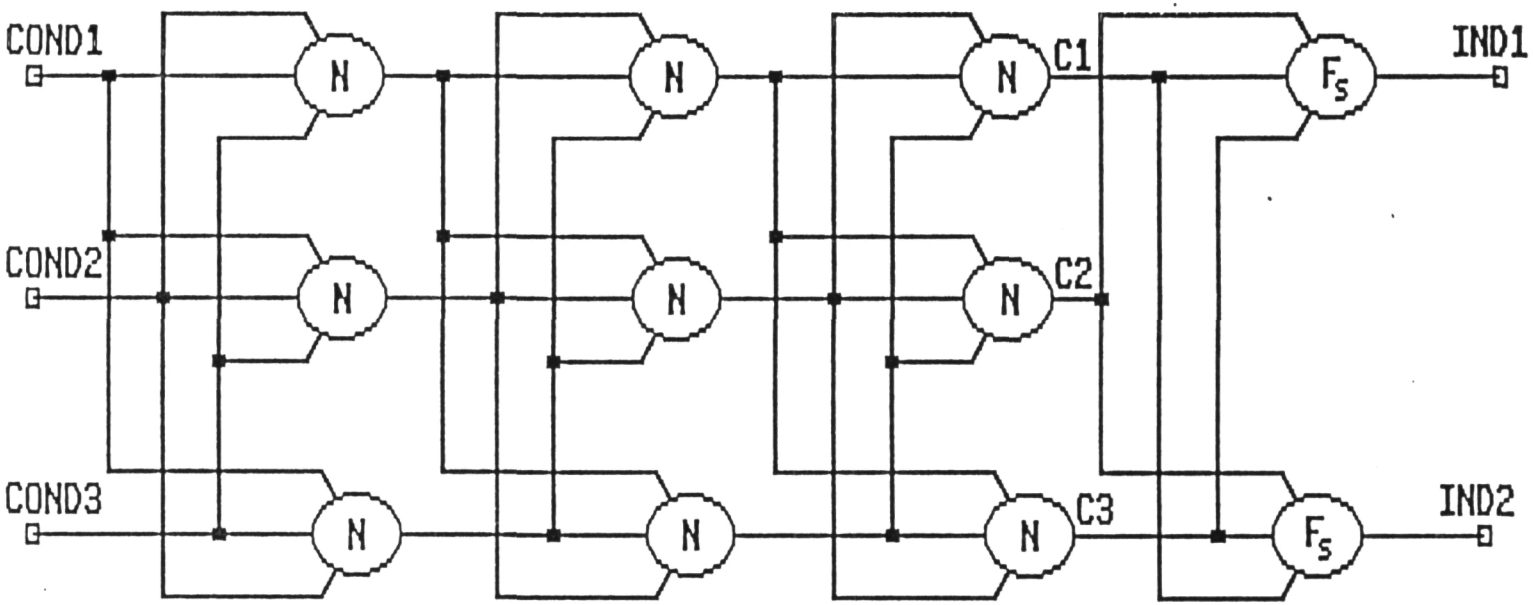

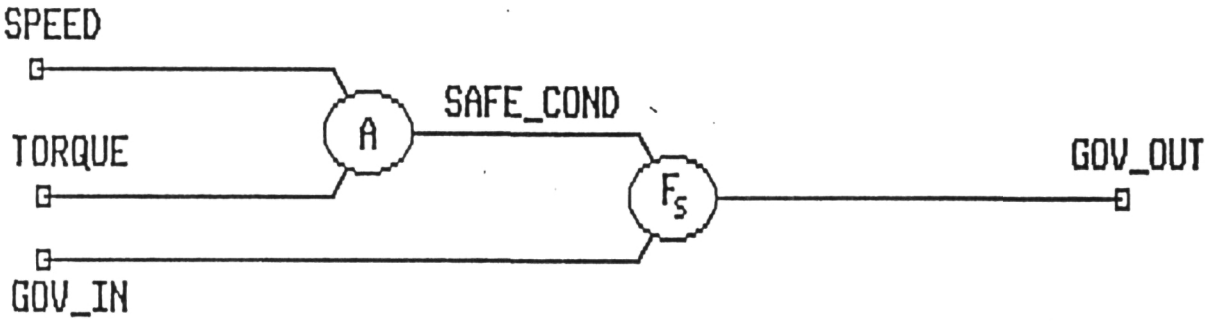

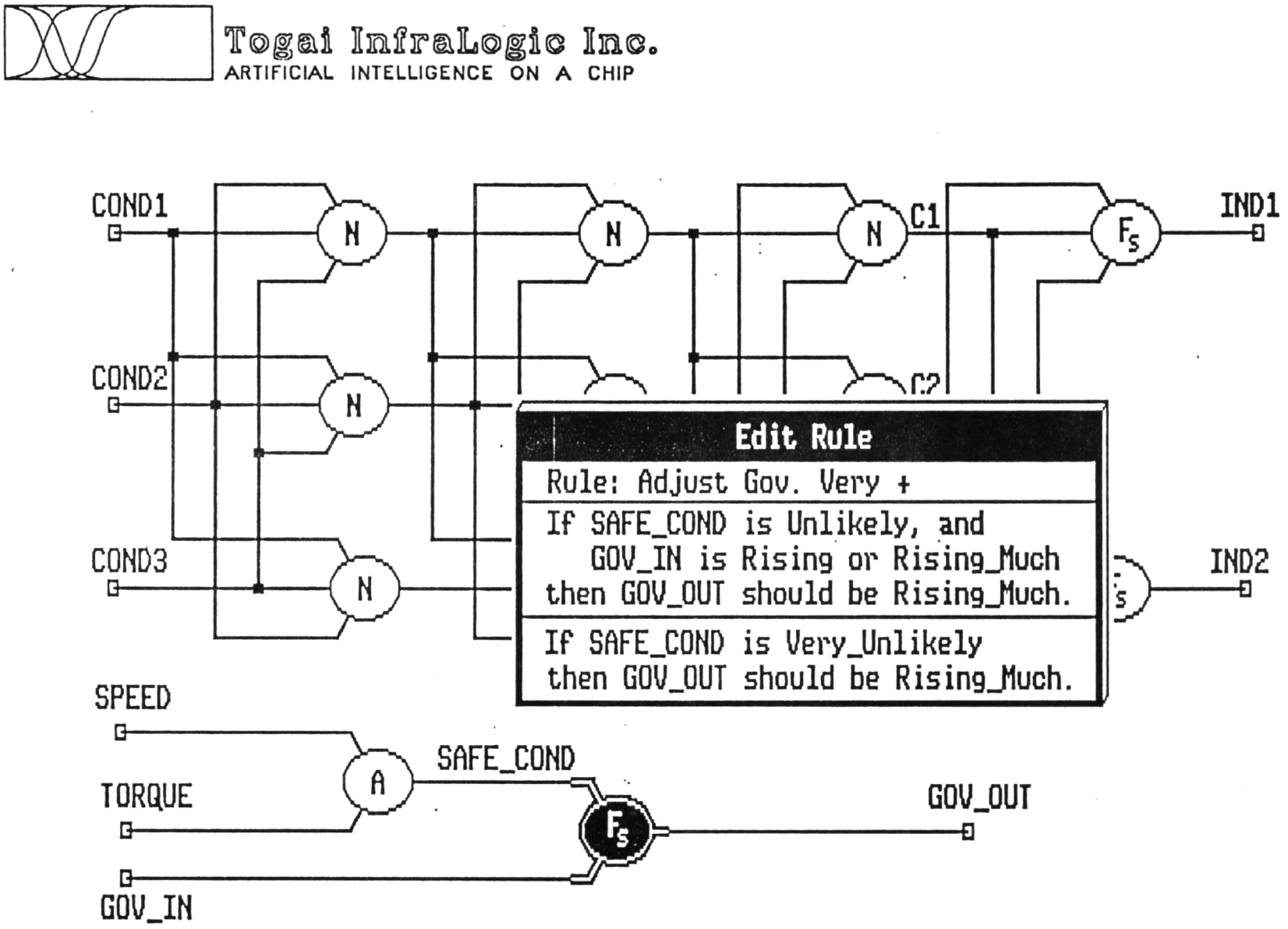
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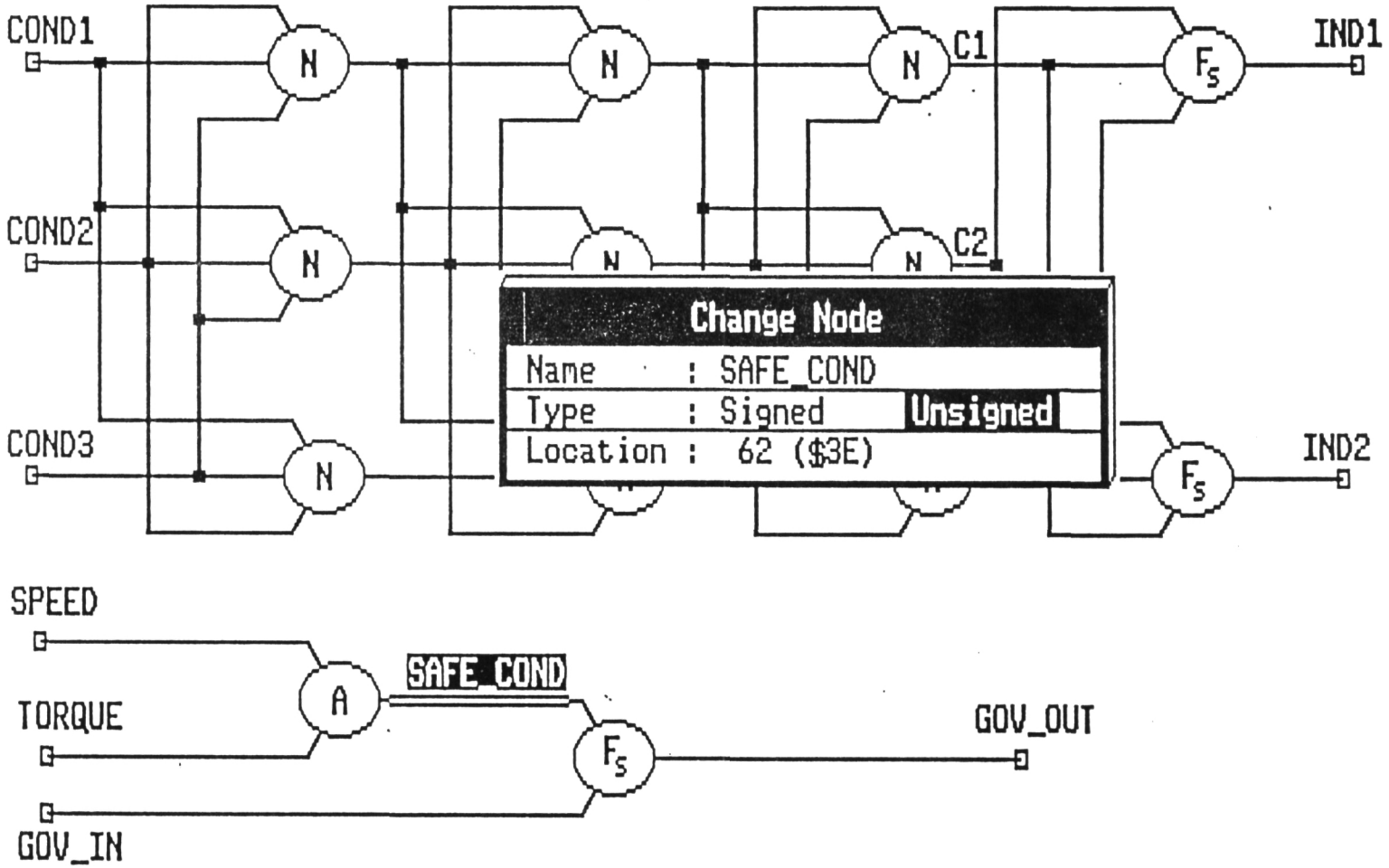
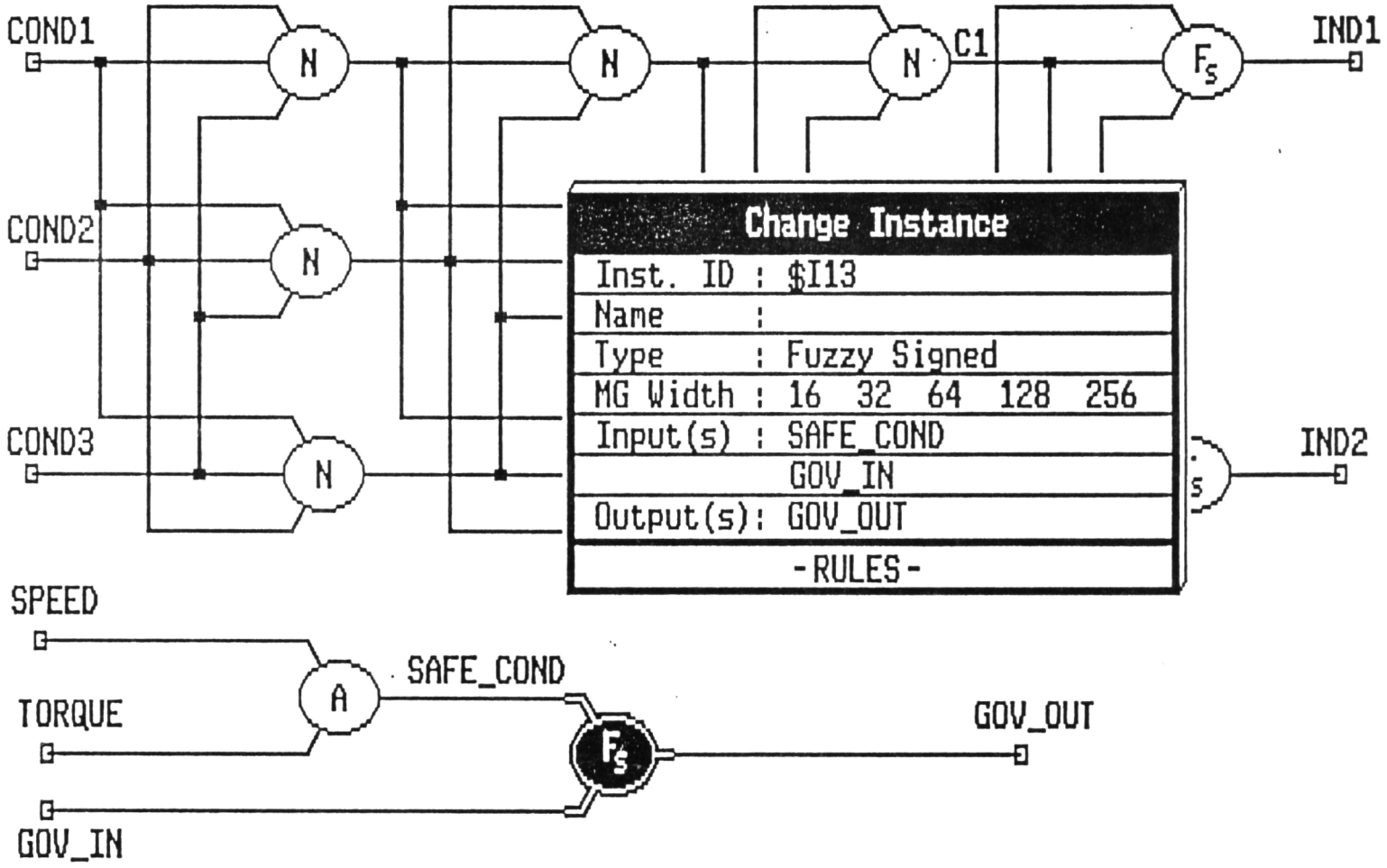
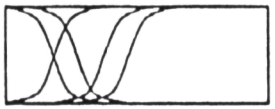
COND1
COND2
COND3
N
N
N
N
C1
C2
IND1
IND2
Edit Rule
Rule: Adjust Gov. Very +
If SAFE_COND is Unlikely, and
GOV_IN is Rising or Rising_Much
then GOV_OUT should be Rising_Much.
If SAFE_COND is Very_Unlikely
then GOV_OUT should be Rising_Much.
SPEED
TORQUE
GOV_IN
A
SAFE_COND
GOV_OUT

VIEW17


COND1
COND2
COND3
N
C1
C2
IND1
IND2
Fs
Change Node
Name : SAFE_COND
Type : Signed
Unsigned
Location : 62 ($3E)
SPEED
TORQUE
GOV_IN
A
SAFE_COND
GOV_OUT


COND1
COND2
COND3
N
N
N
N
C1
F_S
IND1
IND2
Change Instance
Inst. ID : $I13
Name :
Type : Fuzzy Signed
MG Width : 16 32 64 128 256
Input(s) : SAFE_COND
GOV_IN
Output(s): GOV_OUT
-RULES-
SPEED
TORQUE
GOV_IN
A
SAFE_COND
GOV_OUT

VIEW16



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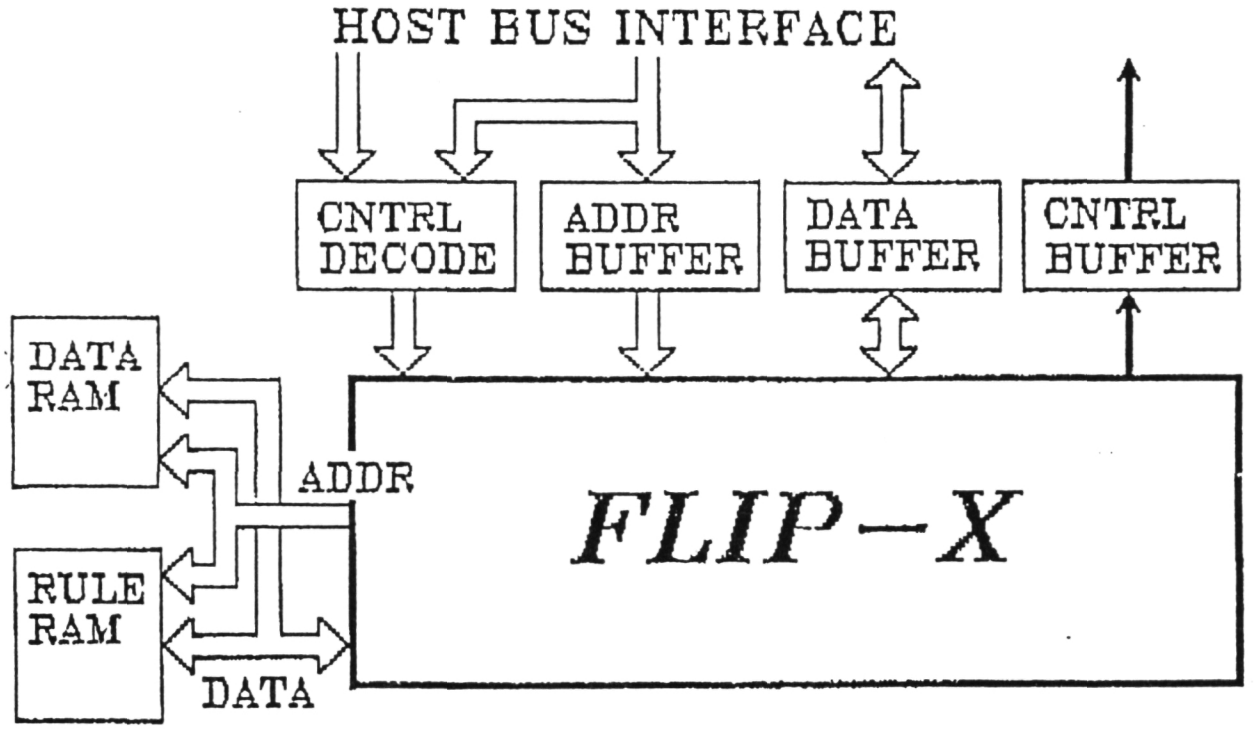
ARTIFICIAL INTELLIGENCE ON A CHIP

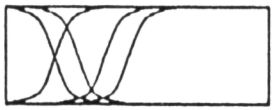
TIL HOST SYSTEM CONFIGURATION

Host System : Togai InfraLogic 386 PC

Minimum Configuration:
- Processor: 16MHz 386
- Memory: 2 Mb
- Monitor: EGA color
- Disk Memory: 20Mb hard disk or greater
  - 1.2 Mb floppy disk drive
  - 360 Kb floppy disk drive
- Disk Operating System: DOS 3.2 or higher
- Slot Configuration: 6 AT slots

Additional Hardware;
- Togai InfraLogic Net-Processor Board
- Togai InfraLogic General Purpose I/O Board


HOST BUS INTERFACE
CNTRL DECODE
ADDR BUFFER
DATA BUFFER
CNTRL BUFFER
DATA RAM
ADDR
FLIP-X
RULE RAM
DATA



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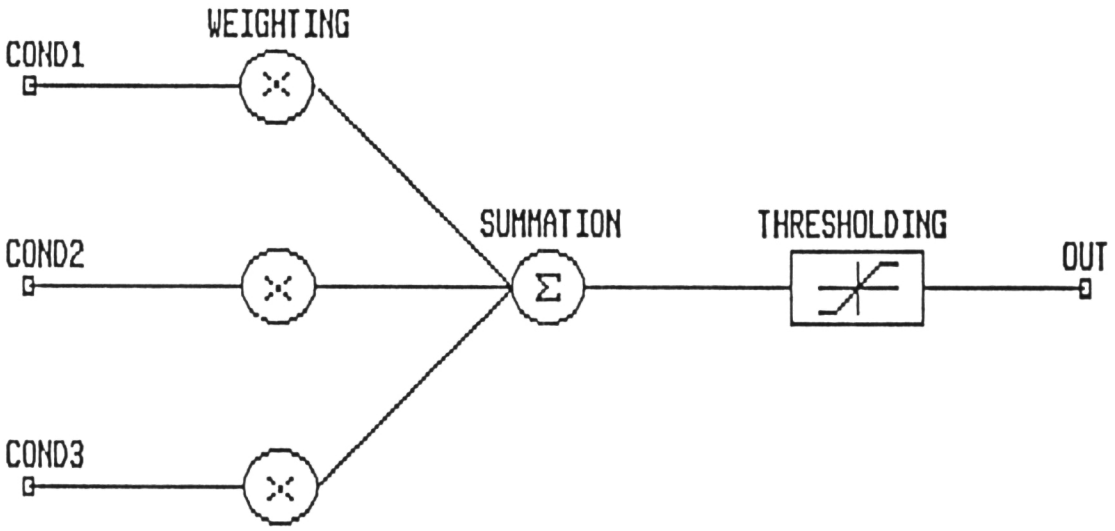
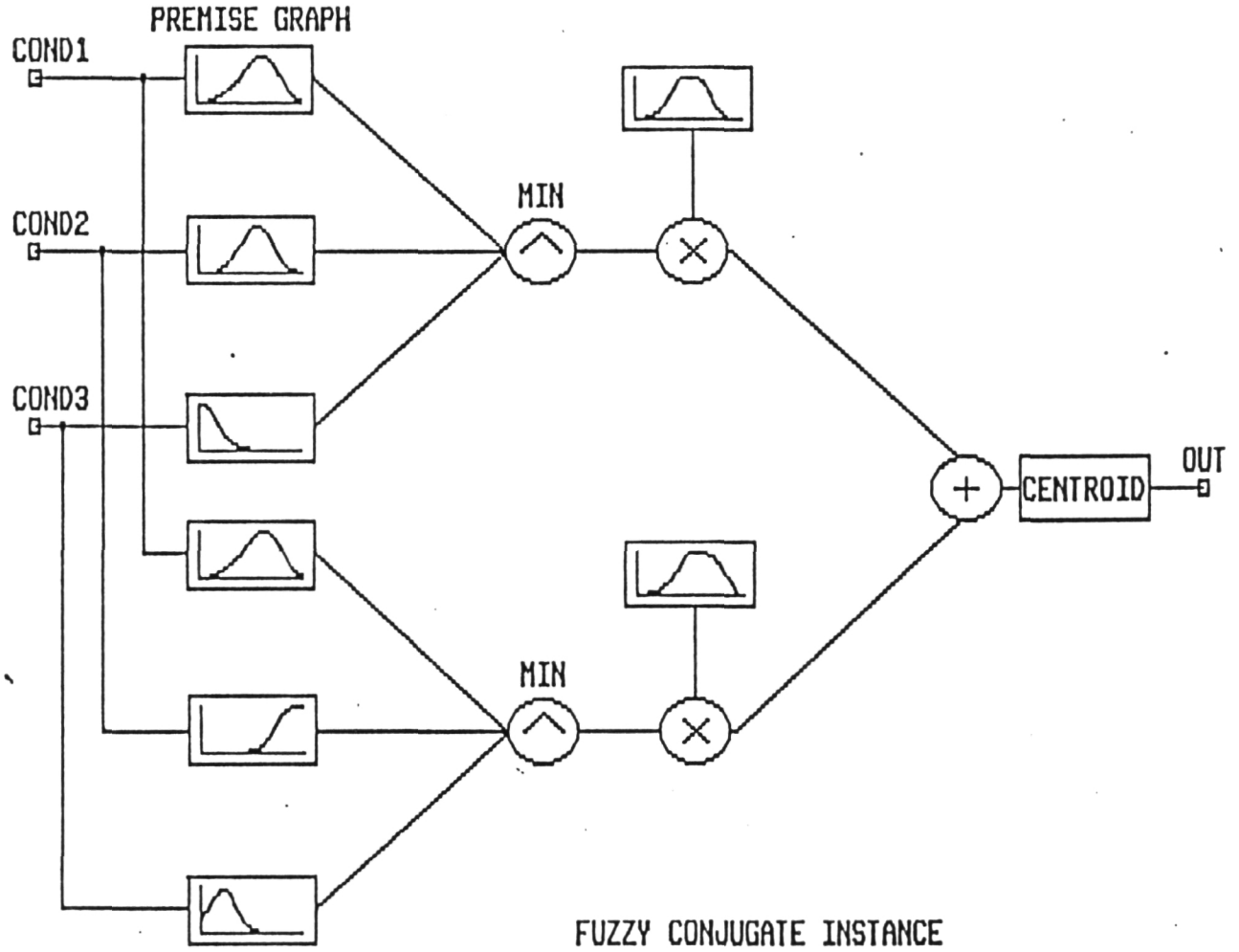
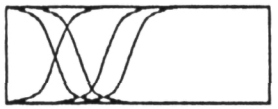


NEURAL COMPUTATIONAL NODE



FUZZY CONJUGATE INSTANCE

VIEW13



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FUZZY NET

Real-Time Inferencing

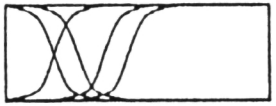
Knowledge Acquisition Support Software

Flexibility of Connection & Membership Graphs

Eight Bit Computational & I/O Resolution

Trace Back & Storage

Reduction in Chip Level I/O



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ARTIFICIAL INTELLIGENCE ON A CHIP

TIL NEURAL PARADIGM

Real-Time Processing

Flexibility of Connection

Eight Bit Computational & I/O Resolution

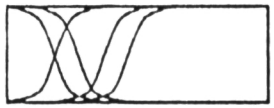
Weighting Accuracy 1%

All Nodes Resident & Visible

Reduction in Chip Level I/O

10^3 X Connectivity of Analog Solutions

Stable Across Voltage and Temperature



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ARTIFICIAL INTELLIGENCE ON A CHIP

NOTABLE SYSTEM PERFORMANCE

CHIP

- Single Chip Net Processor
- Scalable SIMD Architecture
- Cascadable to MSIMD Architecture
- 10-20 MHz Clock Rate

FUZZY APPROXIMATE REASONING

- Processes up to 128 Production Rules Simultaneously
- Up to 256 Inputs and Outputs per Production Rule
- Greater than 20K FLOPs
- Greater than 200K Production Rule Evaluations per Second

NEURAL PROCESSING

- Processes up to 16 Neurons Simultaneously
- Greater than 65,000 Inputs per Neuron
- Transfer Function User Definable
- Greater than 2M Connections per Second