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# A RECONFIGURABLE MULTICARRIER DEMODULATOR ARCHITECTURE

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## ABSTRACT

An architecture based on parallel and pipeline design approaches has been developed for the FDMA/TDM conversion system. The architecture has two main modules namely the transmultiplexer and the demodulator. The transmultiplexer has two pipelined modules. These are the shared multiplexed polyphase filter and the FFT. The demodulator consists of carrier, clock and data recovery modules which are interactive. Progress on the design of the MCD using commercially available chips and ASIC and simulation studies using Viewlogic software will be presented at the conference.

## INTRODUCTION

Presently most satellite communication systems require a large earth station to supply a network with multiplexed speech and video channels. In the future, satellite communication systems will consist of a large number of small capacity, multi-service users. For these systems the conventional transmission methods of FDMA or TDMA access are no longer efficient. One approach to offer these services at a low cost to the user is to use SCPC/FDMA on the uplink and TDM on the downlink [1-3]. The problem with this type of communication is that it transfers the burden of computation on-board the satellite, where power and area requirements are critical. It can thus be seen that hardware that is efficient in terms of speed, power consumption and components needs to be developed for performing the computations on board the satellite. To perform the FDMA/TDM conversion , a Multicarrier Demodulator (MCD), baseband switch matrix, TDM multiplexer and modulator are required on board the satellite. The MCD consists of a transmultiplexer followed by a bank of demodulators. The transmultiplexer is required to separate the FDMA signal into individual channels. The bank of demodulators take the separated channels and recover the data from them.

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To take advantage of the developments in the area of VLSI and digital systems, a digital implementation of the reconfigurable MCD has been proposed [3,5]. The algorithm selected for performing the transmultiplexing is the polyphase FFT method. The polyphase FFT algorithm consists of a filter bank followed by a FFT operation [4,9]. A PROgrammable DEModulator (PRODEM) which uses a single shared device to demodulate all the channels has also been proposed [5]. The demodulator consists of three modules namely carrier recovery, clock recovery and data recovery [6-8].

## SYSTEM DESIGN

Quadrature sampling is used to digitize the analog signal so that the components used in the architecture can operate at a lower rate and also because the complex representation is compatible with the FFT. The RTMUX is capable of demultiplexing channels in three different cases. The three cases are :

1) 800 channels at 64 Kb/s each.
2 (a) A mix of 400 channels at 64 Kb/s and 2 (b) 12 channels at 2.048 Mb/s each.
3) 24 channels at 2.048 Mb/s each.

Since case 2 is a mix of two carriers, each carrier having its own demultiplexing characteristics, it is split into its two constituent parts 2(a) and 2(b) so that each case can then be demultiplexed individually.

The system diagram of the Reconfigurable Transmultiplexer (RTMUX) that is capable of demultiplexing the above three cases is shown in Fig. 1. The front end of the RTMUX consists of a demultiplexer that routes the input FDMA signal to one of the three modules, namely, modules 1, 2 and 3 whose functions are described below. Since cases 2(a) and 2(b) are part of case 2 and each occupies half of the total spectrum, they need to be split into two halves. The individual channels can then be demultiplexed from the two halves. Module 1 is used to split the input FDMA signal into two halves for cases 2(a) and 2(b). Module 2 is designed to demultiplex either case 1 or case 2(a) by reconfiguring itself. Similarly module 3 is designed to demultiplex either case 2(b) or 3 by reconfiguring itself. A Reconfigurable Shared Filter Bank has been designed and is shown in Fig. 2. The FFT pipeline proposed in [3,4] is made reconfigurable by varying the number of FFT stages in the pipeline and by having a programmable FFT coefficient and address generator. A N-1/N stage RFFT that can perform either a $2^{N-1}$ or $2^N$ FFT is shown in Fig. 3. A multiplexed AE (MAE), to implement the FFT butterfly operation is designed along with its interface to the other components in the RFFT pipeline and is shown in Fig. 4.

## Programmable Demodulator (PRODEM)

The PRODEM consists of three main modules namely Multiplexed Carrier Recovery Module (MCRM), Multiplexed Timing Recovery Module (MTRM) and Multiplexed Data Recovery Module (MDRM). The hardware is constructed to demodulate all the channels simultaneously. The number of channels can be varied as long as the total bit rate is below the maximum bit rate sustained by the modules. Moreover the bit rate of a group of channels could also vary.

A MCRM is designed to obtain the carrier phase for each of the channels. Samples of several channels are input serially to this module. At the same time these samples are also input to the Multiplexed RAM Buffer for Samples (MRBS) which stores these samples to be operated on later by the phase recovered information of the MCRM. The output of the MCRM module will be needed by the MDRM. The in-phase and quadrature-phase samples of the channels are input to the MCRM as shown in Fig. 5.

A MRBS is designed to store the incoming samples for the duration of an estimation interval and is shown in Fig. 6. The MCRM operates on the samples obtaining the carrier phase for the channels. Also, at this time the input samples are buffered in the MRBS. The MDRM uses the output of the MCRM along with the stored values of MRBS to recover the digital data. This design uses a single RAM-Latch combination at each stage to store samples of different channels corresponding to each AGC cycle.

A MDRM is designed to extract the digital information. It operates on the samples processed by the MCRM and MRBS. The hardware design is shown in Fig. 7. The MDRM module utilizes the in-phase and quadrature-phase samples from the MRBS along with the sine and cosine values of the MCRM to extract the digital data for all the channels. At any time four values are input to this module. The output is computed and stored in a latch preceeding the Digital Data RAM (DDR). Also, these values are used as an input to the MTRM. After the necessary computations are performed the results are stored in unique locations of the Digital Data RAM (DDR).

A MTRM is designed to extract the timing information needed for tracking the input samples and is shown in Fig. 8. This timing information is used by the interpolator. Its input is available from the latches used preceeding the DDR of the MDRM. The output of these latches is used as an input to the MTRM. The combination of the four modules namely MCRM, MRBS, MDRM and MTRM is collectively called a PRODEM. These four modules need to be appropriately interfaced. The addressing scheme, control circuitry and the integration of addressing units for all the modules need special

attention. A design for each of the modules with proper interfaces is shown in Fig. 9.

## CONCLUSION AND FUTURE DIRECTIONS

In this paper parallel, pipeline and time sharing concepts are used in the design of a digital MCD. The MCD consists of the TMUX and the PRODEM. The TMUX is implemented by means of a shared filter bank module and a pipelined FFT module. The PRODEM consists of three modules namely carrier, clock and data recovery modules, which have been optimized for high speed demodulation. The shared filter bank and PRODEM process the channels in a time multiplexed manner. At present we are designing both TMUX and PRODEM both at the board and ASIC levels.

## REFERENCES


[1] G.Perrota and G.Losquadro, "FDMA/TDM satellite communication systems for domestic/business services", Proceedings International Conference on Digital Satellite Communication -7, pp. 155-162, 1986.

[2] B.G.Evans and F.P.Coakley, "Multi carrier demodulators for OBP satellites", International Journal of Satellite Communication, Vol 6, pp. 243-251, 1988.

[3] J.Campanella and S.Sayegh, "Onboard multichannel demultiplexer/demodulator", NASA contract no cr 1801827 , 1987.

[4] P.J.Fernandes, "A Reconfigurable Transmultiplexer Architecture", M.S.Thesis, University of Toledo, 1991.

[5] L.P.Eugene, "A Parallel Pipelined Architecture for a Multi Carrier Demodulator", M.S.Thesis, University of Toledo, 1991.

[6] E. Del Re and R. Fantacci, "Alternatives for onboard digital multicarrier demodulation," International Journal of Satellite Communications, Vol. 6, pp. 267-281, 1988.

[7] A. J. Viterbi and A. M. Viterbi, "Non-linear estimator of PSK modulated carrierphase with application to burst digital transmission," IEEE Transactions on Information Theory, IT-29, pp. 543- 551, 1983.

[8] F. M. Gardner, "A BPSK /QPSK timing error detector for sampled receivers," IEEE Transactions on Communications, COM-34, pp. 423-429, 1986.

[13] M. Bellanger and P. Daguet , "TDM/FDM transmultiplexers: digital polyphase and FFT," IEEE Transactions on Communication , pp. 1199-1205, Sep. 1974.

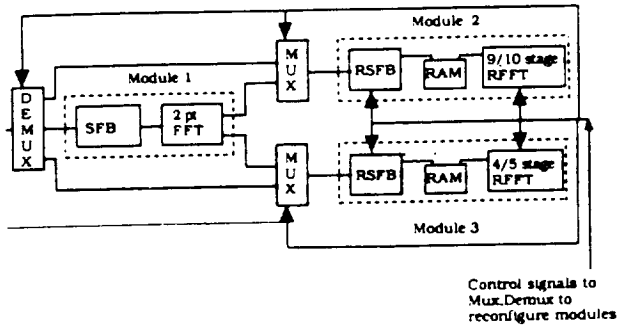


Fig. 1. Reconfigurable Transmultiplexer (RTMUX)

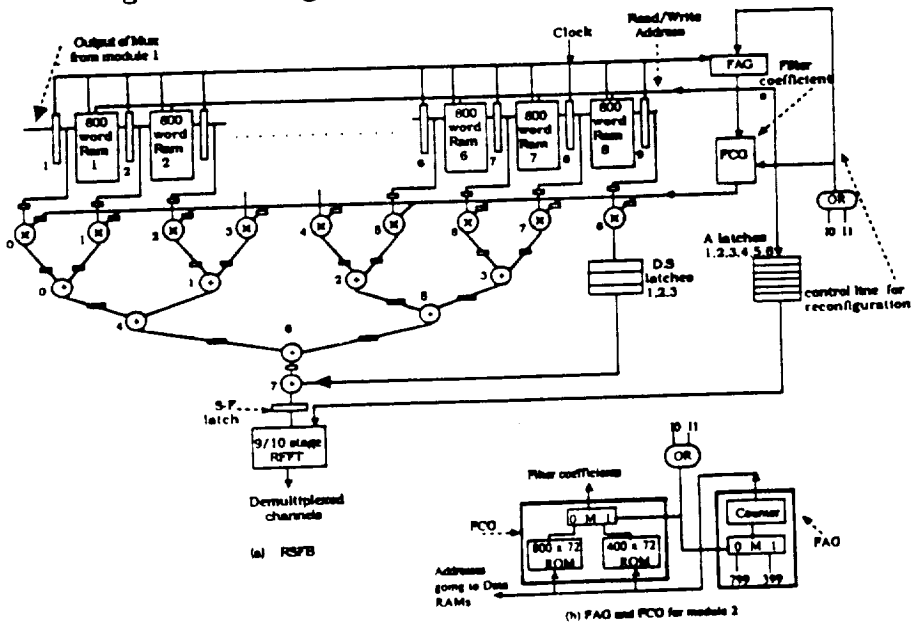


Fig. 2. Reconfigurable Shared Filter Bank (RSFB)

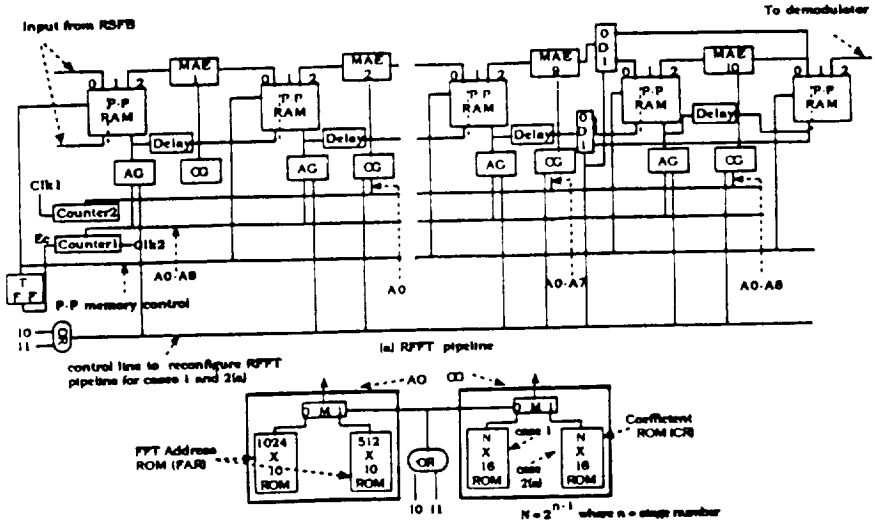


Fig. 3. N-1/N Stage RFFT

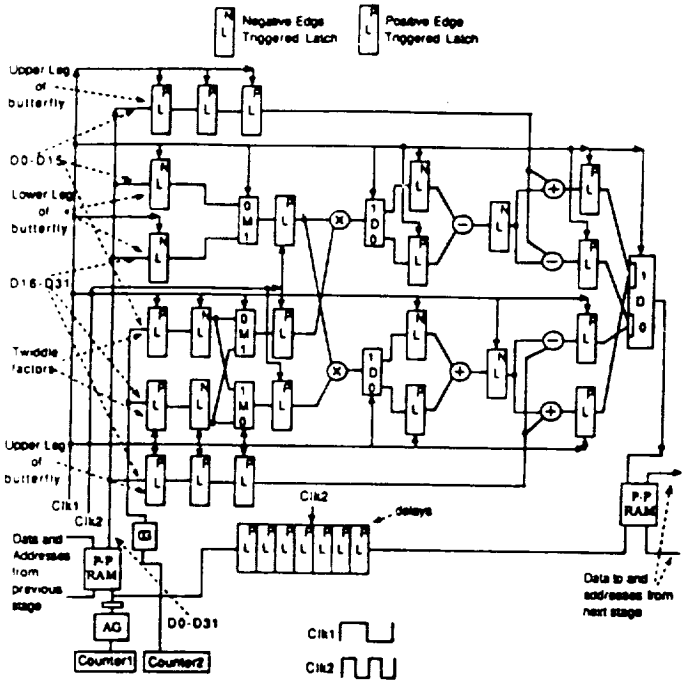


Fig. 4. Detailed Implementation Structure of the MAE in the RFFT

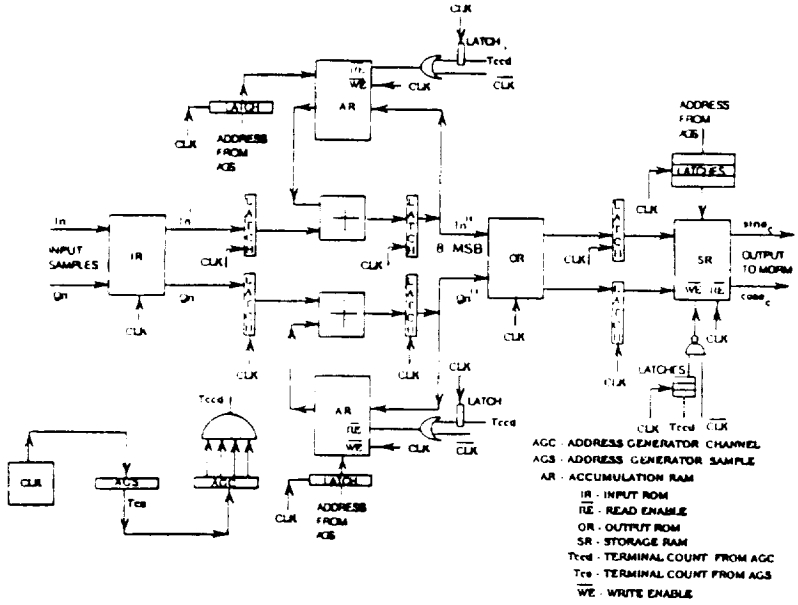


Fig. 5. Multiplexed Carrier Recovery Module (MCRM)

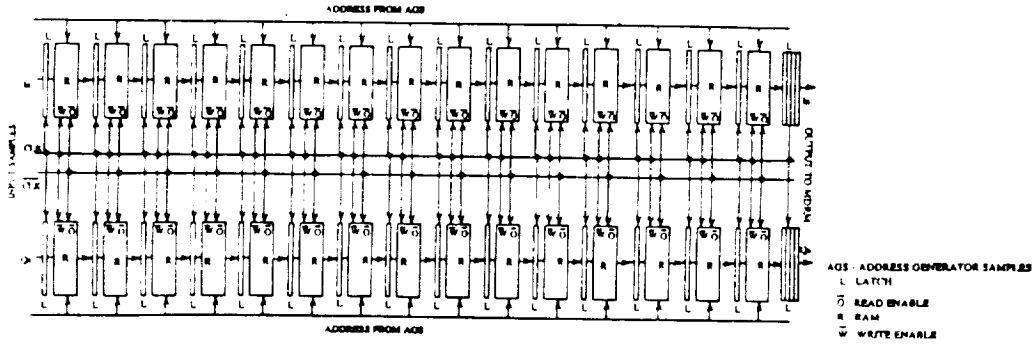


Fig. 6. Multiplexed RAM Buffer for Samples (MRBS)

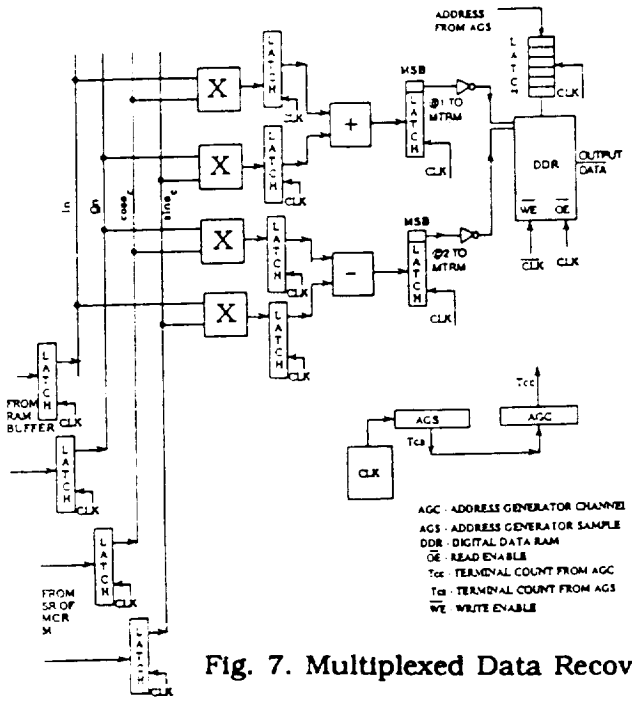


Fig. 7. Multiplexed Data Recovery Module (MDRM)

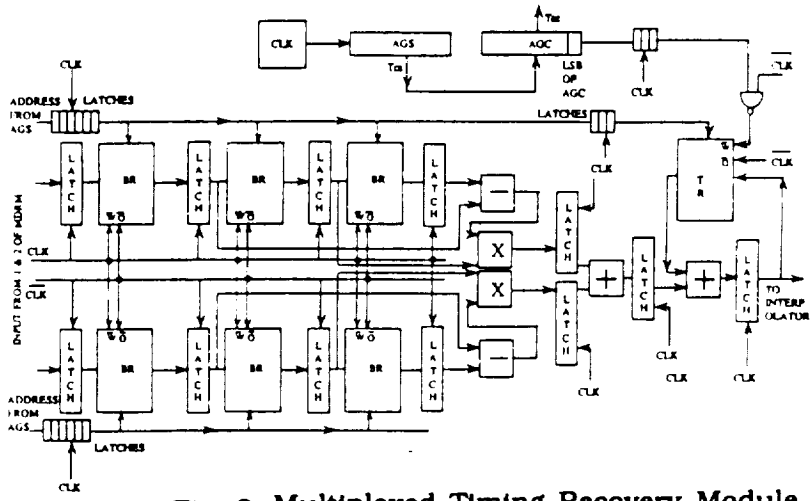


Fig. 8. Multiplexed Timing Recovery Module (MTRM)

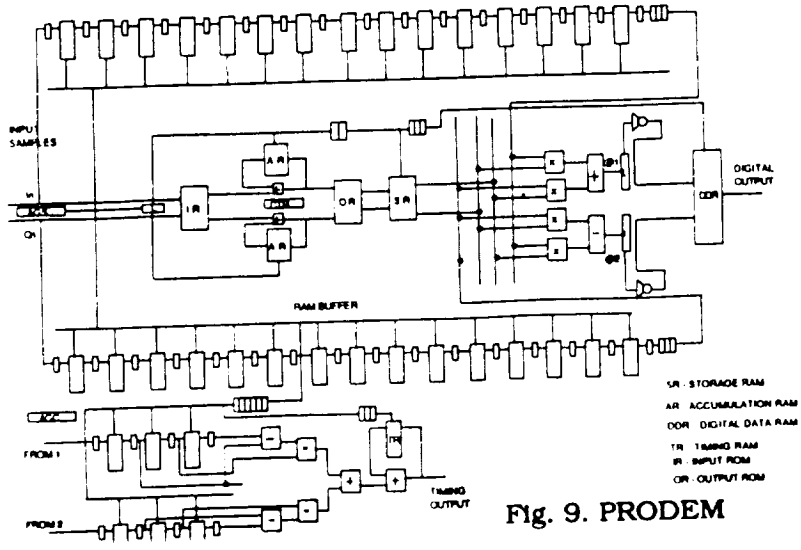


Fig. 9. PRODEM