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APPLICATION OF CONVOLVE-MULTIPLY-CONVOLVE SAW PROCESSOR FOR SATELLITE COMMUNICATIONS*

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ABSTRACT

There is a need for a satellite communications receiver that can perform simultaneous multi-channel processing of single channel per carrier (SCPC) signals originating from various small (mobile or fixed) earth stations. The number of ground users can be as many as 1000. Conventional techniques of simultaneously processing these signals is by employing as many RF-bandpass filters as the number of channels. Consequently, such approach would result in a bulky receiver, which becomes impractical for satellite applications. A unique approach utilizing realtime surface acoustic wave (SAW) chirp transform processor is presented. The application of a Convolve-Multiply-Convolve (CMC) chirp transform processor is described. The CMC processor transforms each input channel into a unique timeslot, while preserving its modulation content (in this case QPSK). Subsequently, each channel is individually demodulated without the need of input channel filters. Circuit complexity is significantly reduced, because the output frequency of the CMC processor is common for all input channel frequencies. The results of theoretical analysis and experimental results are in good agreement.

I. INTRODUCTION

On-board processing of digital communications signals is necessary to maintain good performance quality of satellite repeaters. In the case of SCPC transmissions the necessity for a large number of analog filters can be avoided by utilizing a Fourier transform processor. Realtime Fourier transforms can be obtained via SAW chirp transformers. In this system, each channel is transformed into a timeslot at the output of the processor. These timeslots are organized in a frame defined by the chirp period of the processor. Figure 1 describes the timing architecture of a QPSK receiver, where detection of two channels are shown. It is clear that the entire network must be synchronized in order for the system to function. In Figure 2 a functional diagram of the receiver is shown. In this case a CMC processor is used. The advantage of utilizing the CMC processor is its inherent ability to transform each input carrier frequency into the time domain on a common frequency. Consequently, only a single circuit is needed for demodulation. The framelength of the processor is made equal to the symbol period of the QPSK signal, hence each channel processor has that length of time to make symbol decisions. However, if all users are transmitting simultaneously, then the signals at the output of the demodulator are generated at a much faster rate. Therefore, it is necessary to store these signals temporarily during processing.

II. THE CMC CHIRP TRANSFORM PROCESSOR

The CMC chirp transform processor model is shown in Figure 3. The input and output filters have an impulse response with a positive slope (i.e. an up-chirp) as shown,

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where the rate of the linear frequency change is equal to 2k. The chirp generator produces a linear frequency chirp that has a negative slope equal to -2k. It has been shown elsewhere (Ref. 1,2) that the time-bandwidth product of the input and output filters has to be identical (BT), while the chirp generator time-bandwidth product must be at least four times larger (4BT). Note that the input filter has an inherent characteristic of delaying high frequency signals more than low frequency signals. It will be shown later that the output frequency of the CMC chirp transform is constant (ω_2).
To generalize the analysis, the input signal is represented in complex form, as follows:

$$S_i(t) = e^{j\omega st} \text{ ---------- (1)}$$

The output of the input filter is delayed by d seconds, where d is dependent on the input frequency ω_s, hence

$$S_i(t-d) = e^{j\omega s(t-d)} \text{ ---------- (2)}$$
$$d = (\omega_s - \omega_o)/2k \text{ ---------- (3)}$$

In the Multiplier, the product of the delayed input signal and the chirp signal is generated. This product is convolved with the impulse response of the output filter to produce the output signal $S_o(t)$, therefore,

$$S_o(t) = \int_{-T/2}^{T/2-\tau} x(t).y(t).h_2(\tau - t)d(t) \text{ ---------- (4)}$$
$$\text{For } 0 \le \tau \le T/2$$

Where, x(t) is given by (2), and y(t) and $h_2(t)$ are as follows,

$$y(t) = \text{Exp}[j(\omega_1 t - kt^2] \text{ ---------- (5)}$$
$$h_2(t) = \text{Exp}[j(\omega_2 t + kt^2)] \text{ --------- (6)}$$

Since the input signal $S_i(t)$ is complex, the output, $S_o(t)$, of the processor is also complex. In this analysis, only the real part of $S_o(t)$ is considered. It can be shown that,

$$R_e[S_o(t)] = \text{Cos}[-\omega_s d + \omega_2 \tau + k\tau^2 + k\epsilon\tau]x(T-\tau)(\text{Sinc } q) \text{ ----- (7)}$$

Where,

$$\text{Sinc } q = (\text{Sin } q)/q$$
$$q = [(\omega_s + \omega_1 - \omega_2 - 2k\tau)(T-\tau)/2]$$

ϵ is defined as,

$$\epsilon = \tau - (\omega_s + \omega_1 - \omega_2)/2k \text{ ---------- (8)}$$

ω_s, ω_o, ω_1, and ω_2, are as defined in Figure 3.

Based on the above model, a computer analysis is performed to demonstrate the transform output of a CW input signal. The CMC chirp transform parameters used for this purpose are as follows:

Input frequency: $f_s = 100$ MHz, $\omega_s = 2\pi f_s$
Center frequency of input filter: $f_o = 100$ MHz
Center frequency of output filter: $f_2 = 300$ MHz
Center frequency of the chirp: $f_1 = 200$ MHz
Time-Bandwidth product of the input and output filters is: BT = 512
Time-Bandwidth product of the chirp generator is: 4BT = 2048
The chirp slope is: $2k = 4.2 \times 10^6 \pi$ mrad/second

As can be seen from equations (3) and (8), when the input frequency f_s is equal to f_o, d = 0, and $\epsilon = \tau$. The computer analysis result is shown in Figure 4. The output frequency is

300 MHz, and the envelope of the waveform is a sinc function given by (7). The width of the mainlobe (null-to-null) is approximately 60 nanoseconds, and the peak of the largest sidelobe is 13.5 dB below the main peak as expected from the sinc characteristic. In a multichannel communications system the sidelobes must be suppressed to prevent adjacent channel interference. For that purpose a weighting function can be designed into the SAW chirp filter. In what follows, sidelobe reduction is demonstrated by utilizing Hamming weighting.

III. THE EFFECT OF HAMMING WEIGHTING

To reduce the sidelobes of the chirp transform output, Hamming weighting can be incorporated in the SAW dispersive filter or in the chirp generator. In practice the basic chirp waveform is generated by a software controlled digital circuit. Therefore, it is easier to incorporate the weighting function in the chirp generator, hence the analysis is done with a weighted chirp waveform from the chirp generator. The generalized Hamming (Ref. 3) weighting function is given by:

$$W(t) = a + (1-a)\mathrm{Cos}(\pi t/T) \qquad -T \le t \le T \quad 0 \le a \le 1 \quad \text{------} \quad (9)$$

$$W(t) = 0 \qquad \text{otherwise}$$

In complex form, the chirp function becomes:

$$y(t) = a.\mathrm{Exp}[j(\omega t - kt^2)] + [(1-a)/2]\{\mathrm{Exp}\, j[(\omega + \pi/T)t - kt^2] + \mathrm{Exp}\, j[(\omega t - \pi/T)t - kt^2]\} \quad \text{----------} \quad (10)$$

The chirp transform output, $S_{oh}(t)$, with Hamming weigthing is obtained by replacing the chirp function y(t) in (4) by (10). By solving the resulting convolution integral equation and taking its real value, the transform output, for $0 \le \tau \le T/2$, is as follows:

$$\begin{aligned} R_e[S_{oh}(t)] = {} & a(T-\tau)\mathrm{Cos}[-\omega_s d + (\omega_2 + k\epsilon)\tau + k\tau^2]\,[\mathrm{Sin}\, k\epsilon\,(T-\tau)]/k\epsilon\,(T-\tau) + \\ & [(1-a)(T-\tau)/2]\mathrm{Cos}[-\omega_s d + (\omega_2 - \pi/2T + k\epsilon)\tau + k\tau^2]\,X \\ & \{\mathrm{Sin}[(\pi/T - 2k\epsilon)(T-\tau)/2]\}/[(\pi/T - 2k\epsilon)(T-\tau)/2] + \\ & [(1-a)(T-\tau)/2]\mathrm{Cos}[-\omega_s d + (\omega_2 + \pi/T + k\epsilon)\tau + k\tau^2]\,X \\ & \{\mathrm{Sin}[(\pi/T + 2k\epsilon)(T-\tau)/2]\}/[(\pi/T + 2k\epsilon)(T-\tau)/2] \qquad \text{--------} \quad (11) \end{aligned}$$

Utilizing the above equation performance of the CMC chirp transform is analyzed, and the results shown in Figure 5, for a = .54. As can be seen, the sidelobes are reduced relative to the mainlobe when compared to the result in Figure 4. Note, however, that the mainlobe is also slightly reduced. There are other weighting functions that can produce better sidelobe suppression, e.g. Taylor weighting (Ref. 4).

IV. DIGITAL CHIRP WAVEFORM GENERATOR

In the final system design, recovery of the data will require a chirp waveform of +/-32.8 MHz with a period of 31.250 microseconds. A chirp waveform generator (CWG) was designed to provide the in-phase (I) and quadrature (Q) waveforms for the system. Because the output waveforms are calculated by the CWG's firmware, the chirp characteristics can be easily modified for laboratory tests of the system.

A functional block diagram of the CWG is shown in Figure 6. A microprocessor board communicates with a terminal, host processor, or system controller via RS-232C or IEEE-488 interfaces. Chirp waveform data can either be calculated by the internal microprocessor or downloaded from the host for added flexibility. When the CWG is used with a host or IEEE-488 system controller, the resident EPROM monitor recognizes low

level commands to set the address generator and load data in each of the sixteen fast RAM (25 ns access time) chips. Other commands set the step attenuators, on-board timers, and implement debugging functions.

The address generator receives a clocking signal from the multiplexer circuitry at one-eighth of the high speed clock or 16.384 MHz. Thus adequate time is available for address setup and data access without using extremely fast RAMs. In testing, the CWG has been clocked at 250 MHz with 25 ns RAMs. During synchronous mode operation, the address generator is phase locked to a system timing signal to facilitate data channel separation in the time domain.

Each multiplexer is implemented as a sixty-four bit shift register with successive data bytes interleaved eight at a time via a sixty-four bit input latch. The data is taken out in byte parallel form as the shift register is clocked and applied to the DACs. Each DAC can drive a 37-ohm load or a doubly-terminated 75-ohm line.

Low pass filters with corner frequencies of 50 MHz are included to suppress feedthru of the sampling clock.

V. EXPERIMENTAL RESULTS

To verify the theoretical results described above, an experimental circuit was built using existing dispersive SAW filters. The circuit used for this experiment is shown in Figure 7. The dispersive SAW filters have the following characteristics:

Center frequency: 70 MHz
Bandwidth (40 dB): 20 MHz
Weighting function: Taylor
Chirp slope: .253 MHz/μsecond
Time delay: 80 microseconds

Because both SAW filters operate at the same frequency, frequency conversions have to be incorporated to construct the CMC processor so that its input and output center frequencies are the same. This is accomplished by the two mixers, ZFM-1W, shown in Figure 7. The chirp waveform generator and SSB modulator were developed for the NASA/LEWIS SBIR Contract No. NAS3-25862. The output chirp waveform of the SSB modulator is measured utilizing Hewlett Packard's 400 Msample/second digital oscilloscope, and the result is shown in Figure 8. In this diagram only the center part of the chirp is shown, because of limited resolution of the plotter to cover the entire period of the chirp. The chirp waveform was adjusted to be the same as the SAW filter chirp slope, i.e. .253 MHz/μsecond, and the chirp period is approximately 90 μseconds. Since the Time-bandwidth product of the chirp generator has to be four times the SAW filter's, only the center region of the dispersive filter's passband is used to obtain a proper transform output.

Initially, the input frequency is tuned to 70 MHz and the CMC processor output waveform is plotted as shown in Figure 9. As expected the output frequency is also 70 MHz. Subsequently, the input frequency is changed to 70.0015 MHz, and the output waveform is recorded and shown in Figure 10. Note that the output waveform is shifted in phase by 300^{o}. The significance of this result is that in order to obtain coherent demodulation of phase modulated signals, the carrier phase tracking circuit has to take into account the phase shift introduced by the CMC processor.

It was theoretically established (see equation 11) that the output frequency of the CMC processor is constant, in this case 70 MHz. To test the validity of this theory, the input frequency is arbitrarily changed to 75 MHz, the output waveform of the CMC processor is plotted and shown in Figure 11. By comparing the diagrams in Figures 10 and 11, it can be seen that the two outputs have the same frequency. It is therefore confirmed that a common demodulator can be utilized for all input channels.

Figure 12 shows the center portions of the I and Q baseband chirp waveforms with the parameters given earlier. The filtered outputs are applied to the single sideband modulator.

VI. CONCLUSIONS

The CMC processor reduces the complexity of a satellite borne receiver, by transforming all channels into a common frequency, but in different time slots. Thus only a single demodulator is required for all channels. The chirp transform process has been analyzed and experimentally verified. A software controlled digital chirp waveform generator was developed to replace the conventional SAW chirp generator. This technique provides flexibility to compensate for imperfect chirp slope and also to introduce a weighting function for sidelobe suppression.

VII. REFERENCES

1. Williamson R.C., et.al., "A satellite-borne SAW chirp transform system for uplink demodulation of FSK communication signals", Ultrasonic Symposium, 1979.
2. Otto O.W., "Chirp Transform Signal Processor", Ultrasonic Symposium, 1976.
3. Rabiner L.R., et.al., "Theory and Applications of Digital Signal Processing", p.-91, Prentice-Hall, 1985.
4. Skolnik M.I., "Radar Handbook", Naval Research Laboratory, 1978.

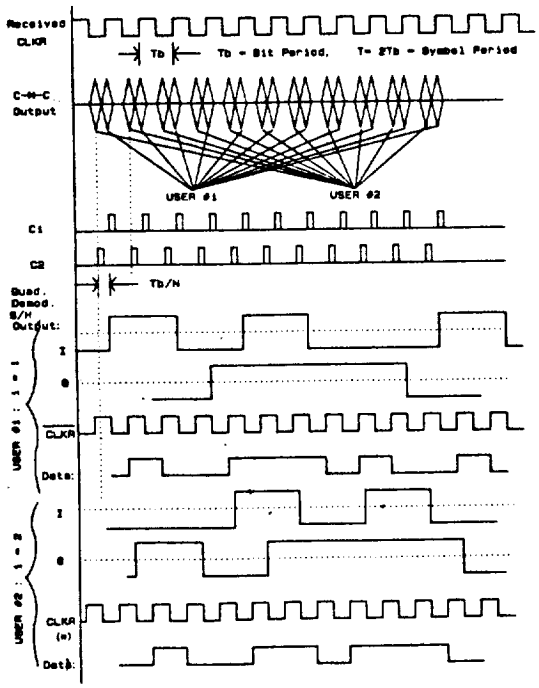

FIGURE 1, SIGNAL AND TIMING ARCHITECTURE OF QPSK RECEIVER

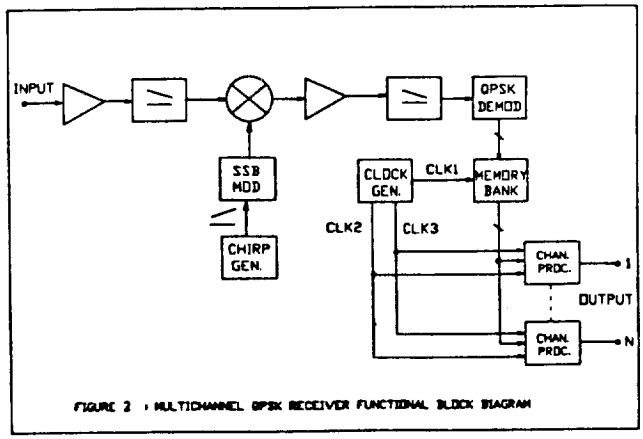

FIGURE 2 : MULTICHANNEL QPSK RECEIVER FUNCTIONAL BLOCK DIAGRAM

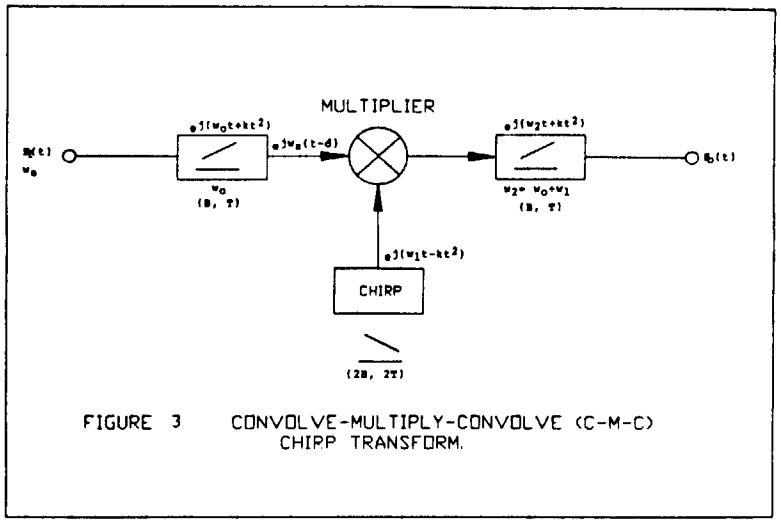

FIGURE 3 CONVOLVE-MULTIPLY-CONVOLVE (C-M-C) CHIRP TRANSFORM.

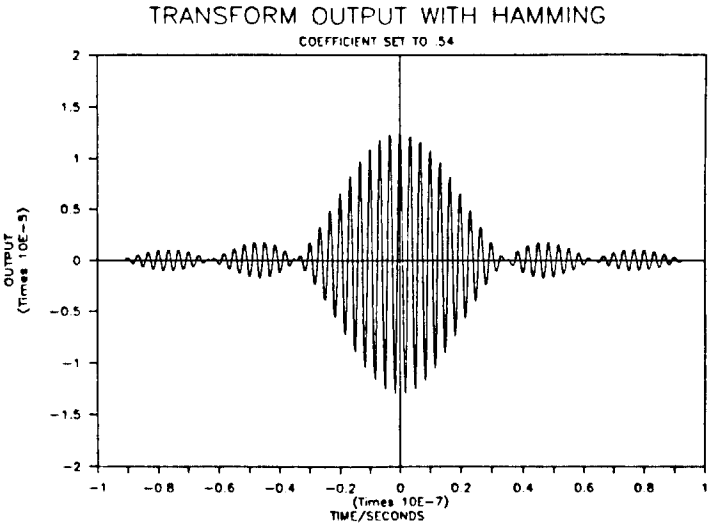

FIGURE 5

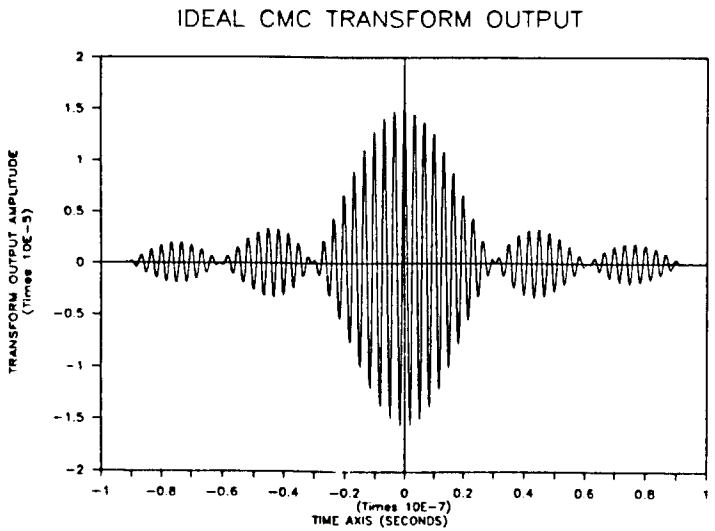

FIGURE 4

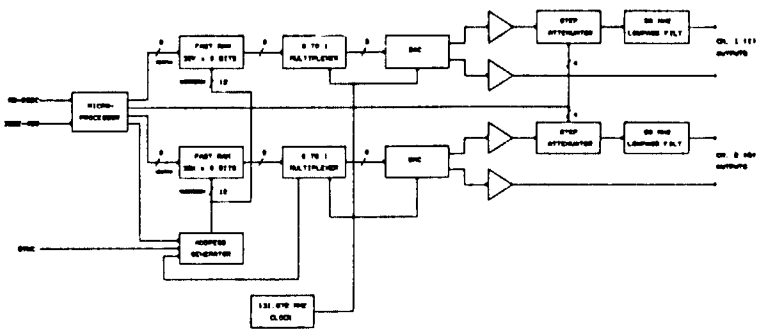

FIGURE 6, BLOCK DIAGRAM OF CHIRP WAVEFORM GENERATOR

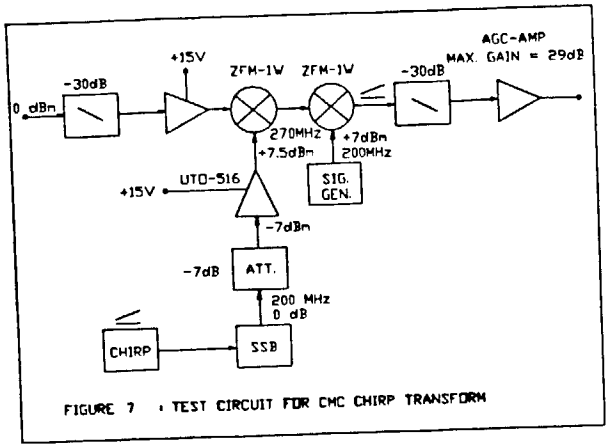

FIGURE 7 : TEST CIRCUIT FOR CMC CHIRP TRANSFORM

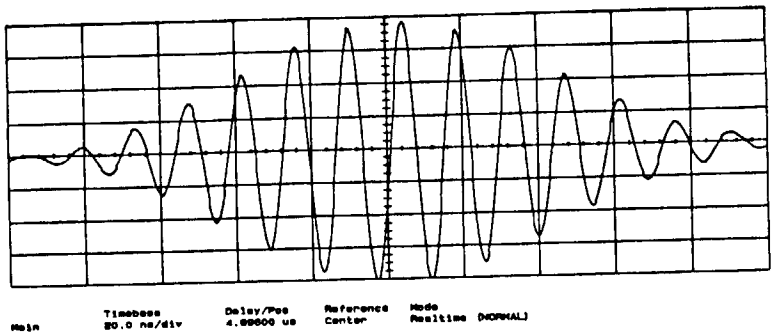

FIGURE 10, OUTPUT OF CMC TRANSFORM PROCESSOR
INPUT SIGNAL FREQUENCY= 70.0015 MHz

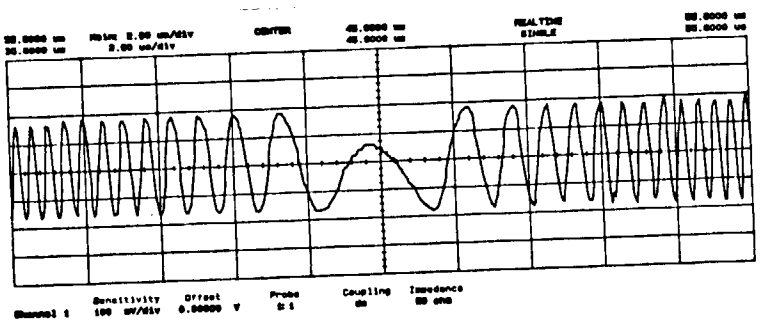

FIGURE 8, OUTPUT WAVEFORM OF SSB MODULATOR

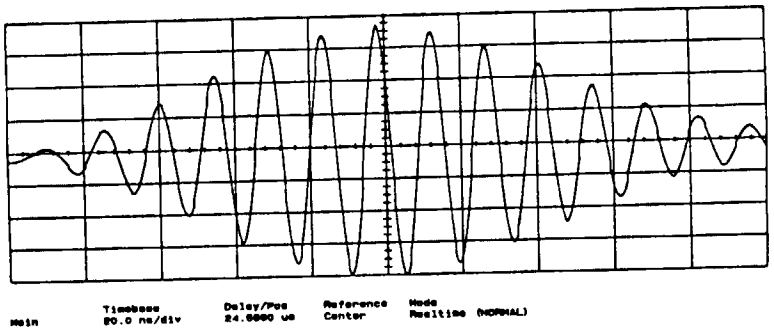

FIGURE 11, OUTPUT SIGNAL WAVEFORM OF CMC PROCESSOR
INPUT FREQUENCY= 75 MHz, OUTPUT FREQUENCY= 70 MHz

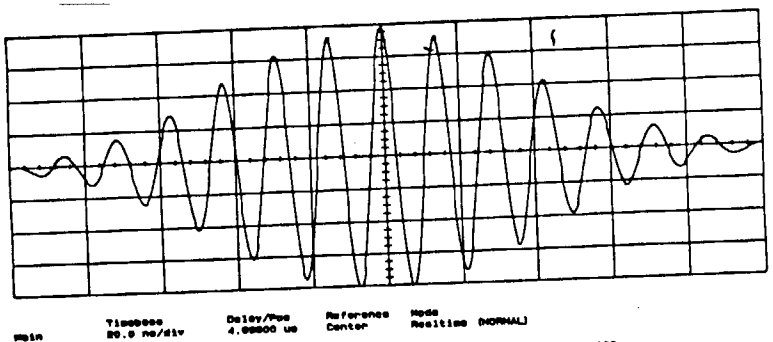

FIGURE 9, OUTPUT WAVEFORM OF CMC TRANSFORM PROCESSOR
INPUT FREQUENCY= 70 MHz

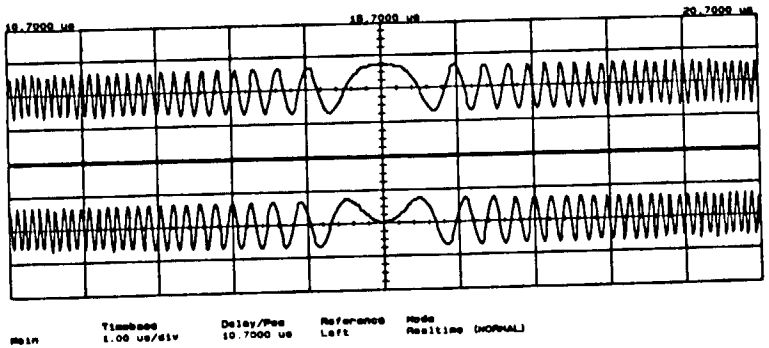

FIGURE 12, I&Q BASEBAND CHIRP WAVEFORMS