

N92-14230

## FLEXIBLE HIGH SPEED CODEC (FHSC)\*

G.P. Segallis and J.V. Wernlund  
Harris, Government Systems Sector  
Melbourne, Florida 32901

## ABSTRACT

This paper describes the on going NASA/Harris FHSC CODEC program. The program objectives are to design and build an encoder decoder that allows operation in either burst or continuous modes at data rates of up to 300 megabits per second. The decoder handles both hard and soft decision decoding and can switch between modes on a burst by burst basis. Bandspreading is low since the code rate is greater than or equal to 7/8. The encoder and a hard decision decoder fit on a single application specific integrated circuit (ASIC) chip. A soft decision applique is implemented using 300K ECL logic which can be easily translated to an ECL gate array.

## INTRODUCTION

Principal use envisioned for the technique is to achieve a significant amount of coding gain on high data rate, bandwidth constrained channels. Satellite channels and line of sight microwave links up to and including T-4 data rates could benefit from this CODEC.

The Hardware being developed for this program consists of 10 BCH ASIC's, two Flexible High Speed CODEC chassis and a Test and Demonstration chassis. The Flexible High Speed CODEC is a high speed stand alone block encoder/decoder. The decoder provides significant gain with hard decisions alone (up to 4dB) and can utilize soft decision information when available from the demodulator to increase the coding gain by as much as 1.5 dB. The Test and Demonstration chassis provides the link simulator, all control signals and the interface between a serial data generator and the Flexible High Speed CODEC. These chassis along with a commercial bit error rate test set, a PC and a synthesizer are the hardware of this program.

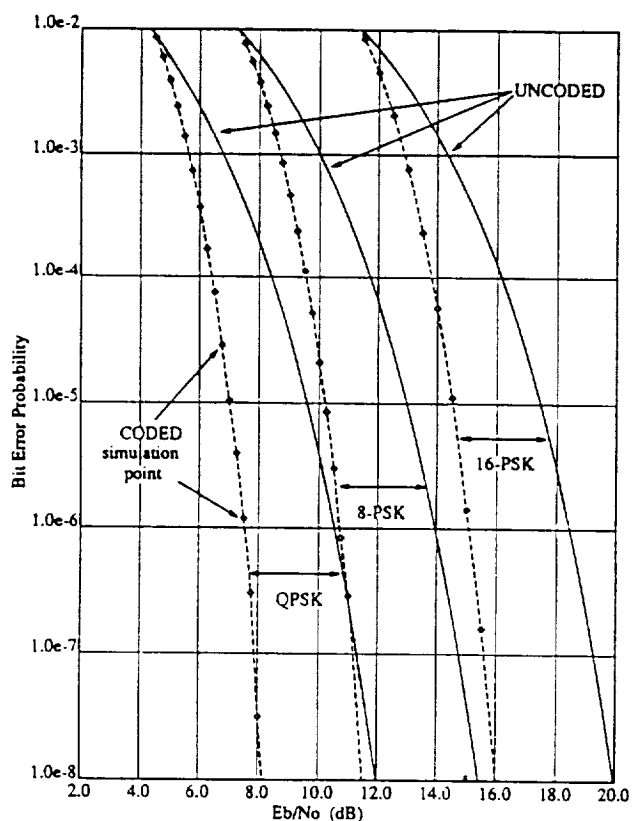
Some interesting aspects of this coding technique include the ability to handle burst (e.g. packet) lengths from 224 bits up, in steps of 32 bits. It may be switched in or out on a burst by burst basis without affecting throughput delay. The interface design allows mating with many forms of M-ary modulation including M=2,4,8 and 16. This paper discusses the FHSC program in general, the approach taken to testing and the hardware. A brief discussion of the program status is presented at the end of the paper.

\*This work is funded by NASA Lewis Research Center under Contract #NAS3-25087;  
Contract Manager: Robert Jones

## ASIC

The HARRIS-NASA BCH CODEC utilizes presolved equations to implement a hard decision, triple error correcting Bose-Chaudhuri-Hocquenghem block codec (ref. 1). This CMOS ASIC contains 18,000 equivalent gates, is packaged in a 132 pin PGA, and consumes 1.5W at +5V. This CODEC will provide up to 4 dB coding gain (see fig. 1) at data rates up to 300 Mbps with low bandspreading. The CODEC may be used in either a full or partial coding scheme and may be interfaced to various types of modems such as m-ary PSK and QAM. The CODEC will correct all patterns of 3 or less errors within a block. In addition, many higher weight error patterns are detected and status lines are provided to the user. Data format may be either continuous or variable length bursts.

**Hard Decision Performance of a (256, 224) Code**



BER	Hard Decision Coding Gain (in dB)					
	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
$10^{-4}$	2.0	2.2	2.4	1.8	2.0	2.2
$10^{-6}$	3.0	3.2	3.4	2.8	3.0	3.2
$10^{-8}$	3.8	3.9	4.0	3.6	3.7	3.8

**Fig. 1 Hard Decision Coding Gains**

The CODEC interface is configurable to be either 1, 2, 4 or 8 bits wide. This allows a single symbol wide interface for several modulation types, or symbols may be stacked up to

increase throughput. The interface will operate up to 43 MHz providing a 38 Mbps, 75 Mbps, 150 Mbps, or 300 Mbps data rate for the specified interface widths. The BCH encoder appends 32 parity bits to a data block. Legal block lengths are from 224 to 480 bits in 16 bit increments. Four of the parity bits are user programmable at the encoder and are provided to the user by the decoder on the receive side. This feature can be used to implement a voice or data order wire. The resulting "codeword" is 256 to 512 bits yielding a very high code-rate of 7/8 to 15/16. Note, the 300 Mbps data rate is data only, the CODEC will operate up to 343 Mbps to account for the coding overhead. Bursts longer than 480 data bits are formed by concatenating 2 or more blocks of length 224 to 480 bits. This allows any burst length from 224 on up in increments of 16 bits (see fig. 2).

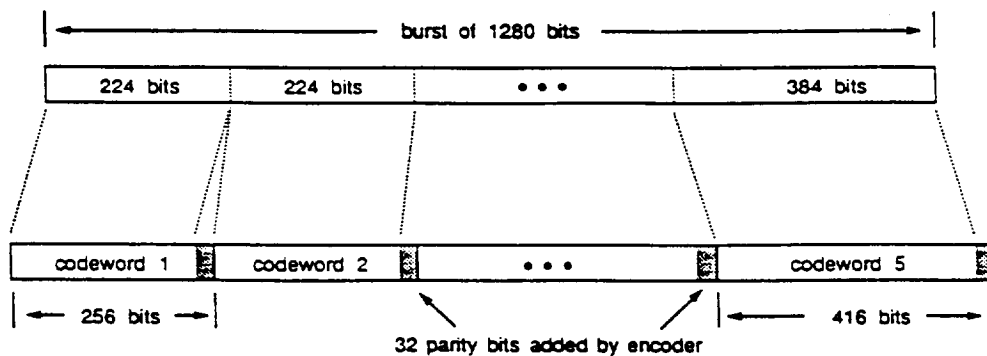


Fig. 2 Concatenated blocks

Block boundaries are either determined by the user and provided to the CODEC or may be internally generated by the CODEC to provide a continuous mode of operation. In this mode the decoder performs a search for codeword position alignment. The decoder can also provide internal demod-carrier phase ambiguity resolution when operating with BPSK, QPSK or 16-ary PSK modems. The codeword position search, phase resolution, as well as lock status are controlled by internal lock circuitry. This lock circuit is externally programmable to allow adaptation to specific performance and acquisition time requirements. All of the lock circuitry inputs and outputs are brought off chip to allow external lock/search control.

Coding may be turned on and off (ie. decoder corrects no errors) on a burst by burst basis without altering the throughput delay. In the uncoded mode data is passed continuously. In this mode block mark is used as a data valid signal and does not transition low until the end of a burst.

The decoder also contains internal fault circuitry providing fault status to the user. Scan chain and mux isolation circuitry allows extensive off-line test of the ASIC.

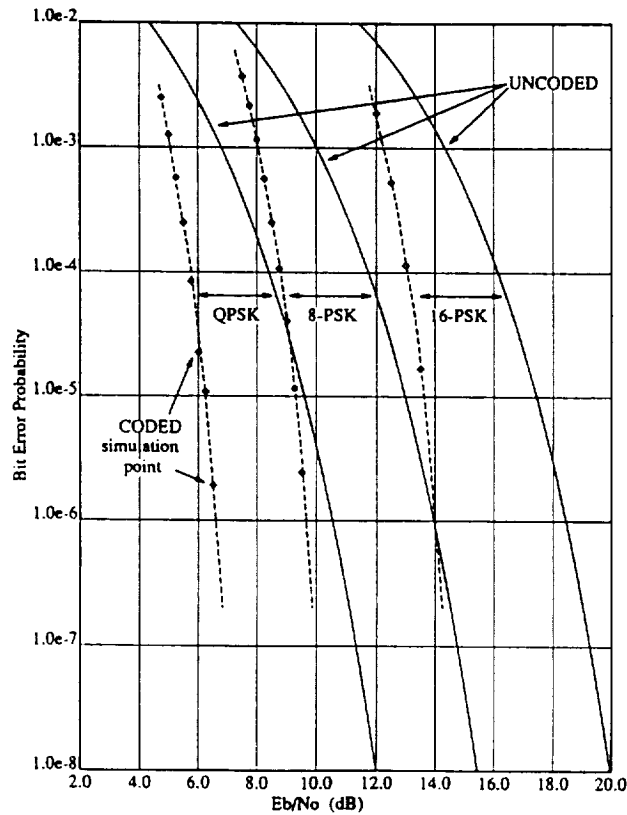
In addition to correcting any errors found, the decoder also provides their locations to the user. This information is used by the FHSC CHASE soft decision algorithm to further increase coding gain.

#### FHSC CODEC

The FHSC chassis utilizes 4 of the BCH ASIC's, the Chase circuits and I.O. formatting circuits to implement the flexible high speed CODEC algorithms. It is designed to operate

from DC to 300 megabits while providing as much as 5.4 dB of coding gain (see fig 3). The interface width can be 3 or 4 bits. It can be used in a burst or a continuous mode. And can operate as a hard decision or soft decision CODEC. The CODEC can be switched between coded and uncoded modes on a burst by burst basis. The four user programmable parity bits are brought out from the ASIC's to enable order wire applications. The delay through the encoder/decoder is essentially independent of its modes of operation. There is a slight difference between the delay in 8-ary and any other mode. This is due to the difference between the 8-ary symbol clock and the 3/4 symbol clock used internally.

Soft Decision Performance of a (256, 224) Code



BER	Soft Decision Coding Gain (in dB)					
	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
$10^{-4}$	2.7	2.9	3.1	2.5	2.7	2.9
$10^{-6}$	4.0	4.3	4.5	3.8	4.1	4.3
$10^{-8}$	4.9	5.2	5.4	4.7	5.0	5.2

Fig. 3 Soft Decision Coding Gains

A single block mark is used to control the all of the circuits with in the FHSC . This signal starts the encoding process the decoding process and controls all of the gated clocks used within the FHSC. In the burst mode this signal is supplied by the user. Because the signal eventually controls the BCH CODEC chips it has the same constraints as it would for the ASIC alone.

In the continuous mode the FHSC generates all block mark signals internally. In this mode the block lengths are forced to 288 bits. An internally generated gated clock is output to the user for clocking data into the encoder. Like the BCH ASIC the FHSC decoder can acquire code word boundaries in all continuous modes. It can also resolve carrier phase ambiguities in hard decision 2-ary, 4-ary and 16-ary modes. Signals out of the FHSC indicate when the decoder is unable to lock or when a fault is detected. In the burst mode a bump phase signal is provided. This signal indicates the BCH decoder would like the TDMA controller to slip the block mark signal one symbol time. The codec is built using 300K ECL, 4 ASIC's and FCT logic. It is designed onto 4 MuPac multi technology wire wrap cards and consumes 350 watts of power.

### THE CHASE

The Chase circuits perform the soft decision decoding of the CODEC (ref. 2). The Chase preprocessor circuits identify the three bit positions, with-in a code word, with the poorest statics. These bit positions are then toggled to produce four code words for decoding by the BCH decoder ASIC's (see fig 4). The code word parity is used to determine which set of four code words is generated. A likelihood for each code word is also calculated. These likelihoods are a measure of the correlation between the original received code word and the four generated code words. These likelihoods and the altered bit locations are then stored in FIFO's for use by the Chase post processor circuits. The post processor circuits read the bit locations changed by the BCH decoder chips and calculate a final likelihood. These final likelihoods are then used to select which decoder's output will be selected as the FHSC decoded output. These circuits are all designed to interface with the BCH chip at bit rates up to 342 Megabits.

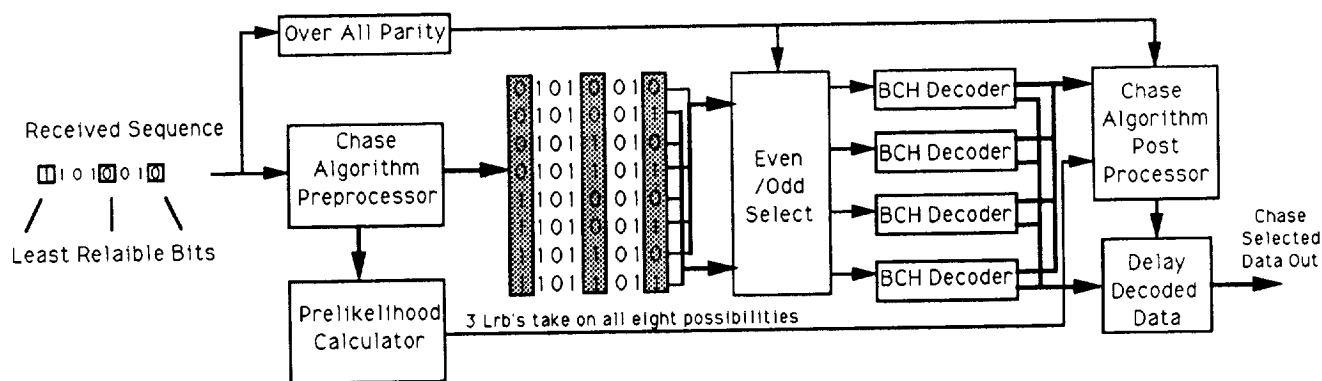


Fig. 4 Chase Algorithm

### INPUT OUTPUT FORMATTERS

The FHSC is designed to interface with two symbol widths. They are 3 bits and 4 bits. With-in a four bit interface there may be more than one symbol. This enables the CODEC to be used with BPSK, QPSK, 8-ary or 16-ary symbols. The input formatters first convert the

incoming symbols into four bit nibbles and then into 8 bit words. The four bit nibbles are used by the Chase preprocessor circuits while the 8 bit words are used by the BCH CODEC chip. Input FIFO's are used to buffer the incoming symbols from the nibbles and words used by the preprocessor and the BCH CODEC's. All symbols be they 2-ary, 4-ary, 8-ary or 16-ary are passed through these FIFO's. This avoids phase problems due to delays between the user and the high speed circuits with in the FHSC CODEC.

#### TDE

The Test and Demonstration equipment is under PC control. It uses test profiles loaded from the PC to generate all the control signals needed by the FHSC. These profiles include number of bursts, burst lengths, modulation modes, coded or uncoded and signal to noise ratios. The burst lengths and number of bursts are used to generate the control signal block mark. The signal to noise ratios and the modulation mode is used to set up the link simulator circuits.

The TDE also serves as a buffer between a serial bit error rate test set and the FHSC chassis. The TDE uses gated clocks to clock serial data to and from the BERT. This data is then formatted into the appropriate symbol width. All clocks needed by the FHSC and BERT's are generated from the synthesizer reference by the TDE.

The link simulator is a full rate simulator. It can generate hard and soft decision symbols at 300 megabits in the 16-ary mode, 225 megabits 8-ary and 150 megabits 4-ary. It is capable of generating noisy symbols for bit error rates from  $10E-1$  to  $10E-10$  (see fig 5). Noise profiles are generated by inputting the desired  $E_b/N_0$  and the modulation mode to a noise generator program resident in the test software. Current modulation profiles include 4-ary, 8-ary and 16-ary PSK signals. Many other modulation modes could be tested by modifying the noise generator software.

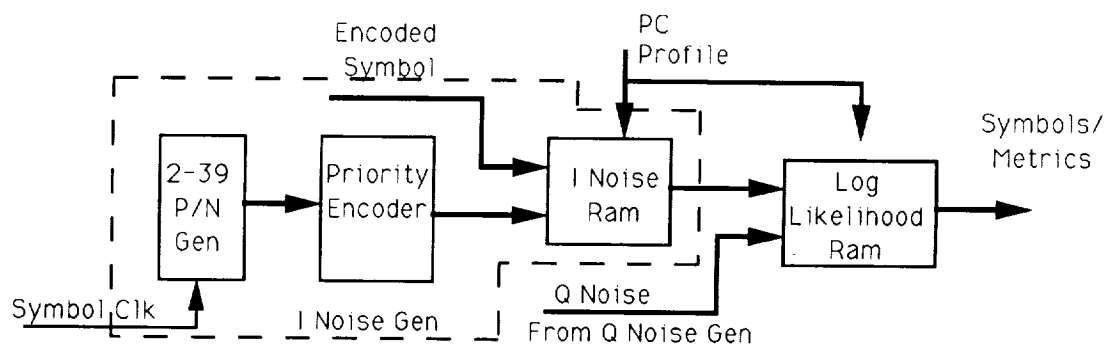


Fig. 5 Noise Generator / Log Likelihood

#### HARDWARE DESIGNS

Both the FHSC and the TDE chassis are fabricated using off the shelf 19" rack mountable chassis. They each contain their own power supplies. The circuits are designed onto MuPac multi-technology wire-wrap cards which fit into a MuPac VME type card cage. There are four card types in each of the chassis. One of the cards in the TDE is a PC design. This

design uses the ECLIPS logic family and clocks to rates in excess of 300 MHz. The wire wrap cards have been auto wrapped from files extracted from CAD captured schematics. All high speed signal interfaces are differential ECL. With the exception of all clocks the signals interface through D connectors on the front and back panels.

The ASIC is designed and scheduled for delivery in early August. The design was fully simulated using VLSI logic simulator tools. The simulations were conducted over the full commercial temperature. Results of these simulations indicate the ASIC will fully support the FHSC 300 megabit requirement over this temperature range. These simulations include the complete encoding and decoding of corrupted random data.

Simulations of the FHSC formatting circuits and the Chase pre and post-processors are currently being run. These simulations are at a card level. Completion of this effort is anticipated in early August.

### OBSERVATIONS

A high-speed, high-rate coding technique suitable for both burst and continuous systems has been presented. It can operate as a single chip hard decision codec or, with the decoding applique, can utilize soft decision information in the decoding process. Coding gains up to 4 dB are obtained in the hard decision mode, increasing to 5.5 dB with soft decisions (at  $10^{-8}$  BER).

Error correction coding has long been considered a good means to lower the required EIRP in communication systems having unlimited bandwidth. However, high-rate codes such as the one described are also well suited for bandwidth efficient systems. The CODEC rate and interface are matched to the larger signaling alphabets used for constrained bandwidth communications. Performance data indicates that coding gain improves slightly with increasing modulation alphabet size and is a weak function of code word length. Even with the overhead required to insert parity bits, the net result is less power required to communicate a given data rate (say 300 Mb/s) over a fixed bandwidth channel (say 200 Mb/s).

The approach is extremely flexible by design. Hard and soft decision operation supports several different interface modes at data rates up to 300 Mb/s. Soft decision operation increases performance by as much as 1.5 dB. The soft decision applique can be easily translated into an ECL gate array considerably reducing the power and size of the FHSC.

It is believed that the approach and hardware resulting from this project will prove useful to a variety of high rate systems.

### References

- 1) Polkinghorn, F. Jr., "Decoding of Double and Triple Error Correcting Bose-Chaudhuri Codes," *IEEE Transactions of Information Theory*, October 1966. pp. 480-481.
- 2) Chase, D., "A Class of Algorithms for Decoding Block Codes With Channel Measurement Information," *IEEE Transactions on Information Theory*, January 1972, pp.170-182.
- 3) Boyd, R. and Hartman, W., "Flexible High Speed CODEC," *Advanced Modulation and Coding Technology Conference Publication*, June 1989, Session 3, article 6.

