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Multi-Rate Demodulator Architecture*

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I. Summary

A unique digital Multi-Rate Demodulator (MRD) architecture is presented for onboard satellite communications processing. The multi-rate feature enables the same demodulator hardware to process either one wideband channel (WBC), or process up to thirty-two independent narrowband channels (NBC) that are time-division-multiplexed (TDM). The MRD can process many quadrature modulation format such as Offset-Quadrature-Phase-Shift-Keying (OQPSK). Possible applications include voice and data transmission for commercial or military users.

II. Introduction

The MRD currently being developed, shown in Figure 1, is configured for Differentially Encoded OQPSK, with a WBC symbol rate of 1.024 Msymbol/sec. and NBC symbol rate of 32 Ksymbol/sec. OQPSK also referred to as Staggered-QPSK (SQPSK), since the Q baseband signal is staggered in time by 1/2 a symbol period relative to the I baseband signal. Each MRD can be configured for processing either a single high data-rate, WBC or for processing up to 32 low data-rate NBC's at 1/32 the WBC data rate. Reconfiguration from WBC to NBC's, or from NBC's to WBC, would be performed on-line. System parameters for the entire MRD were obtained through extensive Block-Oriented-Systems-Simulator (BOSS) simulation.

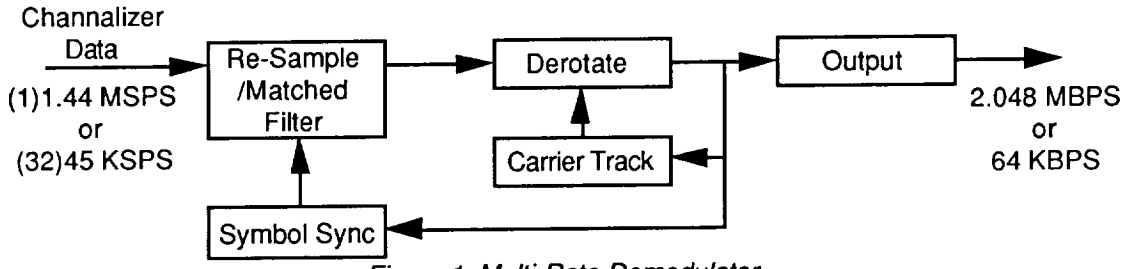

Figure 1. Multi-Rate Demodulator

Each MRD accepts as input, digitized, quadrature down-converted, baseband signals. Quadrature down-conversion decomposes the composite carrier waveform into in-phase (I) and quadrature (Q) components. Data is input to the MRD from a channelizer that performs the quadrature down-conversion, and multiplexing if NBC's. When the MRD is configured for WBC processing the input will be consecutive samples, at 1.44 Msample/sec., from a single channel. If the MRD is configured for NBC processing the input will be TDM'ed samples, at 1.44 Msample/sec., from 32 independent channels. The input data rate for a single NBC will effectively be 45 Ksample/sec. Input data ordering for WBC's and NBC's is shown in Figure 2. All demodulator processing for a channel, if NBC, or an input sample, if WBC, must be performed within the input sample period. If NBC's are processed the MRD hardware is time-shared, with each channel being allocated one input sample epoch to perform demodulator operations. The system clock frequency is 16 times the WBC input data rate with 16 system clock cycles being defined as an input sample epoch. Processing for any of the 32 NBC's is completely independent of the other channels.

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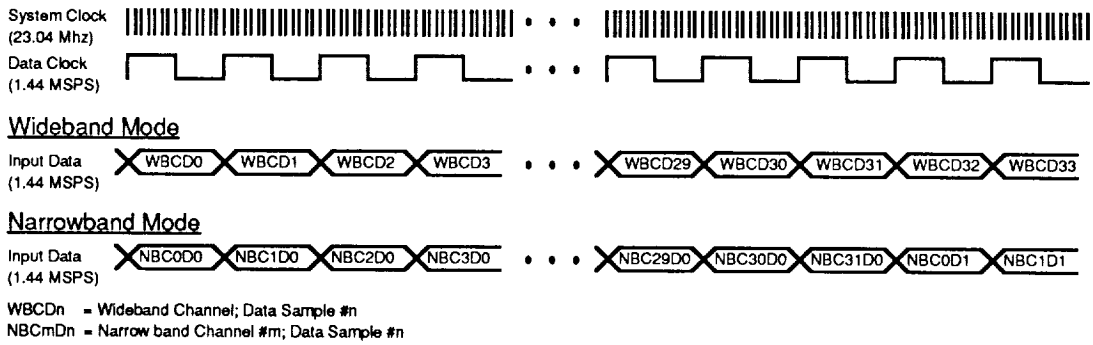


Figure 2. Input Sample/Data Clock/System Clock Timing

The MRD, shown conceptually in Figure 1, is comprised of five functional blocks: Re-Sample/Matched Filter, Derotate, Output, Symbol Sync, and Carrier Track.

The re-sampling filters interpolate the desired input waveform samples from the input channelizer samples. Interpolation is necessary to create samples at the desired sampling interval. The re-sampling filters also provide proper sample positioning, and compensation due to rate offsets. The interpolation filter is combined with a matched filter to accomodate pulse shaping of the baseband waveform.

Residual phase error and carrier frequency offsets are removed by derotation of the complex baseband waveform. The phase error estimate is generated in the carrier tracking loop.

Symbol synchronization is accomplished by means of a symbol sync loop to estimate the timing error, and provide the timing offset for interpolated samples. The current error estimator has been simplified for QPSK operation. The symbol sync also contains a NCO that perfoms the rate conversion for the interpolated samples.

Residual carrier phase is estimated by a second order, type-2, carrier tracking loop to provide a phase error that is then removed by derotation. Different modulation formats can be accommodated by simply modifying the phase error look-up table. The derotation process provides proper quadrature alignment.

Symbol decisions are made upon the midpoint samples generated through interpolation, with a serial data stream and corresponding data clock being output. The output data rate is 2.048 Mbit/sec.for the WBC's, and 64Kbit/sec. for the NBC's. Various modulation formats can be accommodated by modifying the symbol decision look-up table. The output data and clock will be from a single WBC or from 32 NBC's time-division-multiplexed onto the same data and clock line. Thirty-two separate data and clock lines for the NBC's are also available.

III. Architecture

The MRD, a detailed block diagram shown in Figure 3, is comprised of the following processing elements:

- Input Buffer: To store input samples necessary for filter calculation.
- Re-Sampling Filters: For matched / interpolation filtering.
- Derotate: Complex Multiply needed for phase error removal.
- De-Stagger Buffer: To remove staggering and store samples.
- Symbol Timing Error Estimator: Estimates timing error of interpolated samples.
- Symbol Sync Loop Filter: Low-Pass Filters timing estimate.
- Symbol Sync NCO: Provides timing offset for interpolated samples.
- Phase Error Estimator: Estimates residual phase error.
- Carrier Tracking Loop Filter: Low-Pass Filters timing estimate.
- Carrier Tracking NCO: Tracks phase error to be removed by derotation.
- Symbol Decision: For symbol decision, and data/clock formatting.

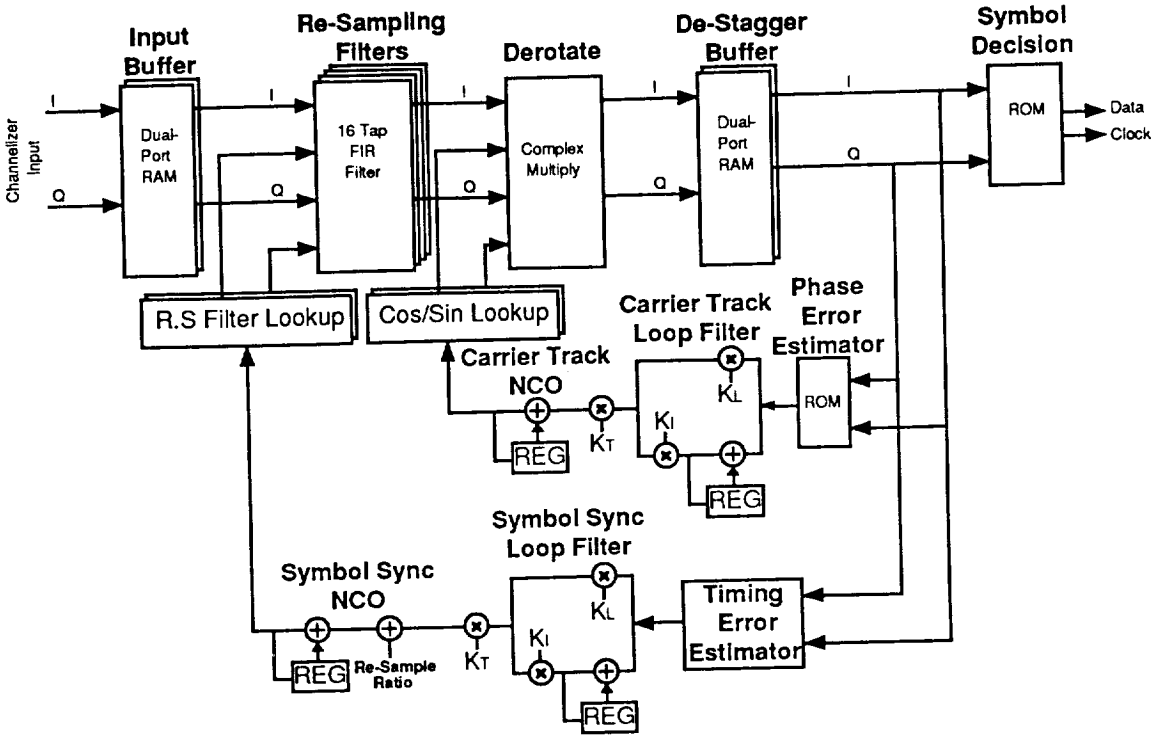


Figure 3. Multi-Rate Demodulator (Detailed)

1. Interpolation / Re-Sampling Filters

The input data is sampled at the Nyquist minimum sampling frequency, and therefore interpolation (or re-sampling) can be performed to generate any desired sample from the input baseband waveform (ref. 1). For the MRD a sample at the midpoint and at the transition point are needed for demodulator processing. The interpolation filter is combined with a matched filter to accommodate various baseband signal conditioning.

The MRD currently being developed has a WBC input data rate of 1.44 Msample/sec. and a NBC input rate of 45 Ksample/sec. This gives a 1.44 Mhz period (or a 16 cycle system clock input sample epoch) in which demodulator processing must be completed for a particular channel, if NBC, or input sample if WBC. The symbol rates, in absence of any offsets, are 1.024 Msymbol/sec. for the WBC and 32 Ksymbol/sec. for the NBC. For demodulator processing it is necessary to generate two samples per symbol giving an interpolated data rate of 2.048 Msample/sec. for the WBC and 64 Ksample/sec. for the NBC. The input waveform is "re-sampled" to give data samples at the desired sampling interval through interpolation of the input data points. The interpolation process is performed by a digital 16 tap (ref. 1) Finite-Impulse-Response (FIR) filter that is combined with a matched filter to accommodate pulse shaping of the baseband waveform. Pulse shaping currently implemented is a Square-Root-Raised-Cosine with filter coefficients being input from a look-up table. Different pulse shaping schemes can be implemented by modification of the filter coefficient look-up table. Two filter outputs are needed per quadrature arm (4 total) to generate the two interpolated output points during an input sample epoch.

All interpolation analysis for the WBC and NBC is identical since both the input and output sample rates for the WBC are 32 times that of the NBC's. Proper symbol synchronization, and position of interpolated samples is achieved through the Symbol Sync NCO that performs the rate conversion. The NCO will provide the 5 bit timing offset, representing ±1/2 an input sample in 32 steps, that the current sample being interpolated will have. The timing offset will select a set of filter coefficients to perform the interpolation. There are 32 sets of 16 filter coefficients, one

coeffiecient set for each posible timing offset, stored in a 512x8 look-up table. The interpolation filters can generate at most two samples, and at least one sample during an input sample epoch with the number of samples generated being determined by the NCO overflow status.

Since the MRD runs at a multiple of the input data rate of 45 Ksample/sec., with the interpolated data rate being 64 Ksample/sec. for NBC's (2.048 Msample/sec. for WBC's), samples out of the re-sampling filters will not be at a uniform rate, however the average rate over time will be 64 Ksamples/sec. This is illustrated in Figure 4.

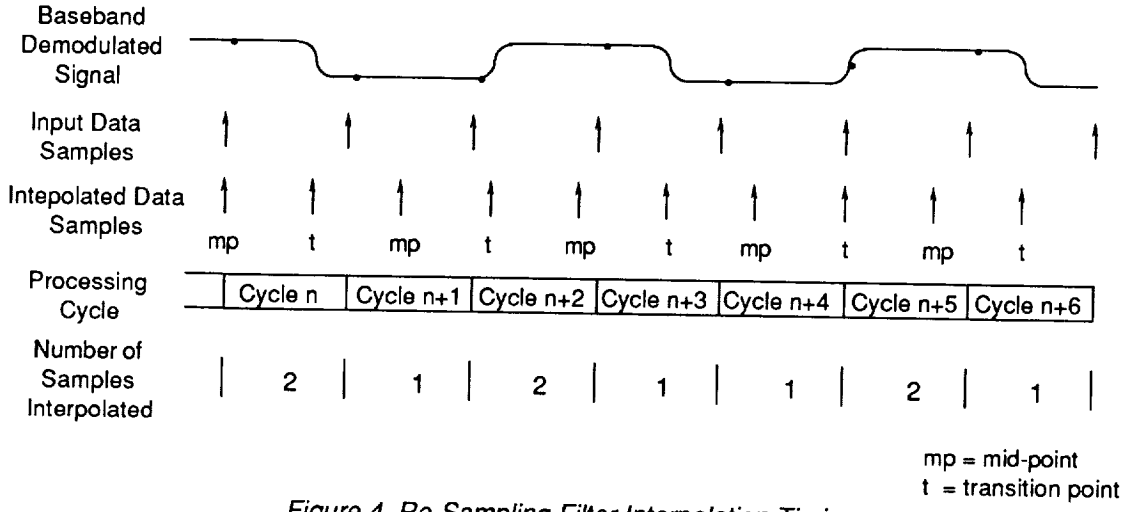


Figure 4. Re-Sampling Filter Interpolation Timing

2. De-Stagger

The modulation format, OQPSK, is such that I and Q samples are staggered by half a symbol period. Besides the staggering, the interpolation process will output data at an irregular rate. Since a previous midpoint, previous transition, and current midpoint are needed for demodulator processing, and due to the staggering and irregular rate, a memory buffer is necessary. If the necessary data samples are not resident in the de-stagger buffer, some processing for the current input sample epoch is bypassed. The symbol sync NCO and carrier tracking accumulator are still updated, but no symbol decisions or symbol timing/ phase error estimates will be made.

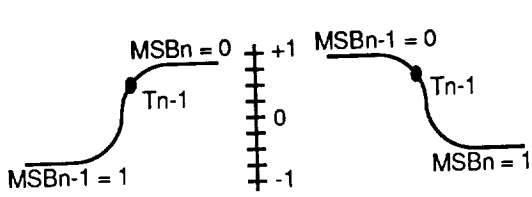
3. Symbol Synchronization Loop

Symbol syncronization loop is comprised of the timing error estimator, the Symbol Sync Loop Filter, and the Symbol Sync NCO.

The Timing Error Estimator generates a non-zero estimate if a transition has occurred between the previous and current midpoint samples. The estimates for both the I and the Q are summed and input to the Symbol Sync Loop Filter. Synchronization loops of this type are sometimes refered to as a Data-Transition-Tracking-Loop or DTTL (ref. 2).

In order to determine whether a transition has occurred, the previous and current midpoints are compared. If a transition did occur, the value of the transition sample, with its polarity adjusted as shown in Figure 5, will represent the error estimate. The end result is that if the transition point is early, a negative error estimate will be created to slow the NCO down, and if the transition point is late a positive estimate will be created to speed the NCO up.

The Symbol Sync Loop Filter acts as a low pass filter, so that depending on the loop bandwidth selected, RMS jitter due to thermal noise can be traded off for pull-in time and phase noise performance.



MSBn	MSBn-1	Error
0	0	0
0	1	+Tn-1
1	0	-Tn-1
1	1	0

Figure 5. Timing Error Estimate

All loop filter coefficients (K_L, K_I and K_T) are powers of two to enable using shifts instead of multiplies and are programmable to accommodate different loop bandwidths. The word width of the loop filter output is 24 bits to allow for a wide range (from 10^{-1} • symbol rate to 10^{-5} • symbol rate) of possible loop bandwidths (ref. 1).

The output of the loop filter is input to the NCO to fine tune the NCO frequency. The coarse tune is determined by the re-sampling ratio. As mentioned previously, the NCO determines if one or two interpolated samples, for both I and Q, are generated during the current input sample epoch. If the NCO overflows on the first update, then the current input samples are only sufficient to generate one interpolated sample. If however the NCO does not overflow on the first update, it is updated again, and two interpolated samples will be generated. The most-significant 5 bits of the 24 bit NCO output are used as a re-sampling filter select, giving 32 posible timing offsets.

4. Carrier Tracking Loop

Carrier Tracking Loop (ref. 3) is comprised of the Phase Error Estimator, the Carrier Tracking Loop Filter, and a Carrier Tracking NCO (or accumulator).

The Carrier Tracking Estimator uses the current midpoint from both the I and Q arm to estimate the phase error. This estimate is computed as: (1)

$$\theta_{error}(I,Q) = TAN^{-1}(Q/I) - \theta_{optimum}$$

where $\theta_{optimum}$ is computed depending on which quadrant the current symbol resides as shown in Figure 6.

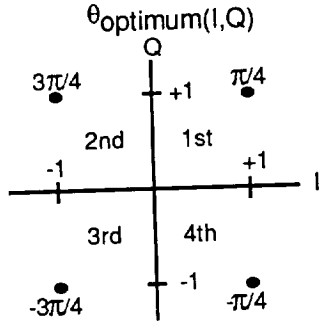


Figure 6.

The phase error estimate is computed by means of a look-up table (1024 x 8) that could be modified to accommodate different modulation schemes.

The phase error estimate is input to the Carrier Tracking Loop Filter which is of the same type as the Symbol Sync Loop Filter. The output of the loop filter is input to the 24 bit Carrier Tracking NCO which will track the phase error of the input waveform. The most-significant 8 bits of the NCO output will be mapped into $\pm\pi$ radians and will be used as an address to a sin/cos look-up

table (256 x 8). A complex multiply is necessary to remove the estimated phase error from the baseband waveform as shown below:

$$X_{de\text{-}rot} = X_{rot} \cdot e^{-j\theta est} \quad (2)$$

$$= [X_{rotI} \cdot \cos\theta_{est} + X_{rotQ} \cdot \sin\theta_{est}] + j[X_{rotQ} \cdot \cos\theta_{est} - X_{rotI} \cdot \sin\theta_{est}] \quad (3)$$

where,

$X_{de\text{-}rot}$ = Derotated complex baseband waveform
X_{rot} = Rotated input complex baseband waveform
X_{rotI} = Real componant of X_{rot}
X_{rotQ} = Imaginary component of X_{rot}
θ_{est} = phase error estimate from carrier tracking accumulator

5. Symbol Decision

The output symbol decisions are made upon the I and Q arm independently using the previous and current midpoint samples. The data is differentially encoded with the decision being made on the most-significant (sign) bit of the two midpoints. OQPSK will generated two bits per symbol, one for the I arm and one for the Q arm. The data bits are muxed onto the same line to create a serial data stream, with a corresponding data strobe. The data for the NBC's can be separated into 32 independent data and clock lines, or muxed onto the same data and clock lines in a TDM'ed fashion. A corresponding index is also output for the TDM'ed clock and data to determine the current channel. The symbol decision look-up can be modified to accommodate various modulation formats.

IV. Conclusions

The digital Multi-Rate Demodulator with many modulation dependent functions being performed in look-up tables, has a high degree of inherent flexibility. This flexibility will allow the consideration of different modulation formats without hardware modification. The MRD currently being developed is a prototype for definition of a future Application-Specific-Integrated-Circuit (ASIC) implementation. The ASIC implementation will be a compact, low power unit for insertion into future satellite systems with overall system channel capacity easily expanded by the addition of MRD modules.

The digital Multi-Rate Demodulator architecture, with it's high degree of flexibility can accommodate a wide variety of modulation formats and symbol rates without design modification. The MRD provides an efficient, low-complexity, digital implementation that can be suited to a host of different satellite applications.

References

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