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Circuit-Switch Architecture for a 30/20-GHz FDMA/TDM Geostationary Satellite Communications Network

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CIRCUIT-SWITCH ARCHITECTURE FOR A 30/20-GHz FDMA/TDM GEOSTATIONARY SATELLITE COMMUNICATIONS NETWORK

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Abstract

This report describes a circuit-switching architecture for a 30/20-GHz frequency-division, multiple-access uplink/time-division-multiplexed downlink (FDMA/TDM) geostationary satellite communications network. Critical subsystems and problem areas are identified and addressed. Work was concentrated primarily on the space segment; however, the ground segment was considered concurrently to ensure cost efficiency and realistic operational constraints.

Introduction

In the mid-1980's NASA began the Advanced Communications Technology Satellite (ACTS) Program to develop a 30/20-GHz geostationary communications satellite. This satellite, which is to be launched in 1993, will open up the Ka-band frequency for commercial communications, develop multibeam and hopping-beam antennas, and demonstrate onboard processing technology. The ACTS system uses time-division, multiple-access (TDMA) uplinks and time-division-multiplexed (TDM) downlinks. One drawback of TDMA uplinks is that they force Earth terminals to transmit at a rate much higher than their actual throughput rate. For example, in the ACTS system, an Earth terminal wishing to transmit a single voice channel at 64 kbps would have to transmit at a burst rate of 27.5, 110, or 220 Mbps.[1] This, in effect, drives the cost of the Earth terminals up dramatically by requiring either substantially higher power transmitters or larger antennas, both of which are major cost drivers. Realizing this, researchers have recently emphasized bringing the cost of the Earth terminals down. One way to accomplish this is to eliminate the need for high-power transmitters on Earth by allowing the user to transmit at a lower data rate with a frequency-division, multiple-access (FDMA) uplink architecture. TDM is chosen for the downlink transmission technique so that the high-power amplifier (HPA) can be operated at maximum power, thereby increasing the downlink signal strength and enabling the use of very small aperture terminals (VSAT's).[2]

Currently, NASA envisions the need for meshed VSAT satellite communication systems for direct distribution of data to experimenters and for direct control of space experiments. In the commercial arena, NASA envisions a need for low-data-rate, direct-to-the-user communications services for data, voice, FAX, and videoconferencing. Such a system would enhance current communications services and enable new services. However, for this type of satellite system to exist, it must be cost competitive with terrestrial systems at the user level while enhancing the existing quality of service. The key is to drive the cost of the Earth terminals down and spread the cost of the satellite among tens of thousands of users. NASA has completed and is continuing to perform studies on such communication systems.[3-6]

Meshed VSAT satellite networks can be implemented with either a circuit-switched architecture, a packet-switched architecture, or a combination of the two. Intuitively, it appears that a circuit-switched network would be far simpler to implement; however, packet switching has many potential advantages over circuit switching. The Digital System Technology Branch at NASA Lewis Research Center is currently investigating circuit- and packet-switched satellite networks to identify

the common subsystems and to quantify the complexity of a packet-switched network versus a circuit-switched network. This report is a direct result of those studies. It describes for a circuit-switched, geostationary satellite network the overall network requirements, the network architecture, the protocols and congestion control, and the individual subsystems.

Network Requirements

The salient requirements of the network architecture follow. First, the system has to be economically viable and cost competitive with existing terrestrial telecommunication systems while enhancing existing services and adding new ones. Second, the system must provide voice, data, FAX, datagram, teleconferencing, and video communications services. To provide these services, the Earth terminals will transmit continuously at either 64 kbps or 2.048 Mbps. Third, the system must be capable of point-to-point, multicast, and broadcast transmissions. Multicast capability is a necessity to provide teleconferencing and videoconferencing services.

Network Architecture Description

The network consists of meshed VSAT's operating at 30/20 GHz and transmitting through a processing satellite, where transmission is FDMA up and TDM down. There are eight uplink beams and eight downlink hopping beams covering the continental United States. Each downlink beam has eight dwell locations. Associated with each uplink beam is a multichannel demultiplexer/demodulator (MCDD) capable of demultiplexing and demodulating 1024 64-kbps channels, a decoder, and a formatting buffer. Associated with each downlink is a burst buffer, an encoder, and a 150-Mbps burst modulator. In between is the switching and routing system. The switching, routing, and congestion control are the responsibility of the network control (Figs. 1 and 2).

Many of the relative numbers used to establish the network size and data rates are taken from an architecture study performed by TRW. This report includes a complete link budget and hardware analysis in sufficient detail to estimate size, weight, and power requirements for the satellite and Earth terminals.[7]

Protocols

Initial Access

Initial access to the system will be via a reserved signaling channel. One 64-kbps channel for each multichannel demultiplexer will be reserved for requesting entry into the system. This channel will be set up in a slotted ALOHA format.[8] Requests for data-transmission rates corresponding to either 64 kbps or 2.048 Mbps will be made through this channel. Also, during initial access, the Earth terminal will have to specifically request for multicast services. This is necessary so that the system can verify that the downlink has sufficient capacity to handle the request and so that the user can be properly billed. For multicasting, the satellite will have to duplicate the received message up to 64 times onboard the satellite and route that information to the correct downlink beam and dwell.

Upon reception of the initial access request, the satellite will grant or deny the request to the requesting terminal via a downlink inband orderwire message and will allocate a corresponding frequency. In addition, the ground terminal will allocate a downlink time slot in the destination dwell and will notify the receiving terminal of the time slot that was allocated.

TDM Frame Structure

The TDM frame structure has yet to be defined in detail. However, the TDM frame will be between 1 and 32 msec long since the

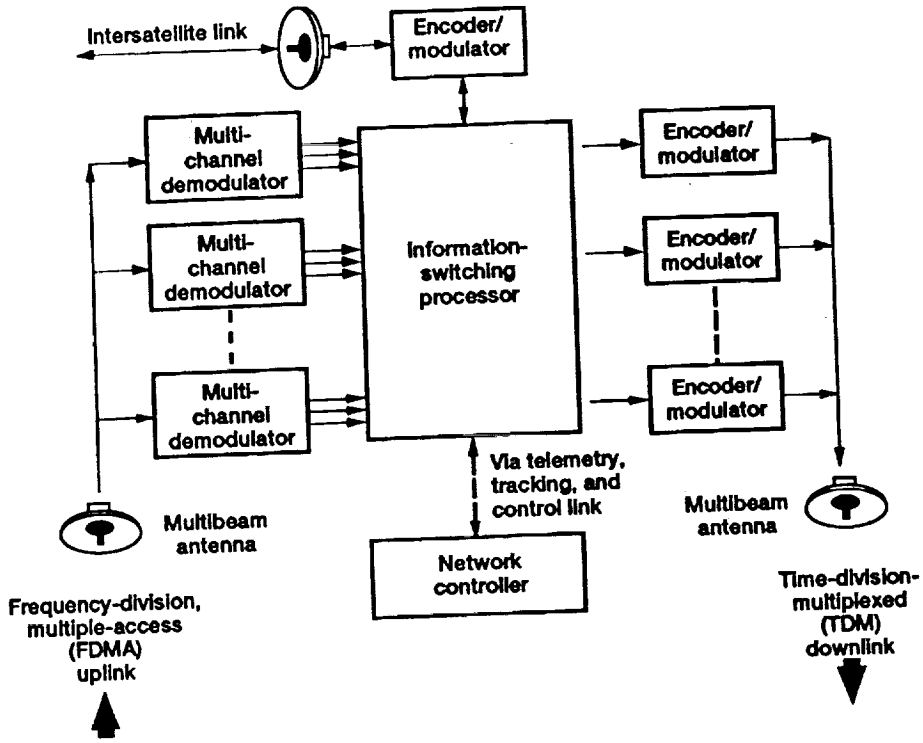

Fig. 1.—Information-switching processor.

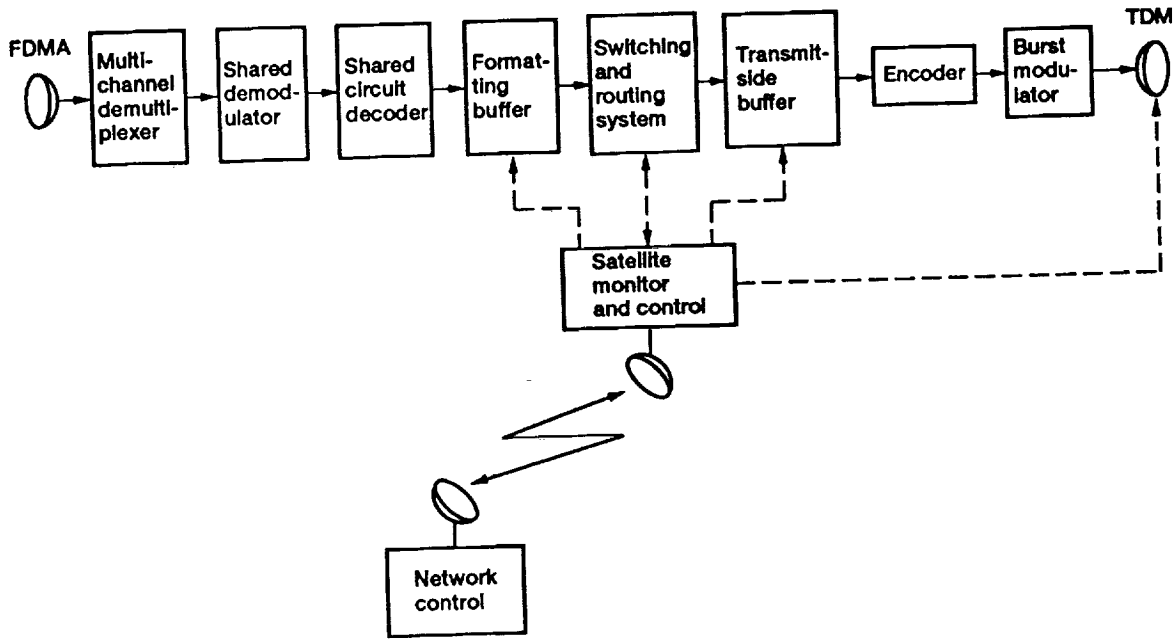

Fig. 2.—Detailed diagram of information-switching processor.

frame efficiency increases with frame length. In addition, if the dwell time and frame length are made as long as possible, the hopping-beam antenna system will not be required to switch as often, thus improving system efficiency. However, a longer frame will require greater onboard storage capability. A superframe structure will be placed over the TDM frame structure, and various orderwire messages will be reserved for particular frames within a superframe.

Downlink Orderwire Message Format

Orderwires will be used to convey satellite switch status, system timing information, initial access granted and denied messages, and other information. The downlink orderwire message will be the first message of each dwell.

Congestion Control

For this satellite system, congestion is defined as having more information destined for a specific downlink/dwell than the available bandwidth can handle. In a circuit-switched satellite network, congestion control is managed by the network control via granting or denying access into the network.

Network Hardware

Earth Terminals

The Earth terminal will be composed of indoor and outdoor units (Fig. 3). The indoor unit will consist of a terrestrial interface, encoder, low-data-rate continuous modulator, burst demodulator, decoder, first-in, first-out (FIFO) buffer, orderwire processor, and timing and control circuity.

The terrestrial interface will allow the Earth terminals to interface to the terrestrial telecommunications network at the digital signal level 0 (DS0) rate (64 kbps), integrated services digital network (ISDN) basic service rate, 2B+D (144 kbps), and T1-type rates (1.544 or 2.048 Mbps). In addition, the Earth terminal will be capable of interfacing to commercial communications equipment and will be compatible with commercial standards.

The uplink modulator will produce an offset quadrature phase-shift keying (OQPSK) signal and will transmit continuously at either 64 kbps or 2.048 Mbps. Filtered OQPSK will be used on the uplink to obtain a bandwidth efficiency of approximately 1.45 to 1.6 b/sec/Hz. On the downlink, a burst demodulator is required. The modulation format has yet to be determined, but the data rates will be in the 150- to 180-Mbps range.

The message assembler will read the demodulated data, strip off the portion of the burst destined for that Earth terminal, and place that information into an FIFO. This information will be read out of the receiver FIFO continuously at the channel data rate and passed on to the terrestrial interface.

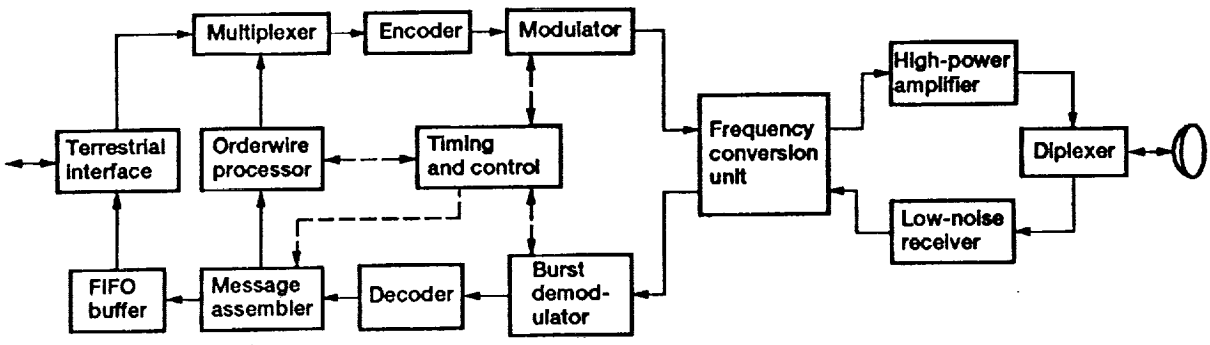

Fig. 3.—Earth terminal.

The orderwire processor will continuously monitor the received bursts. The first message of each burst will be read and interpreted and passed on to the timing and control circuity. The orderwire processor also will place call connect and disconnect messages into the uplink communication stream.

The timing and control system (T&CS) will be responsible for obtaining and maintaining synchronization with the satellite. The T&CS will inform the burst demodulator of the approximate time of the burst arrival and will receive a signal indicating actual burst arrival times. The T&CS will use the information from the demodulator to adjust the Earth terminal's receiver side timing in order to synchronize the Earth terminal to the network. The T&CS also will receive network control information from the orderwire processor. In addition, the T&CS will turn off the transmitter and modulator during periods where the Earth terminal has relinquished access to the satellite uplink channel.

The outdoor unit will contain the radio-frequency (RF) equipment consisting of the frequency-conversion system, high-power transmitter, diplexer, antenna system, and low-noise receiver (LRN). The HPA is required to produce approximately 2 W of transmitter power. The required noise figure for the LRN is approximately 2.6 dB. The outdoor unit will comprise the majority of the Earth terminal cost.

Multichannel Demultiplexer/Demodulator

Onboard demultiplexing and demodulation of narrowband traffic will be provided by the MCDD. In general, the MCDD can be viewed as a multifrequency channelizer and a demodulator system. The channelizer operates relatively independent of the modulation scheme - although some optimization for the channelizer may be performed if the modulation format has been identified early on. The demodulator system is either a time-shared demodulator, a bank of individual demodulators, or a combination of the two.

The MCDD has been identified as a critical subsystem that needs to be developed for an FDMA/TDM architecture. Acousto-optical, optical, and digital signal processing technologies have all been identified as candidates for implementing an MCDD. NASA is currently investigating each of these approaches. Amerasia Technology Incorporated is in the second phase of a Small Business Innovative Research Contract, NAS3-25862, to develop a proof-of-concept (POC) MCDD that uses a convolve-multiply-convolve technique to perform the demultiplexing function and that is implemented using a surface acoustic wave herringbone-shaped reflective array compressor with hyperbolically shaped transducers (Fig. 4). Westinghouse Electric Corporation Communications Division is under contract to NASA Lewis (NAS3-25865) to develop a POC multichannel demultiplexer (MCD) implemented as a coherent acousto-optic RF spectrum analyzer utilizing heterodyne detection with a modulated reference. Figure 5 shows a completely optical MCDD. Currently, only the demultiplexer is being developed. The integrated optical detector and demodulator are to be developed when the channelizer has been proven in hardware. TRW is under contract with Lewis (NAS3-25866) to develop a POC MCDD with advanced digital technologies (Fig. 6). The University of Toledo is in the third year of grant (NAG3-799) to develop a programmable architecture for multicarrier demodulation based on parallel and pipeline digital design techniques for increased throughput. Lewis has begun an in-house effort to develop an MCDD by using commercial digital signal processors.

Demodulator/Decoder System

After the composite RF signal has been demultiplexed, the individual channels have to be demodulated and decoded. Two approaches have been identified to accomplish this: (1) complete parallel processing of individual channels or (2) time sharing the demodulator and decoder.

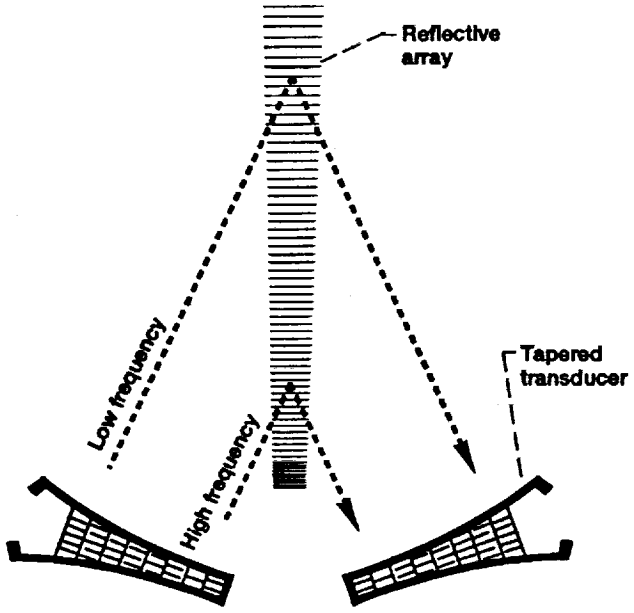

Fig. 4.—Hyperbolic reflective array compressor.

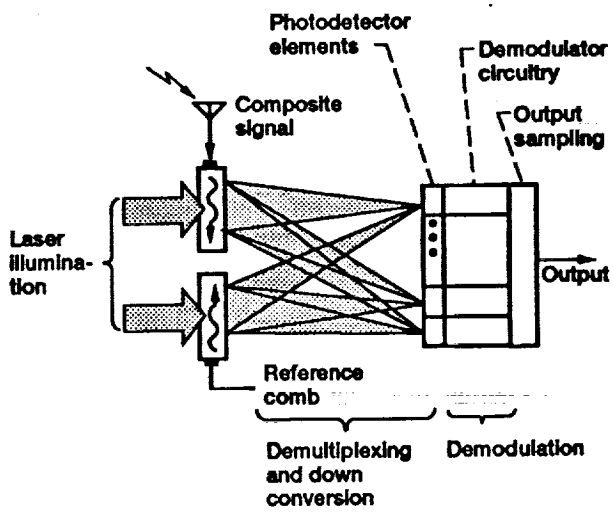

Fig. 5.—Optical multichannel demultiplexer/demodulator.

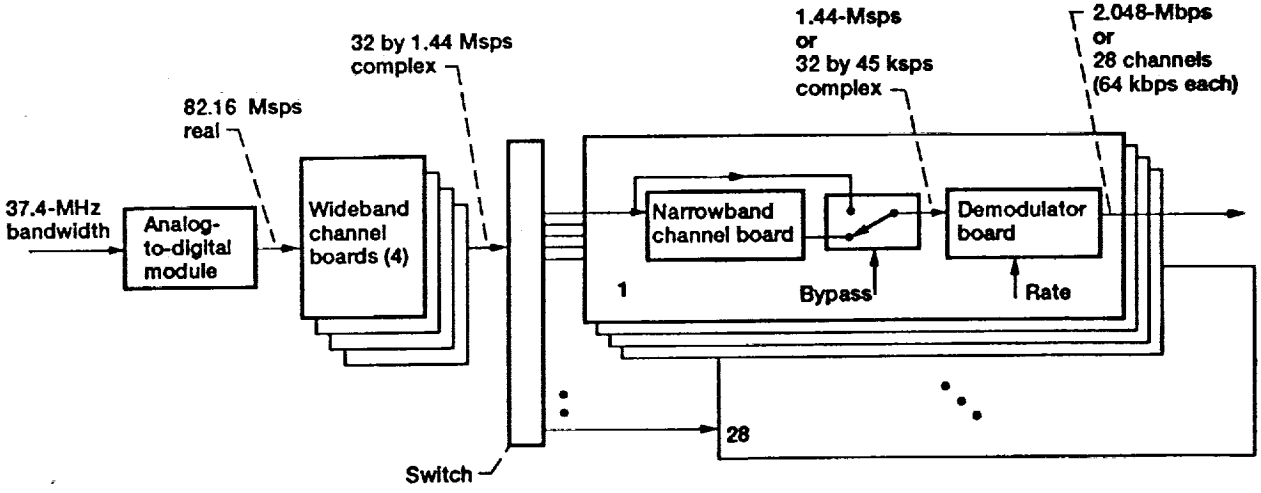

Fig. 6.—Digital multichannel demultiplexer/demodulator. Rate shown in megasymbols per second (Msps).

The parallel-processing approach is conceptually simple and fault tolerant but considered hardware intensive. Each channel out of the demultiplexer has its own demodulator and decoder. With this architecture, the data flow is continuous through the system; therefore the decoding can be performed with a convolutional decoder. The drawback of this approach is that the same circuity would have to be duplicated over 8000 times, one time for each channel.

The present approach is to time share a bank of continuous demodulators that can each handle 24 to 32 channels. A unique characteristic of the FDMA-processing, time-shared demodulator is that the information comes out in a bit-interleaved cyclical order (Fig. 7). Because of this, a buffer is required between the shared decoder and shared demodulator in order to assemble a segment of information for each channel that is long enough to be efficiently decoded by the shared decoder. The decoder decodes information blocks from each channel on a segment-by-segment basis. Both, convolutional and block decoders have been considered. If a convolutional decoder were used, one could either throw away a predetermined number of bits at the beginning of each information segment to allow the decoder to initialize, or one could save the previous state of the codec and jam this state into the decoder at the beginning of the next time slot for that particular source channel. If a block decoder were used, the information originating from the Earth station would have to be in the form of continuously concatenated, fixed-length packets. In addition, these packets would have to be synchronized within a demodulator-to-decoder buffer.

Formatting Buffer

The formatting buffer takes parallel messages and stores them in a single 8K deep memory block. The width is equal to or greater than the minimum length of a single channel's bursted downlink message. Although simple in concept, this is an extremely difficult problem because of the amount of hardware necessary to convert 8192 individual 64-kbps channels and 256 individual 2.048-Mbps channels into separate address locations within a single block of memory.

Switching and Routing System

The switching and routing system effectively acts as a combination of an 8192 by 64 circuit switch and a 256 by 64 circuit switch assuming eight MCDD's with either 1024 users of 64 kbps or 32 users of 2.048 Mbps. This is where the actual FDM-to-TDM conversion occurs. If one assumes that for any given frequency into the multichannel

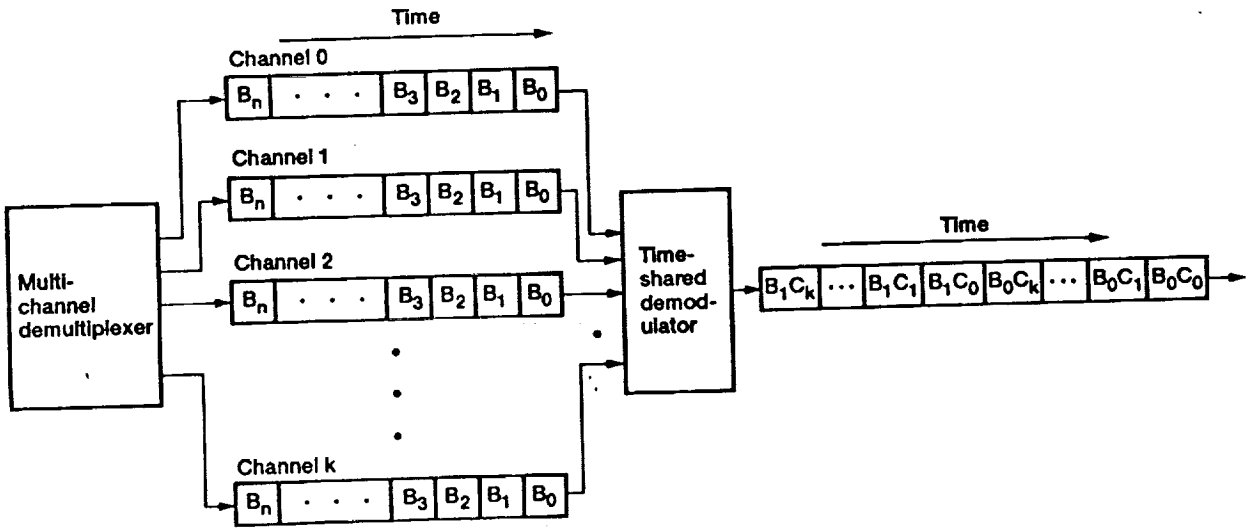

Fig. 7.—Bit interleaving.

demultiplexer, one and only one path through the hardware is available, then messages may be sorted and routed by network control through frequency allocations. However, there is a problem with this method when considering multicast capability. Depending on the implementation of this switch, additional circuitry may be required for multicasting.

Numerous studies and papers have been published in this area of switching and routing, including optical switching and the use of neural networks.[9-16] One candidate method that fits well in circuit-switch applications is memory-to-memory sorting through a high-speed bus (Fig. 8). Here, the system switches and routes the signals by controlling the read address on the FDM buffer and the write address on the TDM buffer. Via this method, all switching and routing can take place—including multicasting. Once per frame, the FDM buffer and the formatting buffer are swapped as are the TDM buffer and transmit-side burst buffers, thereby updating the FDM and burst buffers. Orderwire messages are also inserted into the downlink buffers through the same switching and routing scheme.

Transmit-Side Burst Buffer

The transmit-side burst buffer is arranged so that each section corresponds to a particular downlink dwell location for the hopping beams. There must be reserved time slots within each dwell array for orderwires, for each 64-kbps circuit, and for each 2.048-Mbps circuit destined for that particular downlink dwell.

Encoder

The encoder is required to provide coding gain on the downlink. This encoder may be either a convolutional encoder or a block encoder capable of operating at 150 to 200 Mbps. A

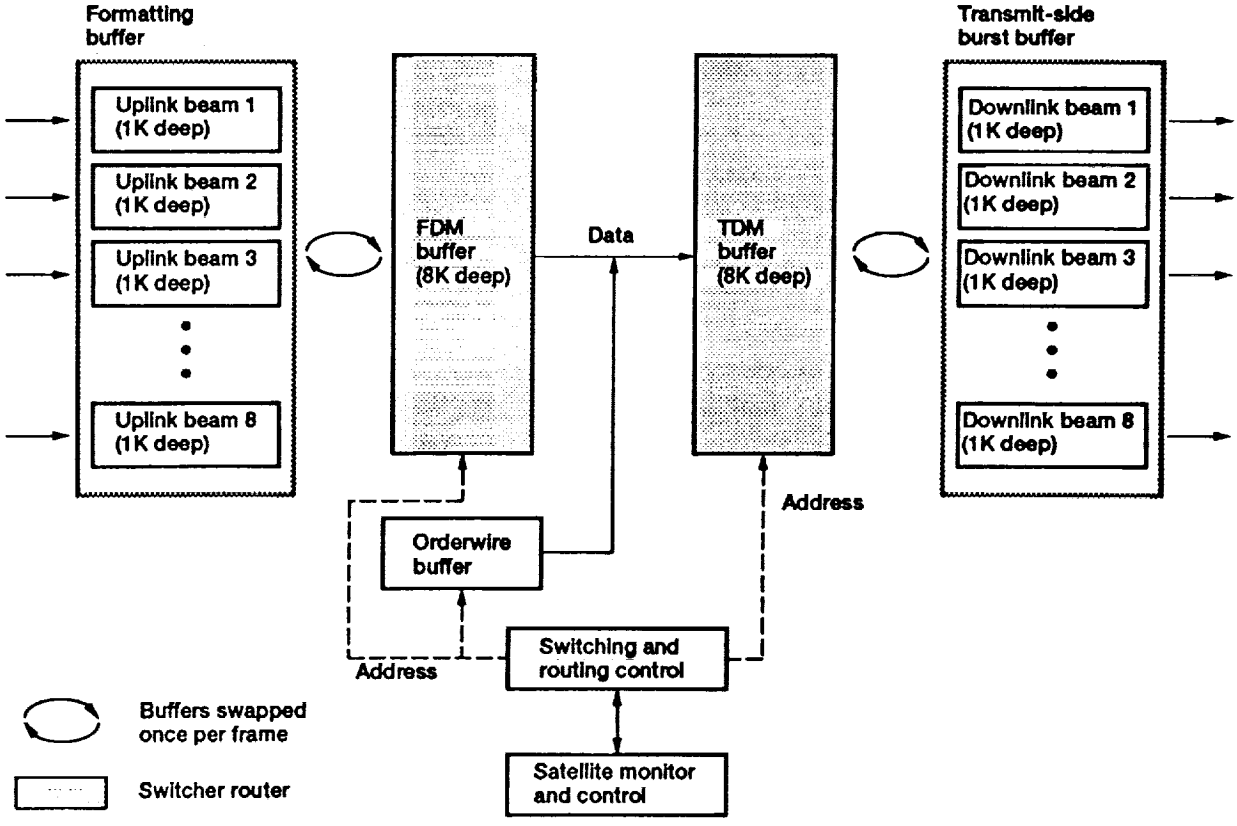

Fig. 8.—Switching and routing system.

corresponding decoder is required at the Earth terminal. Presently, block decoders that handle these rates are available as commercial products. Convolutional decoders are much more difficult to implement but are easier to apply in cases involving data bursts of continually varying lengths. In addition, the onboard convolutional encoder is extremely simple to implement. Therefore, the initial assumption is that convolutional encoding will be used.

Modulator

A burst modulator capable of a bandwidth-efficient modulation scheme is required. A continuous-phase modulation format is desired to run the satellite's high-power amplifiers at saturation, thus improving the downlink efficiency. NASA Lewis has an ongoing program in modulation and coding directed at such requirements. Among these are two completed contracts for 200-Mbps burst modems for satellite-to-ground applications: (1) a 16-CPFSK (continuous-phase frequency-shift-keying) modem and (2) an 8-PSK modem.[17-18] Additional work is being performed by COMSAT Laboratories (under contract NAS3-319317) on a programmable digital modem capable of binary, QPSK, 8-PSK, and 16-QAM (quadrature amplitude modulation) with up to 300 Mbps of data throughput.

Satellite Monitor and Control

The Satellite Monitor and Control (SM&C) interfaces with network control via a telemetry, tracking, and control link, and SM&C performs two basic functions: real-time health monitoring and fault recovery of the onboard communication systems and onboard network control. The SM&C can be viewed as the onboard extension of the network control. It receives antenna dwell plans, orderwire information, and switching and routing information from network control and passes this information on to the proper circuitry. In addition, the SM&C reports satellite health status and relays acquisition requests to network control.

Network Controller

In a circuit-switch network, most of the network control can be performed in a master control Earth station. The network controller is responsible for allocation of the space and ground resources. In particular, traffic allocation and routing functions, including generation of burst time plans, will be performed on the ground.

Concluding Remarks

From an overall systems view, the problem of getting tens of thousands of low-data-rate users to communicate with each other through a processing satellite is of equal complexity whether it is accomplished using TDMA/TDM, FDMA/TDM, CDMA/TDM or another type of architecture. FDMA and, more recently, CDMA techniques have been touted as being superior to TDMA because of the reduced uplink transmitting power required versus TDMA which, in turn, implies reduced Earth terminal cost. These techniques, however, mandate that extremely complicated and hardware- and memory-intensive functions be performed onboard.

Any onboard processing system requires fault-tolerant implementation. With size, weight, and power at a premium, traditional fault-tolerant methods such as simple two-for-one redundancy of components and systems or majority voting will not suffice. NASA Lewis Research Center plans to address these issues in all aspects of the information-switching processor (ISP) design and is pursuing innovative fault-tolerant approaches that optimize redundancy requirements. Presently, the issue of fault tolerance in the digital multichannel demultiplexers, time-shared demodulators, and convolutional decoders are being addressed through a grant with the University of California at Davis (NAG3-1166).

The present data rates of 64 kbps and 2.048 Mbps were chosen as a starting point and to be compatible with terrestrial ISDN networks. It is understood that these data rates may not be optimum. In particular, the uplink transmission rates may be sightly higher to accommodate the forward error correction overhead.

Status and Future Directions

NASA plans to develop and construct a POC information-switching processor in-house at NASA Lewis. Lewis-developed POC hardware will be supplemented by advanced fault-tolerant components developed under contracts. The ISP architecture will ultimately be demonstrated in a satellite network simulation: an integration of the ISP with high-speed codecs, programmable digital modems, a multichannel demultiplexer/demodulator currently being developed under industry contracts and university grants,[19] compatible Earth terminals, and onboard and ground-based network control.

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