NASA Technical Memorandum 105422

68743

p.8

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Prepared for the
Ninth International Conference on Digital Satellite Communications
cosponsored by Intelsat and Telecom Denmark
Copenhagen, Denmark, May 18–22, 1992

(NASA-TM-105422) MULTIPLE-ACCESS PHASED ARRAY ANTENNA SIMULATOR FOR A DIGITAL BEAM FORMING SYSTEM INVESTIGATION (NASA) 8 p
N92-17062
CSCL 20N
Unclas
G3/32 0068743

MULTIPLE-ACCESS PHASED ARRAY ANTENNA SIMULATOR FOR A DIGITAL BEAM FORMING SYSTEM INVESTIGATION

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Abstract

Future versions of data relay satellite systems are currently being planned by NASA. Being given consideration for implementation are on-board digital beamforming techniques which will allow multiple users to simultaneously access a single S-band phased array antenna system. To investigate the potential performance of such a system, a laboratory simulator has been developed at NASA's Lewis Research Center. This paper describes the system simulator, and in particular, the requirements, design, and performance of a key subsystem, the phased array antenna simulator, which provides realistic inputs to the digital processor including multiple signals, noise, and nonlinearities.

1. INTRODUCTION

Multiple access techniques have been employed by NASA to allow several users to simultaneously access the Tracking and Data Relay Satellite (TDRS). In the TDRS system, an S-band multiple access receive system collects the signals incident on the antenna and transmits them to the ground station, where the beams are separated through beamforming processing. In the advanced TDRS (ATDRS) system currently under development by NASA, studies indicate the feasibility of performing the beamforming functions on the satellite [1], [2].

The ATDRS is a follow-on program to the original TDRS System. The TDRS System is a geosynchronous satellite system consisting of two satellites plus one on-orbit spare. It is a space-based communications and data relay system communicating with a single ground station providing services for the Space Shuttle, orbiting science platforms, and other near-Earth orbiting payloads up to 10 000 km. The ATDRS system, along with enhancements to the ground segment, will provide increased capacity as well as new services and features for NASA near-Earth missions past the year 2000 into the early 21st century. These service enhancements include increased EIRP and data rates for the S-band Multiple Access (SMA) services, the addition of Ka-band Single Access (KaSA) service, and coverage to geosynchronous orbit. Additionally, the ATDRS space segment will consist of four operational satellites and one on-orbit spare thereby increasing the overall capacity of the system compared to the TDRS system.

NASA Lewis Research Center has investigated a digital approach to on-board beamforming by building a laboratory simulation of a seven element receive antenna and digital beamforming processor (DBFP). This simulator represents a subset of a full 13 by 13 (169 element) array proposed for the ATDRS S-band multiple access system. A set of experiments using this simulator investigated digital beamforming methods as applied to the ATDRS architecture, including the effects of noise, interferers, and distortion.

The digital beamforming system investigation requires a realistic simulation of the S-band phased array antenna. To meet this requirement, a phased array simulator (PAS) has been developed. This paper describes the requirements and design of the PAS, its integration into the overall test system, and results of subsystem and system performance measurements.

2. SYSTEM DESCRIPTION

The digital beamforming system block diagram is shown in Figure 1. The DBFP will be tested for its ability to discriminate a "desired" signal from one or two "interferer" signals in the presence of noise and analog and digital nonlinearities, as a function of signal level and A/D resolution. This discrimination ability will be measured quantitatively in terms of bit-error rate (BER). The phased array simulator is thus required to provide an input to the DBFP representing three signals incident on the antenna at various angles relative to the antenna boresight axis.

The DBFP is described by Figure 2. The signals from the seven antenna elements, downconverted to a 20 MHz IF, are converted to digital samples and mixed with in-phase and quadrature clocks to produce seven pairs of I and Q channels. Complex weighting is applied to align the "desired" signal components in phase while the "interferer" signals remain unaligned, after which the signals are recombined. The resulting signal is upconverted to a 70 MHz IF and returned to the modem for demodulation and bit-error rate measurement.

3. PHASED ARRAY SIMULATOR REQUIREMENTS

The Phased Array Simulator must simulate the outputs of seven phased array antenna elements. Figure 3 shows the geometrical considerations for the phased array simulator. The antenna is required to scan ±13° to cover users in low earth orbit, plus an additional ±4.1° to test over the entire null-to-null bandwidth of the main antenna lobe. Simulating a 13 by 13 array with a seven-element linear array requires scaling the PAS scan range to 24° (+4.1°). As shown in Figure 3(b), the maximum phase delay across the seven elements is 2041°. To run a series of tests in which the scan angle is varied in 1° steps, the maximum allowable phase error across the seven elements is $2041° \div (24 + 4.1)° = 72.6°$. The maximum phase error per element is $(72.6° \div 6) = 12.1°$. This requires the PAS to have a minimum four-bit (11.25°) phase resolution.

The PAS, in addition to meeting the phase error requirements, must provide a variable output signal power level to test the effects of A/D nonlinearity at the DBFP input. Also, a variable output energy-per-bit to noise power density ratio (E_b/N_o) is required to allow BER measurements to be made over a range of conditions. The test signals being used are 2.048 Mbps QPSK modulated signals, transmitted through a 4 MHz channel bandwidth. To cover a range of BERs of 10^{-2} to 10^{-8}, and considering the processing gain for a seven-element array of $10*\log(7) = 8$ dB, the E_b/N_o range for each antenna element is -4 to 6 dB. One final requirement of the PAS is to allow analog channel nonlinearities to be simulated.

4. PHASED ARRAY SIMULATOR DESIGN

The system designed to meet these requirements is shown in Figure 4. The desired signal, S1, and the two interferer signals, S2 and S3, from three QPSK modulators (downconverted from 70 to 20 MHz, see Figure 1) are distributed to each of eight antenna simulator elements (including one redundant element). Each element produces an output signal to the DBFP and two monitor signals for calibration.

Each element has at its input three phase shifters. The three phase shifters in each element are connected to signals S1, S2, and S3, respectively. Figure 5 shows how the three signals can be simulated to have three different incident angles with respect to the antenna boresight axis by independently varying the phase in each of the phase shifters.

Figure 6 shows the design details for an individual PAS element. A white noise source is used in conjunction with a variable attenuator to allow a variable E_b/N_o for each PAS element. A second attenuator controls the input to an amplifier which can be driven into saturation to allow analog nonlinearities to be introduced. A third attenuator controls the element output power and can be used to over or under drive the A/D converters in the DBFP. Bandpass filtering in each element limits the channel bandwidth and noise bandwidth to 4 MHz. All of the attenuators and phase shifters are under direct control of the test control computer. Thus, the system configuration can be automatically changed in terms of angle of incidence of received signals, E_b/N_o, and amount of analog and digital nonlinearity.

5. PHASED ARRAY SIMULATOR PERFORMANCE

Testing of each PAS element has indicated that the performance does not vary significantly from element to element. The insertion gains for all elements are within ±1.2 dB and the insertion phase is within ±3° with the phase shifters set to 0°. The available noise power output varies ±1.8 dB between the elements. The elements average 0.87 deg/dB AM/PM in linear operation and 2.27 deg/dB in nonlinear operation.

The output power can be varied over a 20 dB range, and the noise power can be varied over a range of greater than 30 dB. The required E_b/N_o range of -4 to 6 dB is easily achieved. Figure 7 is a plot of the output spectrum showing an unmodulated carrier combined with noise over a 4 MHz bandwidth for a typical PAS element. In summary, the measured performance of the PAS is well within the requirements for the digital beamforming simulation.

Each PAS element was also tested for its digital data transmission performance. This was accomplished by bypassing the DBFP and connecting the output of a PAS element directly to the upconverter (see Figure 1). The bit error rate was measured as the E_b/N_o was varied from 3 to 12 dB. The average performance of the PAS elements is 10^{-6} BER at an E_b/N_o of 11.5 dB. This is approximately 1 dB of loss compared to the theoretical QPSK case.

In applying the PAS outputs to the DBFP, cross coupling between elements is an important consideration. The digital processor must determine a set of complex weights to be applied to the signals from each element of the array. These weights are chosen to offset the phase and gain differences between the individual elements such that the signals become colinear and sum to a single maximized output signal. For an n-element array, this requires multiplication of the received signal set by an n X n complex weight matrix. This is the inverse of the complex gain matrix representing the amplifier/translator chain from the antenna through each element to the DBFP input. Cross-coupling terms between the elements produce off-diagonal terms in this gain matrix. If cross-coupling terms are zero or negligible, the set of n^2 complex multipliers can be reduced to a set of n multipliers, thereby greatly reducing the complexity of the digital processing.

The PAS was tested to determine the differential gain and phase between elements, including cross coupling terms, to produce the n X n set of complex gain terms. The inverse gain matrix was then computed from the results of these tests. The cross coupling measured between the elements of the PAS was found to be negligible, and the inverse gain matrix could be reduced to a diagonal matrix with zero off-diagonal terms.

6. EXAMPLES OF DIGITAL BEAMFORMING RESULTS

The successful operation of the PAS has allowed a large set of data to be acquired by the digital beamforming system simulator. Two examples of these results are given. The first, shown in Figure 8, is a beam pattern produced by varying the antenna pointing angle over a range of ±13°. The PAS in this configuration is simulating a boresight signal with no interfering signals present. The DBFP controls the beam pointing angle by varying the complex weights applied to the I and Q signals developed from each antenna element.

Figure 9 shows a BER plot demonstrating the performance of the DBFP in discriminating a desired signal in the presence of an interferer. The desired signal is incident at the antenna boresight angle and the interferer is incident at an angle of 3.8° from boresight. The upper curve was produced by summing four of the seven I and Q channels, while the lower curve was produced by summing all seven channels.

7. CONCLUSIONS

This paper has described the system and circuit level design of a multiple access phased array antenna simulator (PAS). The antenna simulator is a key part of a simulation system designed to investigate the application of on-board digital beamforming to the ATDRS system. The system requires that the PAS provide signals simulating the outputs of antenna elements with up to three signals incident on the antenna at various angles relative to the antenna boresight, as determined by the physical parameters of the proposed ATDRS system. Additionally, the PAS must provide for variable signal power, E_b/N_o, and nonlinearity. The PAS met all of the system requirements, and performed consistently between individual elements. Examples of the results of digital beamforming experiments using this system indicate that the PAS is successful in providing the proper simulation of the outputs of a phased array antenna. The system simulator has thus been able to provide a large set of test data indicating the performance of digital beamforming.

8. REFERENCES

[1] ATDRSS Digital Beamforming Simulation, Phase A Final Report. The Johns Hopkins University Applied Physics Laboratory, Laurel, Maryland, July 1988.

[2] TDAS/SMA On-Board Beamforming Technology and System Definition Study, Final Report. Harris Corporation, Melbourne, Florida, May 1985.

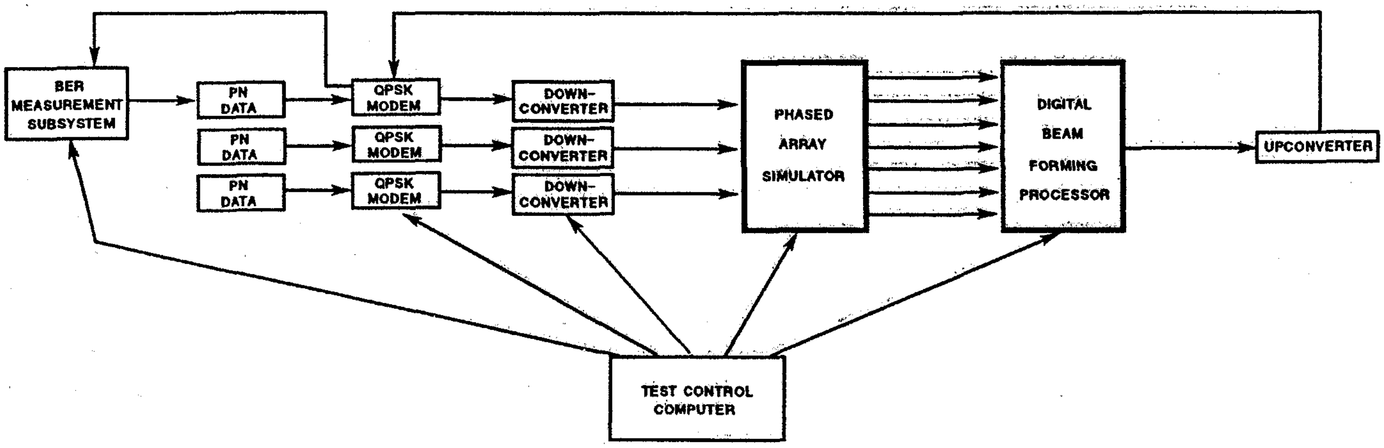


Figure 1.—Digital beamforming system simulator block diagram.

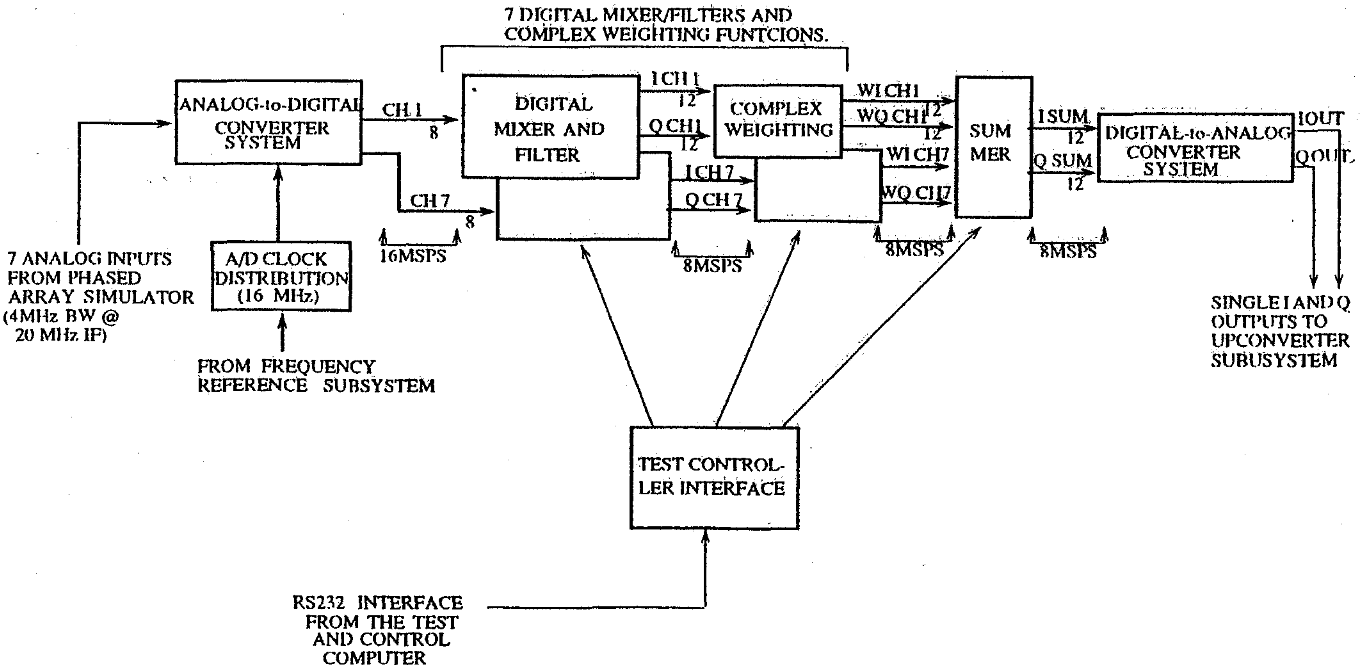
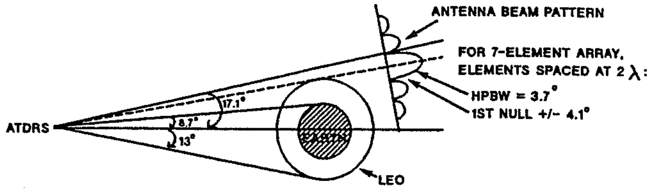
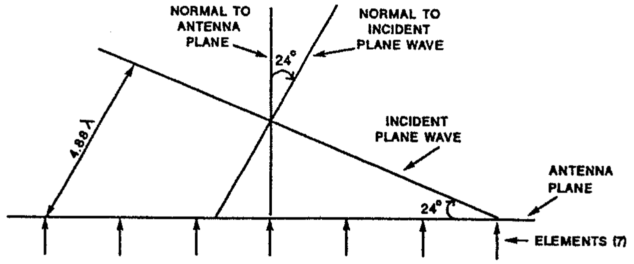


Figure 2.—Digital beam forming processor.



(a) ATDRSS system geometry.



MAXIMUM POINTING RANGE FOR TESTING = +/- 24°
MAXIMUM DELAY AT END ELEMENT = 4.88 λ = 1757°

TO TEST FROM 1ST NULL TO 1ST NULL:
POINTING RANGE = +/- (24 + 4.1)
MAXIMUM DELAY AT END ELEMENT = 5.67 λ = 2041°

(b) ATDRS SMA antenna geometry.

Figure 3.—Geometrical considerations for the phased array simulator design.

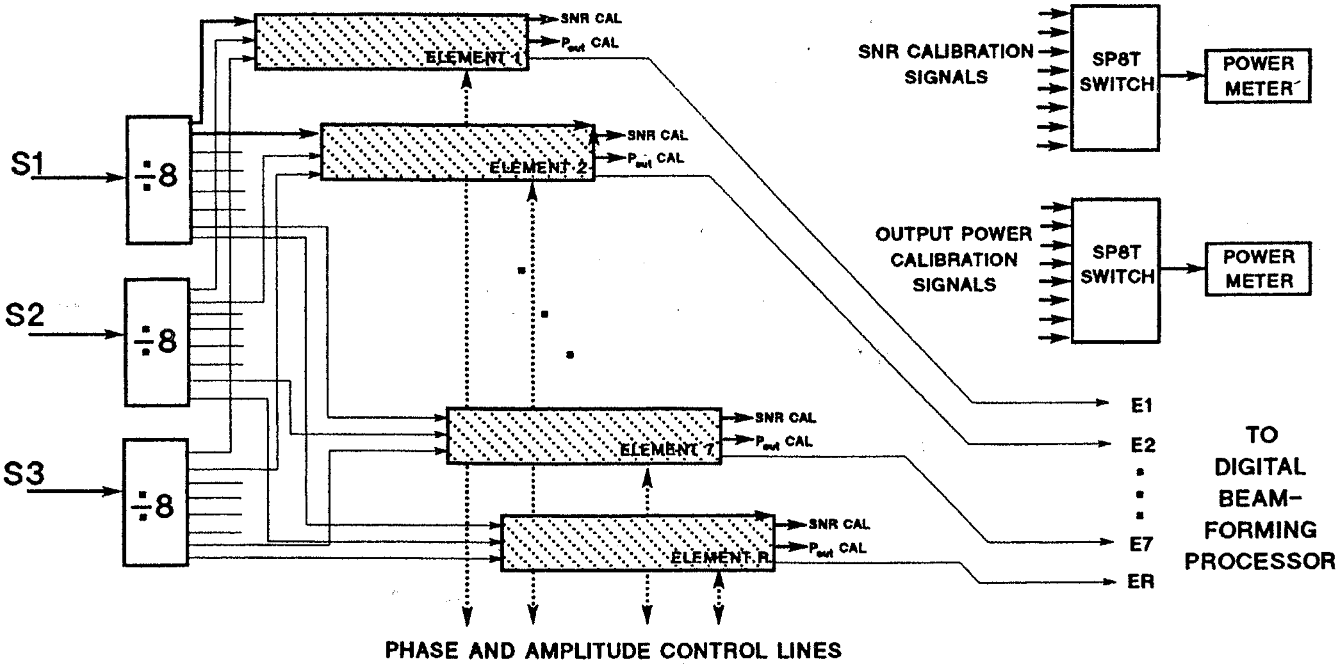
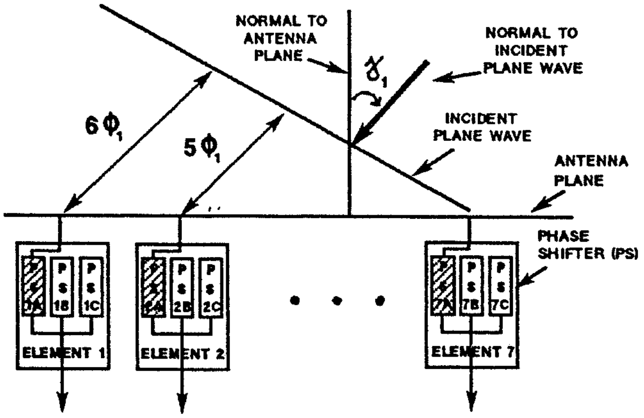
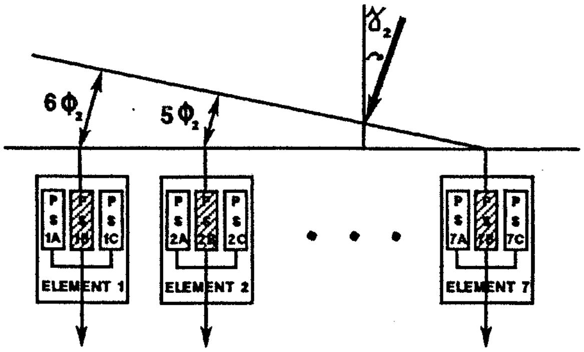


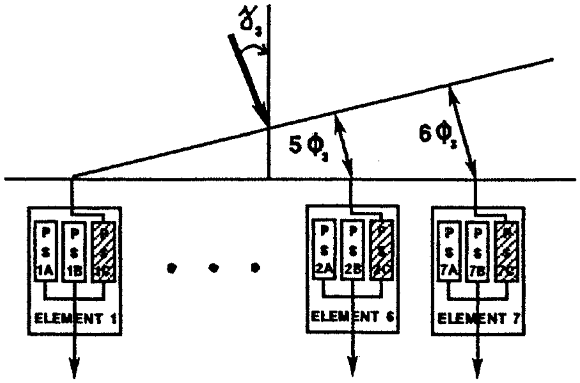
Figure 4.—Phased array simulator block diagram.



(a) Simulation of "desired" signal (S1).



(b) Simulation of interfering signal (S2).



(c) Simulation of interfering signal (S3).

Figure 5.—Simulation of incident signals by the phased array simulator.

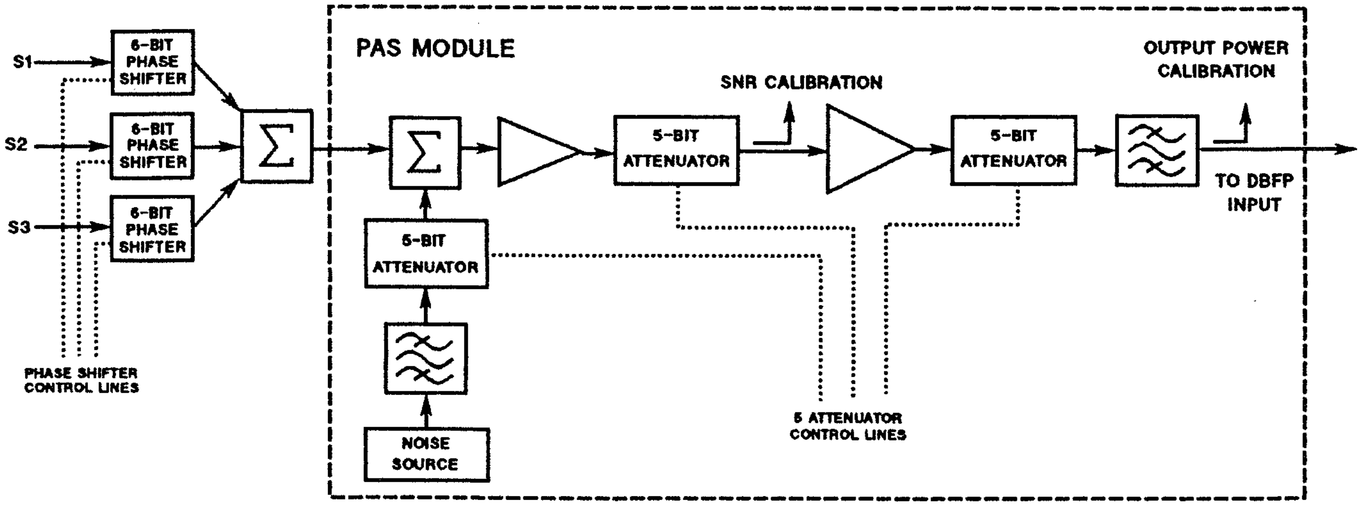


Figure 6.—Phased array simulator element block diagram.

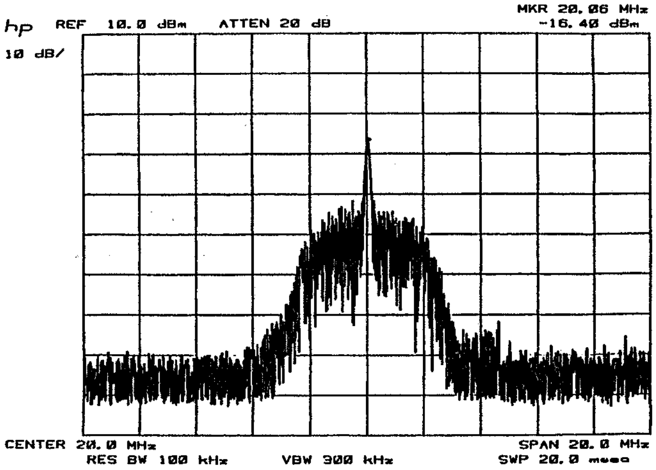


Figure 7.—Typical signal plus noise output spectrum of a phased array simulator element.

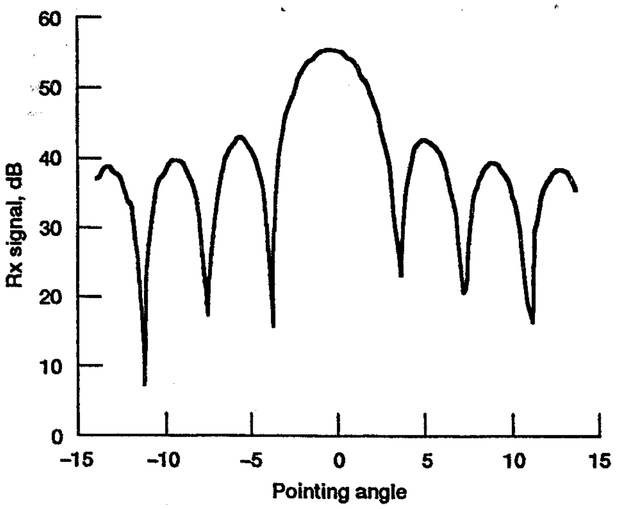


Figure 8.—Beam pattern developed by the digital beam forming system.

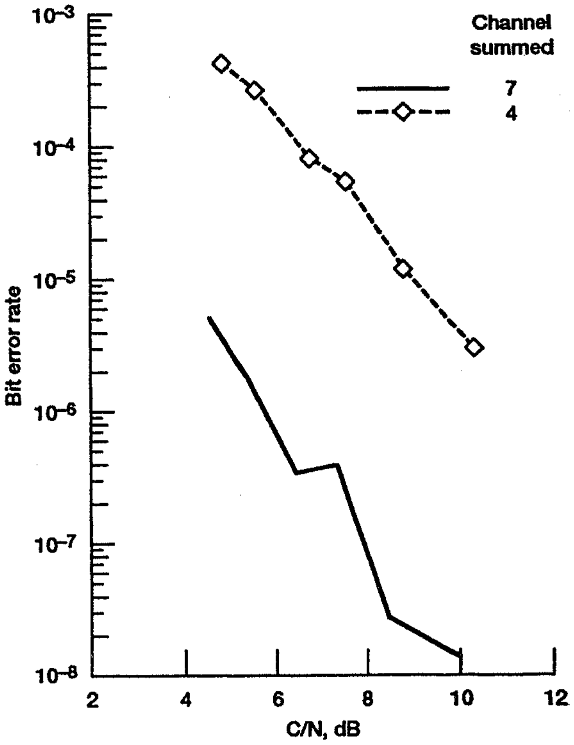


Figure 9.—Bit error rate measurement with interferer at 3.8 deg from boresight.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	**2. REPORT DATE** 1992	**3. REPORT TYPE AND DATES COVERED** Technical Memorandum

4. TITLE AND SUBTITLE

Multiple-Access Phased Array Antenna Simulator for a Digital Beam Forming System Investigation

5. FUNDING NUMBERS

WU-650-60-23

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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Cleveland, Ohio 44135-3191

8. PERFORMING ORGANIZATION REPORT NUMBER

E-6838

9. SPONSORING/MONITORING AGENCY NAMES(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Washington, D.C. 20546-0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA TM-105422

11. SUPPLEMENTARY NOTES

Prepared for the Ninth International Conference on Digital Satellite Communication cosponsored by Intelsat and Telecom Denmark, Copenhagen, Denmark, May 18-22, 1992. Robert J. Kerczewski, John Yu, Joanne C. Walton, Thomas D. Perl, Monty Andro, NASA Lewis Research Center, and Robert E. Alexovich, Analex Corporation, 3001 Aerospace Parkway, Brook Park, Ohio 44142. Responsible person, Robert J. Kerczewski, (216) 433-3434.

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Unclassified - Unlimited
Subject Category 32

12b. DISTRIBUTION CODE

13. ABSTRACT ***(Maximum 200 words)***

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14. SUBJECT TERMS

Digital beamforming; Phased array antenna; ATDRS multiple access

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT**

National Aeronautics and
Space Administration

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