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LEWIS ADVANCED MODULATION AND CODING PROJECT: INTRODUCTION AND OVERVIEW

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National Aeronautics and Space Administration
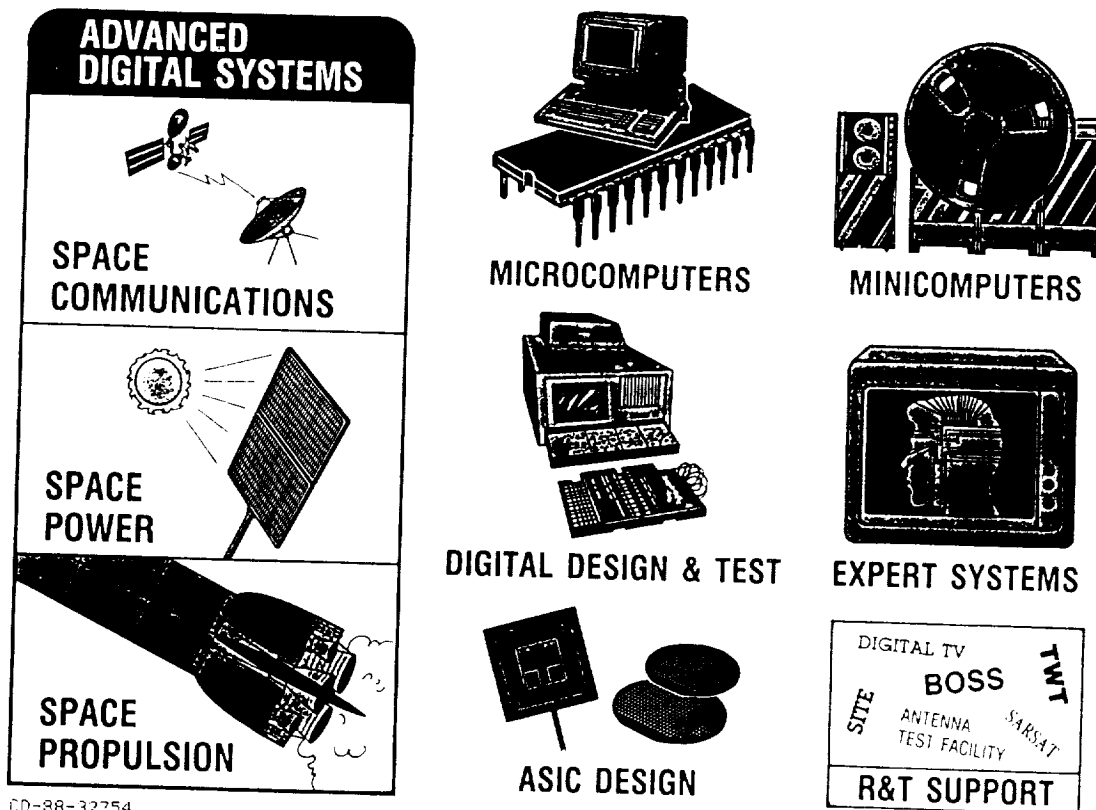Lewis Research Center
Cleveland, Ohio 44135

ABSTRACT

The Advanced Modulation and Coding Project at NASA Lewis Research Center is sponsored by the Office of Space Science and Applications, Communications Division, Code EC, at NASA Headquarters and conducted by the Digital Systems Technology Branch of the Space Electronics Division. Advanced Modulation and Coding is one of three focused technology development projects within the branch's overall Processing and Switching Program. The program consists of industry contracts for developing proof-of-concept (POC) and demonstration model hardware, university grants for analyzing advanced techniques, and in-house integration and testing for performance verification and systems evaluation. The Advanced Modulation and Coding Project is broken into five elements: (1) bandwidth- and power-efficient modems; (2) high-speed codecs; (3) digital modems; (4) multichannel demodulators; and (5) very high-data-rate modems. At least one contract and one grant have been awarded for each element.
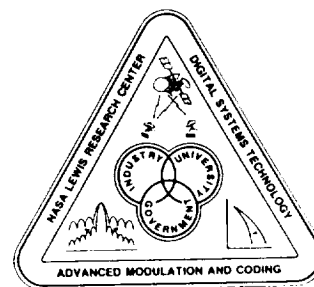
DIGITAL SYSTEMS TECHNOLOGY MISSIONS

The Space Electronics Division has maintained prime responsibility for space communications research and technology development at Lewis and has recently expanded its charter to provide electronics technology support to space power and propulsion missions. The Digital Systems Technology Branch provides expertise in advanced digital systems development disciplines including design of custom, computer-based, digital equipment, mini- and microcomputer software and control, application-specific integrated circuits (ASIC), and most recently, expert systems. To date, the branch's activities have been predominantly directed toward space communications.

In-house facilities and hardware and software expertise have been applied to the development of ground terminal digital subsystems, link effects simulation, and experiment control for evaluating microwave components and time-division- multiple-access (TDMA) networks. The branch also provides custom hardware and computer support to division research facilities for traveling wave tube amplifiers, near-field antenna pattern measurements, and digital video signal compression.

ADVANCED DIGITAL SYSTEMS

SPACE COMMUNICATIONS

SPACE POWER

SPACE PROPULSION

CD-88-32754

MICROCOMPUTERS

MINICOMPUTERS

DIGITAL DESIGN & TEST

EXPERT SYSTEMS

ASIC DESIGN

DIGITAL TV   TWT
BOSS
SITE   ANTENNA   SARSAT
TEST FACILITY
R&T SUPPORT

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PROGRAM GOALS AND FOCUS

The main goals of the Processing and Switching Program are shown below. The intention of the program is to identify and develop critical digital components and technologies that either enable new commercial and civil missions or significantly enhance the performance, cost efficiency, or reliability of existing and planned space communications systems. The sketch is intended to indicate that both frequency- and time-division multiple access (FDMA and TDMA), with onboard information processing and switching, and multiple-beam, time-division-multiplexed (TDM) downlink systems are investigated. Space and ground segment component designs are addressed concurrently to ensure cost efficiency and realistic operational constraints. Advanced theoretical concepts are implemented in hardware suitable for demonstrating risk reduction and commercial potential. Eventually the application of fault-tolerant design techniques and real-time expert system controls will address fully autonomous operation of onboard systems.

To date, the program has been focused on developing of advanced modulation and coding technologies through contracts and grants and on ground-based processing and control through in-house design, fabrication, and evaluation. The Digital Systems Technology Branch plans to significantly increase the attention paid to space-based processing and control through design and development of fault-tolerant, autonomous, onboard processors for information processing and switching.

DIGITAL SYSTEMS TECHNOLOGY
PROCESSING AND SWITCHING PROGRAM

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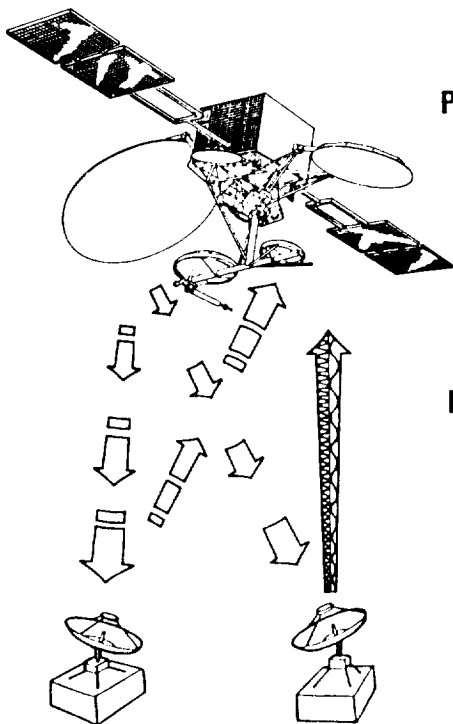
PROGRAM GOALS:
- **MISSION-ENABLING TECHNOLOGIES**
- **APPLICATION-FOCUSED MODELS**
- **DEVICES, COMPONENTS, AND SUBSYSTEMS**
- **CONCURRENT SPACE AND GROUND SEGMENTS**
- **ONBOARD FAULT TOLERANCE AND AUTONOMY**
- **RISK REDUCTION AND TECHNOLOGY TRANSFER**

PROGRAM FOCUS:
- **ADVANCED MODULATION AND CODING**
- **SPACE-BASED PROCESSING AND CONTROL**
- **GROUND-BASED PROCESSING AND CONTROL**

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DEVELOPMENT PLAN

The Digital Systems Technology Branch has successfully implemented the technology development plan shown below. Depending on program priorities, multiple contract awards and multiple phased developments can be accommodated to increase the probability of achieving viable solutions. Fully digital solutions are sought to exploit inherent advantages of reduced size, power consumption, and production cost; increased reliability; and avoidance of alignment, drift, and aging problems associated with analog techniques. Most contract developments address flexible, programmable, or extendable designs to reduce nonrecurring engineering costs and to ease the development of mission-focused hardware. Proposers are encouraged to identify preliminary designs, plans for transferring technology development into commercial products, and cost-sharing approaches in their proposals.

DIGITAL SYSTEMS TECHNOLOGY
TECHNOLOGY DEVELOPMENT PLAN

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- **CONTRACTS FOR ADVANCED IMPLEMENTATIONS OF THEORETICAL CONCEPTS**

- **MULTIPLE CONTRACTS; MULTIPLE DEVELOPMENT LEVELS**

- **GRANTS TO EXPLORE PROMISING TECHNIQUES THROUGH DESIGN AND BREADBOARD**

- **IN-HOUSE VERIFICATION AND SYSTEMS EVALUATION**

- **ADVANCED, DIGITAL SOLUTION—RECOGNIZED BENEFITS**

- **STUDY TASK AND TECHNOLOGY ASSESSMENT ADDRESSED IN PROPOSAL**

- **TECHNOLOGY TRANSFER AND COMMERCIALIZATION PLANS**

- **COST SHARING**

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Advanced techniques investigated under university grants, small business innovative research (SBIR) contracts, and aerospace industry study contracts help to establish the requirements for developing critical components and subsystems. Both universities and industry fabricate hardware models and special test equipment (STE) appropriate for demonstrating the advanced techniques on a stand-alone basis. The photograph on the left shows a portion of Ford Aerospace's 8-PSK POC demodulator.

Digital subsystems for communications network and transponder test facility experiments, as well as some necessary STE and experiment controllers, are designed and developed in-house. The center photograph shows the 220 Mbps digital range delay simulator designed and fabricated in-house to simulate coarse and fine satellite motion. The simulator is used to evaluate network timing acquisition and synchronization techniques.

Under Lewis' Systems Integration, Test, and Evaluation (SITE) Project, POC and demonstration models are integrated with in-house and commercial hardware and software to create an end-to-end simulation facility of a satellite-switched, time-division-multiple-access (SS-TDMA) satellite network. The photograph on the right shows one of the TDMA ground terminals that incorporate 220/110-Mbps serial minimum shift keying (SMSK) modems developed under contract by Motorola, commercial 6809- and 68000-based microcomputer chassis, and in-house designed and fabricated TDMA controllers and multiple terrestrial user simulators.
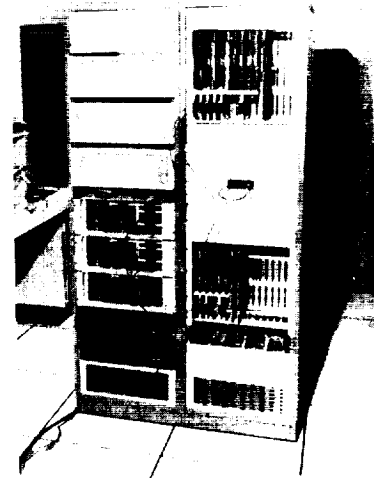
UNIVERSITY AND
INDUSTRY
DEVELOPMENT
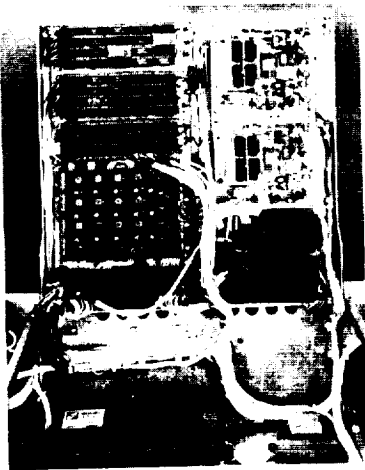
IN-HOUSE
DEVELOPMENT
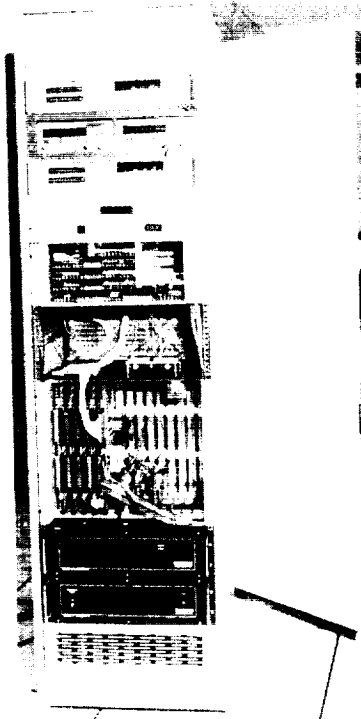
IN-HOUSE
EXPERIMENTAL SYSTEMS
INTEGRATION, TEST
AND EVALUATION

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READINESS LEVELS

The Office of Aeronautics and Space Technology (OAST) at NASA Headquarters defines seven levels of technology readiness shown in the left two columns below. The Space Electronics Division at Lewis has used the terms in the right column for several years in its requests for proposals and technical reports. The Processing and Switching Program addresses technology development from level 2 through level 5. In general, a POC model development (level 3) is selected when the first conversion of an advanced theoretical concept into hardware is required. A study and refinement of proposed design phase (level 2) is usually conducted by the contractor in an early POC contract task. For those technologies that currently exist in some hardware form, and where a significant increase in performance or packaging efficiency is necessary, the demonstration model approach (level 4) will be pursued. Finally, a flight-qualifiable model (level 5) may be fabricated for those technologies that require demonstration in a relevant environment to ensure mission readiness. Typically, the flight-qualified model and the flight model itself will be developed by a flight mission project office.

DIGITAL SYSTEMS TECHNOLOGY
TECHNOLOGY READINESS LEVELS

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LEVEL	NASA DEFINITION	LEWIS NOMENCLATURE
1	BASIC PRINCIPLES OBSERVED	BASIC RESEARCH AND TECHNOLOGY DEVELOPMENT
2	TECHNOLOGY CONCEPT AND/OR APPLICATION FORMULATED	PROOF-OF-CONCEPT STUDY PHASE
3	ANALYTICAL OR EXPERIMENTAL CRITICAL FUNCTION OR CHARACTERISTIC PROVED	PROOF-OF-CONCEPT MODEL DEVELOPMENT
4	COMPONENT AND/OR BREADBOARD VALIDATION IN THE LABORATORY	DEMONSTRATION MODEL DEVELOPMENT
5	COMPONENT AND/OR BREADBOARD DEMONSTRATION IN A RELEVANT ENVIRONMENT	FLIGHT-QUALIFIABLE MODEL
6	SYSTEM VALIDATION MODEL DEMONSTRATION IN A SIMULATED ENVIRONMENT	FLIGHT-QUALIFIED MODEL
7	SYSTEM VALIDATION MODEL DEMONSTRATION IN SPACE	FLIGHT MODEL

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# ADVANCED MODULATION AND CODING PROJECT OBJECTIVES

The objectives of the Advanced Modulation and Coding Project are shown below. The primary goal of this project is to develop bandwidth-efficient digital modulation schemes that are suited to the power, cost, and complexity constraints of an operational system. These schemes should provide bit-error-rate performance comparable to commercial quadrature phase shift keying (QPSK) standards. As is true of all three projects within the Processing and Switching Program, an underlying objective is to reduce the development risk and cost and thereby increase the potential for technology transfer to the commercial industry.

The highlighted blocks in the diagram indicate a concentration of effort on combined modulation and coding techniques and on forward-error-correction (FEC) coding. Techniques and components are under development for both space and ground segment applications.

An overview of the recent and current contracts and grants under the Advanced Modulation and Coding Project is presented later in this paper.
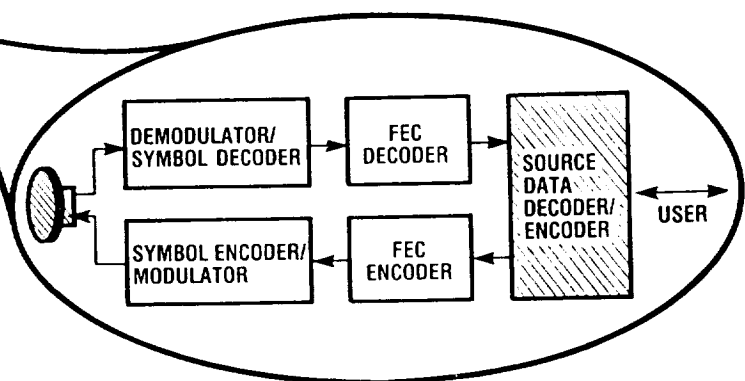
DIGITAL SYSTEMS TECHNOLOGY
ADVANCED MODULATION & CODING

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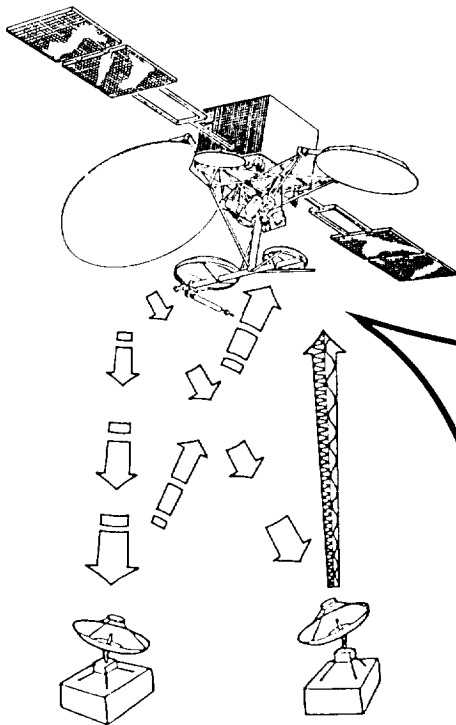
OBJECTIVES:
- BANDWIDTH AND POWER EFFICIENCY
- INCREASED INFORMATION CAPACITY
- MAINTAIN COMMERCIAL BER vs E_b/N_0 STANDARDS
- SIZE AND COST-EFFICIENT DIGITAL IMPLEMENTATION
- TECHNOLOGY DEMONSTRATION FOR MISSION READINESS
- SERVICE-ENABLING TECHNIQUES AND SUBSYSTEMS

DEMODULATOR/ SYMBOL DECODER → FEC DECODER → SOURCE DATA DECODER/ ENCODER ↔ USER
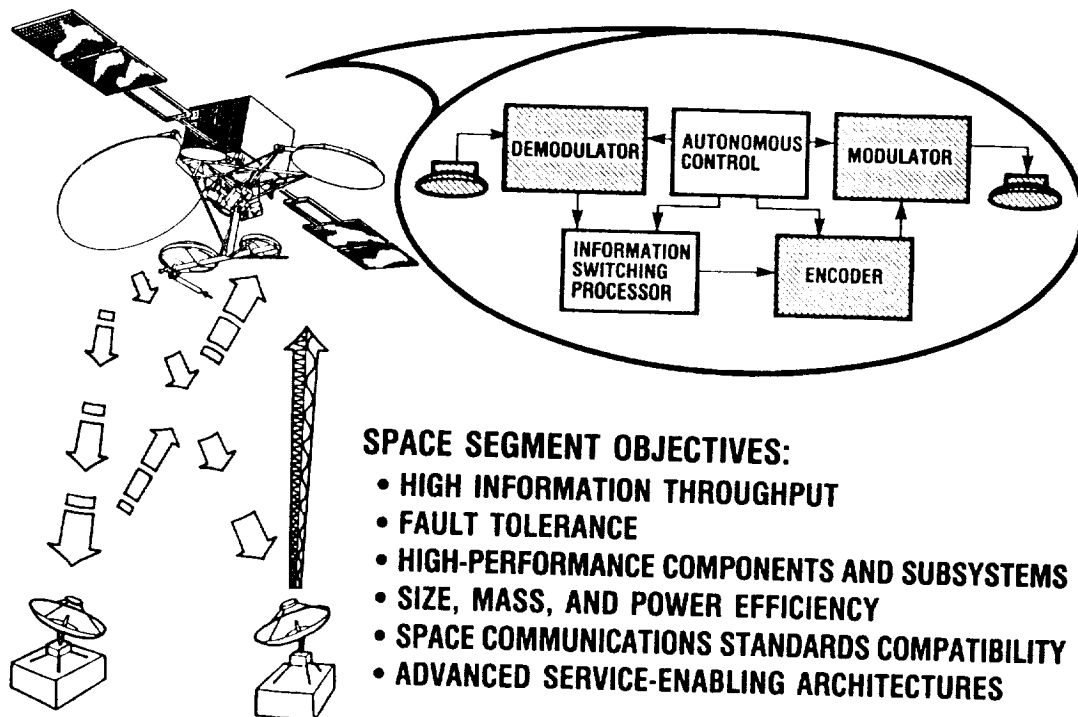
SYMBOL ENCODER/ MODULATOR ← FEC ENCODER ←

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SPACE-BASED PROCESSING AND CONTROL PROJECT OBJECTIVES

The objectives of the Space-based Processing and Control Project are shown below. The project has two primary goals associated with the two highlighted blocks in the diagram. The first goal is to develop a high-throughput, fault-tolerant, information-switching processor with circuit and packet switching capabilities compatible with emerging commercial and international space communications standards. The second goal is to incorporate into the onboard electronics package selected network control and data-processing functions traditionally performed in various locations within a terrestrial network.

Both the information-switching processor and the autonomous controller will require radiation-tolerant components with built-in testability and some level of real-time artificial intelligence for fault detection and isolation and real-time reconfiguration of onboard resources. When combined with advanced modulation techniques such as multichannel demultiplexing and programmable digital modems, fault-tolerant onboard processing and autonomous control can enable new commercial and civil satellite services.

DIGITAL SYSTEMS TECHNOLOGY
SPACE-BASED PROCESSING AND CONTROL

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SPACE SEGMENT OBJECTIVES:
- HIGH INFORMATION THROUGHPUT
- FAULT TOLERANCE
- HIGH-PERFORMANCE COMPONENTS AND SUBSYSTEMS
- SIZE, MASS, AND POWER EFFICIENCY
- SPACE COMMUNICATIONS STANDARDS COMPATIBILITY
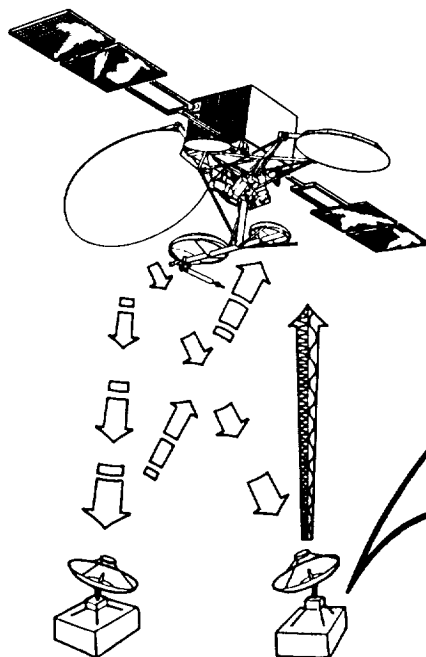- ADVANCED SERVICE-ENABLING ARCHITECTURES

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GROUND-BASED PROCESSING AND CONTROL PROJECT OBJECTIVES

The objectives of the Ground-based Processing and Control Project are shown below. The primary goal of this project is to develop flexible FDMA and TDMA controllers and terrestrial user interfaces for cost-efficient ground terminals. The controllers and interfaces must be compatible with the evolving processing satellite network architectures envisioned by NASA.

To date, only in-house activities have been pursued under this project. In support of the Systems, Integration, Test, and Evaluation (SITE) Project, multiple TDMA ground terminal digital subsystems have been designed and developed. Modems and codecs developed under the Advanced Modulation and Coding Project will be integrated with the digital, ground-based processing and control hardware for performance evaluation in the SITE satellite network simulation facility.
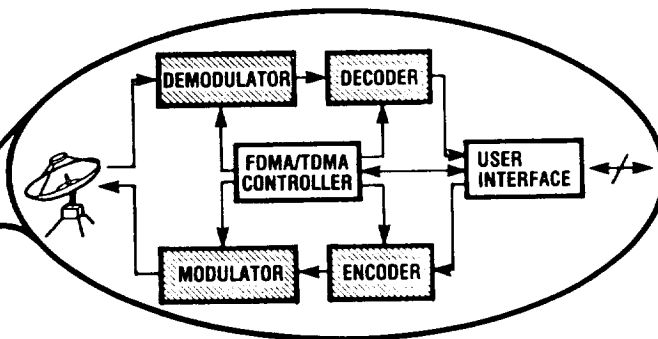
DIGITAL SYSTEMS TECHNOLOGY
GROUND-BASED PROCESSING AND CONTROL

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GROUND SEGMENT OBJECTIVES:
- COST-EFFICIENT IMPLEMENTATION
- HIGH-PERFORMANCE COMPONENTS
- FLEXIBILITY AND PROGRAMMABILITY
- INDUSTRY STANDARDS COMPATIBILITY
- INTELLIGENT SYSTEMS APPLICATIONS
- NETWORK SERVICE ENABLING

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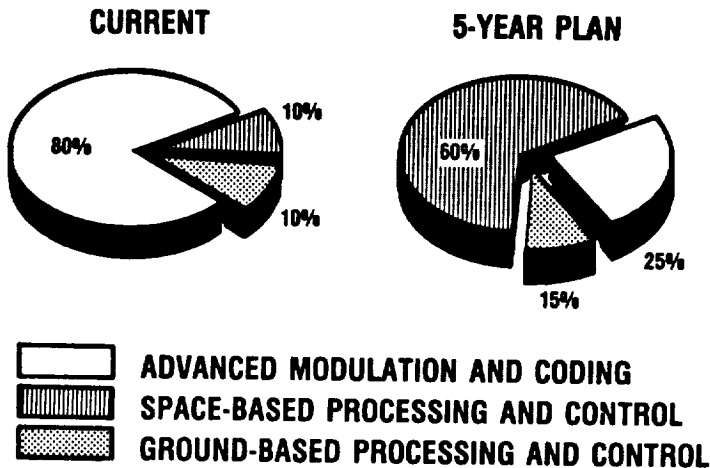
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PROGRAM FUNDING DISTRIBUTION

Currently, about 80 percent of the Processing and Switching Program funding is expended on the Advanced Modulation and Coding Project. The Space- and Ground-based Processing and Control Projects each consume about 10 percent of the remaining funds. Within 5 years the Digital Systems Technology Branch plans for the Space-based Processing and Control Project funding level to grow to about 60 percent of available funds and Ground-based Processing and Control funding to grow to about 15 percent. Since the total Processing and Switching Program funding projections vary yearly according to NASA priorities, funds available for the Advanced Modulation and Coding Project will vary as well.

The distribution of funds among industry contracts, university grants and in-house projects over the next 5 years is expected to remain nearly constant. The percentage distribution is shown below.

DIGITAL SYSTEMS TECHNOLOGY
PROCESSING AND SWITCHING PROGRAM

NASA
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FUNDING DISTRIBUTION BY PROGRAM ELEMENT

FUNDING DISTRIBUTION BY PROGRAM APPROACH

CURRENT

5-YEAR PLAN

CURRENT AND PLANNED

10%
80%
10%

60%
25%
15%

20%
70%
10%

ADVANCED MODULATION AND CODING
SPACE-BASED PROCESSING AND CONTROL
GROUND-BASED PROCESSING AND CONTROL

CONTRACTS
IN-HOUSE
GRANTS

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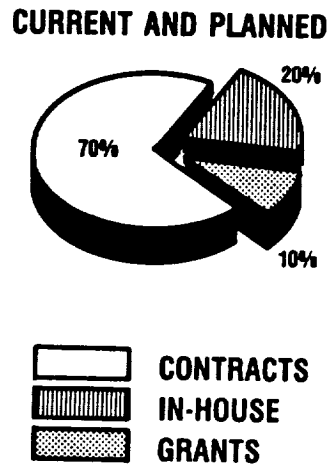
ADVANCED MODULATION AND CODING PROJECT
CONTRACTS AND GRANTS

The Advanced Modulation and Coding Project consists of five elements: (1) bandwidth- and power-efficient modems; (2) high-speed codecs; (3) digital modems; (4) multichannel demodulators; and (5) very high-data-rate modems. Contracts and grants are in place for each of the first four elements. Nearly all current and planned contracts are the cost-plus-fixed-fee type. Work under the fifth element is planned to begin in fiscal year 1990. Whenever possible, the Digital Systems Technology Branch has attempted to pursue each element by awarding a mix of openly competed hardware development contracts, SBIR contracts, and university grants. The unifying goal of this approach is the implementation and demonstration of advanced concepts and techniques.

DIGITAL SYSTEMS TECHNOLOGY
ADVANCED MODULATION & CODING CONTRACTS & GRANTS

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BANDWIDTH- AND POWER-EFFICIENT MODEMS:

- **ADVANCED MODULATION TECHNOLOGY DEVELOPMENT**

  FORD AEROSPACE, TRW, COMSAT LABS, HARRIS

- **AMTD FOLLOW-ON**

  CONTRACT(S) TO BE DETERMINED

- **MODULATION TECHNIQUES FOR POWER- AND SPECTRALLY EFFICIENT SATCOM SYSTEMS**

  UNIVERSITY OF CALIFORNIA, DAVIS

HIGH-SPEED CODECS:

- **FLEXIBLE HIGH-SPEED CODEC**

  HARRIS

- **IMPLEMENTATION OF ADVANCED CODING CONCEPTS**

  UNIVERSITY OF SOUTHERN CALIFORNIA

DIGITAL MODEMS:

- **PROGRAMMABLE RATE MODEM USING DIGITAL SIGNAL PROCESSING TECHNOLOGY**

  MULTIPOINT (T.I.W. SYSTEMS)

- **DIGITAL MODEM DEVELOPMENT**

  UNIVERSITY OF TOLEDO

- **PROGRAMMABLE DIGITAL MODEM**

  COMSAT LABS

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DIGITAL SYSTEMS TECHNOLOGY

ADVANCED MODULATION & CODING CONTRACTS & GRANTS

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MULTICHANNEL DEMODULATORS:

- ADVANCED TECHNOLOGY FOR A MULTI-CHANNEL DEMULTIPLEXER/DEMODULATOR — CONTRACTS (2) TO BE DETERMINED

- FDMA/TDM CONVERSION FOR NONCONTIGUOUS CARRIERS — UNIVERSITY OF TOLEDO

- INNOVATIVE PULSE COMPRESSORS FOR SATELLITE COMMUNICATIONS — AMERASIA

- DIGITAL SIGNAL PROCESSING FOR MULTI-CHANNEL DEMODULATION — LEWIS IN-HOUSE

VERY HIGH-DATA-RATE MODEMS:

- VERY HIGH-DATA-RATE MODEM — CONTRACT TO BE DETERMINED

- MODEMS FOR COMPRESSED VIDEO TRANSMISSION — GRANT TO BE DETERMINED

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ADVANCED MODULATION AND CODING PROJECT
CONTRACTS AND GRANTS (CONCLUDED)

The schedule below shows the Digital Systems Technology Branch's past, present, and planned contracts and grants in advanced modulation and coding and their phased relationship to each other. Contracts and grants are located from top to bottom by the level of attention paid to modulation techniques, coding techniques, and the combination of the two. All but the following two contracts are described further in this paper and in papers by the responsible contractors and universities.

The branch's responsibility for advanced modulation hardware development contracts began in mid-1983 with a modification to the baseband processor POC contract with Motorola Government Electronics Group (NAS3-22502). Under the modification, Motorola fabricated four sets of 220/110-Mbps SMSK modem pairs and six 27.5-Mbps SMSK modulators. The modems are similar to those being designed for the Advanced Communications Technology Satellite (ACTS) and have been used extensively in the SITE Project. They have also been included in the in-house link evaluation terminal (LET) designed to characterize the on-orbit performance of the ACTS high-burst-rate (HBR) subsystem.

Under a study contract funded by another branch within the Space Electronics Division, COMSAT Laboratories developed the conceptual design for an "onboard multichannel demultiplexer demodulator" (NAS3-24885). Several digital approaches were investigated and compared by computational complexity. The selected design featured a single, large, forward fast Fourier transform (FFT) processor followed by an inverse FFT for individual channel demultiplexing and a fully digital demodulator. The study served as the basis for a grant in FDMA/TDM conversion and both the multichannel demultiplexer demodulator (MCDD) and programmable digital modem (PDM) statements of work.


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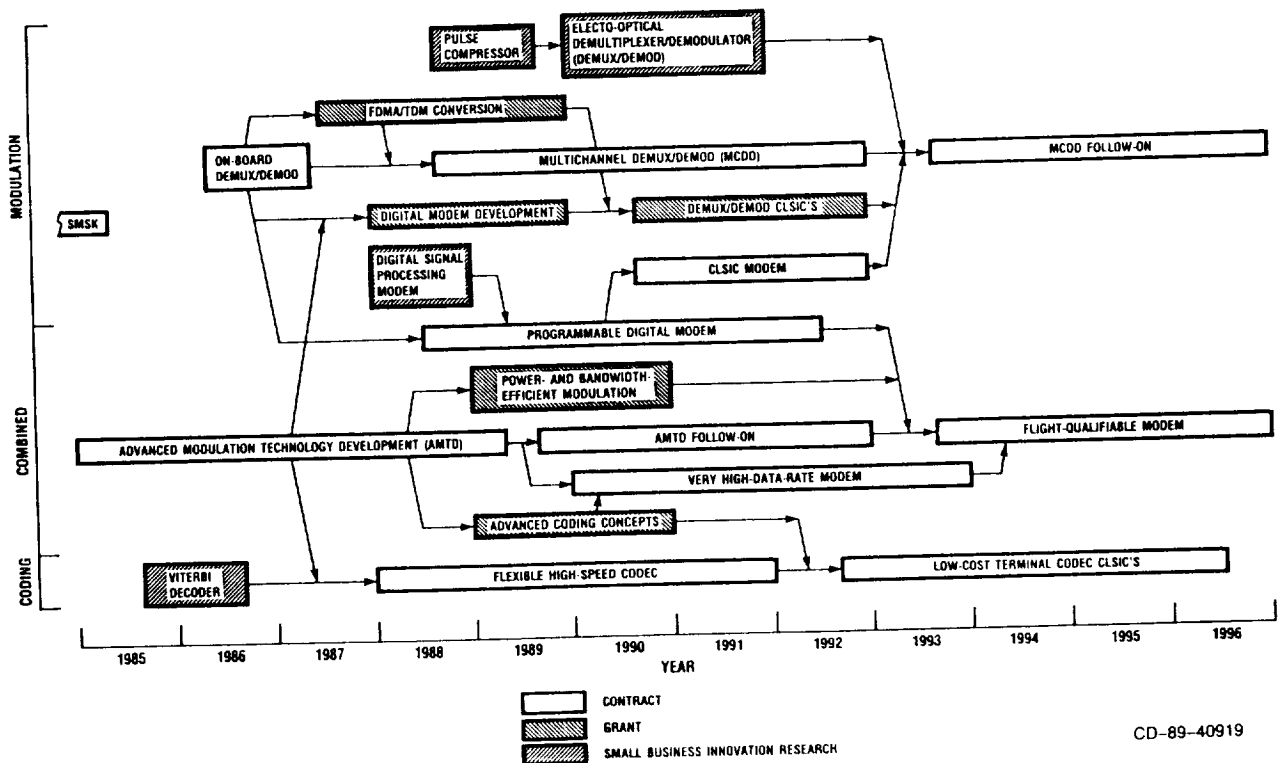
BANDWIDTH- AND POWER-EFFICIENT MODEMS

The curve shown below is based on the Shannon-Hartley capacity theorem, with the information bit rate equal to the capacity of the ideal channel. It illustrates the tradeoff between bandwidth and power efficiency for a given probability of bit error in a practical system. When both bandwidth and power are constrained, combined modulation and coding techniques such as trellis-coded modulation offer improved bandwidth efficiency with BER performance nearly identical to that of practical QPSK systems. The drawback of this approach is increased computational complexity.

The purpose of this project element is to develop practical implementations of bandwidth- and power-efficient modems that are suitable for application in space and ground environments. For spacecraft demodulators, rapid, independent acquisition and small size, mass and power consumption are desirable. For ground terminal demodulators, high data rates and low-cost implementations are the primary goals. The techniques demonstrated under this project element are scalable in information rate, largely independent of the frequency band of operation, and applicable to a variety of spacecraft communications links.

DIGITAL SYSTEMS TECHNOLOGY
BANDWIDTH- AND POWER-EFFICIENT MODEMS

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R/W (bps/Hz) vs E_b/N_0 (dB), with BANDWIDTH EFFICIENT and POWER EFFICIENT regions.
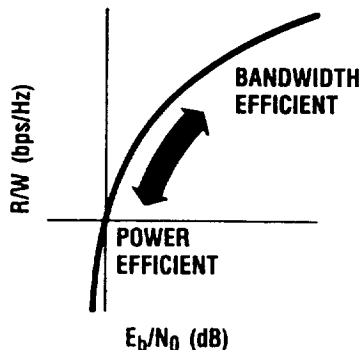
OBJECTIVES:

- TRIPLE ACTS SMSK BANDWIDTH EFFICIENCY
- MAINTAIN QPSK BER vs E_b/N_0
- ACQUIRE BURSTS INDEPENDENTLY
- RAISE INFORMATION RATE TO 200 Mbps OR HIGHER
- COMBINE MODULATION AND CHANNEL SYMBOL ENCODING

BENEFITS:

- CAPACITY DOUBLE THAT OF EXISTING LINKS
- IDENTICAL OR REDUCED TRANSMITTER POWER
- OPERATION AT OR NEAR SATURATION
- REDUCED RISK AND COST

APPLICATIONS:

- PROCESSING SATELLITES:
  TDMA UPLINKS
  WIDEBAND CROSSLINKS
  MULTIPLE-BEAM TDM DOWNLINKS
- SATELLITE-SWITCHED TDMA:
  LOW-COST GROUND TERMINALS

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BANDWIDTH AND POWER EFFICIENT MODEM APPROACH

The four advanced modulation technology development (AMTD) contracts have addressed the implementation of bandwidth-efficient, combined modulation and coding techniques in high-data-rate, TDMA environments with varying degrees of success. All have selected some form of channel symbol encoding to overcome the effects of the bandlimited channels. Although each was required to implement independent burst acquisition, the satellite demodulators were designed to a more difficult adjacent-channel interference requirement. The power efficiency of the modem was a secondary constraint.

The University of California will bring an increased emphasis on power efficiency to this project element. The investigators intend to design modulation systems that are suitable for use with nonlinear high-power amplifiers and to implement and test a slow-speed version of the modems.

If program priorities permit, the Digital Systems Technology Branch intends to pursue a "follow-on" to the AMTD contracts. An openly competed demonstration model contract would address the packaging issues uncovered during the POC developments, while further increasing data rate and bandwidth and power efficiency in a design optimized for application in TDM downlinks. A statement of bidder qualifications will ensure that high-data-rate, bandwidth-efficient modem hardware comparable to the AMTD POC models has already been developed by potential contractors.

DIGITAL SYSTEMS TECHNOLOGY

BANDWIDTH- AND POWER-EFFICIENT MODEMS—APPROACH

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MULTIPLE PROOF-OF-CONCEPT MODEL CONTRACTS
"ADVANCED MODULATION TECHNOLOGY DEVELOPMENT" (AMTD)

- $\geq$ 2 bps/Hz; 200 Mbps; $\leq$ 500-ns ACQUISITION
- SATELLITE DEMODULATORS:
   FORD (NAS3-24678), RATE-5/6-CODED 8-PSK
   TRW (NAS3-24679), RATE-3/4-CODED 16-QAM
- GROUND TERMINAL DEMODULATORS:
   COMSAT (NAS3-24680) RATE-8/9-CODED 8-PSK
   HARRIS (NAS3-24681) RATE-1/2-CODED 16-CPFSK

GRANT—UNIVERSITY OF CALIFORNIA, DAVIS (NAG3-1007)
"MODULATION TECHNIQUES FOR POWER- AND SPECTRALLY EFFICIENT SATCOM SYSTEMS"

- SUPERPOSED QAM AND BANDLIMITED SQAM AND QPSK
- OPTIMIZED FOR NONLINEAR HIGH-POWER AMPLIFIERS
- 1.5 bps/Hz
- 64- TO 300-kbps ENGINEERING PROTOTYPE

DEMONSTRATION MODEL CONTRACT—TO BE DETERMINED
"AMTD FOLLOW-ON"

- ADVANCED PACKAGING FOR SIZE, MASS, AND POWER REDUCTIONS BY FACTOR OF 3 TO 5 EACH
- 25% IMPROVEMENT IN BANDWIDTH OR POWER EFFICIENCY OVER AMTD
- ANALOG/DIGITAL CHIP SET ON BOARD-LEVEL PRODUCT

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The curve shown below illustrates the primary goal of forward-error-correction (FEC) encoding - to reduce the received E_b/N_0 required to yield a specific probability of decoded bit error. Codecs that meet the combination of objectives shown below will provide an alternative to convolutional and block decoding approaches while preserving the best features of each. Such codecs will be well suited to onboard and ground-based processing of a variety of TDMA and FDMA signal formats in both dedicated and shared hardware applications.

DIGITAL SYSTEMS TECHNOLOGY
HIGH-SPEED CODECS

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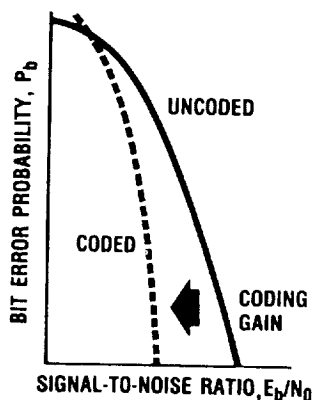
OBJECTIVES:

- RAISE UNCODED DATA RATES TO 300 Mbps
- ACHIEVE HIGH CODE RATES AND CODING GAIN
- SUPPORT SOFT DECISION DECODING AND MULTIPLE MODULATION SCHEMES
- OPERATE ON SHORT, INDEPENDENT BURSTS AND CONTINUOUS DATA
- IMPLEMENT CLSIC CHIP SETS

BENEFITS:

- REDUCED ANTENNA SIZE AND TRANS- MITTER POWER
- BANDWIDTH EXPANSION LIMITED BY EFFICIENT CODES
- SUITABLE FOR TDMA AND CONTINUOUS LINKS
- IMPROVED DATA QUALITY FOR GIVEN POWER

APPLICATIONS:

- PROCESSING SATELLITES:
  TDMA UPLINKS
  WIDEBAND CROSSLINKS
  SHARED DECODER AFTER BULK DEMODULATOR
  MULTIPLE-BEAM TDM DOWNLINKS
- SATELLITE-SWITCHED TDMA TERMINALS

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HIGH-SPEED CODEC APPROACH

The SBIR Phase 1 contract with Stanford Telecommunications, Inc. (STI) provided a design approach for increasing the throughput of convolutional decoders by interconnecting an array of commercially available decoders. When the contract was completed in late 1986, single-chip decoders with data rates to 10-Mbps were the state of the art. Although a Phase 2 contract was not awarded (STI was no longer a small business), their design defined a fundamental approach to high-speed decoding with high coding gain but low code rates.

Key features of the flexible, high-speed codec from Harris include its ability to utilize soft decision information, to independently decode short bursts or packets, and to yield high coding gain with high code rates. The hardware will be configurable for operation with multiple phase- and frequency-shift keying (PSK and FSK) modulation schemes. Under this demonstration model contract, Harris will implement two, independent, hard decision, 300-Mbps BCH codecs on each 50,000 gate CMOS gate array.

Under a recently awarded grant, the University of Southern California (USC) has begun investigating jointly designed decoders and equalizers to yield performance superior to that obtained from independent designs. USC will also investigate methods of exploiting soft decision information with RS decoding. In the future both techniques will be demonstrated in commercial digital signal processing hardware.

DIGITAL SYSTEMS TECHNOLOGY
HIGH-SPEED CODES—APPROACH

NASA
Lewis Research Center

SBIR PHASE 1 CONTRACT—STANFORD TELECOMMUNICATIONS, INC. (NAS3-24742)
"A NOVEL HIGH-SPEED VITERBI DECODER DESIGN WITH ROBUST ATTRIBUTES"

- MASSIVE PARALLEL BLOCK DECODING HARDWARE DESIGN
- ARRAY OF TWELVE 256-kbps TO 10-Mbps VITERBI DECODERS FOR 2- TO 100-Mbps THROUGHPUT

DEMONSTRATION MODEL CONTRACT—HARRIS (NAS3-25087)
"FLEXIBLE HIGH-SPEED CODEC"

- DUAL 300-Mbps BCH CODECS PER CLSIC FOR HARD DECISION
- CHASE ALGORITHM APPLIQUE FOR SOFT DECISION
- INDEPENDENT DECODING OF 256- TO 512-BIT BURSTS
- VARIABLE CODE RATES FROM 7/8 TO 15/16
- CODING GAIN > 5 dB TOTAL
- TWO 10-in. BY 10-in. BOARDS; 60-W TOTAL POWER

GRANT—UNIVERSITY OF SOUTHERN CALIFORNIA (NAG3-982)
"IMPLEMENTATION OF ADVANCED CODING CONCEPTS"

- CODESIGNED DECODER AND EQUALIZER
- REED-SOLOMON DECODING WITH FULL SOFT DECISION
- MOTOROLA DIGITAL SIGNAL PROCESSOR IMPLEMENTATION OF BOTH

CD–89–40925

DIGITAL MODEMS

Digitally implemented modems offer significant advantages over analog modems: potential for reduced size, mass, and power consumption in very large-scale integrated (VLSI) versions; elimination of alignment, drift, and aging problems; improved reliability; reconfigurability for data rates, modulation schemes, and operational modes; and reduced production costs. A programmable digital modem has the additional advantage of being remotely reconfigurable to increase the fault tolerance of processing satellites and to enable new services over the life of the satellite. For low-cost ground terminal applications the digital modem offers the potential for implementation as a custom chip set.

Because of its digital architecture much of the nonrecurring engineering effort expended in the initial design of a digital modem can be applied to a mission-focused version. The digital approach will also benefit directly from advances in high-performance, radiation-tolerant VLSI technology.

DIGITAL SYSTEMS TECHNOLOGY
DIGITAL MODEMS

NASA
Lewis Research Center

CONTROL — MODULATOR

m-PSK
MSK
QAM

DEMODULATOR
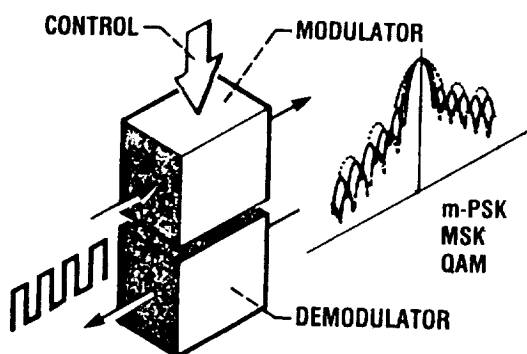
OBJECTIVES:

- MINIMIZE ANALOG COMPONENTS
- ACHIEVE RECONFIGURABLE OR PROGRAMMABLE
    INFORMATION BIT RATES
    MODULATION SCHEMES
    OPERATIONAL MODES
- IMPLEMENT IN DSP OR CLSIC

BENEFITS:

- SIGNIFICANTLY REDUCED COST AND RISK
- REDUCED SIZE, MASS, AND POWER OVER ANALOG
- ELIMINATION OF ALIGNMENT, DRIFT, AND AGING
- LONGER SERVICE LIFE DUE TO RELIABILITY AND RECONFIGURABILITY
- GREATER COMMERCIALIZATION POTENTIAL

APPLICATIONS:

- PROCESSING SATELLITES:
    UPLINKS
    CROSSLINKS
    SHARED DEMODULATOR AFTER
        MULTICHANNEL DEMULTIPLEXER
    MULTIPLE-BEAM DOWNLINKS
- COST-EFFICIENT GROUND TERMINALS

CD-89-40926

DIGITAL MODEM APPROACH

Under a Phase 1 SBIR contract TIW Systems Incorporated (formerly Multipoint Communications Corporation) outlined tradeoffs for nine critical digital modem design issues: (1) modulator data filtering; (2) clock generation; (3) carrier synthesizer; (4) demodulator automatic gain control; (5) data filtering; (6) radiofrequency oscillator phase noise; (7) carrier selectivity; (8) carrier recovery; and (9) timing recovery. For each issue Multipoint investigated multiple implementation techniques and provided specific recommendations on realizable circuit designs with special attention to utilizing digital signal processing (DSP).

The University of Toledo has also been investigating the implementation of digital QPSK burst modems. A digital demodulator design algorithm was implemented on a commercial Motorola DSP56001 evaluation board to identify limitations on information bit rate due to both the algorithm and the DSP hardware. Modifications to the software and hardware algorithms will be addressed in the parallel and pipelined version being designed to substantially increase the speed of a VLSI version.

NASA is currently negotiating a contract with COMSAT Laboratories for fabrication of a demonstration model, programmable digital modem (PDM) with the features shown below. The PDM will be programmable over six modulation schemes, the full range of data rates from 1.92 to 300 Mbps and three satellite operational modes. The proposed design offers excellent potential for a full custom VLSI chip set implementation.

DIGITAL SYSTEMS TECHNOLOGY
DIGITAL MODEMS—APPROACH

NASA
Lewis Research Center

SBIR PHASE 1 CONTRACT—MULTIPOINT (T.I.W. SYSTEMS) (NAS3-25336) "PROGRAMMABLE RATE MODEM USING DIGITAL SIGNAL PROCESSING TECHNOLOGY"

- BPSK AND QPSK BURST AND CONTINUOUS MODES
- ALL DIGITAL, COMMERCIAL DSP-BASED DESIGNS
- REALIZABLE CIRCUIT DESIGN TRADEOFFS ADDRESSED NINE MAJOR ISSUES

GRANT—UNIVERSITY OF TOLEDO (NAG3-865) "DIGITAL MODEM DEVELOPMENT"

- MOTOROLA DSP56001-BASED QPSK DEMODULATOR
- PARALLEL/PIPELINED VLSI TO INCREASE SPEED

DEMONSTRATION MODEL CONTRACT—(COMSAT, UNDER NEGOTIATION) "PROGRAMMABLE DIGITAL MODEM"

- QPSK, OPSK, 16-PSK, OQPSK, MSK, AND 16-QAM
- 1.92- TO 75-Msps (1.92- TO 300-Mbps) CHANNEL SYMBOL RATES
- CONTINUOUS, DEPENDENT, AND INDEPENDENT BURST MODES
- FULLY PROGRAMMABLE
- MULTIPLE USE OF ECL GATE ARRAY
- UNDER 150 in.^{2} AND 100 W TOTAL

CD–89–40927

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MULTICHANNEL DEMODULATORS

The multichannel demodulator has been identified in advanced architecture studies as an enabling technology for a cost-efficient network with FDMA on the uplinks, onboard processing and switching, and TDM downlinks. The goal of this project element is to demonstrate digital and optical techniques that can be extended to enable simultaneous demultiplexing and demodulation of hundreds to thousands of channels. In an operational system the channel mix may consist of several channel bandwidths and multiple modulation techniques.

DIGITAL SYSTEMS TECHNOLOGY
MULTICHANNEL DEMODULATORS

NASA
Lewis Research Center
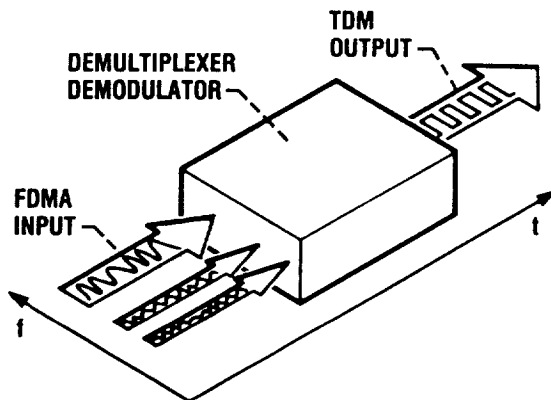
OBJECTIVES:

- ACHIEVE SIMULTANEOUS DEMULTI-PLEXING AND DEMODULATION OF HUNDREDS OF FDMA CHANNELS
- ACCOMMODATE MULTIPLE-CHANNEL BANDWIDTHS
- IMPLEMENT IN ADVANCED DIGITAL AND OPTICAL TECHNOLOGIES
- MINIMIZE GROUND SEGMENT IMPACT

BENEFITS:

- ENABLING TECHNOLOGY FOR FDMA NETWORK WITH ONBOARD PROCESSING
- REDUCED GROUND TERMINAL COSTS COMPARED WITH TDMA: LOWER EIRP AND SIMPLIFIED SYNCHRONIZATION

APPLICATIONS:

- PROCESSING AND SWITCHING SATELLITES WITH FDMA UPLINKS
- COST-EFFICIENT GROUND TERMINAL PROCESSING OF FDM DOWNLINKS

CD-89-40928

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MULTICHANNEL DEMODULATOR APPROACH

Because of the importance of the multichannel demodulator to the success of future missions, a multifaceted approach is being pursued. Since the study contract by COMSAT Laboratories (see page 11), the Digital Systems Technology Branch has awarded a grant and a Phase 1 SBIR contract to investigate viable digital and optical techniques for multichannel demultiplexing and demodulation. The University of Toledo is investigating FFT techniques, and Amerasia Technology, Incorporated is applying innovative transducers and a single reflective array compressor (RAC) approach to the problem.

NASA intends to award multiple contracts for the development of multichannel demultiplexer/demodulators. A demonstration with two channel bandwidths and a total of six channels is required for proof of the proposed concept and its implementation technique.

The branch has begun an in-house activity to augment the university and industry investigations and to better understand their approaches. The short-term objective is to implement a multichannel demodulator with 144-kbps information rate channels. The microcoded implementation of a high-performance FFT processor is being pursued for the long-term solution.

DIGITAL SYSTEMS TECHNOLOGY
MULTICHANNEL DEMODULATORS—APPROACH

NASA
Lewis Research Center

GRANT—UNIVERSITY OF TOLEDO (NAG3-799)
"FDMA/TDM CONVERSION FOR NONCONTIGUOUS CARRIERS"

- GWHT FOR LIGHTLY POPULATED SYSTEM
- PIPELINED VLSI ARCHITECTURE FOR FFT-BASED TRANSMULTIPLEXER

SBIR PHASE 1 CONTRACT—AMERASIA (NAS3-25617)
"INNOVATIVE PULSE COMPRESSORS FOR SATELLITE COMMUNICATIONS"

- SAW CHIRP FOURIER TRANSFORM TECHNIQUE
- HYPERBOLIC RAC TRANSDUCER FOR FSK DEMULTIPLEXING

MULTIPLE PROOF-OF-CONCEPT MODEL CONTRACTS—TO BE ANNOUNCED
"ADVANCED TECHNOLOGY FOR A MULTICHANNEL DEMULTIPLEXER/ DEMODULATOR"

- PROOF-OF-CONCEPT APPROACH EXTENDABLE TO SYSTEM WITH HUNDREDS OF CHANNELS
- FOUR NARROWBAND, TWO WIDEBAND CHANNELS
- DIGITAL AND/OR OPTICAL SOLUTIONS

LEWIS IN-HOUSE
"DIGITAL SIGNAL PROCESSING FOR MULTICHANNEL DEMODULATION"

- MOTOROLA DSP56000-BASED DEMULTIPLEXER/DEMODULATOR
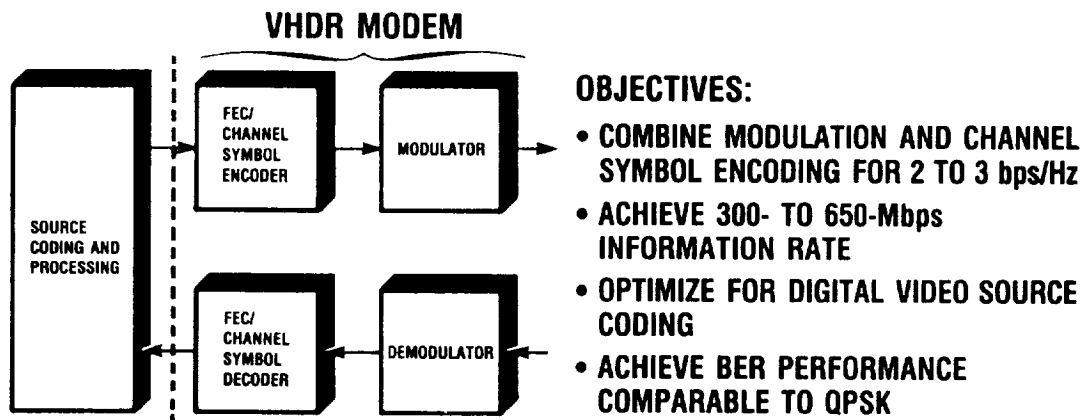- SYSTOLIC ARRAY FFT PROCESSOR

CD-89-40929

VERY HIGH-DATA-RATE MODEMS

For real-time transmission of very high information rate signals (from 300 to 650 Mbps), modems with 2 to 3-bps/Hz bandwidth efficiency are required for transmitting the signals via existing and planned satellite links. Both FEC and channel symbol coding must be employed in a very high-data-rate (VHDR) modem to ensure a specific BER performance level under specific constraints imposed by the link budget.

In applications where the information present in the source signal can be compressed into a lower data rate signal, as in most digital video applications, tradeoffs among source coding, FEC coding, and channel symbol coding must be addressed in order to maximize the quality of the transmission and minimize the hardware complexity. It is anticipated that such a real-time transmission capability can enable "telescience" - ground-based control of space experiments.

The Digital Systems Technology Branch plans to discuss potential applications of the VHDR modem technology within NASA in order to establish a priority for its development. The branch will pursue its development if sufficient rationale and interest exist.

DIGITAL SYSTEMS TECHNOLOGY
VERY HIGH-DATA-RATE MODEMS

NASA
Lewis Research Center

VHDR MODEM

SOURCE CODING AND PROCESSING

FEC/ CHANNEL SYMBOL ENCODER → MODULATOR →

FEC/ CHANNEL SYMBOL DECODER ← DEMODULATOR ←

OBJECTIVES:

- **COMBINE MODULATION AND CHANNEL SYMBOL ENCODING FOR 2 TO 3 bps/Hz**
- **ACHIEVE 300- TO 650-Mbps INFORMATION RATE**
- **OPTIMIZE FOR DIGITAL VIDEO SOURCE CODING**
- **ACHIEVE BER PERFORMANCE COMPARABLE TO QPSK**

BENEFITS:

- **CAPACITY DOUBLE THAT OF EXISTING WIDEBAND LINKS**
- **REAL-TIME TRANSMISSION OF VERY HIGH INFORMATION RATES**

APPLICATIONS:

- **WIDEBAND CROSSLINKS AND DOWN-LINKS FOR PROCESSING SATELLITES**
- **HIGH-RESOLUTION, HIGH-FRAME-RATE VIDEO TRANSMISSION (HHVT) AND TELESCIENCE**

CD-89-40930

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Depending on program priorities a potential development approach would include a university grant and a demonstration model contract. The university would address modem design issues for "broadcast quality" transmission of moderate-information-rate digitized video such as the existing National Television Standards Committee (NTSC) and emerging high-definition television (HDTV) signals. A contractor would develop advanced bandwidth efficient modulation and coding techniques and VHDR modem hardware to demonstrate real-time transmission of very high-data-rate signals such as the high-resolution, high-frame-rate video technology (HHVT) signal format envisioned for microgravity science experiments.

DIGITAL SYSTEMS TECHNOLOGY
VERY HIGH-DATA-RATE MODEMS—APPROACH

NASA
Lewis Research Center

GRANT—TO BE DETERMINED
"MODEMS FOR COMPRESSED VIDEO TRANSMISSION"

- 2- TO 3-bps/Hz BANDWIDTH EFFICIENCY
- OPTIMIZED FOR COMPRESSED NTSC AND HDTV SIGNAL FORMATS

DEMONSTRATION MODEL CONTRACT—TO BE DETERMINED
## "VERY HIGH-DATA-RATE MODEM"

- 650-Mbps INFORMATION RATE
- NEARLY 3-bps/Hz BANDWIDTH EFFICIENCY
- RAPID SIGNAL ACQUISITION
- OPTIMIZED FOR HHVT SIGNAL FORMAT
- SUITABLE FOR DEMONSTRATION VIA ACTS HBR

CD-89-40931

POC AND DEMONSTRATION MODEL EVALUATION

A multiple-ground-terminal satellite network simulation facility has been developed under the Space Electronics Division's System Integration, Test, and Evaluation (SITE) Project. The facility integrates POC model modems, low-noise receivers, intermediate frequency matrix switches, and traveling-wave tube amplifiers with in-house-developed rain fade and range delay hardware simulators and TDMA ground terminal digital subsystems. The SITE facility has been used to characterize the performance of a variety of microwave components. In addition to repeating the acceptance testing performed by the contractors, the Digital Systems Technology Branch intends to incorporate the hardware models developed under the Advanced Modulation and Coding Project into the SITE facility for further testing and evaluation.

SITE MULTI TERMINAL NETWORK SIMULATION

GROUND TERMINAL DIGITAL

TWO CHANNEL TRANSPONDER
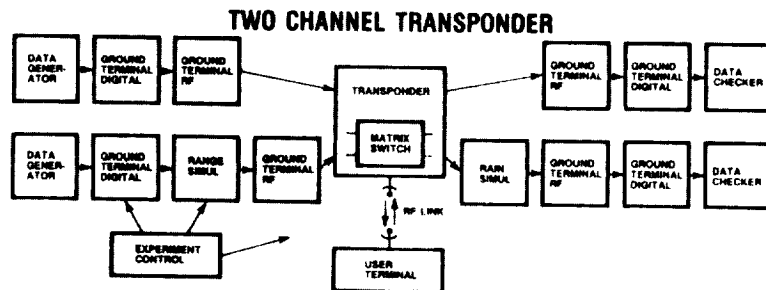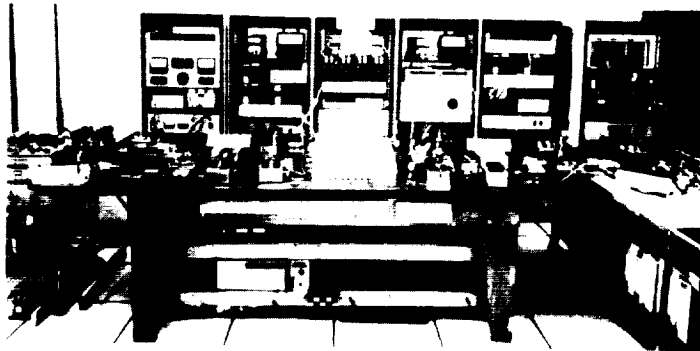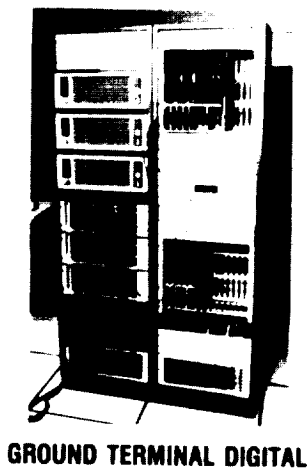
CD-88-34583

FEATURES

- TWO CHANNEL OPERATION
- DYNAMIC SWITCHING
- SIMULATED RANGE DELAY
- SIMULATED RAIN FADE
- NETWORK CONTROL
- BURSTED DATA (220 Mb/s)
- REMOTE RF LINK (SETS)
- EXPERIMENT CONTROL

SESSION II

LEWIS BANDWIDTH EFFICIENT MODULATION —ADVANCED MODULATION TECHNOLOGY DEVELOPMENT (AMTD) CHAIR: M.J. SHALKHAUSER

8-PSK CODED TDMA SATELLITE DEMODULATOR
S.A. AMES
FORD AEROSPACE CORPORATION

RATE 3/4 CODED 16-QAM FOR UPLINK APPLICATIONS
E.M. MROZEK AND J.K.N. WONG
TRW, INCORPORATED

AN 8-PSK TDMA UPLINK MODULATION AND CODING SYSTEM
S.A. AMES
FORD AEROSPACE CORPORATION

RATE 8/9 CODED 8-PSK SYSTEM FOR DOWNLINK APPLICATIONS
R. FANG, M. KAPPES, AND S. MILLER
COMSAT LABORATORIES

CODED 16-CPFSK FOR DOWNLINK APPLICATIONS
R. DAVIS
HARRIS CORPORATION

I