N92-22003

8-PSK CODED TDMA SATELLITE DEMODULATOR

S.A. Ames
Ford Aerospace Corporation
Space Systems Division
Palo Alto, California 94303

FINAL BRIEFING

ADVANCED TECHNOLOGY SATELLITE DEMODULATOR DEVELOPMENT

NAS3-24678

PRESENTED AT

NASA LEWIS RESEARCH CENTER

JUNE 8, 1989

ABBREVIATIONS USED IN BRIEFING

• ACI	adjacent channel interference
• AMTD	Advanced Modulation Technology Development
• ASIC	application specific integrated circuit
• AWGN	additive white Gaussian noise
• BER	bit error rate
• CCI	co-channel interference
• codec	coder/decoder
• ECL	emitter coupled logic
• MCD	multi-channel demultiplexer and demodulator
• MMIC	monolithic microwave integrated circuit
• modem	modulator/demodulator
• SAW	surface acoustic wave
• TDMA	time division multiple access

EXECUTIVE SUMMARY

- OBJECTIVES
- REQUIREMENTS
- PHASES
- COSTS AND DURATION
- PROOF-OF-CONCEPT MODEL BLOCK DIAGRAM
- PROOF-OF-CONCEPT MODEL PHYSICAL CONFIG.
- PERFORMANCE OF POC MODEL
- CONCLUSIONS OF PROGRAM
- RECOMMENDATIONS FOR FUTURE

OBJECTIVES:

- Develop a proof-of-concept uplink modulation system which will significantly increase the bandwidth efficiency of a TDMA uplink system
- Maintain present performance levels
- POC model should exhibit potential for low weight and power consumption

SALIENT REQUIREMENTS FROM RFP:

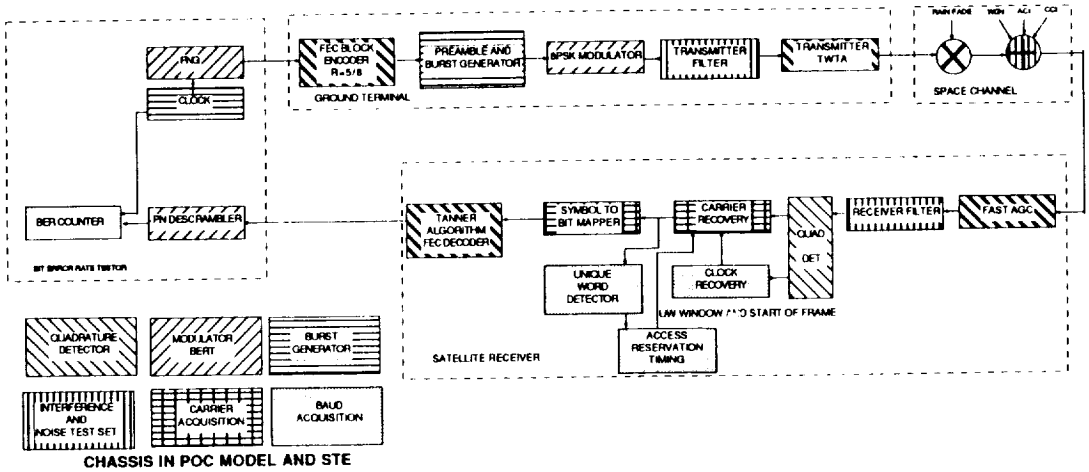
- Bandwidth Efficiency > 2 bits/ sec/ Hz
- Implementation loss < 2 dB
- 1 dB degradation in 20 db ACI or CCI
- TDMA burst mode with preamble < 100 bit periods
- Throughput > 200 Mbps

DERIVED REQUIREMENTS:

- 8PSK modulation
- Nyquist filter with rolloff factor of 0.2
- CCI spec requires forward error correction coding
- Mostly digital mechanization for eventual ASIC design

PHASES:

- Refine preliminary design
- Develop preliminary design
- Build and test breadboard
- Plan, specify, and fab POC model
- Test POC model and establish POC
- Product assurance



BLOCK DIAGRAM OF GROUND AND SATELLITE TDMA TEST SYSTEM

CONCLUSIONS OF PROGRAM

- CONCEPT OF THE POWER AND BANDWIDTH EFFICIENT SATELLITE DEMODULATOR HAS BEEN PROVEN WITHIN THE BUDGETARY CONSTRAINTS OF THE PROGRAM
- BANDWIDTH EFFICIENCY COULD BE DEMONSTRATED (I.E., ACI SPEC MET) THROUGH FILTER IMPROVEMENTS
- POWER EFFICIENCY COULD BE DEMONSTRATED (I.E., BER SPEC MET IN AWGN) THROUGH IMPROVEMENTS IN CLOCK RECOVERY LOOP AND FILTERS
- DIGITAL PORTION OF THE SATELLITE DEMODULATOR COULD BE REALIZED IN TWO GATE ARRAYS PLUS SOME MEMORY CHIPS, ANALOG PORTION COULD BE GREATLY REDUCED IN SIZE AND WEIGHT BY UTILIZING SAW FILTERS AND AN MMIC QUADRATURE DETECTOR
- CODEC PERFORMANCE WITH DEMOD IN CCI PROVEN BY SIMULATION

RECOMMENDATIONS FOR FUTURE

- CONTINUE SATELLITE MODEM DEVELOPMENT IN COMPACT FORM

  (A) ASIC REALIZATION OF DIGITAL PORTION (TWO ECL GATE ARRAYS)

  (B) DEVELOPMENT OF STEEP SKIRTED NYQUIST FILTERS IN SAW TECHNOLOGY AT ABOUT 300 MHz

  (C) MMIC OR HYBRID QUADRATURE DETECTOR AND LO

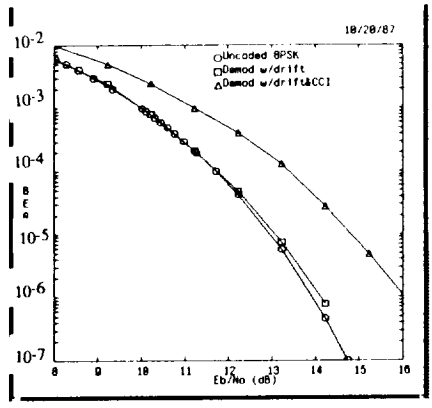
- CONTINUE DEVELOPMENT OF SATELLITE CODEC IN ASIC

- CONTINUE DEVELOPMENT OF LOW BIT RATE MCD IN ASIC AND/OR DSP

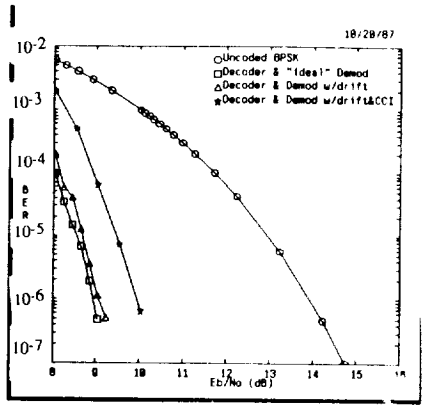
SPECIFICATIONS OF POC MODEL

PARAMETER	VALUE	TEST SPEC NO. OR METHOD OF DETERMINING COMPLIANCE
Bandwidth Efficiency	> 2 Bits/sec/Hz	1
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.373056 GHz±1.5KHz	by design
Input level at receiver filter	-30 dBm±0.5 dB	by design
BER at Es/No=21 dB	$< 5 \times 10^{-7}$	2
Degradation Due to +20 dB ACI	< 1 dB	3
Degradation Due to -20 dB CCI	< 1 dB	3
Probabiltiy of bit error due to missing unique word	$< 1 \times 10^{-7}$ at Es/No =13 dB	by computation (4)
Probability of Carrier Cycle Slip	< TBD at Es/No= TBD dB	5
Bit-timing Jitter	< 125 ps RMS	6
Probability of Clock Cycle Slip	< TBD at Es/No=TBD dB	7
Minimum Guard Time Between Bursts		25 ns by design of STE

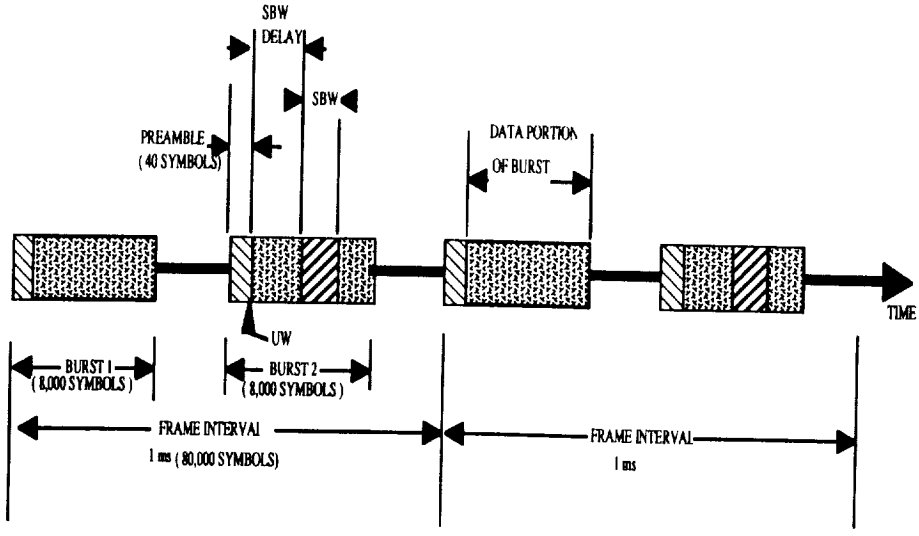
SIMULATIONS OF DEMOD PERFORMANCE WITH DRIFT AND CCI

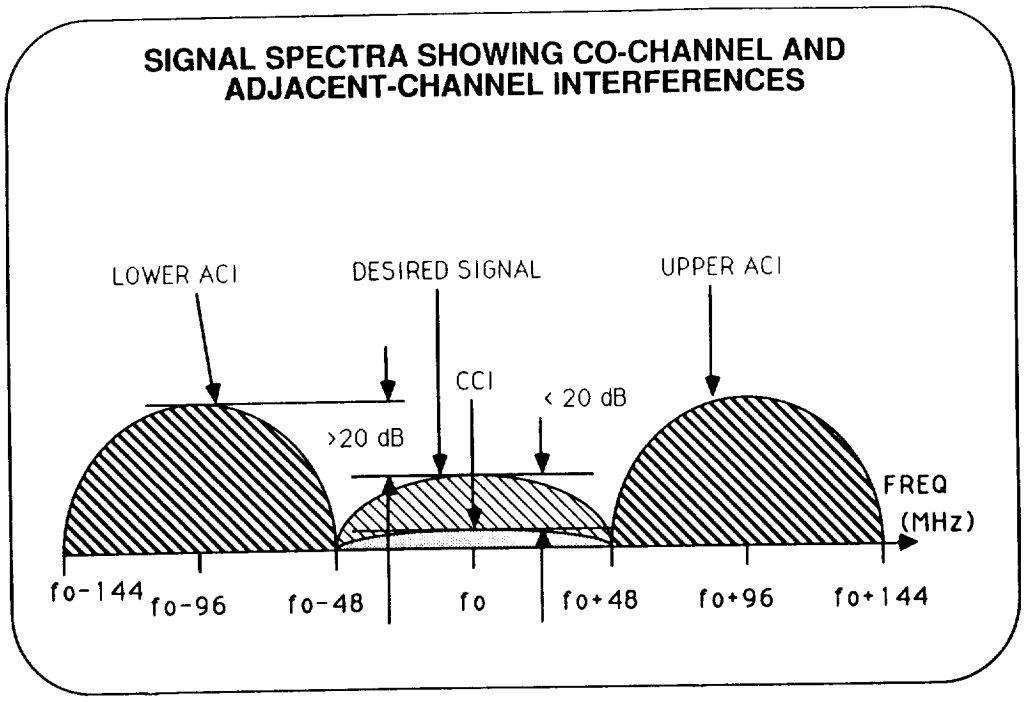


SIMULATIONS OF DEMOD AND DECODER PERFORMANCE WITH DRIFT AND CCI



PREAMBLE AND BURST STRUCTURE





AMTD INTERFERENCE AND NOISE TEST SET CHASSIS

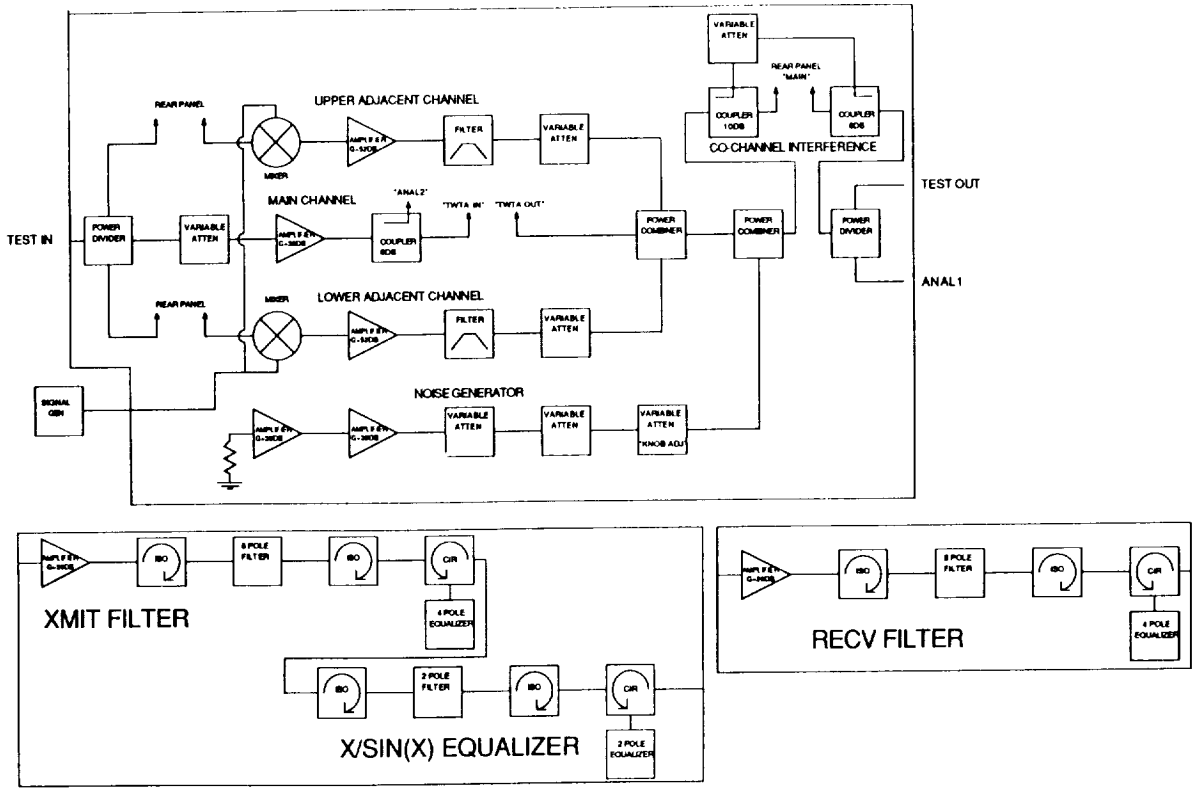
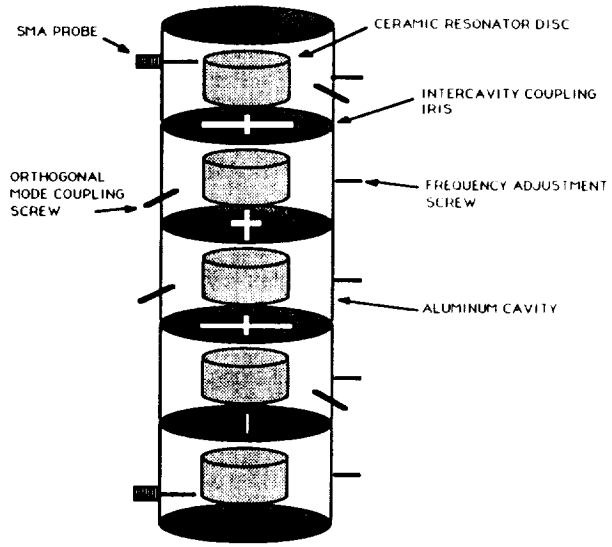
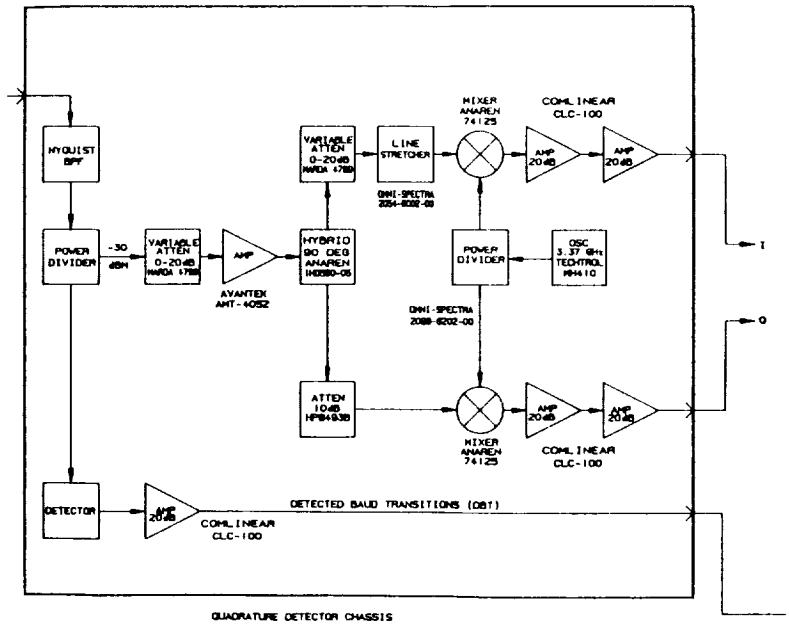


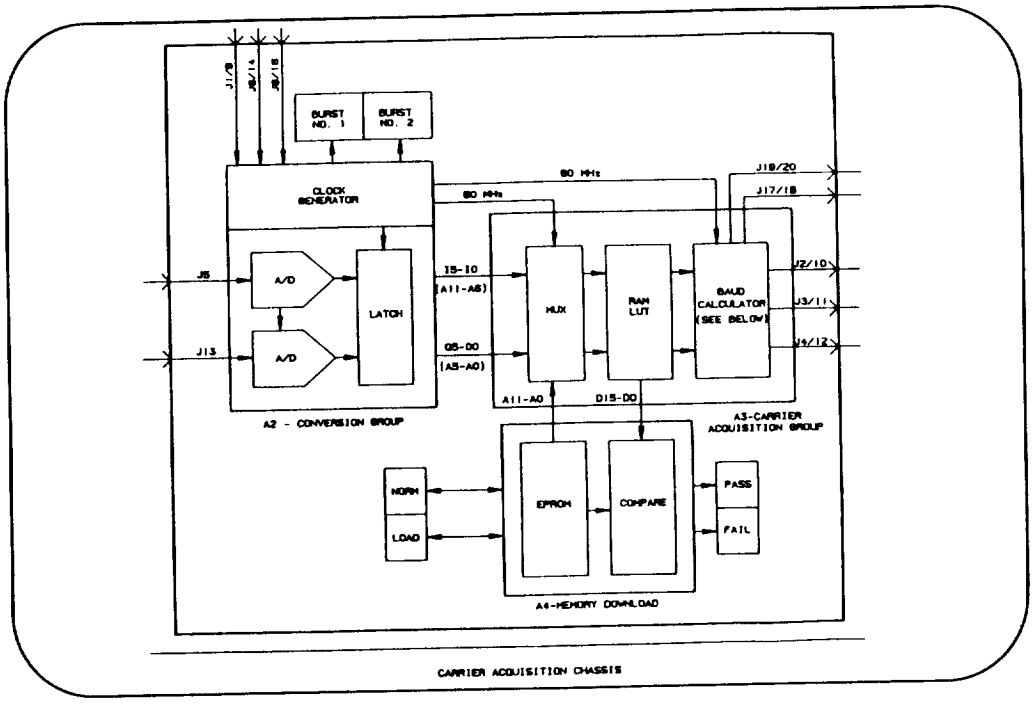
Figure 1 Interference/Noise Generator Block Diagram

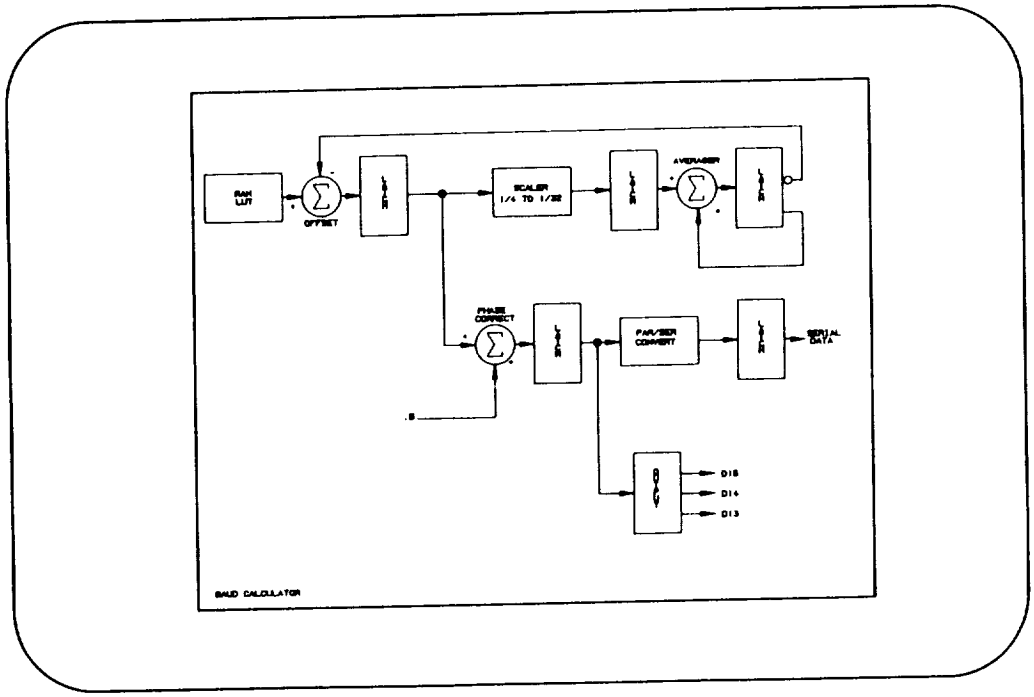
MECHANICAL CONFIGURATION OF NYQUIST FILTERS

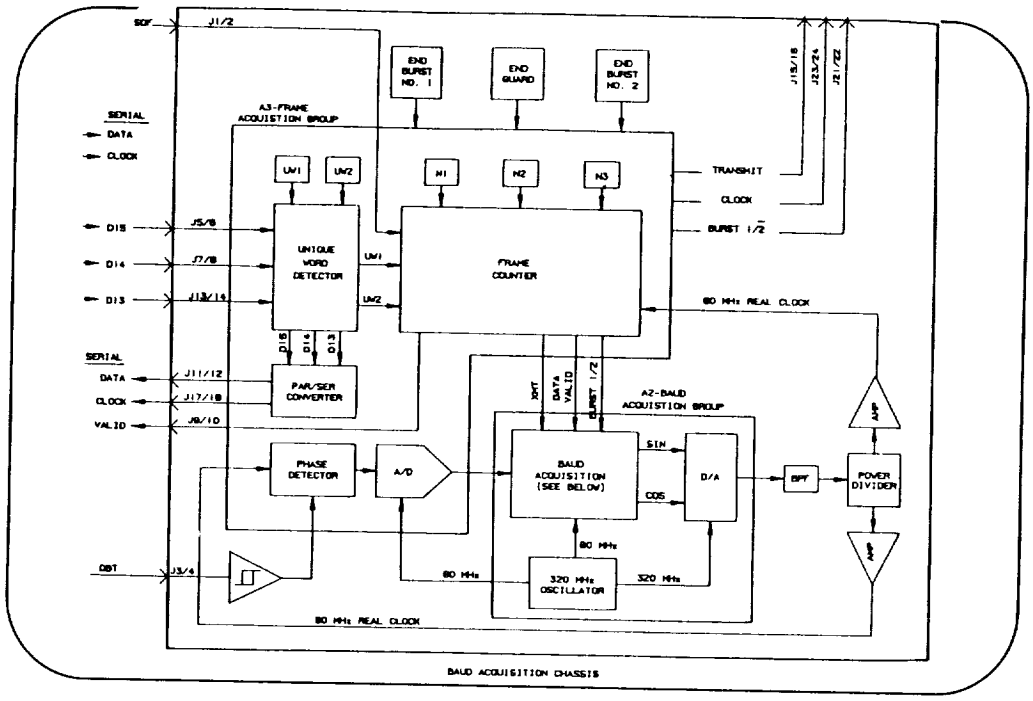
9 Pole Dielectric Resonator Filter

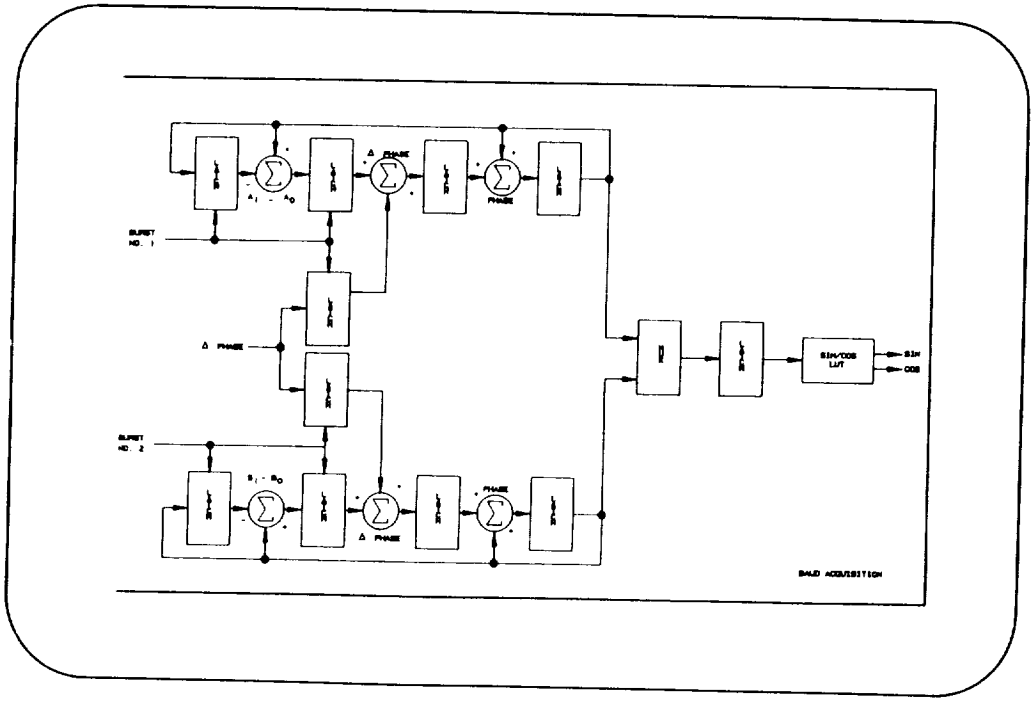




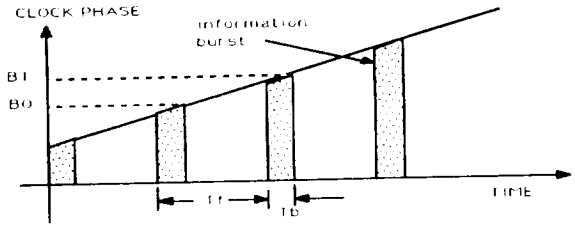

BURST NO. 1
BURST NO. 2
CLOCK GENERATOR
80 MHz
80 MHz
J19/20
J17/18
J5
J13
A/D
A/D
LATCH
15-10 (A11-A6)
09-00 (A5-A0)
MUX
RAM LUT
BAUD CALCULATOR (SEE BELOW)
J2/10
J3/11
J4/12
A11-A0
D15-D0
A2 - CONVERSION GROUP
A3-CARRIER ACQUISITION GROUP
NORM
LOAD
EPROM
COMPARE
PASS
FAIL
A4-MEMORY DOWNLOAD
CARRIER ACQUISITION CHASSIS


RAM LUT
OFFSET
SCALER 1/4 TO 1/32
AVERAGER
FINE CORRECT
PAR/SER CONVERT
SERIAL DATA
.8
D15
D14
D13
BAUD CALCULATOR


SOF
J1/2
END BURST NO. 1
END GUARD
END BURST NO. 2
J15/16
J23/24
J21/22
SERIAL
DATA
CLOCK
A3-FRAME ACQUISITION GROUP
UW1
UW2
H1
H2
H3
TRANSMIT
CLOCK
BURST 1/2
D15
D14
D13
J5/6
J7/8
J13/14
UNIQUE WORD DETECTOR
FRAME COUNTER
80 MHz REAL CLOCK
SERIAL
DATA
CLOCK
VALID
J11/12
J17/18
J9/10
PAR/SER CONVERTER
DVT
DATA VALID
BURST 1/2
A2-BAUD ACQUISITION GROUP
AMP
PHASE DETECTOR
A/D
BAUD ACQUISITION (SEE BELOW)
SIN
COS
D/A
BPF
POWER DIVIDER
AMP
OBT
J3/4
80 MHz
320 MHz OSCILLATOR
320 MHz
80 MHz REAL CLOCK
BAUD ACQUISITION CHASSIS

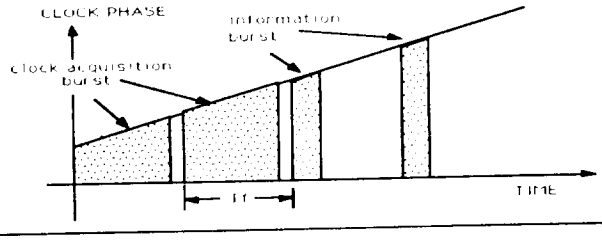

Δ PHASE
PHASE
BURST NO. 1
Δ PHASE
BURST NO. 2
PHASE
Δ PHASE
SIN/COS LUT
SIN
COS
BAUD ACQUISITION

SYMBOL CLOCK ACQUISITION

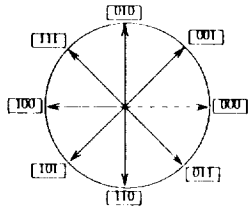


phase slope= (B1-B0)/Tf

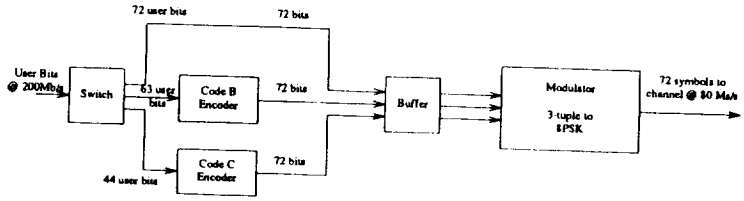
phase correction=phase slope•(Tf-TB)+(B1-B0)•(Tf-TB)/Tf



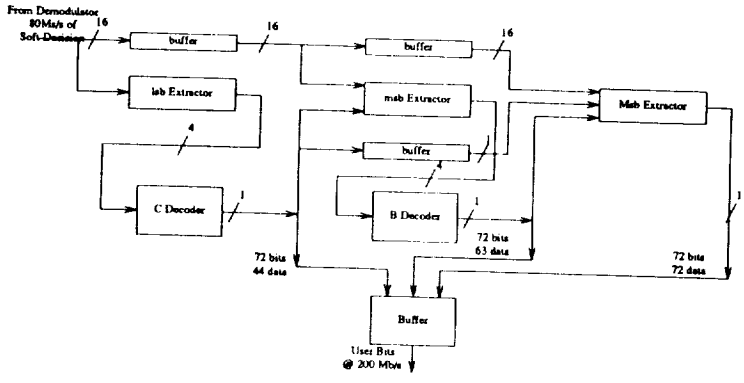
SIGNIFICANT BIT 8PSK TO 3-TUPLE MAPPING



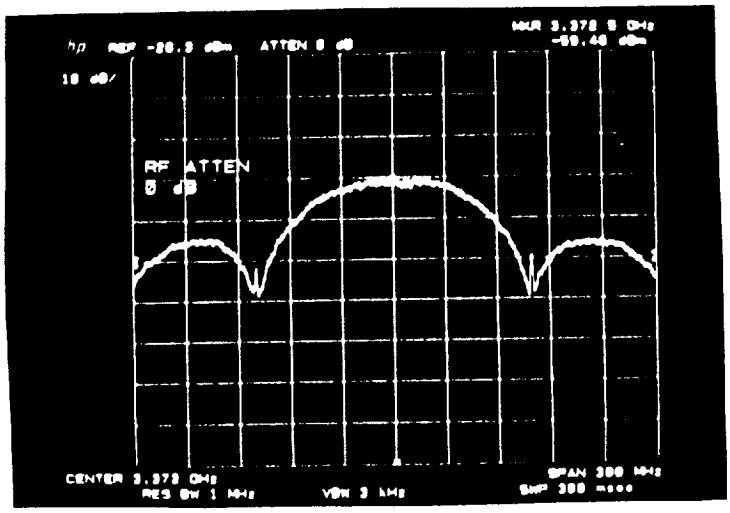
ENCODER SYSTEM



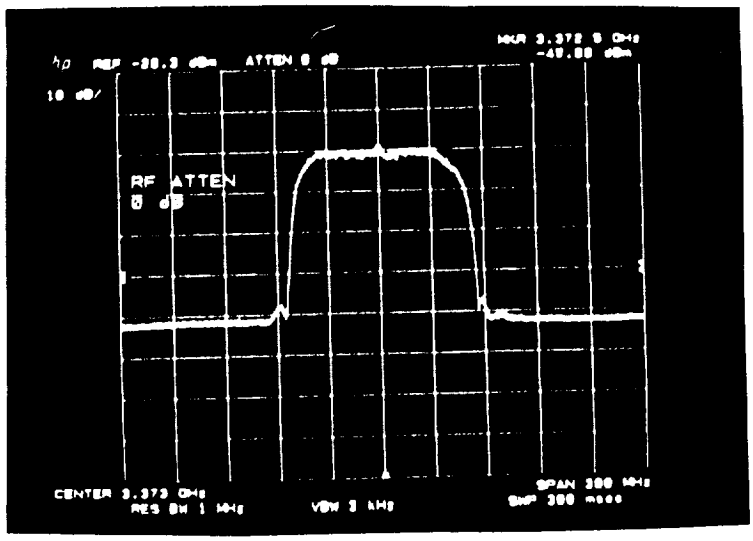
DECODER SYSTEM



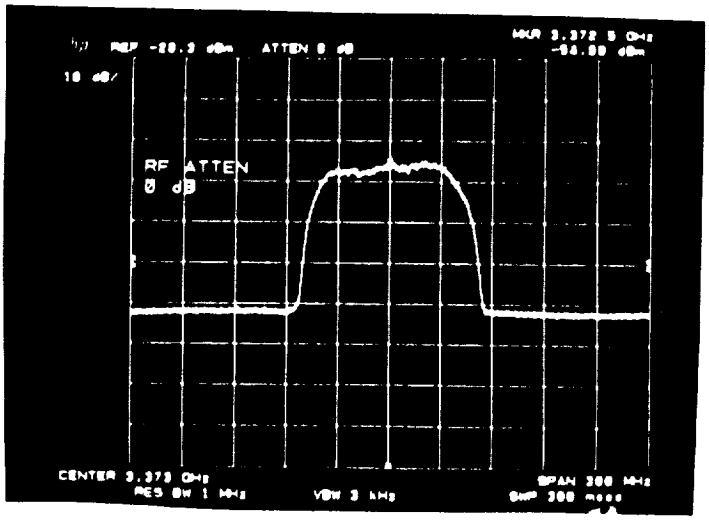
MODULATOR OUTPUT SPECTRUM



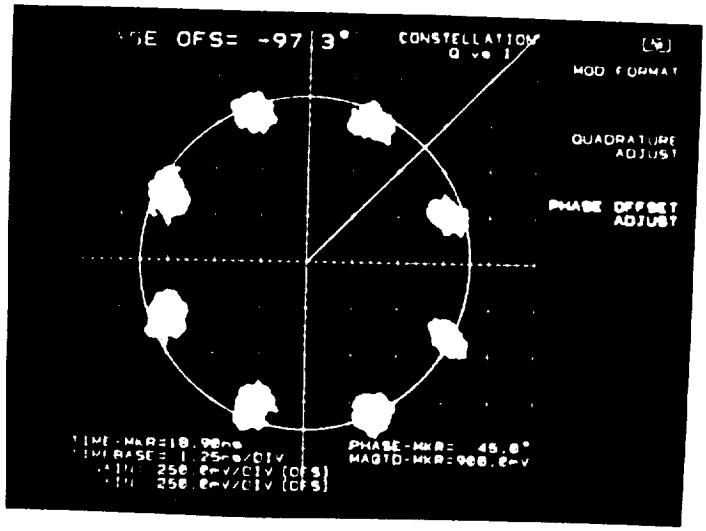
TRANSMITTER FILTER OUTPUT SPECTRUM



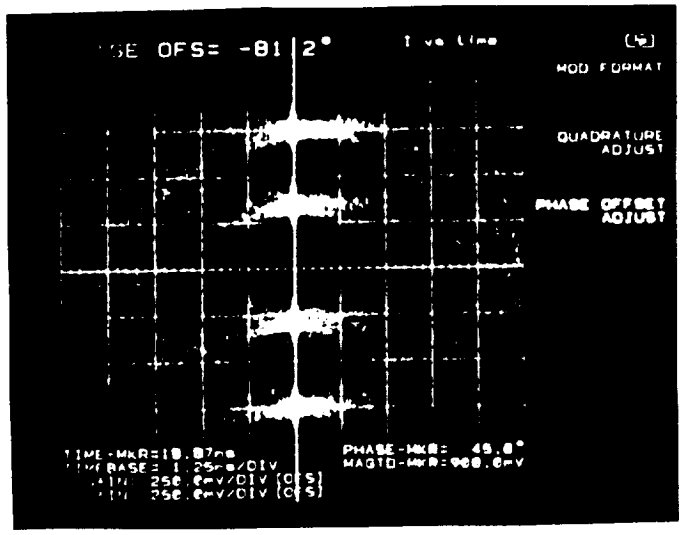
RECEIVER FILTER OUTPUT SPECTRUM



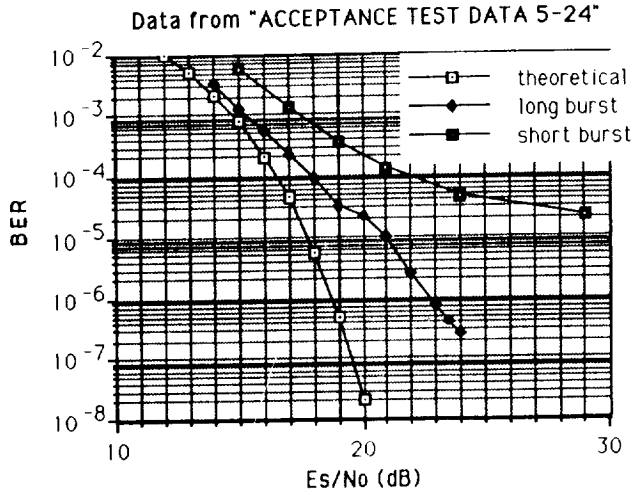
CONSTELLATION OUTPUT AT RECEIVER QUADRATURE DETECTOR



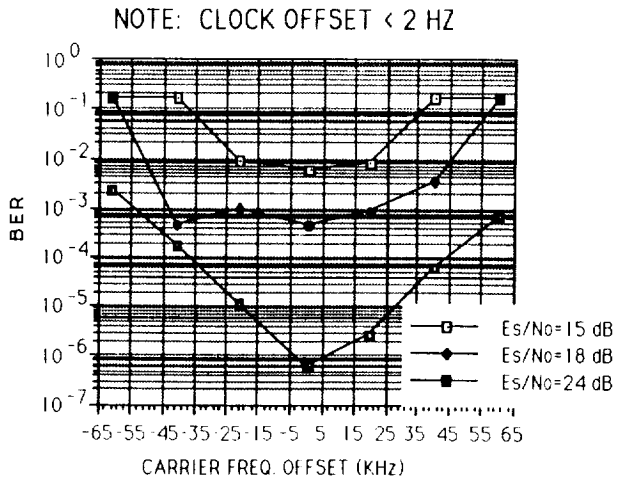
EYE PATTERN AT "I" SIDE OF QUADRATURE DETECTOR



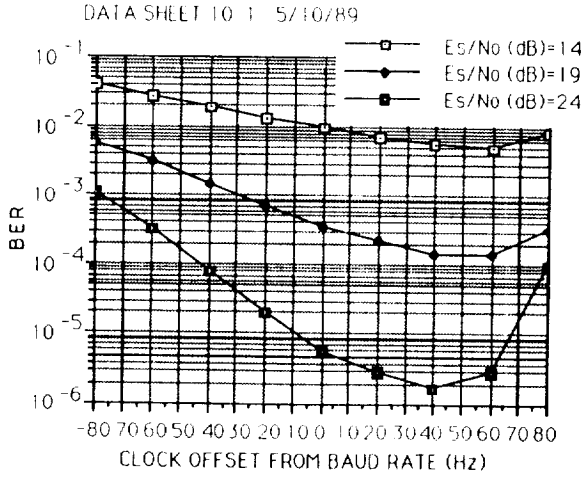
BIT ERROR RATE VERSUS Es/No IN AWGN FOR LONG AND SHORT BURSTS



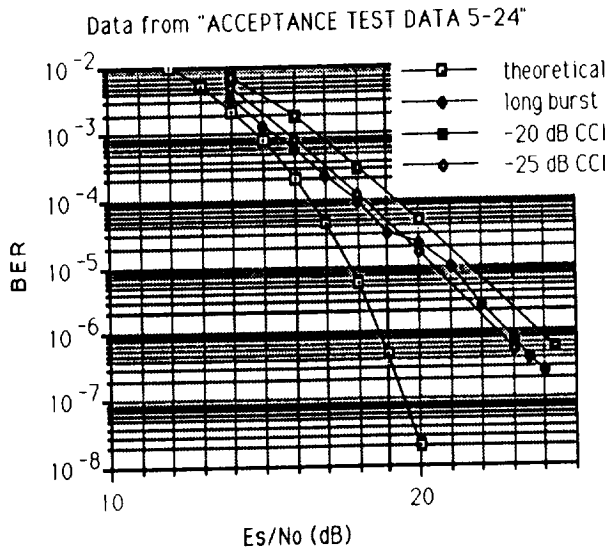
BER VERSUS CARRIER FREQUENCY OFFSET



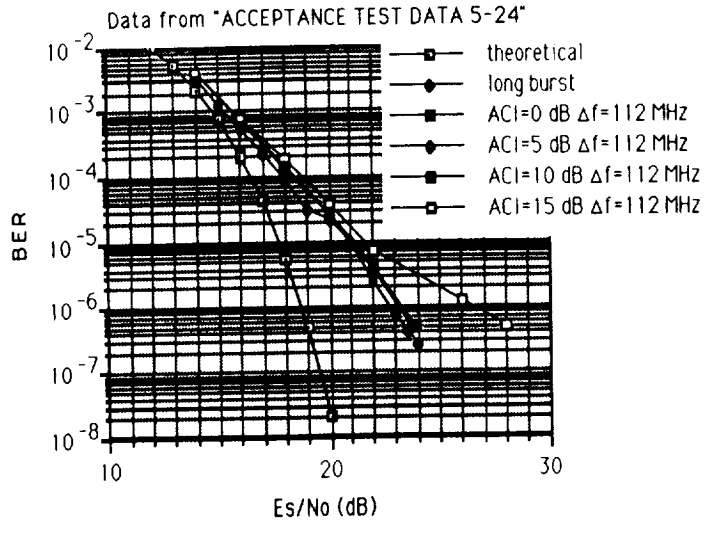
BER VERSUS CLOCK OFFSET FREQUENCY



BER VERSUS ES/NO IN CCI



BER VERSUS Es/No IN ACI FOR 112 MHz SPACING



INPUT SPECTRUM TO RECEIVER WITH +20 dB ACI AT ±112 MHz