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HIGH SPEED HARDWARE DEVELOPMENT FOR FDMA/TDM SYSTEM

S. C. Kwatra, M. M. Jamali
Department of Electrical Engineering
The University of Toledo
Toledo, Ohio 43606

Abstract

In satellite communications systems incorporating small earth stations, the application of multiple-access techniques of single channel per carrier/frequency division multiple access (SCPC/FDMA) in the uplink, on-board switching and time division multiplexing (TDM) in the downlink is significantly effective in improving satellite transponder utilization and reducing the required effective isotropic radiated power (EIRP) in both the earth stations and the satellite. A conceptual block diagram of the multicarrier demodulator is shown in Figure 1.

For FDMA/TDM conversion, the uniformly spaced FDMA channels have to be separated which can be accomplished with a transmultiplexor. After separating these channels, they are demodulated using a QPSK demodulator. The transmultiplexor is implemented with the aid of a commutator, bank of polyphase filters and discrete Fourier transform (DFT) implemented via FFT.

Development and advances in the area of VLSI and digital systems can be exploited for the development of a transmultiplexor and QPSK demodulator. Goals for designing the architecture for the transmultiplexor and QPSK demodulator are that the system should meet real time signal processing requirements of the future satellite systems and should consume very small amount of power. In this work we design the architecture of this transmultiplexor and the demodulator by pipelining all the modules namely commutator, filter bank FFT and the internal modules of the QPSK. The architecture is designed for the case of 800 channels each having a bandwidth of 45 KHz and a bit rate of 64 Kb/s. In this case each module will have (1/45 KHz=22.22 micro seconds) 22.22 micro seconds to complete computation.

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A uniform channel filter bank consists of a polyphase filter bank, phase shifter, DFT block and multiplication by a constant. This uniform filter bank is shown in Figure 2. The polyphase filter bank will require 800 9 tap FIR filters and a 1024 point FFT operation.

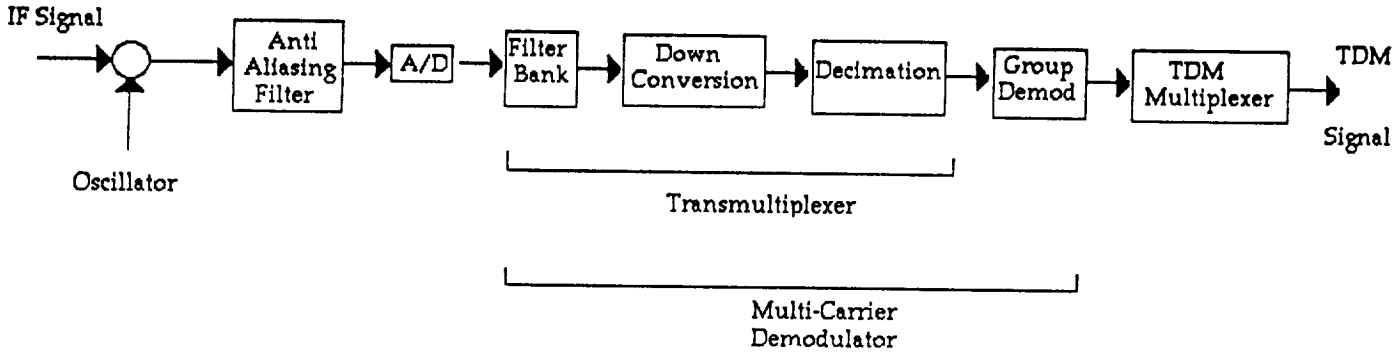


Figure : 1 SYSTEM FOR FDMA/TDM CONEVRSION

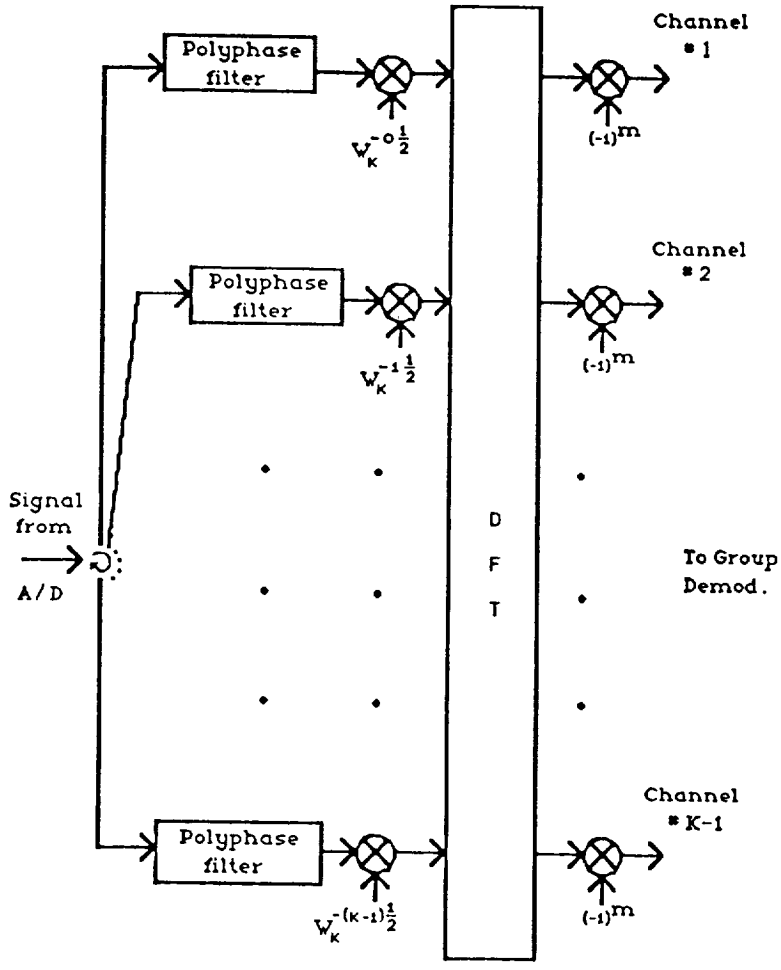


Figure 2: Uniform Channel Filter Bank

Filter banks can be implemented using 800 different 9 tap FIR filters. The amount of required hardware will be prohibitive for our application because of size and power requirements. A multiplexed 9 tap FIR filter architecture has been designed which will meet the speed requirements. This structure utilizes RAM's to store data and tree structure for multiplication and add operations as shown in Figure 3.

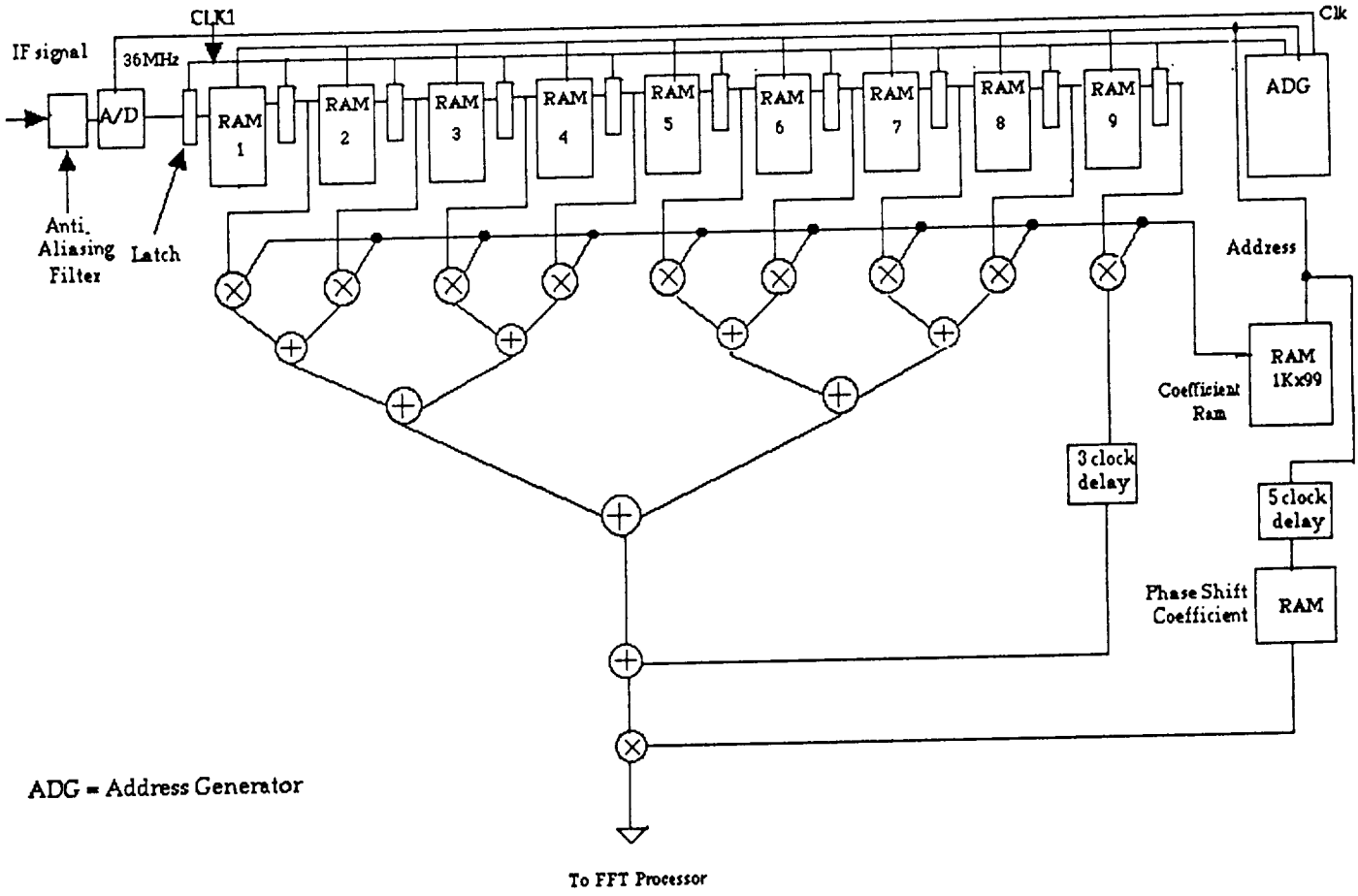


Figure 3: Shared Filter Architecture

In order to meet the speed requirements of this system, a pipelined FFT structure has been designed. This structure has 10 stages with dual memories in between the stages. It is capable of performing 1024 point complex FFT in 22.22 micro seconds which is the pipeline speed of this system. The structure is shown in Figure 4.

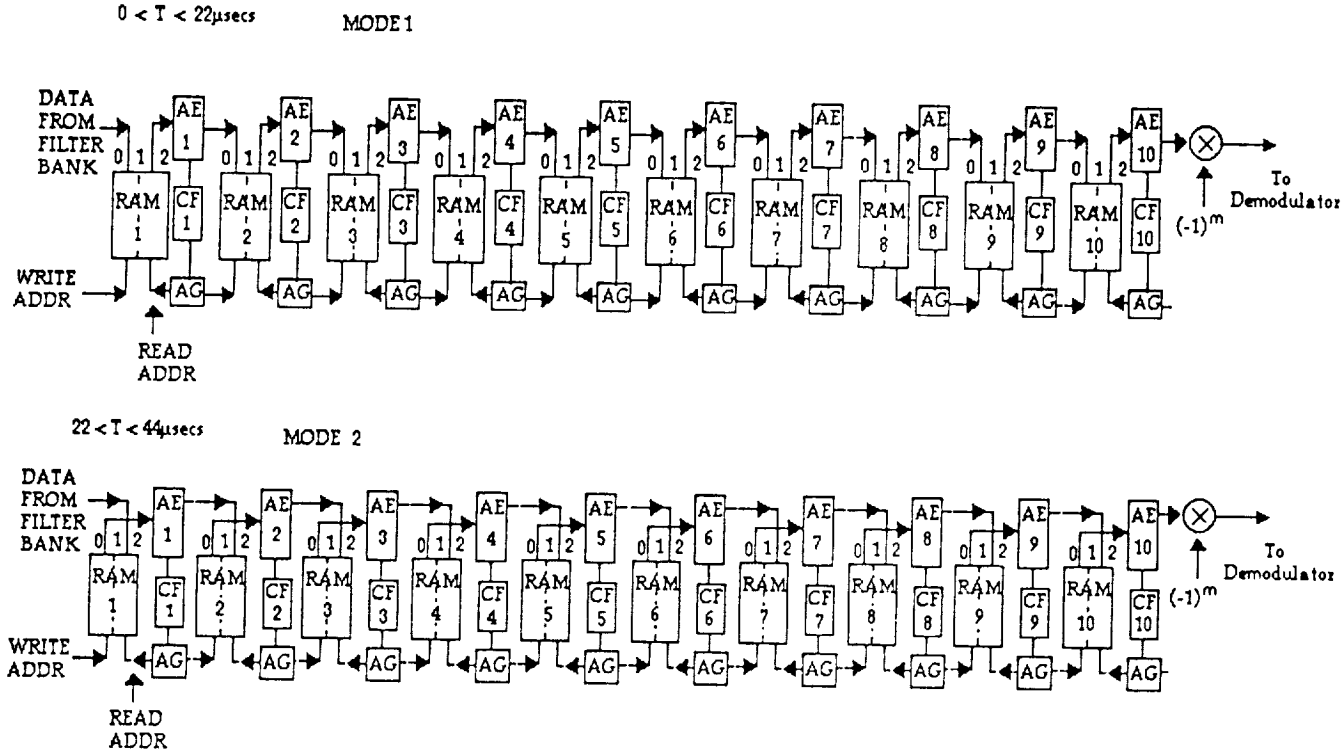


Figure 4: FFT Pipeline Processor

A FFT multiplexed butterfly arithemetic element has also been designed and is shown in Figure 5. The data flow through this arithmetic element moves according to specified pipeline speed. This element also performs parallel arithmetic operations.

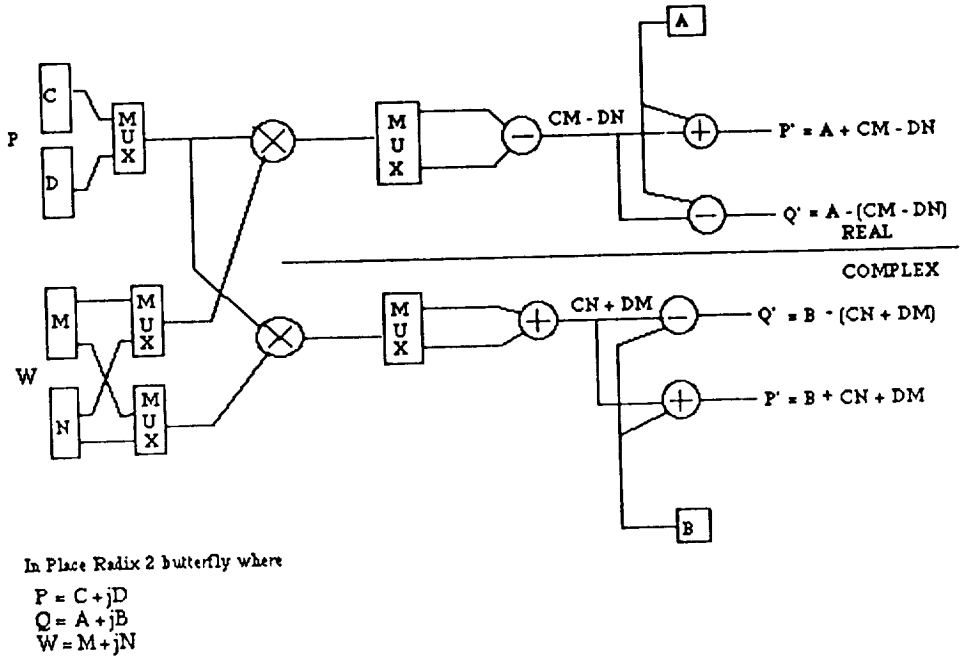


Figure 5: FFT Muxed Butterfly Arithmetic Element (MAE)

A TDMA frame consists of guard bits, preamble, unique word and data bits. The demodulator has to process the preamble, unique word and data bits to recover the message. A block diagram of a QPSK demodulator is shown in Figure 6.

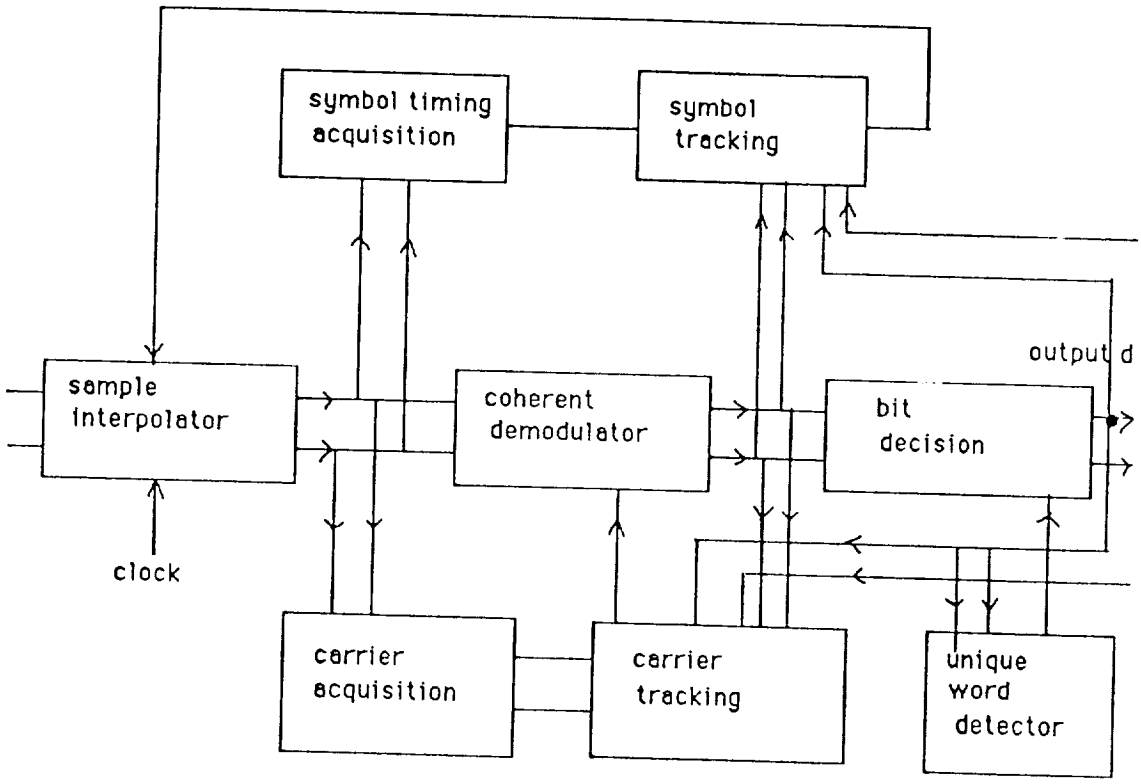
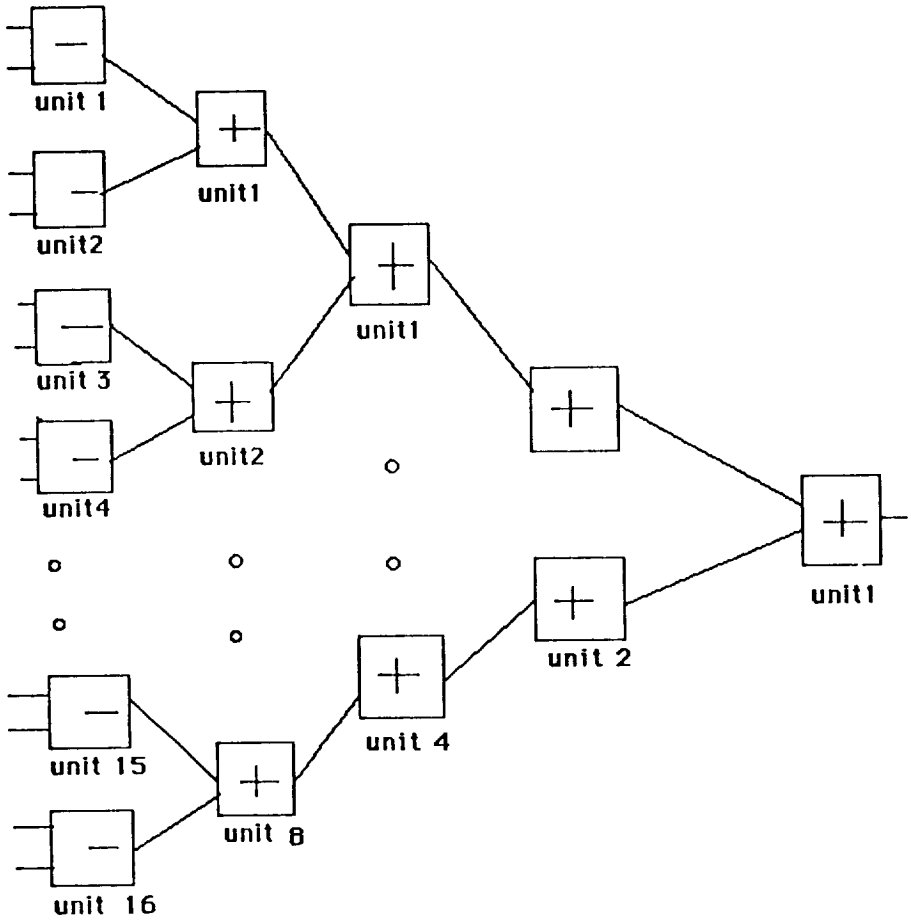


Figure 6: QPSK Demodulator

Preamble processing involves the carrier acquisition and timing acquisition modules. A tree structure based module has been designed for the preamble processing which computes the carrier phase and symbol timing. The hardware structures for various demodulator modules are shown in Figures 7 to 11.



Initial block of the preamble

The input to the subtractor units are the sample values.

Figure 7

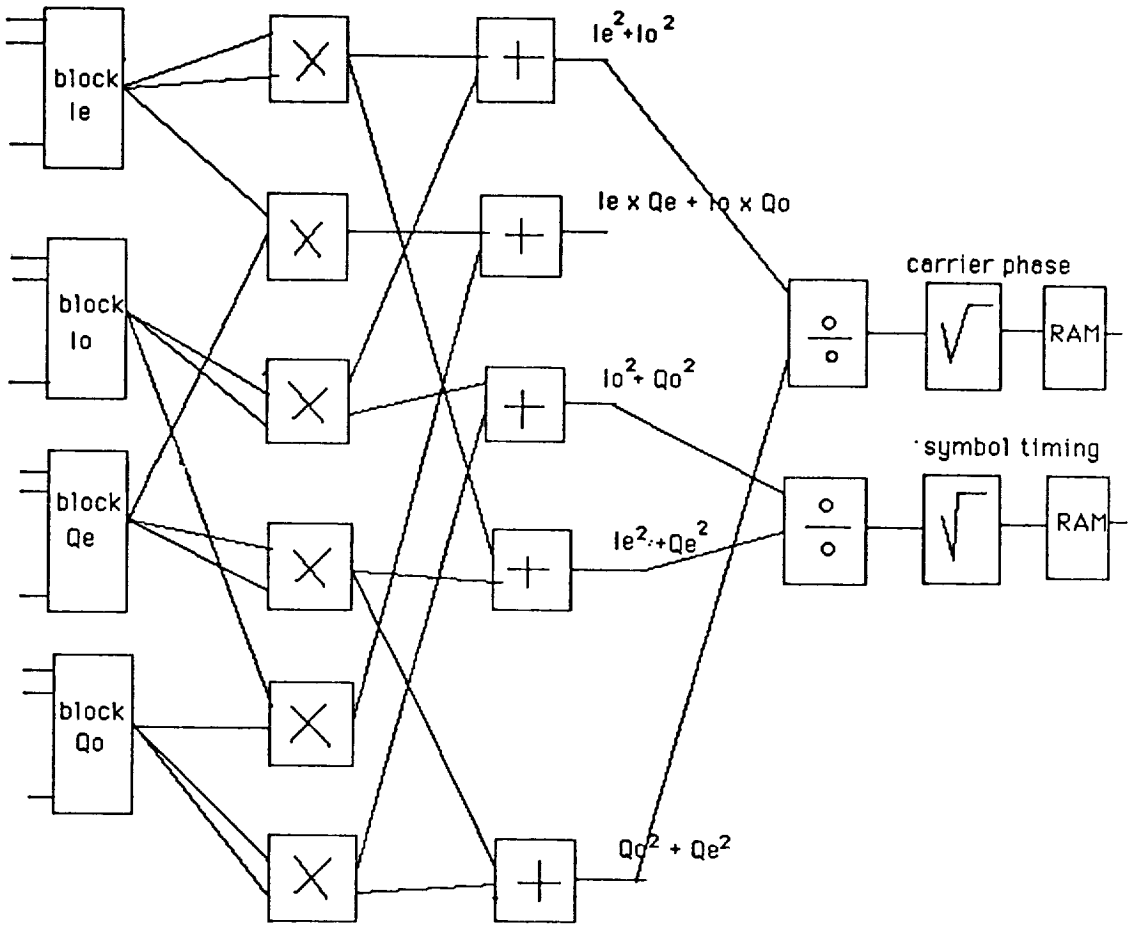
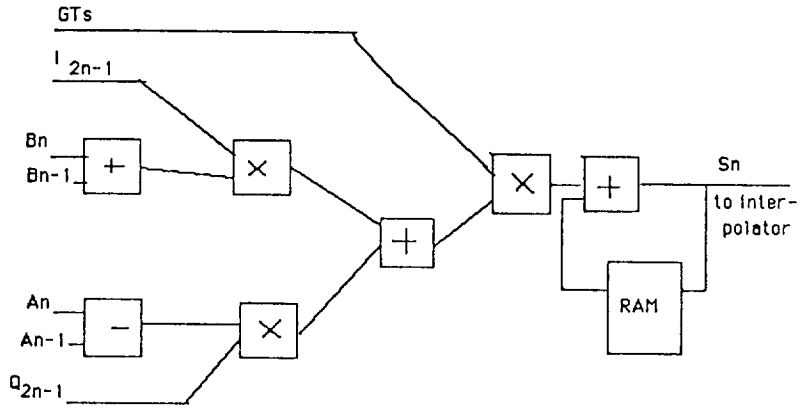
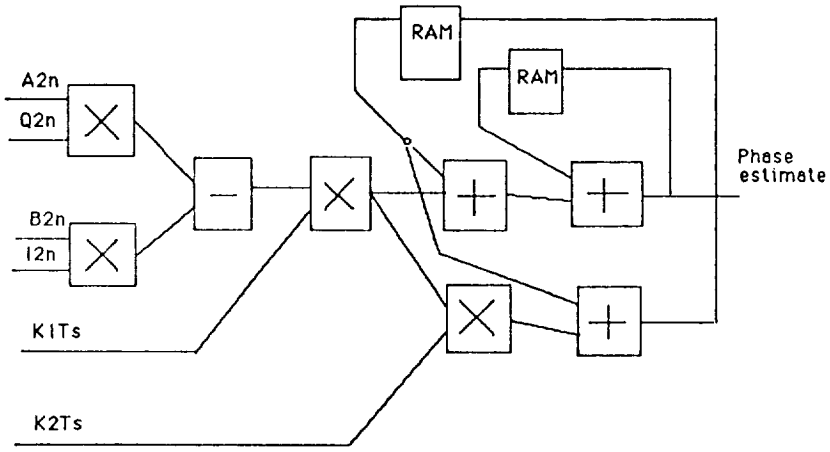


Figure 8: Preamble Module Units



I_{2n-1}, Q_{2n-1} are odd numbered samples from the coherent demodulator
An,An-1,Bn,Bn-1 are the bit decision outputs
Sn is the output from the the module which is used by the sampling clock

Figure 9: Symbol Timing Tracking Module

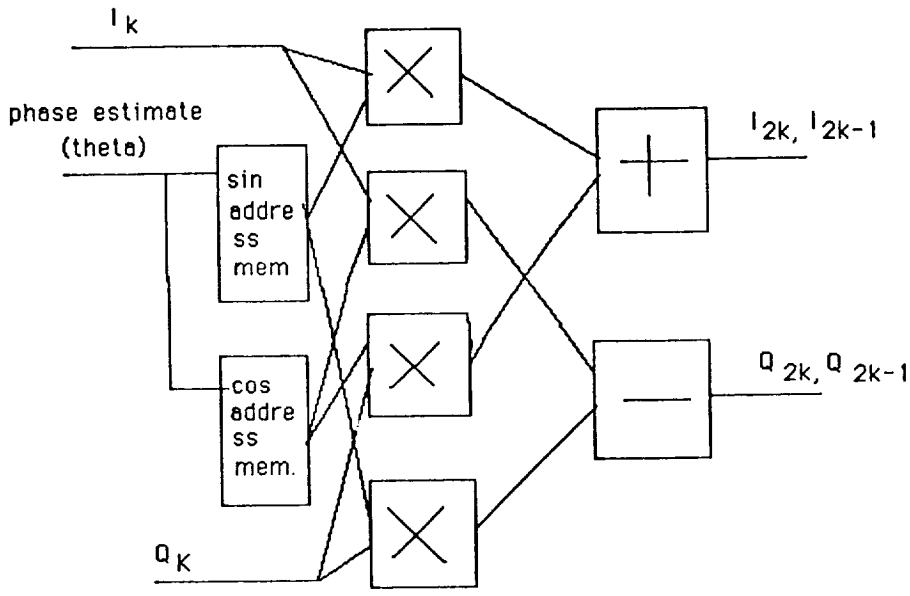


An,Bn are outputs of bit-decision module

KITs,K2Ts are the gain values of the loop

X2n,Y2n are even samples output from the coherent demodulator

Figure 10. Carrier Tracking Module



I_k, Q_k are the outputs from the interpolator

Phase estimate is the output from the carrier tracking

The output samples are used by the bit decision,timing tracking & carrier tracking.

Even numbered samples are used by the bit-decision & carrier tracking ; odd numbered by the timing tracking.

Figure 11: Coherent Demodulator

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