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FLEXIBLE HIGH SPEED CODEC

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ABSTRACT

This project's objective is to develop and demonstrate an advanced high-speed coding technology that provides substantial coding gains with limited bandwidth expansion for several common modulation types. The resulting technique is applicable to several continuous and burst communication environments. Decoding provides a significant gain with hard decisions alone and can utilize soft decision information when available from the demodulator to increase the coding gain.

The hard decision codec will be implemented using a single application specific integrated circuit (ASIC) chip. It will be capable of encoding and decoding as well as some formatting and synchronization functions at data rates up to 300 megabits per second (Mb/s). Code rate is a function of the block length and can vary from 7/8 to 15/16. Length of coded bursts can be any multiple of 32 that is greater than or equal to 256 bits. Coding may be switched in or out on a burst-by-burst basis with no change in the throughput delay.

Reliability information, in the form of 3-bit (8-level) soft decisions, can be exploited using applique circuitry around the hard decision codec. This applique circuitry will be discrete logic in the present contract; however, ease of transition to LSI is one of the design guidelines.

This paper discusses the selected coding technique and describes its application to some communication systems. Performance with 4, 8 and 16-ary PSK modulation is also presented.

A triple error correcting Bose-Chadhuri Hacqenghem (BCH) code was chosen as providing the best compromise between coding gain and implementation complexity. It is possible to reach decoding speeds of 300 Mb/s with reasonable complexity using a pre-solved approach (ref. 1). A BCH codeword has a maximum length of 2^m-1 when defined over the Galois field $GF(2^m)$. The minimum possible value was chosen for m (9) in order to minimize hardware complexity. Twenty-seven parity bits are necessary to obtain a triple error correcting code (distance=7) with m=9. A 28th parity bit is used to simplify soft decision decoding, but provides no gain in a hard decision environment.

The number of overhead bits is padded out to 32 in order to simplify the numerology associated with coding. These extra 4 bits are not part of the code and are available for functions such as unique (synchronization) sequence transmission. The result is an encoder that appends 32 bits to the end of each codeword. Unaltered data precedes these overhead bits since the code is systematic. The number of data bits in a codeword is a multiple of 32 in the range of 224 to 480, resulting in codewords of from 256 to 512 bits.

An arbitrary length burst may be encoded by breaking the data into the appropriate number of 224 bits segments followed by one segment that can be up to 480 bits in length. Every segment is encoded separately, effectively adding 32 bits to each. The resulting overall code rate will be at least 7/8. Continuous mode simply uses consecutive (288,256) codewords.
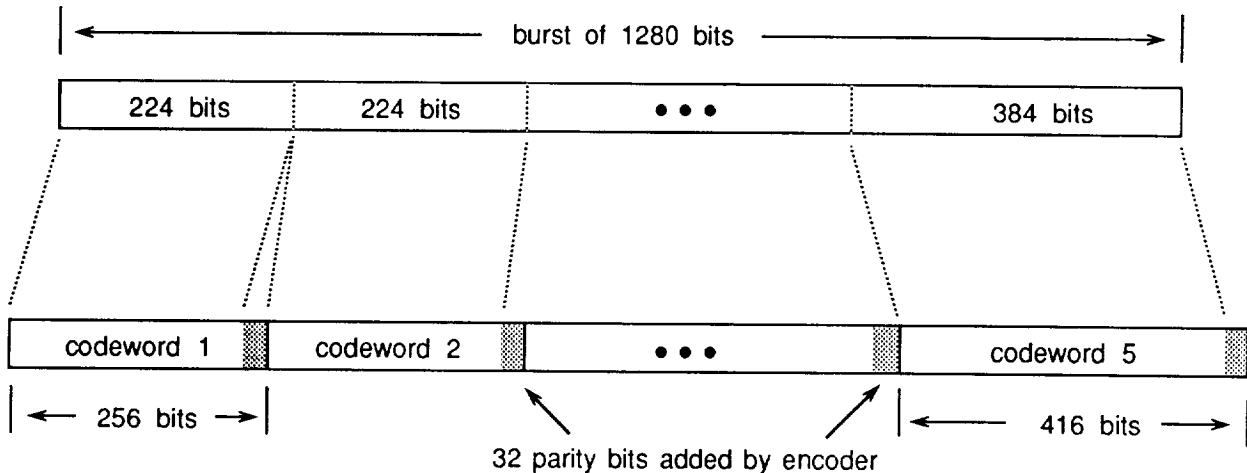

Partitioning a Burst Among Codewords

The ASIC codec can provide encoding and hard decision decoding at data rates up to 300 Mb/s in a stand-alone fashion, given a compatible interface. Data, both coded and uncoded, has a eight-wide interface with the codec chip (six-wide with 8-ary modulations). This is necessary to reduce the 343 Mb/s (maximum) channel rate to an 43 Mb/s interface rate. Also, a format generator, that directs overhead insertion while holding off new data, is assumed. This implies that data is received from the source (e.g. a queue) in bursts (at the channel rate) separated by blank intervals that allow parity insertion. The format generator may also indicate that the burst is not to be coded, in which case the encoder and decoder simply act as delay lines.

Generation of fractional rate clocks and the rate buffering that would be required to accept continuous data from the source and deliver encoded data at a higher rate is extremely difficult with arbitrary data rates. These functions must be provided externally if required in a specific application.

Encoder and decoder on single ASIC Chip
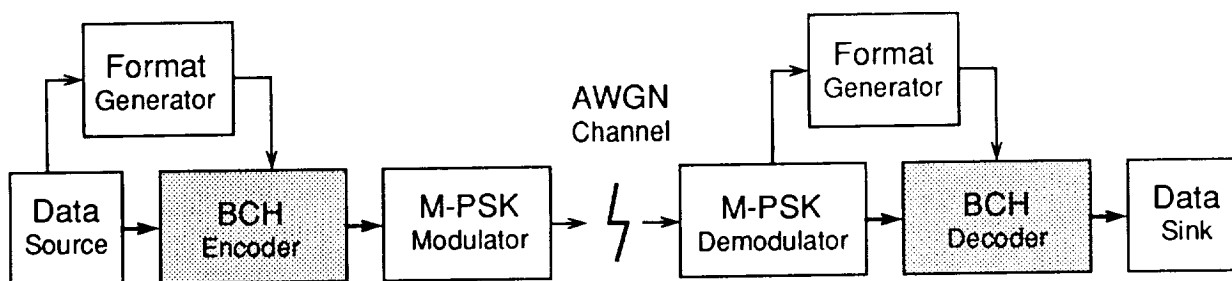
Stand Alone Codec Configuration   (Hard Decisions)
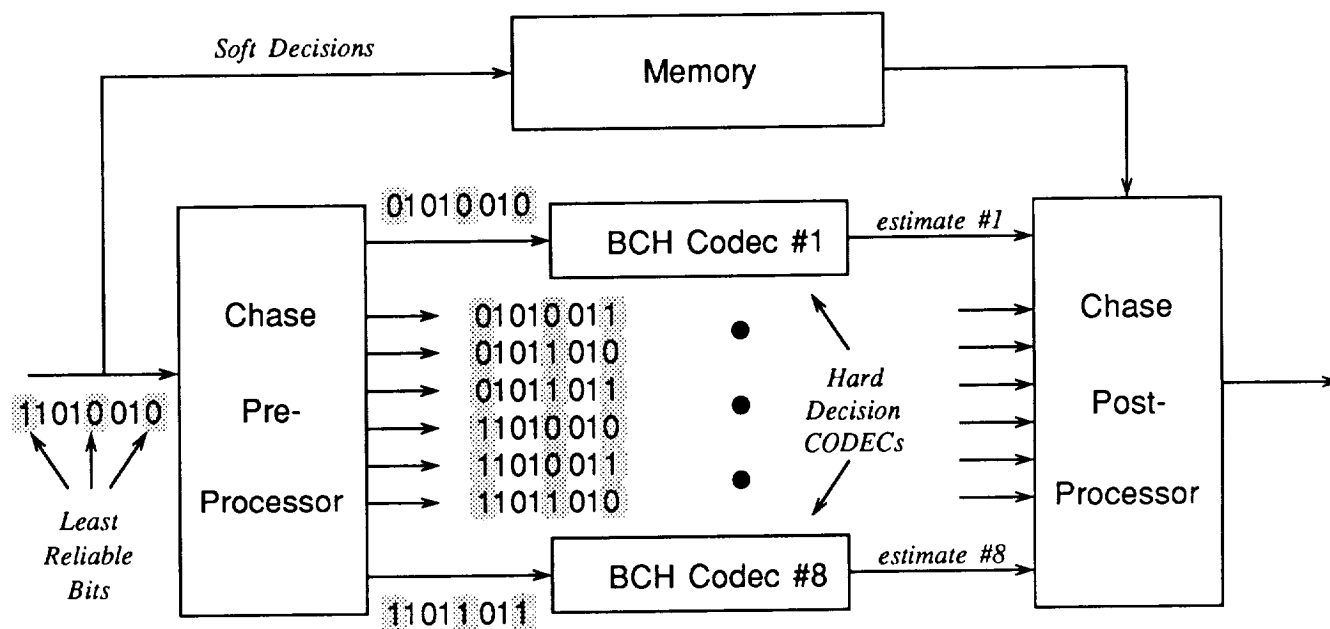
HARD DECISION PERFORMANCE

The figures below relate to the expected bit error rate (BER) after decoding when M-ary PSK modulation is used to communicate coded data over an additive white guassian noise (AWGN) channel. Coding gain with hard decisions is seen to range from 2 to 4 dB in the operational range of $10^{-4} \leq BER \leq 10^{-8}$. Coding gain is a weak function of codeword length and is greatest for the shortest length (224 data bit) codeword.

Hard Decision Performance of (256,224) Code
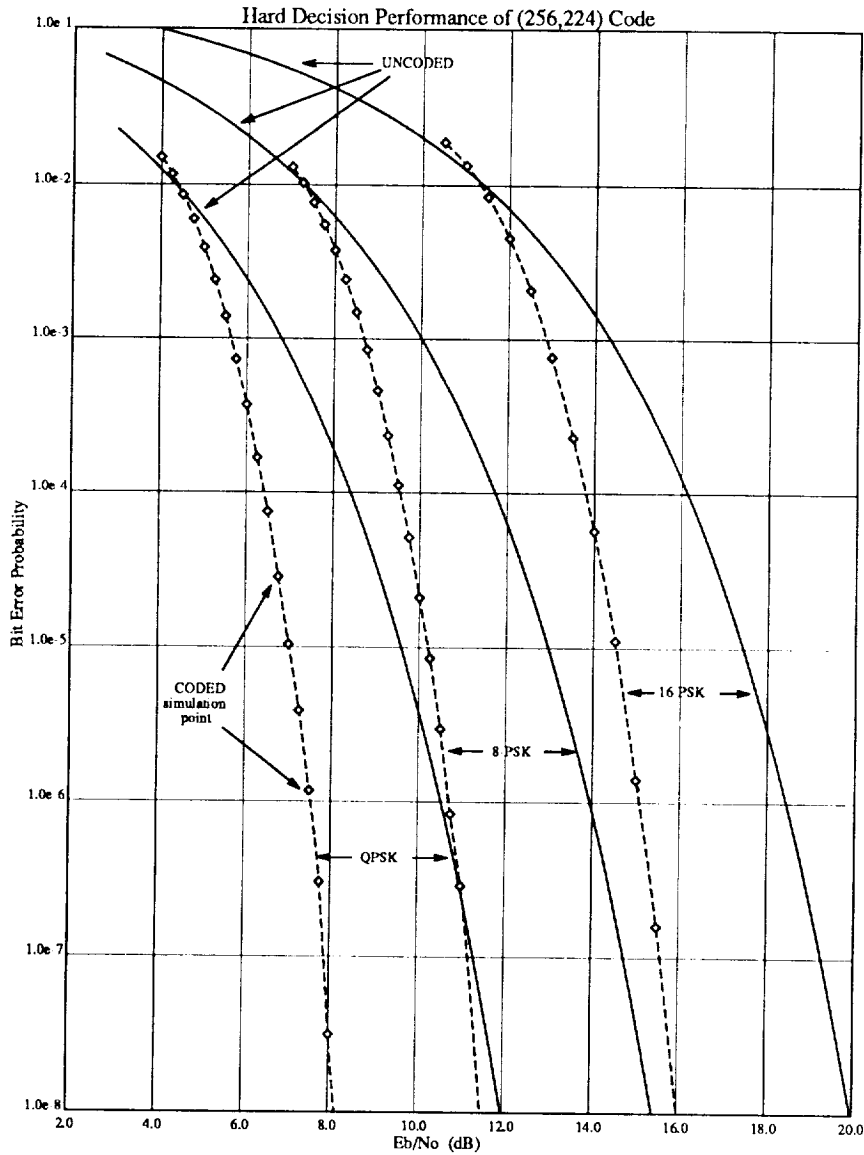
Hard Decision Coding Gain (in dB)						
BER	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
10^{-4}	2.0	2.2	2.4	1.8	2.0	2.2
10^{-6}	3.0	3.2	3.4	2.8	3.0	3.2
10^{-8}	3.8	3.9	4.0	3.6	3.7	3.8

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A Chase (ref. 2) algorithm is employed to utilize soft decision information. Soft decision decoding requires hardware appliques as well as multiple hard decision codecs. The Chase preprocessor uses soft decision information to identify the three least reliably received bits of each codeword . It then generates eight sequences by letting the three least reliable bits take on all possible values. Each of these sequences is hard decision decoded to obtain (possibly different) estimates of the true codeword. A post-processor selects the most likely of these estimates by doing eight correlations, again using the soft decision information. In addition to pre- and post-processors, additional memory to buffer reliability information is required in the soft decision configuration.

Soft Decisions

Memory

01010010

BCH Codec #1

estimate #1

Chase Pre- Processor

11010010

Least Reliable Bits

01010011
01011010
01011011
11010010
11010011
11011010

Hard Decision CODECs

Chase Post- Processor

BCH Codec #8

11011011

estimate #8

Chase Algorithm Decoder

The Chase decoder for this project will differ from the figure above in that it will only process four estimates. Using a 28th parity bit, performance can be maintained while cutting hardware complexity nearly in half by observing overall parity condtition. It is also expected that a single ASIC chip will hold two complete hard decision codecs.

The figures below relate to the expected bit error rate (BER) after decoding when M-ary PSK modulation is used to communicate coded data over an additive white guassian noise (AWGN) channel. Coding gain with soft decisions is from .7 to 1.4 dB greater than with hard decisions alone. The data below corresponds to a Chase algorithm using 3 least reliable bits and analog metrics (infinite quantization).

Soft Decision Performance of (256,224) Code
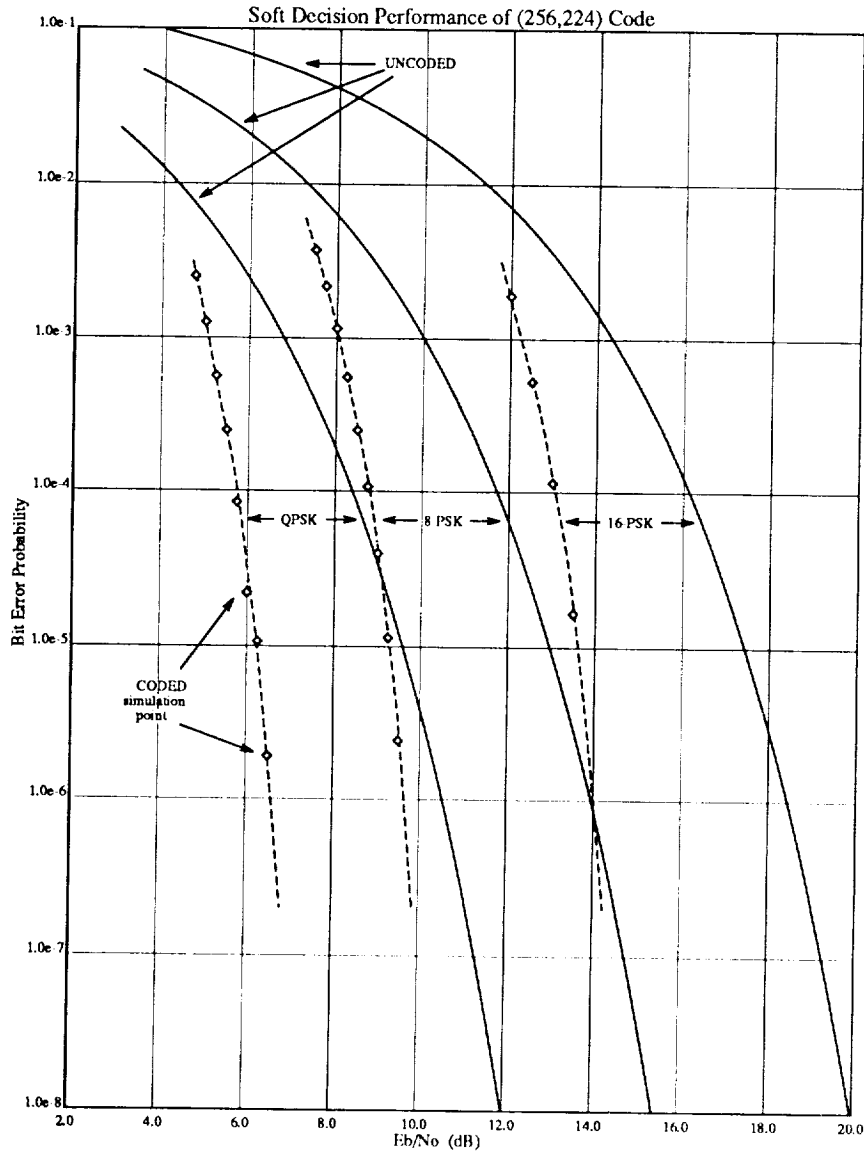
Soft Decision Coding Gain (in dB)						
BER	(256,224) Code			(512,480) Code		
	QPSK	8-PSK	16-PSK	QPSK	8-PSK	16-PSK
10^{-4}	2.7	2.9	3.1	2.5	2.7	2.9
10^{-6}	4.0	4.3	4.5	3.8	4.1	4.3
10^{-8}	4.9	5.2	5.4	4.7	5.0	5.2

OBSERVATIONS

A high-speed, high-rate coding technique suitable for both burst and continuous communication systems has been presented. It can operate as a single chip hard decision codec or, with decoding appliques, can utilize soft decision information in the decoding process. Coding gains up to 4 dB are obtained in the hard decision mode, increasing to as much as 5.5 dB with soft decisions (at 10^{-8} BER).

Error correction coding has long been considered a good means to lower the required EIRP in communication systems having unlimited bandwidth. However, high-rate codes such as the one described are also well suited for bandwidth efficient systems. The codec rate and interface are matched to the larger signaling alphabets used for constrained bandwidth communications. Data has been given indicating that coding gain improves slightly with increasing modulation alphabet size. Even with the overhead required to insert parity bits, the net result is less power required to communicate a given data rate (say 300 Mb/s) over a fixed bandwidth channel (say 200 MHz).

The coding approach is extremely flexible by design. Hard decision operation supports several different interface modes at data rates less than 300 Mb/s. Soft decision performance can be enhanced by increasing the number of least reliable bits identified. Complexity of the Chase algorithm hardware can be reduced at data rates significantly less than 300 Mb/s by using a single hard decision codec to form multiple estimates.

It is believed that the coding approach and hardware resulting from this project will prove useful to a varitey of high rate systems.

REFERENCES

1) Plokinghorn, F. Jr., "Decoding of Double and Triple Error Correcting Bose-Chaudhuri Codes," *IEEE Transactions on Information Theory*, October 1966, pp. 480-481.

2) Chase, D., " A Class of Algorithms for Decoding Block Codes With Channel Measurement Information," *IEEE Transactions on Information Theory*, January 1972, pp. 170-182.

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