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ADVANCED SILICON ON INSULATOR TECHNOLOGY

D. Godbey
Research Chemist
Naval Research Laboratory
Electronics Science and Technology Division
Code 6812
Washington, D.C. 20375-5000

H. Hughes
Research Physicist
Naval Research Laboratory
Electronics Science and Technology Division
Code 6812
Washington, D.C. 20375-5000

F. Kub
Research Engineer
Naval Research Laboratory
Electronics Science and Technology Division
Code 6812
Washington, D.C. 20375-5000

ABSTRACT

Undoped, thin-layer silicon-on-insulator has been fabricated using wafer bonding and selective etching techniques employing an MBE grown $Si_{0.7}Ge_{0.3}$ layer as an etch stop. Defect free, undoped 200-350 nm silicon layers over silicon dioxide are routinely fabricated using this procedure. A new selective silicon-germanium etch has been developed that significantly improves the ease of fabrication of the BESOI material.

INTRODUCTION

Silicon on insulator (SOI) technology is evolving as the older silicon on sapphire technology is replaced by newer technologies capable of supporting smaller geometry devices. Several technologies are competing to produce the next generation of SOI materials, and among the most important are silicon implanted with oxygen (SIMOX) and bond and etch back silicon-on-insulator (BESOI). There is also a subset of BESOI technologies under study that uses a combination of thinning techniques and different etch stops. The etch stops currently under study in the BESOI community include a heavily boron doped silicon layer [1] and a silicon-germanium alloy [2,3] as well as others.

Silicon on insulator has been identified as one of the candidate substrate materials for VLSI circuits in the decade beginning in the year 2000 [4]. Advantages of the SOI VLSI technology compared to conventional bulk VLSI technology include higher packing density, simpler process, and higher performance. Of the available SOI technologies including SIMOX and zone melt recrystallization, BESOI offers advantages in terms of lower defect density and the potential for lower manufacturing cost for large area (6, 8, or 12 inch) SOI wafers.

This work has focused on BESOI fabrication because the buried oxide, unlike with SIMOX material, can be hardened for operation in a radiation environment. As a result, large threshold voltage shifts are experienced in SIMOX devices following irradiation by ionizing sources. An added advantage is that the defect free BESOI device layers are better suited for high voltage and high temperature applications than SIMOX layers. BESOI utilizing a SiGe etch stop is preferred over BESOI employing boron or carbon doped silicon etch stops because of defects induced in the silicon device layer by the presence of these etch stops. An additional advantage that BESOI with the SiGe etch stop has over the boron etch stop process is the elimination of residual electrically active elements (boron) in the device layer following the etch stop removal.

These techniques are also compatible for the fabrication of thin silicon films such as silicon membranes, bolometers, and other devices and structures requiring free standing thin film silicon. Other potential applications include high voltage-high temperature power devices, backside illuminated thinned CCD imagers, and X-ray masks.

EXPERIMENTAL: BESOI Fabrication

A schematic of the BESOI fabrication process is shown in figure 1. Prime wafers were fabricated using molecular beam epitaxy (MBE) on Si(100) substrates that were cleaned chemically using a modified Shiraki procedure prior to being loaded into the MBE system. The oxide was removed *in vacuo* by heating to 800°C in a 0.1 Å/sec silicon flux. The structure was fabricated by growing the following layers: a 20 nm silicon buffer layer, a 60 nm $Si_{0.7}Ge_{0.3}$ alloy etch stop layer, and a 200-350 nm silicon epilayer. After MBE growth the wafers were evaluated by low energy electron diffraction (LEED) and optical microscopy with Nomarski.

The MBE grown prime wafer and the handle wafer were bonded together by the following procedure. Thermal oxides were grown on both the MBE prime wafer (850°C) and the handle wafer. The oxides were both hydrophilyzed in an NH_3:H_2O_2:H_2O solution, and then stacked together oxide to oxide in a microclean environment. Pre- bonding between the two wafers was established at room temperature [3]. The prebonded wafers were inspected using an infrared imaging system to determine the quality of the bond, and unqualified wafers (those showing voids) were reworked. Qualified wafers were annealed at 850°C, and this treatment was sufficient to produce a bond strength that allowed mechanical grinding and polishing of the wafer. The 850°C temperature was sufficiently high to cause some relaxation of the alloy etch-stop layer. As shown later, it did not have a negative impact on the stopping capability of the etch stop. In addition, dislocations formed by relaxation in the etch layer did not propagate into the epitaxial layer as shown by plan view transmission electron microscopy (TEM)[2]. Since no threading dislocations were observed by TEM, an estimate of the upper limit of dislocations in the Si epilayer is set at 10^4 cm^{-2}.

After bonding the prime and handle wafers, the backside Si of the prime wafer and the etch stop must be removed. The back side of the bonded prime wafer was thinned to the desired SOI thickness (200-350 nm) by a combination of mechanical thinning followed by selective etching [3]. Mechanical thinning was employed to bring the backside silicon plus etch stop layer thickness to less than 2 μm before chemical thinning. First, precision diamond grinding was used to reduce the thickness of the active wafer to about 25 μm. The depth of the damaged layer was about 3 μm following this step, and a micrograph of this surface is shown in figure 2. The wafers were then transferred to a precision polisher built by ARACOR to thin the backside layer to less than 2 μm. Figure 3 shows a very smooth layer, indicating that the damage layer was less than 100 nm thick. Optical interference fringe patterns were used to determine the thickness variation of the remaining semiconductor layer. For this sample, the film thickness was determined to vary between 1.5 and 2 μm. Further thinning used a selective silicon etch composed of 100 g. KOH, 4 g. $K_2Cr_2O_7$, 100 ml. propanol, and 400 ml. H_2O [2,3], which removed the silicon selectively from the etch stop layer. The $Si_{0.7}Ge_{0.3}$ alloy etch stop layer was selectively removed by a HNO_3:H_2O:HF(0.5%) solution, 35:20:10 vol:vol [5]. The selective etches for Si and SiGe are discussed below.

Following the removal of the etch stop layer, the finished silicon on insulator material is obtained. A cross sectional transmission electron micrograph of a 200 nm silicon on insulator film is presented in figure 4.

RESULTS AND DISCUSSION

The etches used for the BESOI process must have a high selectivity, defined as the ratio of the etch rate of the top layer to the etch rate of the sublayer. For example, the etch used to remove the remaining Si above the $Si_{0.7}Ge_{0.3}$ etch stop layer must have a fast etch rate for Si and a slow rate for $Si_{0.7}Ge_{0.3}$. Conversely, the etch which is used to remove the etch stop, must have a fast etch rate for $Si_{0.7}Ge_{0.3}$ and a slow rate for Si. An additional constraint on the etches is that the final surface must be left polished, suitable for device processing.

The selective silicon etch showed the behavior indicated in figure 5. The slope of the steep curves on the left side of the plot is the etch rate of the silicon layer. The rate obtained was 19 nm/minute and did not change following heat treatment to 850°C as shown in the plot. The shallow curves on the right give the etch rates

through the alloy etch stop layer and were 0.8 and 1.1 nm/minute for the as grown alloy layer and the layer heated to 850°C for 30 minutes respectively. The selectivity was approximately 20:1.

The selective removal of the $Si_{0.7}Ge_{0.3}$ alloy etch stop layer is shown in figure 6. The slope of the left side of the curve gives the etch rate through the etch stop layer which was 41 nm/minute. The etch rate through the underlying silicon layer was 0.4 nm/minute, giving a selectivity for the etch stop removal of 100:1. The alloy etch left the surface polished, as required.

Spreading resistance profiling was done on a 200 nm Si BESOI layer. The results showed the fabricated device layers to have a residual doping level of $8x10^{14}$ cm^{-3} p-type. Thus we have the basis for a fully depleted BESOI technology. MOS devices have been fabricated, and their performance is shown in figures 7 and 8 for n-channel and p-channel MOSFET's, respectively. The n-channel devices show the well known "kink" effect typical of thin film MOS devices. These devices were well behaved as shown, and future work will include research on the radiation tolerance of the NRL BESOI compared to other SOI technologies.

CONCLUSIONS

The use of an epitaxial $Si_{0.7}Ge_{0.3}$ layer etch stop in the fabrication of BESOI has been developed. This technique utilizes thermal and deposited oxides to form the buried oxide layer, thereby enabling the use of standard radiation hardening techniques in the growth of the buried oxide. The use of an epitaxial $Si_{0.7}Ge_{0.3}$ layer as an etch stop results in a defect free and undoped silicon on insulator film. The silicon film can be grown to any thickness desired, and silicon films in the 200-350 nm range are routinely fabricated.

ACKNOWLEDGMENT

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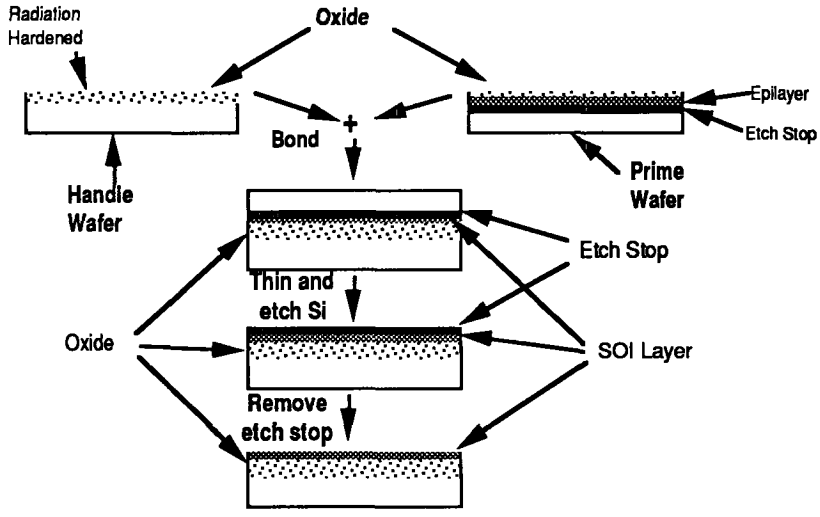

Figure 1. Schematic representation of bond and etch back silicon on insulator fabrication.

Figure 2. Active side of bonded wafer after being ground to thickness of 25 μm showing the 3 μm surface damage.

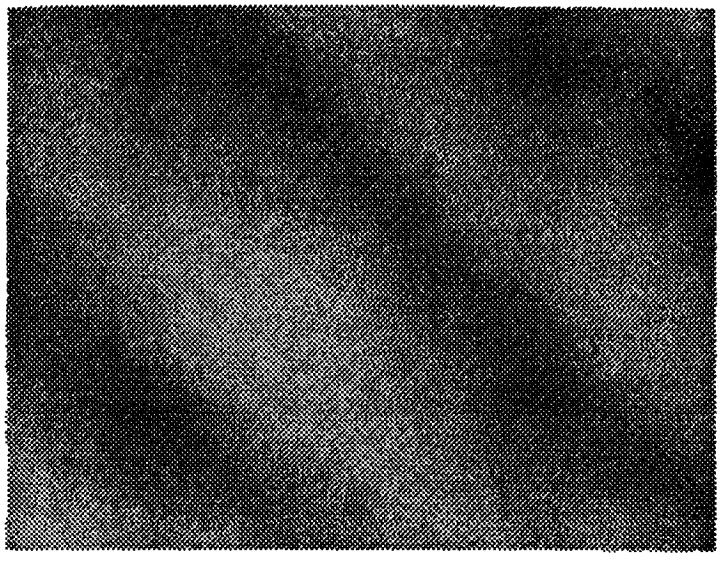

Figure 3. Active side of bonded wafer after being precision polished to a thickness of 2-1.5 μm showing a smooth surface and interference fringes.

Figure 4. Silicon on insulator fabricated by bond and etch back using a SiGe alloy as etch stop showing a 200 nm SOI layer on a 920 nm oxide layer.

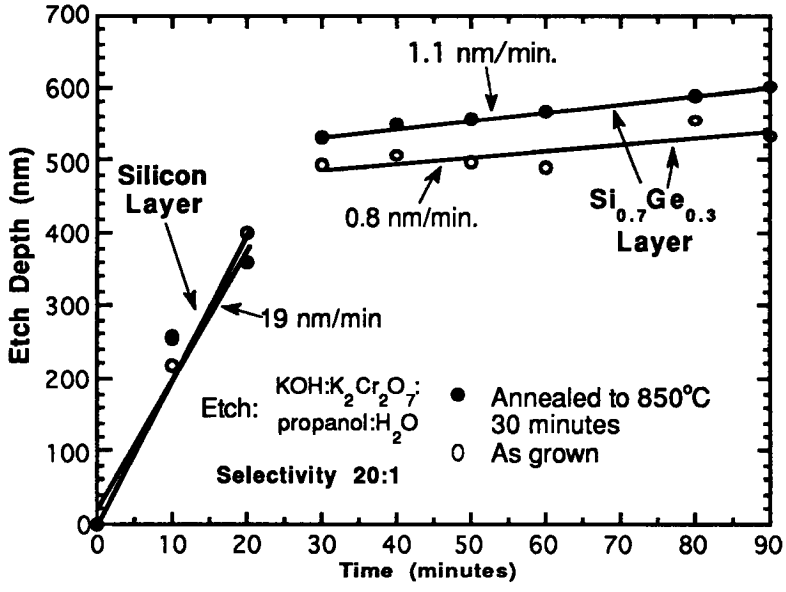

Figure 5. Silicon selective etch. The steep slope gives the silicon etch rate, while the shallow slope gives the alloy etch rate.

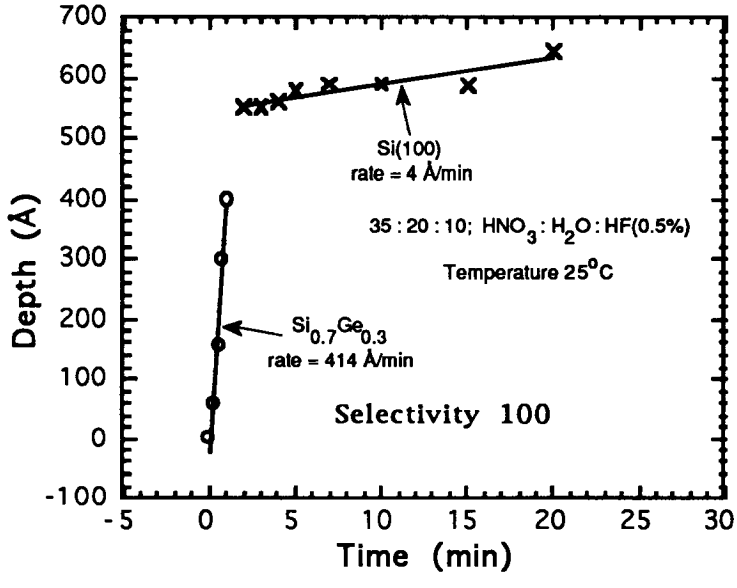

Figure 6. SiGe (30% Ge) selective etch. The steep slope gives the alloy etch rate, while the shallow slope gives the silicon etch rate.

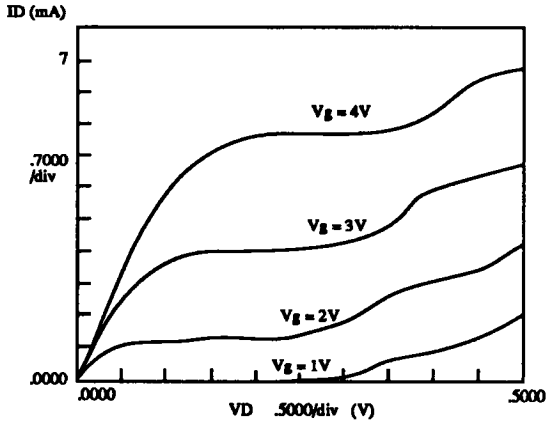

Figure 7. Drain characteristics of the 1.0 μm n-channel MOSFET. The floating-body related kink effect is seen for this device.

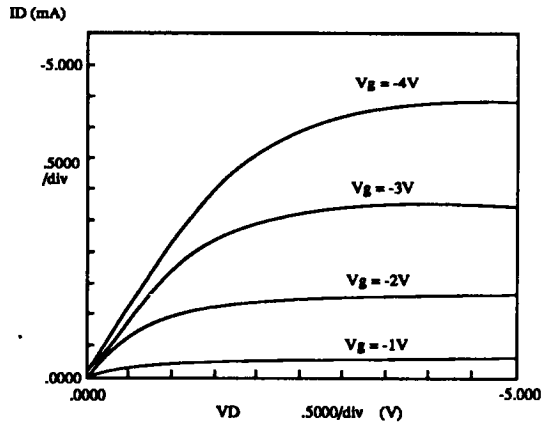

Figure 8. Drain characteristics of the 1.0 μm p-channel MOSFET. The applied bias to the substrate was +5 V during measurement to control the back-channel threshold.