FEC Decoder Design Optimization for Mobile Satellitel Communications

Ashim Roy, Leng Lewi

Hughes Network Systems, Inc.
11717 Exploration Lane
Germantown, MD - 20874, USA
Ph. (301) 428-5649, Fax. (301) 428-1868

ABSTRACT

A new telecommunications service for location determination via satellite is being proposed for the continental USA and Europe, which provides users capability to find the location of, and communicate from, a moving vehicle to a central hub and vice versa. This communications system is expected to operate in an extremely noisy channel in the presence of fading. In order to achieve high level of data integrity, it is essential to employ forward error correction (FEC) encoding and decoding techniques in such mobile satellite systems. A constraint length $k=7$ FEC decoder has been implemented in a single chip for such systems. The single chip implementation of the maximum likelyhood decoder helps to minimize the cost, size and power consumption, and improves the bit error rate (BER) performance of the mobile earth terminal (MET).

INTRODUCTION

The Location Determination Service (LDS) provides the end users location determination capability based on satellite ranging techniques and communication capability, via satellite, to a central hub. The LDS communications system comprises three main elements: a mobile earth terminal (MET), an LDS hub and a subscriber's hub, as shown in Figure 1. In mobile satellite communication systems such as LDS, size, cost and power consumption of the MET are major system constraints. The signal to noise ratio at the MET input is typically very low and the system operates in a fading environment. Under these circumstances, it is not possible to achieve end-to-end data integrity without a forward error correction (FEC) scheme. The FEC decoder presented here is a maximum likelihood decoder and therefore, offers the highest coding gain among convolutional decoders of a given constraint length. A single chip, constraint length $k=7$, FEC decoder based on the Viterbi algorithm has been developed for the mobile satellite communications application described above[1].

SYSTEM REQUIREMENTS

One of the key requirements for the LDS remote terminal unit is that it must be reliable under a wide range of operating conditions. The efficient usage of VLSI technology in the MET has made it possible to achieve very high MTBF for the unit. The LDS communications system may be visualized with respect to the LDS hub, where, the inbound channel provides a link from the MET to the hub and the outbound channel provides a link from hub to the MET. In the land mobile application, the MET must operate within harsh electrical and environmental condition. The MET operating conditions are listed in Tables 1.

Decoder Requirements

The information is encoded by a constraint length k = 7 convolutional code. The encoding polynomials, G1 and G2 are:

$$G1 = 1 + X2 + X3 + X5 + X6 = (133)_o \quad [1]$$

$$G2 = 1 + X1 + X2 + X3 + X6 = (171)_o \quad [2]$$

The rate 1/2 encoder described by the above polynomials may be easily built from shift registers. The encoder register is reset to logic "zero" at the beginning of a data frame and flushed with six "zeroes" at the end of the frame. Rate 3/4 encoding is provided using the same encoder by means of puncturing the encoded symbols. A puncture pattern, which causes the minimum loss in the BER performance compared to the rate 1/2 operation, is $(110)_b$ and $(101)_b$, for the I and Q outputs respectively. In order to meet the size and power consumption requirements of the MET, the decoder for the LDS must meet the requirements outlined in Table 2.

The Viterbi decoding algorithm may be implemented by either performing a fixed number (N) of mathematical operations serially in an ALU at a speed N times the input data rate or performing these operations in parallel in N ALUs. The serial scheme minimizes the silicon area while increasing the computation speed. The parallel implementation increases the silicon area and therefore, the cost, while minimizing the computation speed. The increased gate complexity of the parallel implementation results in higher power consumption for the decoder. An alternative to either the serial or the parallel implementation is a hybrid approach, where a small number of ALUs operating in parallel at a speed higher than the input data rate perform all the operation within the duration of each input data period. The hybrid approach also allows the designer to perform the speed, power and area optimization by selecting a sufficient number of math units (ALUs) to cater for the data rates involved in the application.

THEORY OF OPERATION

The FEC decoder is implemented as a rate 1/2 decoder with the capability to accept rate 3/4 encoded data and puncture inputs. A block diagram of the decoder implementation will be presented. The decoder receives convolutionally encoded symbol pairs, either in serial or parallel format and provides one corrected information bit for each symbol pair. The symbol output of the demodulator is available as 3-bit soft decision values, which are represented in sign-magnitude form. The decoder uses the 3-bit sign-magnitude symbol values as an indication of "strength" of logic "one" and "zero" at the output of the demodulator[2].

The branch metric logic uses the soft decision values to compute the branch metrics, M_i; i = 1,4 once every information bit period. The branch metrics are the total distance of each received symbol pair from the hypothesized symbol pair and represent the probability of bit error.

For constraint length k = 7, the decoder has $2^{(k-1)}$ or 64 states. The state metric computation is an iterative process, where the state value, $S_t(p)$, for state p at time t is computed from state values, $S_{t-1}(2p)$ and $S_{t-1}(2p+1)$ for states 2p and 2p + 1 at time t-1 as defined by the equations below.

$$S_t(p) = \text{Min}[X, Y] \quad [3]$$

$$S_t(p+32) = \text{Min}[X', Y'] \quad [4]$$

where:

$$X = S_{t-1}(2p) + M_i \quad [5]$$

$$Y = S_{t-1}(2p+1) + M_j \quad [6]$$

$$X' = S_{t-1}(2p) + M_j \quad [7]$$

$$Y' = S_{t-1}(2p+1) + M_i \quad [8]$$

where:
S is the state metric value and
M is the branch metric value

The state metric values are stored in the State Metric Memory (SMM). For each present state, its originating state is stored as a pointer, in the Trellis Memory (TM). For most practical implementation of Viterbi decoder, the trellis depth is traded with the maximum data rate of operation and the BER performance of the decoder. The traceback is initiated by first computing the present best state, which has the minimum state metric value. The best state becomes the starting point, for the traceback operation, in the trellis memory. The decoder then searches backwards based on the pointer values stored in the trellis memory. Traceback is completed when the decoder has searched the entire depth of the traceback memory, and decoder outputs a decoded information bit. The decoder operation for rate 3/4 encoded symbols is identical to that for rate 1/2 symbols with two differences:

1. The trellis depth for rate 3/4 operation is longer, and
2. The dummy data contained in the punctured bit locations are ignored.

DECODER DESIGN OPTIMIZATION

The FEC decoder performs many computations during every information bit period. These mathematical operations relate to two major tasks performed by the FEC decoder:

1. Generation of the state metrics and the trellis pointers, and

2. Traceback of the trellis to provide decoded data.

These two tasks are mainly independent and, therefore, may be performed concurrently. The computation clock frequency is selected based on providing sufficient number of computation clock cycles within each data rate clock for completing these concurrent tasks. Main mathematical operations, performed to decode an encoded symbol pair, are:

State Metric Computation	Trellis Computation
64 x 1 Memory Read	Trellis Memory Write
64 x 1 Memory Write	Address Generation
64 x 2 Additions	Trellis Memory Read
64 x 2 Compare	Iterative Traceback

The design partitioning is performed with a view to select an optimal set of design parameters for the above operations. These parameters include:

Size of State Metric Memory
Size of Trellis Memory
Number of ALU Units
Computation Clock Frequency
Power Consumption
Silicon Area

State Metric Memory

The constraint length $k = 7$ decoder has 64 states. The State Metric Memory stores the metrics for all of these states. The word length of the SMM is dependent upon number of soft decision bits and SMM overflow protection algorithm. The decoder implementation presented here employs some unique properties of the state metrics:

1. Each present state is computed from two previous states, one of which is an even parity state and other is an odd parity state. The parity, considered here is, of the state number (i.e. index of S) not of the state value.

2. The states p and $(p + 2^{(k-1)/2})$ are computed from the same set of inputs as defined by the equations above.

3. The input states to the ALU and the output statess of the ALU form even-odd parity pairs.

These properties provide the means of computing two state metrics simultaneously, with minimal increase in additional logic. The routing on the silicon and the size of the state metric memory is optimized by employing butterfly memory technique. The butterfly architecture used in the present design has two ALU units coupled to two 32 x 6 state RAMs. One RAM is used for storing state metrics for even parity states and the other RAM is used for storing state metrics for odd parity states. The storage of new state values in the butterfly arrangement is explained in Figure 2. The computation clock frequency is further optimized by keeping the state RAM bus active at all times, alternating between read and write cycles as shown in the the pipeline arrangement in Figure 3. The chip power consumption is further lowered by the use of psuedo static RAMs rather the power hungry fully static RAMs.

Trellis Memory

The trellis depth is selected to meet the BER performance of the decoder for the LDS application. In an FEC decoder, infinite trellis depth provides the highest coding gain. The land mobile channel is such that traceback path in the trellis merges and it is sufficient to provide a trellis depth which is a small multiple of the constraint length. The trellis depth requirement increases with the coding rate [3]. The trellis memory is implemented as a byte-addressable RAM. The read and write operations to this RAM are interleaved during one information bit period. The addresses for present memory read operation during the traceback is computed from the contents of the previous memory read operation. Starting at the best state, traceback logic reads the pointers at each step to determine whether the state, p, originated from state, 2p, or 2p + 1. The implementation of the trellis memory address generator, therefore, simplifies to a shift register implementation, which is initialized with the best state number. At each traceback step, the shift register is shifted left by one and the trellis pointer loaded into the least significant bit position of the shift register to generate the address of the previous state from which the present state was derived.

Power Consumption

The power consumption in a CMOS device is a function of gate complexity and the frequency of operation. A major part of the operations for the decoder are related to the state metric computations. These memory I/O and ALU operations must be repeated $2^{(k-1)}$ times every information bit period. These state metric computations are largely sequential, in that memory read is followed by addition, which is followed by comparison and finally memory write. The computation speed required to complete these operations within a single information bit period is dependent upon the number of ALU's available to complete these tasks. Increasing the number of ALU units from 1 to 2 reduces the power consumption of the decoder a considerable amount at a cost of 4% increase in gate complexity and 2% increase in silicon area of the decoder. Further increase in the number of ALU units reduces the power consumption but has a larger impact on the silicon area. This is due to the exponential increase in interconnect buses from the ALU units to the state and trellis memories. Therefore, the FEC decoder for this application was based on two ALU units generating all the state metrics and trellis pointers. The results of this optimization are presented in Table 3.

PERFORMANCE

The performance of the decoder was measured under a variety of noise environments. The BER performance of the decoder is shown in Figure 4. The present implementation of the decoder provides coding gain within 0.2 dB of a FEC decoder with infinite trellis depth. This performance has been achieved within the constraints of the LDS require-

ments. A summary of the characteristics of FEC decoder is presented in Table 4.

CONCLUSIONS

A low cost, constraint length k = 7 FEC decoder for Location Determination Service has been implemented in a single VLSI chip. This device has been extensively tested and provides very high coding gain necessary for LDS applications. The low cost and low power implementation of the decoder in a single chip makes the device ideally suited to mobile satellite communication applications. The inclusion of features such as rate 3/4 operation and QPSK modulation makes the device applicable for Very Small Aperture Terminal (VSAT) applications as well. The applicability of this technology for other mobile satellite communication systems based on Inmarsat Standard-M is being investigated.

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Table 1. MET Operating Environment

Temperature	-30°C to +60°C
Relative Humidity	0 to 100%
Altitude	0 to 3000 meters
Vibration @ 1kHz	+/- 5 g

Table 2. FEC Decoder Requirements

Max. Encoded Data Rate	250 Ksps
Maximum Clock Freq.	10 MHz
Constraint Length	7
Encoding Polynomials	$(133)_o$, $(171)_o$
Coding Rates	1/2, 3/4
Rate 3/4 Puncture Pattern	$(110)_b$, $(101)_b$
Demodulation Interface	BPSK, QPSK
Rate 1/2 Coding Gain	5.1 dB @BER = 10^{-5}
Rate 3/4 Coding Gain	4.2 dB @BER = 10^{-5}
Code Synchronization	Yes
Active Power Consumption	150 mW
Standby Power Consumption	10 mW
Operating Temperature	-40°C to +85°C

Table 3. FEC Decoder Optimization for LDS

ALU's	Clock Freq. MHz.	Size K mil^2	Power mW
1	25	55.1	260
2	10	56.2	105
4	4	62.5	75

Table 4. FEC Decoder Characteristics

Fabrication Technology	1.5 micron CMOS
Number of Transistors	52,000
Decoder Dimensions	5.7 mm x 6.3 mm
Viterbi Decoder Package	44-pin PLCC
Active Power Consumption	105 mW
Standby Power Consumption	3 mW
Highest Data Rate	320 kbps

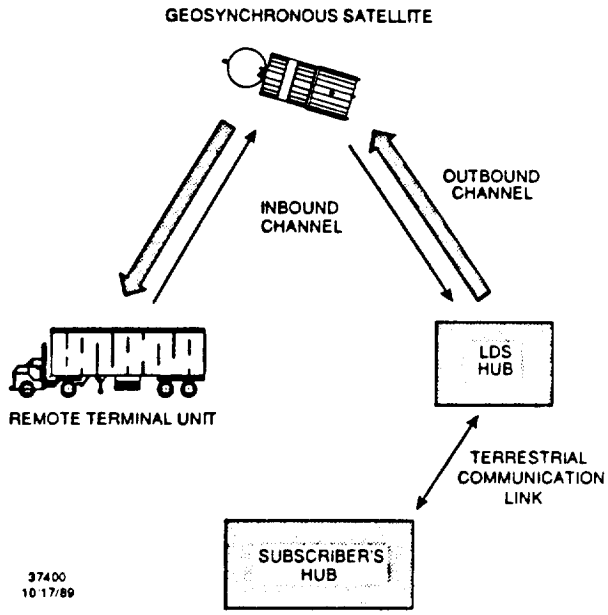

Fig. 1. LDS Communications System

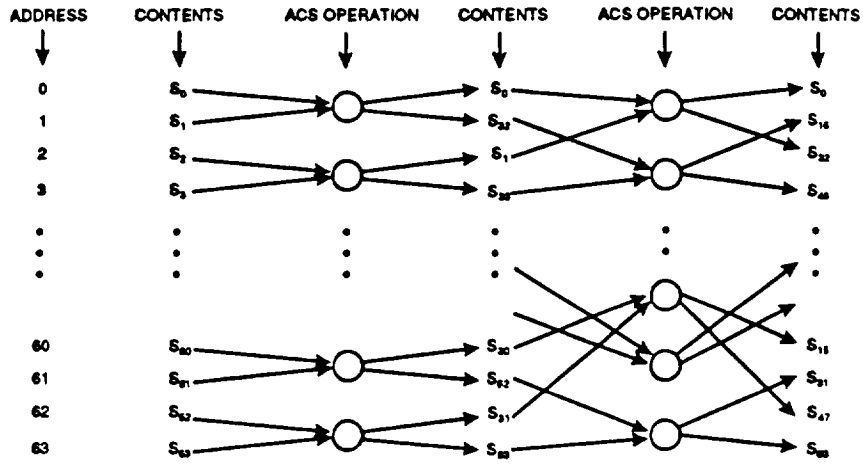

Fig. 2. Butterfly Memory Operation for k = 7 Decoder

ALU Cycle 1	ALU Cycle 2	ALU Cycle 3	ALU Cycle 4
RD (n)	WR (n-1)	RD (n + 1)	WR (n)
NO-OP	ADD (n)	NO-OP	ADD (n + 1)
SEL (n-1)	NO-OP	SEL (n)	NO-OP

Fig. 3 ALU Pipeline Operation