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Output Data Formatter for the Electronically Scanned Thinned Array Radiometer (ESTAR) Instrument

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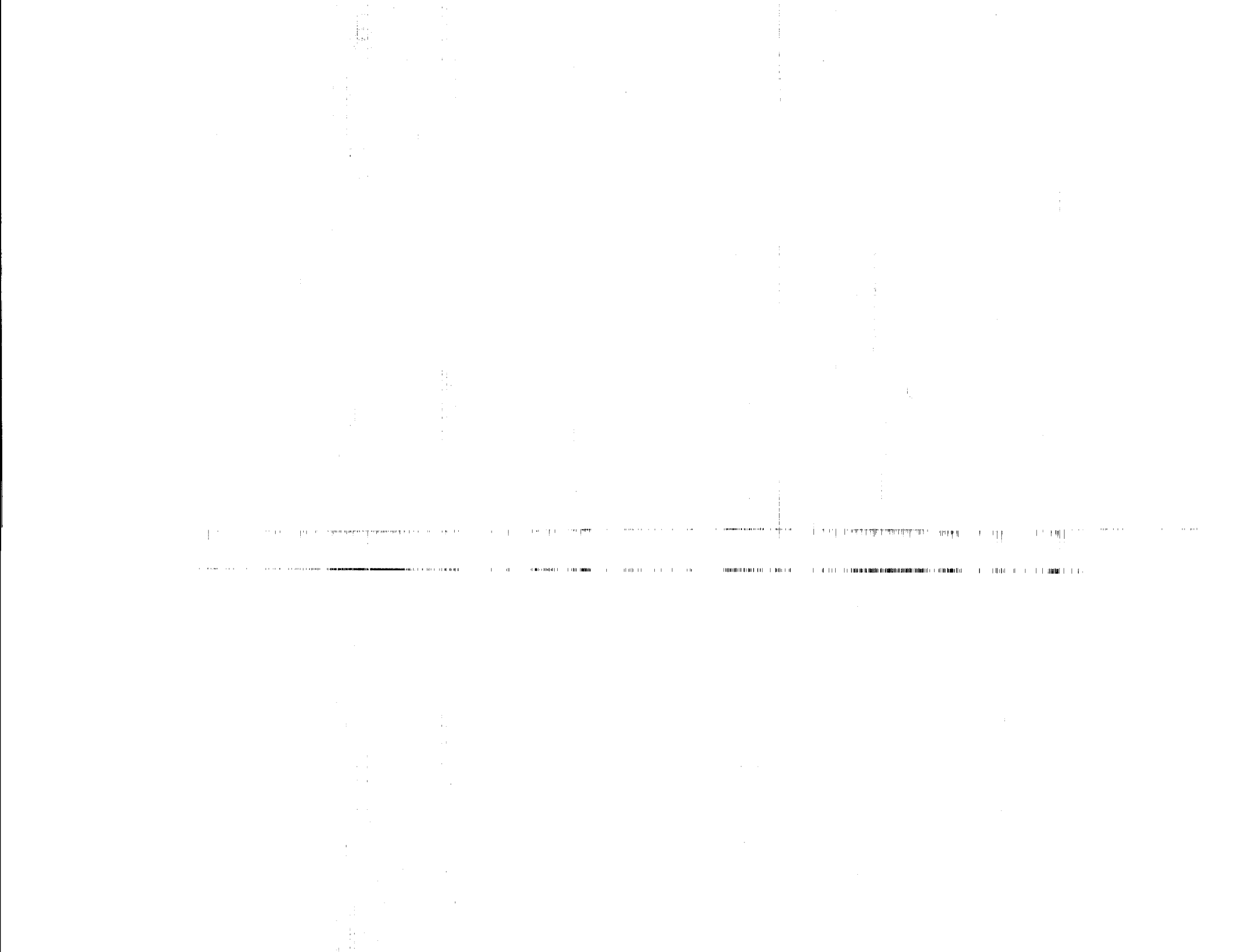


Abstract: *A prototype Output Data Formatter (ODF) for the ESTAR (Electronically Scanned Thinned Array Radiometer) instrument has been designed and tested. It employs programmable logic devices to format and tag correlator data for transmission to earth. After accepting 170 bits of correlator and error data in parallel, it appends an identification word and then serially passes the data to the Small Explorer Data System (SEDS) for transmission at a maximum rate of greater than 15 Mb/sec. Implemented with two reprogrammable field programmable gate arrays (FPGAs) each contained in a 132-pin plastic pin grid array (PGA) package, the design is cascadeable, fully testable, and low-power.*

1. Introduction

ESTAR (Electronically Scanned Thinned Array Radiometer) is a passive synthetic-aperture radiometer designed to sense soil moisture and ocean salinity in L-band. It is being developed as an earth probe mission intended for launch in the late 1990's as part of the Earth Observing System (EOS).

A recent feasibility study [1] of the ESTAR concept recommended that a two-dimensional prototype be built in order to study further the design issues involved. Grand Valley State University Professor William A. Chren, Jr. was awarded NASA JOVE Grant NAG 8-226 to design and build four subsystems that will be part of the digital data subsystem (DDS) in this prototype. The first of these four subsystems, the Output Data Formatter (ODF), has been completed, and is the subject of this paper.

Section 2 is a presentation of background information about the ESTAR. Subsequent sections present the details of the ODF.

2. ESTAR Background

The synthetic aperture sensing technique employed by ESTAR is a method whereby the high spatial resolution and sensitivity of a large dish antenna can be duplicated with a small, lightweight T-shaped array of dipole antennas (see Figure 1).

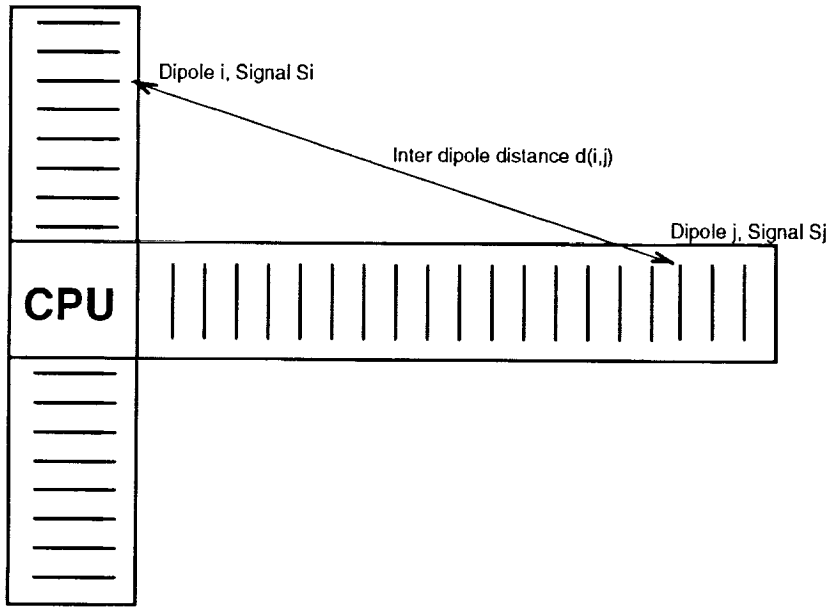


Figure 1: Dipole Antenna Locations on ESTAR Instrument

Such a duplication yields size and weight advantages which make it attractive for use on earth-sensing spacecraft. It is made possible by the calculation, for all pairs (i,j), of the pairwise complex correlation between dipole signals S_i and S_j using the formula

$$\langle S_i, S_j \rangle = \frac{1}{T} \int_0^T S_i(t) S_j^*(t) dt \quad , \tag{1}$$

in which "*" denotes the complex conjugate and T is a suitably chosen integration period. It can be shown that each of these correlations is a sample, in frequency space, of the spatial Fourier Transform of the brightness temperature distribution over the field-of-view (FOV) of the antenna. Consequently, the visibility function in the FOV can be computed by inverting the sampled transform. Furthermore, the location of the sample in frequency space is determined only by the inter-dipole distance and not by the absolute locations of the dipoles themselves [2].

The data processing system on ESTAR will compute, in real time, these correlations for each dipole pair (i,j). The processing will be done digitally at a centrally located processing unit called the CPU, as shown in the figure. The results will then be sent to earth where the inverse transform will be computed. Necessary dipole signal preprocessing, including down-mixing and A/D conversion, will be done at each dipole by circuitry contained in a "Front End Module" (FEM).

2.1 Major Digital Data Subsystem Components

At the functional level, the digital data subsystem (DDS) consists of six major components [3]. The first of these, the Digitizer, must convert the FEM data to digital form before sending it to the CPU. This will be done by an A/D converter in each FEM. The second, the Data Bus, must transport the digitized data from the FEMs to the CPU. The third, the CPU, must compute the correlations for each pair of FEMs. It is also responsible for overall control of the DDS. Furthermore, it must interface with the Small Explorer Data System (SEDS), which is a software and hardware "operating system" on the space vehicle. Among other tasks, SEDS performs overhead functions such as data encoding and transmission to earth, earth command processing and system test. The CPU must pass the correlation products to SEDS for transmission to earth. The fourth part, the System Clock, is necessary to ensure that dipole data samples are generated synchronously by all FEMs. In effect, the Clock signals the FEMs to generate data samples at the same instant. The fifth part, the Phase-Aligner, removes the phase differences between FEM samples when they arrive at the CPU. These differences are caused by unequal data propagation times to the CPU from distant and nearby FEMs. The Phase-Aligner must hold the early-arriving data until the late-arriving data is available. Only when all FEM data for a particular sample time have arrived at the CPU will the Phase-Aligner signal the CPU that the data is ready for correlation. The sixth part, the Walsh Function Generator, generates a unique Walsh function signal for each FEM. This signal is used to cancel low frequency noise generated by the analog circuitry in the FEM. These six components fit together as shown in Figure 2.

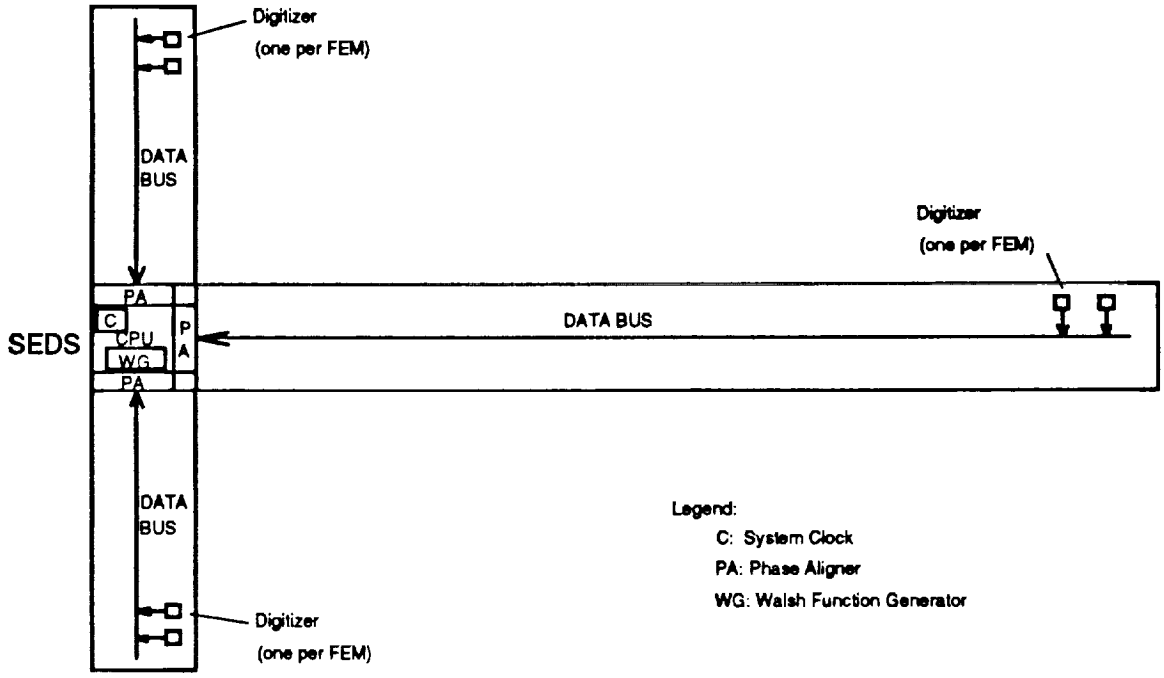


Figure 2: Six Major Components of the DDS

2.1.1 The CPU and the ODF

The CPU is responsible for computing the pairwise correlations of the FEM data. It must also control the DDS and pass the correlation products, suitably tagged and including error information, to SEDS. The design of the CPU is shown in Figure 3. It consists of 3 subsystems, called the

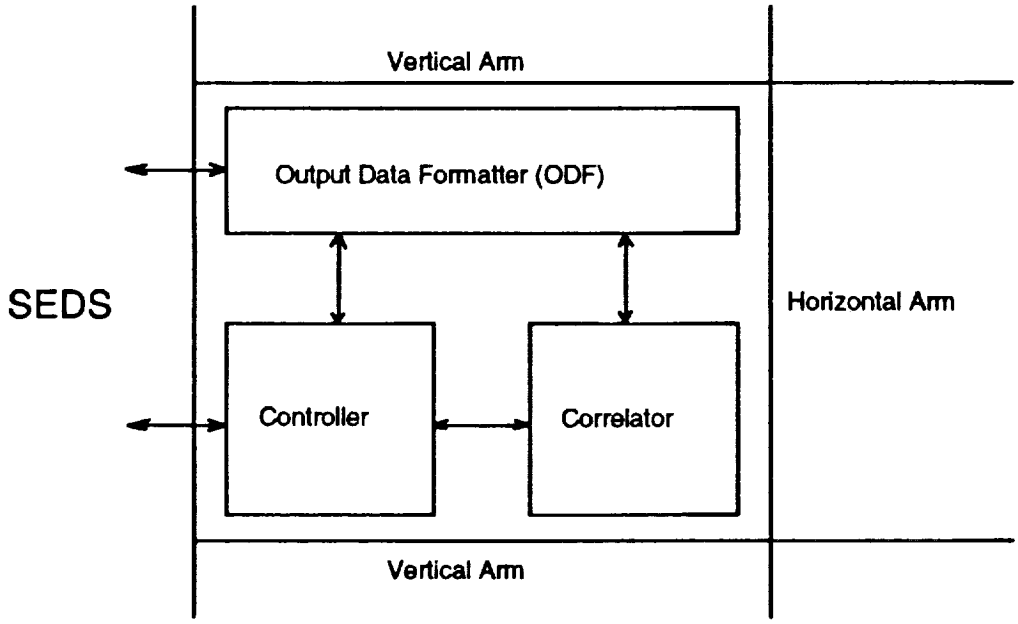


Figure 3: CPU Functional Block Diagram

Controller, Correlator and Output Data Formatter (ODF). These subsystems will be implemented using three different Application Specific Integrated Circuits (ASICs). The first two subsystems will be discussed immediately, in the remainder of this section. Discussion of the ODF is the topic of the remainder of this paper.

Controller

The Controller orchestrates the operation of the DDS, and is implemented by an ASIC of the same name. It controls the Data Bus, Phase-Aligner, System Clock, CPU and Walsh Function Generator during five possible modes of operation called the correlate, output, calibrate, command and test modes. During the first two modes, FEM data are correlated and passed to SEDS, respectively. The latter three modes support the first two. In calibrate mode, the FEMs process antenna data received from known, on-board calibration sources. This allows error compensation to be performed on the data. These errors are caused by drift in the FEM analog circuitry. In command mode, the instrument carries out SEDS commands. These commands originate either locally (with SEDS) or on the ground. In test mode, parts of the Digitizer, data link, Phase-Aligner and CPU are exercised. The results are used by the Controller and/or SEDS to diagnose errors.

Correlator

The Correlator must compute the correlation formula (1) for each of the approximately 8500 possible pairs of FEM signals. It will be implemented using an ASIC being developed at the NASA SERC for VLSI Systems Design at the University of Idaho [4]. This ASIC computes all 1600 pairwise correlations between two sets of 40 signals each (see Figure 4).

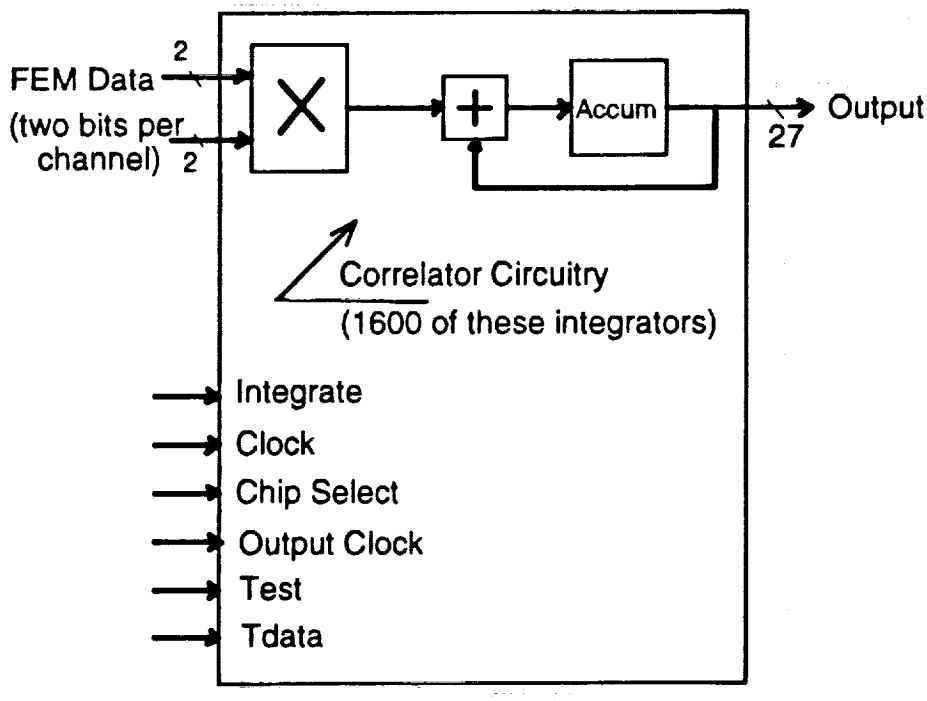


Figure 4: University of Idaho Correlator Chip

The results, each in 25 bits of 2's complement, are clocked out serially under the control of external circuitry. Because the DDS requires approximately 8500 correlations to be performed, six of these ASICs will be needed to implement the correlator.

The design of the third major component of the CPU, the ODF, will now be discussed. Section 4 presents the specifications of the ASIC used in its implementation.

3. Output Data Formatter Design

3.1 General Description

The Output Data Formatter (ODF) is responsible for passing the correlator output data, suitably tagged and including error data, to SEDS for transmission to earth. It must accept the correlator data in parallel, and serialize it for output to SEDS.

The design of the ODF has been partitioned into identical halves, as shown in Figure 5. Each

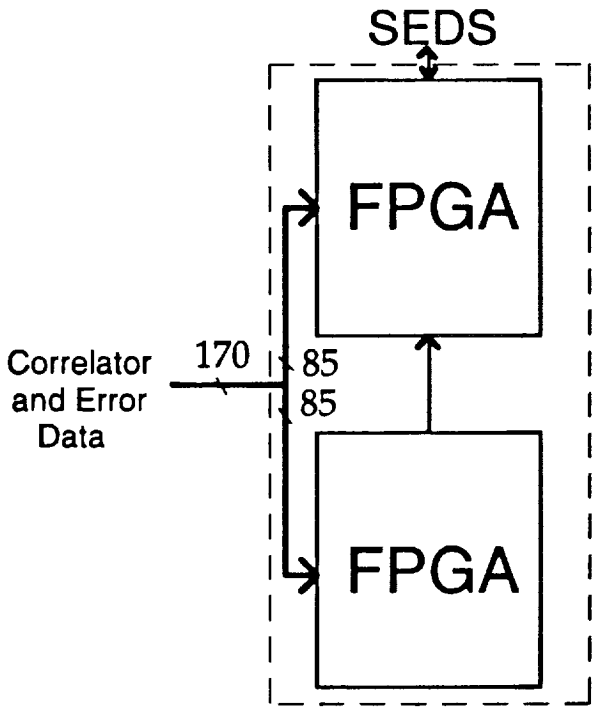


Figure 5: ODF Partitioning

half has been implemented using a Xilinx FPGA. These devices were chosen because they are reprogrammable and allow rapid prototyping and design enhancement. They can be converted to permanent, "hard wired" parts when the complete DDS design has been integrated and tested. The FPGA design was made cascadeable in order to accomodate DDS expansion. In the discussion that follows, the acronym ODF will retain its original meaning, and in addition will sometimes refer to the circuitry residing on either of the identical FPGAs. The intended meaning will be clear from the context.

The inputs and outputs of the ODF FPGAs are shown in Figure 6. The LOAD_ENABLE and

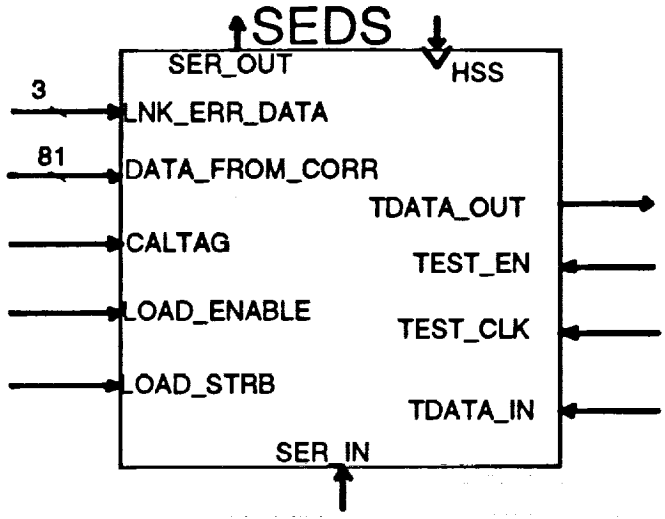


Figure 6: ODF FPGA Inputs and Outputs

LOAD_STRB inputs enable a broadside load of DATA_FROM_CORR, CALTAG and LNK_ERR_DATA into the ODF. DATA_FROM_CORR is an input bus containing the correlator output data. CALTAG is a flag input which when asserted means that the loaded correlation products are for FEM data produced during calibration mode. The LNK_ERR_DATA inputs signify that the correlator data has been corrupted somewhere on the Data Bus. SER_IN and SER_OUT allow cascadability. HSS is used by the SEDS HSS line to strobe out the correlator data for transmission to earth. TEST_EN, TEST_CLK, TDATA_IN and TDATA_OUT are used in test mode, where they allow special diagnostic data to be loaded and circulated in the ODF. This data can then be passed to the controller, where a determination of service readiness can be made.

A simplified block diagram of the ODF FPGA is shown in Figure 7. As can be seen from the figure, it

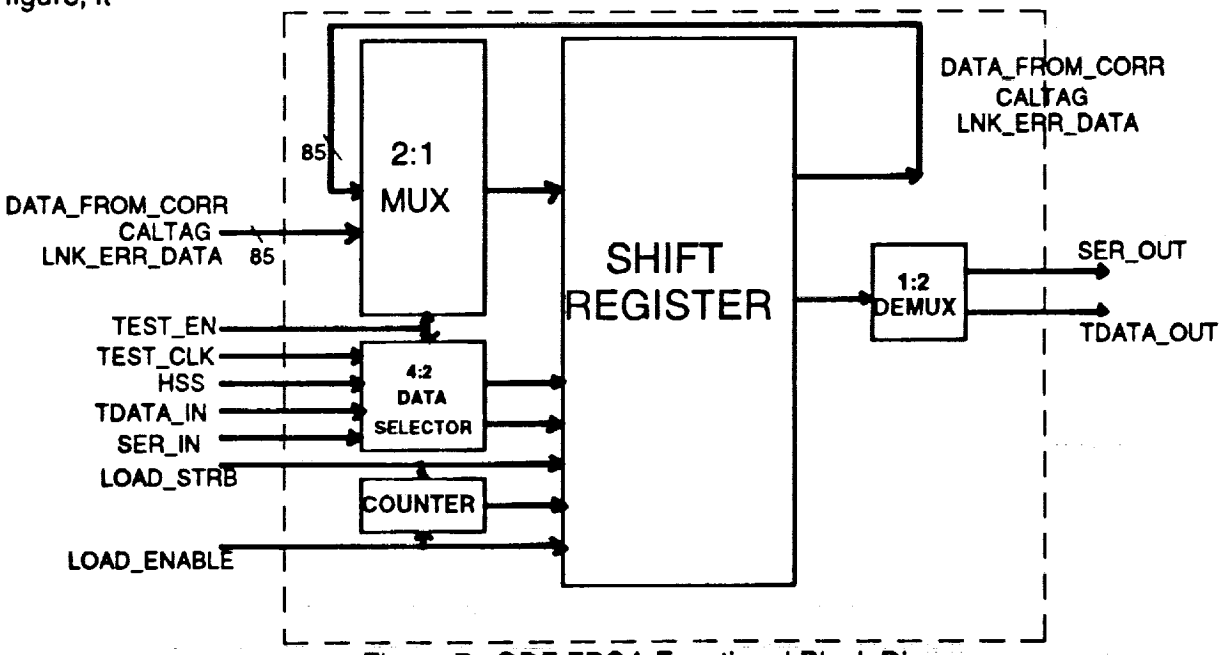


Figure 7: ODF FPGA Functional Block Diagram

is basically a shift register which performs a parallel-to-serial conversion of DATA_FROM_CORR, CALTAG, LNK_ERR_DATA and an internally generated count. The count serves as a data tag to allow determination of which pair of FEMs corresponds to which correlator output product. These four data items are broadside loaded into the shift register by asserting the active-high LOAD_ENABLE input and then strobing the LOAD_STRB (asserted low-to-high) input. This data is then shifted out to SEDS on the SER_OUT line, at a rate controlled by the SEDS handshake line HSS. The 2:1 multiplexer allows the shift register to be parallel-loaded from either the normal source (correlators and controller) or from its own outputs, selectable by the level on the TEST_EN input. This allows a "data loopback" for test mode. The 4:2 data selector allows the TEST_CLK input to be substituted for HSS during test mode. It also allows the serial load data for the shift register to be derived from TDATA_IN. The 1:2 demultiplexer allows the serial output data during test mode to be passed to the controller (rather than SEDS) for diagnosis.

3.2 Circuit Operation

Initialization

Initialization is performed by asserting the Master Reset input. This clears the count and sets all shift register data to zero.

Data Load

All input data (DATA_FROM_CORR, CALTAG and LNK_ERR_DATA) are parallel loaded into the ODF by asserting LOAD_ENABLE and LOAD_STRB. The former is asserted high and must be stable before the low-to-high transition on LOAD_STRB begins. Consult the table of AC electrical specifications in Section 4.1 for timing values. Data is strobed into the ODF during this transition. Also at this time the counter is incremented.

Data Output

All input data and the count are serially shifted out on the SER_OUT output. One bit is shifted out for every low-to-high transition on the HSS input; the shift register is filled with the data present on the SER_IN input.

Test Mode

Test mode is initiated by asserting the LCA Master Reset input (which clears both the shift register and the counter) and then bringing TEST_EN high. This performs functional substitutions of signals TEST_CLK, TDATA_IN and TDATA_OUT for HSS, SER_IN and SER_OUT, respectively. It also establishes a loopback connection from the output of each "non-counter" shift register flip/flop to its input, so that known data can be loaded into the shift register in parallel and will remain unchanged during subsequent parallel loads.

All major functions of the ODF can be tested. A typical test sequence would include:

1. Clocking a known bit sequence through the shift register and back to the controller. This tests the shift capability of the ODF.

2. Clocking a known bit sequence into the shift register and then performing repeated parallel loads. A subsequent shift of the contents to the controller allows the count sequence to be examined and the parallel load function of the device to be validated.

4. Specifications

The schematic diagram of the ODF is shown in Figure 8. The AND and OR gates on the

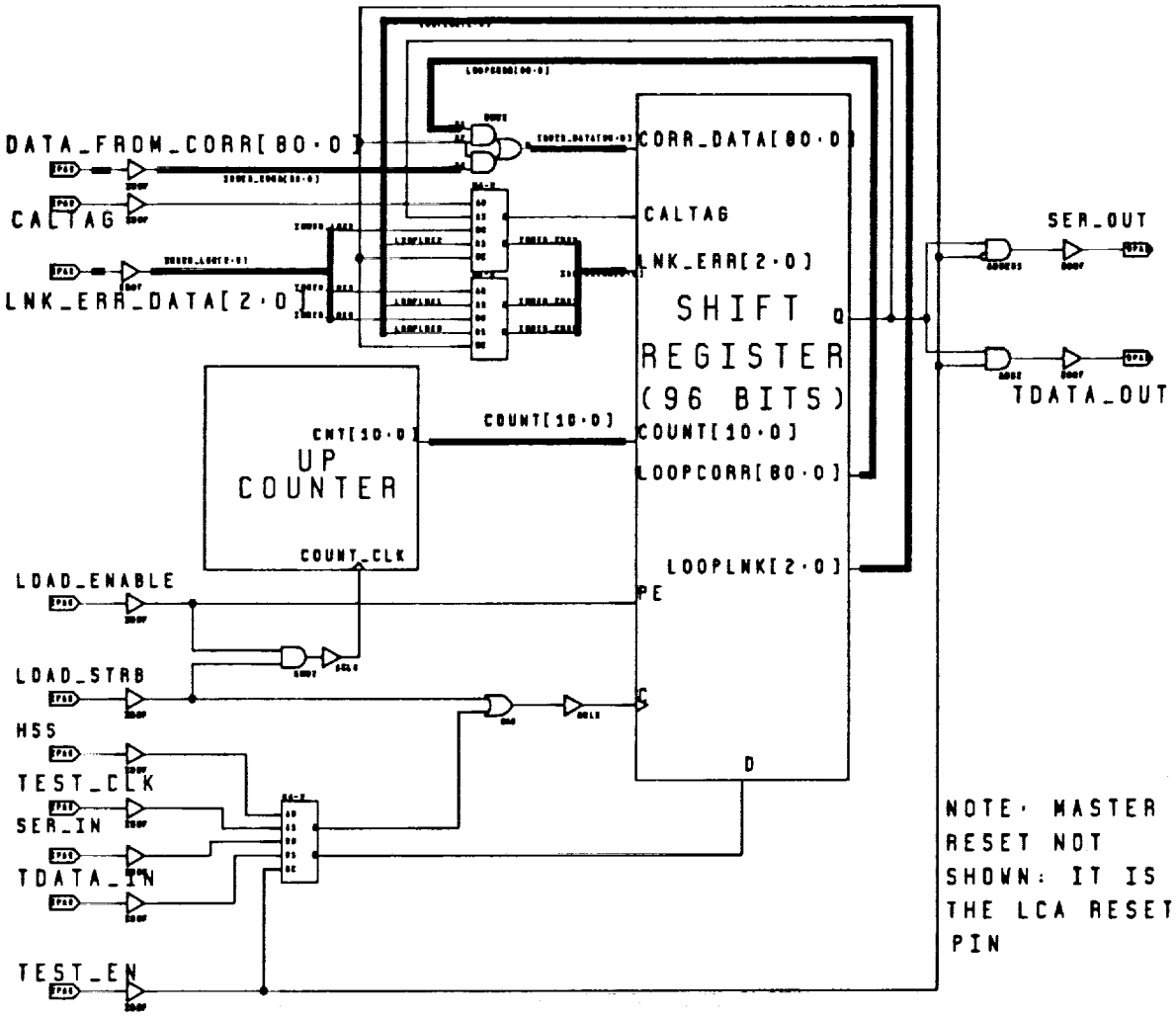


Figure 8: ODF Schematic Diagram

load-control data path are needed to allow the counter to be incremented only when new correlator data is loaded into the shift register. They prevent the counter from being incremented when the data are being shifted. The GCLK and ACLK buffers allow fast driving of the highly-loaded COUNT_CLK and C inputs of the counter and shift register, respectively.

The format of the output data is given in Table 1 below. The first bit shifted out is at the top. Vectors are shifted out with the LSB (bit 0) last.

Table 1: Output Data Format

Data Field Number	Contents
1	CALTAG
2	COUNT[10:0]
3	DATA_FROM_CORR[26:0]
4	LNK_ERR_DATA0
5	DATA_FROM_CORR[53:27]
6	LNK_ERR_DATA1
7	DATA_FROM_CORR[80:54]
8	LNK_ERR_DATA2

4.1 Electrical Specifications

Maximum Absolute Ratings:

Symbol	Description	Value	Units	Conditions
V_{CC}	Supply Voltage	-.5 to +7.0	V	
V_{in}	Input Voltage	-.5 to Vcc + .5	V	
V_{TS}	Tri-state applied voltage	-.5 to Vcc + .5	V	
T_{STG}	Storage Temperature	-65 to +150	Degrees Centigrade	
T_{SOL}	Max. Soldering Temperature	+260	Degrees Centigrade	
T_J	Junction Temperature	+125	Degrees Centigrade	

Recommended Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{CC}	Supply Voltage 0°C to 70°C	4.75	5.25	V	
V_{IHT}	TTL High-Level Input	2.0	Vcc	V	
V_{ILT}	TTL Low-Level Input	0	0.8	V	
V_{IHC}	CMOS High-Level Input	70%	100%	V	
V_{ILC}	CMOS Low-Level Input	0	20%	V	
T_{IN}	Input Transition Time		250	ns	

DC Characteristics Over Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{OH}	High-Level Output Voltage	3.86		V	I_{OH}=-4.0mA V_{CC} min
V_{OL}	Low-Level Output Votage		.32	V	I_{OL}=4.0 mA V_{CC} max
V_{CCPD}	Power-Down Supply Voltage	2.3		V	
I_{CCPD}	Power-Down Supply Current		120	µA	V_{CC} max T max
I_{IL}	Input Leakage Current	-10	+10	µA	
C_{IN}	Input Capacitance		10	pF	Sample Tested

AC Electrical Characteristics Over Operating Conditions:

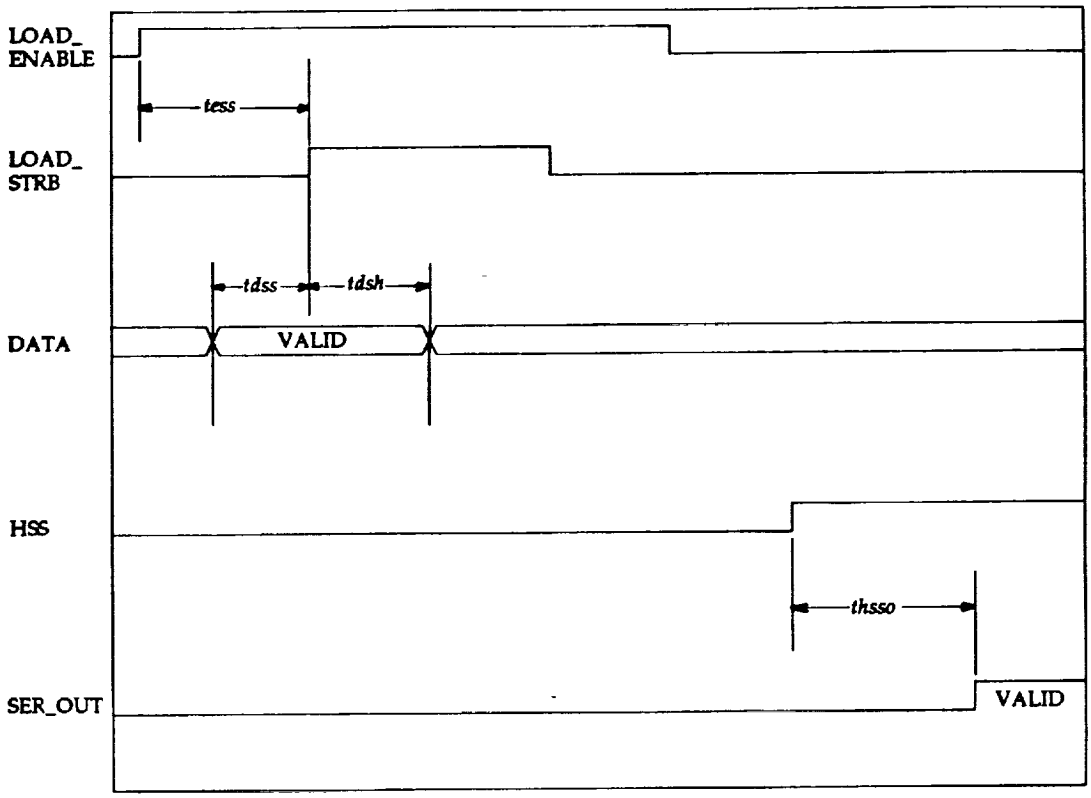
Symbol	Description	Min	Max	Units	Conditions
t_{rise}	Input rise time		250	ns	Worst case[2]
t_{fall}	Input fall time		250	ns	Worst case[2]
t_{ess}	LOAD_ENABLE to LOAD_STRB setup time	24		ns	Worst case[2]
t_{dss}	DATA[1] to LOAD_STRB setup time	12		ns	Worst case[2]
t_{dsh}	DATA[1] to LOAD_STRB hold time	0		ns	Worst case[2]
t_{hsso}	HSS to valid SER_OUT		53	ns	Worst case[2]

Notes:

1) The signal DATA is shorthand for any of DATA_FROM_CORR[80:0], LNK_ERR_DATA[2:0] or CALTAG.

2) 70°C and 4.75 volt supply.

Timing Diagram:



5. Signal Descriptions

5.1 Control Inputs

HSS	Shift clock during non-test mode. SEDS handshake input for reading data from ODF (low-to-high asserted)
LOAD_ENABLE	High prepares ODF for parallel load upon receipt of LOAD_STRB
LOAD_STRB	Initiates parallel load of shift register on low-to-high transition
TEST_CLK	Shift clock during test mode
TEST_EN	High signifies test mode; low signifies SEDS (normal) mode

5.2 Control Outputs

None.

5.3 Data Inputs

CALTAG	High signifies that the correlator data was taken during calibrate mode
DATA_FROM_CORR[80:0]	Correlator data in 3 words of 27 bits each: DATA_FROM_CORR[26:0], [53:27] and [80:54]. MSB is bit with largest index.
LNK_ERR_DATA[2:0]	High signifies that the particular correlator word experienced possible data link corruption; one bit per correlator data word, in order LNK_ERR_DATA0, 1, 2 respective to above
SER_IN	Source of fill bits for shift register during normal mode
TDATA_IN	Source of fill bits for shift register during test mode

5.4 Data Outputs

SER_OUT	Output pin for shifted data during normal mode
TDATA_OUT	Output pin for shifted data during test mode

6. Package Type

The FPGAs are implemented in 132-pin plastic Pin Grid Array (PGA) packages with a speed grade of 125 MHz (part number XC3042PG132-125). The locations of the 94 signal pins can be selected at the time of board layout with minimal impact on circuit timing. The FPGA gate density is 72% (103/144 available CLBs used); the pin density is 98% (94/96 available I/O pins used).

7. References

[1] Levine, D. M., Hilliard, L., et. al., 1990, *Electronically Scanned Thinned Array Radiometer (ESTAR) Earth Probe Concept: An Engineering Feasibility Analysis*, Goddard Space Flight Center, page 9.

[2] Levine, D. M., Good, J. C., 1983, "Aperture Synthesis for Microwave Radiometers in Space", NASA TM 85033, page 1.

[3] *A Digital Data Subsystem Design for an L-band ESTAR Instrument: A Summary of Research Performed in the JOVE Fellowship Program, 6/1/91 thru 11/30/91,* page 5, Appendix A of *ESTAR Digital Data Subsystem Development,* Chren, W. A., Jr., Grand Valley State University, 12/15/91.

[4] *CMOS Digital Correlator: Preliminary Product Specification,* NASA SERC for VLSI Systems Design, University of Idaho, Moscow, Idaho, March 24, 1992.

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11. SUPPLEMENTARY NOTES

William A. Chren, Jr. is currently at Grand Valley State University, Grand Rapids, Michigan. For additional information, contact Larry Hilliard, Code 740.4, NASA GSFC, Greenbelt, Maryland.

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13. ABSTRACT *(Maximum 200 words)*

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