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Design and Qualification of the SEU/TD Radiation Monitor Chip

Martin G. Buehler
Brent R. Blaes
George A. Soli
Nasser Zamani
Kenneth A. Hicks

October 1, 1992

Prepared for

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Massachusetts Institute of Technology
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Pasadena, California

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This report describes the design, fabrication, and testing of the Single-Event Upset/Total Dose (SEU/TD) Radiation Monitor chip. The Radiation Monitor is scheduled to fly on the Mid-Course Space Experiment Satellite (MSX). The Radiation Monitor chip consists of a custon-designed 4-bit SRAM for heavy ion detection and three MOSFETs for monitoring total dose.

In addition the Radiation Monitor chip was tested along with three diagnostic chips: Process Monitor and the Reliability and Fault chips. These chips revealed the quality of the CMOS fabrication process. The SEU/TD Radiation Monitor chip had an initial functional yield of 94.6 percent. Forty-three (43) SEU SRAMs and 14 Total Dose MOSFETs passed the hermeticity and final electrical tests and were delivered to LL.

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EXECUTIVE SUMMARY

This report describes the design, fabrication, and testing of the Single-Event Upset/Total Dose (SEU/TD) Radiation Monitor chip and three diagnostic chips. The Radiation Monitor is scheduled to fly on the Mid-Course Space Experiment Satellite (MSX). The Radiation Monitor chip consists of a custom-designed 4-kbit SRAM for heavy ion detection and three MOSFETs for monitoring total dose. They were fabricated in a 1.6-μm n-well double-level metal CMOS process brokered by MOSIS as run N06J. These chips were fabricated with diagnostic chips on three wafers.

The diagnostic chips are the Process Monitor and the Reliability and Fault chips. The following results were measured from wafers 2, 11, and 12. Metal1 had no breaks in 9.0 meters and no metal bridges in 1.8 meters. Metal2 had no breaks in 7.6 meters and no metal bridges in 1.5 meters. Poly had 1 break in 13.6 meters and 2 poly bridges in 2.7 meters. Oxide pinhole density for n-MOSFETs was 17 defects/cm^2 and for p-MOSFETs was 5 defects/cm^2. Poly, Metal1, and Metal2 step resistances were excellent, being about a few percent. Metal2 electromigration results were excellent with $t_{0.01}$ = 416 years. Standard deviations for p-Poly, n-Poly and n-Diff contact resistances were higher than expected.

To choose superior wafers, it is necessary to acquire data identified by wafer. In addition, the calibration of the Radiation Monitor's SRAM particle response requires accurate intra-chip data. Inter-wafer process monitor MOSFET threshold voltages varied widely from 14 to 37 mV depending on the wafer and overestimated the SRAM threshold variability. In addition results from wafers 2 were distinctly different from wafers 11 and 12. Inter-chip inverter-matrix thresholds were tight and varied from 2 to 8 mV depending on inverter geometry. For the same geometry these inter-chip results agreed closely with SRAM thresholds, which varied by 10 mV.

The 4-kbit SEU SRAM was designed to monitor the heavy ion upset rate. The SRAM has an externally adjustable offset voltage, V_0. The SRAM was irradiated with 0.55 and 1.0 MeV protons and 4.7 MeV alpha particles. From an analysis of the SRAM particle upset rate, it was determined that the overlayer thickness is 4.32 μm and collection depth is 6.64 μm. Using this data a LET = 2.88 MeV·cm^2/mg is estimated for the MSX operating conditions of V_0 = 5 V.

The total dose MOSFETs are a calibrator p-MOSFET, a floating gate p-MOSFET, and a standard n-MOSFET. The calibrator and standard MOSFETs monitor total dose via the threshold shift due to radiation-induced oxide charging. The floating gate MOSFET monitors dose via the channel conductance shift of the floating gate p-MOSFET due to the accumulation of gate charge.

The SEU/TD Radiation Monitor chip had an initial functional yield of 94.6 percent. SRAM electrical tests consisted of power up, walking ones, checker board, access time, and standby power tests. The chips were given a static powered burn-in for 24 hours at 125°C. During electrical tests, various failure modes were detected including stuck memory cells, large chip stand-by leakage, and large transistor leakage. It should be noted that the total dose MOSFETs have unprotected gates and 29 MOSFETs were lost during the hermetic seal lidding operation. It appears that normal ESD prevention practices were not sufficient to protect MOSFETs with unprotected gates. Forty-three (43) SEU SRAMs and 14 Total Dose MOSFETs passed the hermeticity and final electrical tests and were delivered to LL.

ABSTRACT

This report describes the design, fabrication, and testing of the Single-Event Upset/Total Dose (SEU/TD) Radiation Monitor chip. The Radiation Monitor is scheduled to fly on the Mid-Course Space Experiment Satellite (MSX). The Radiation Monitor chip consists of a custom-designed 4-kbit SRAM for heavy ion detection and three MOSFETs for monitoring total dose.

In addition the Radiation Monitor chip was tested along with three diagnostic chips: Process Monitor and the Reliability and Fault chips. These chips revealed the quality of the CMOS fabrication process. The SEU/TD Radiation Monitor chip had an initial functional yield of 94.6 percent. Forty-three (43) SEU SRAMs and 14 Total Dose MOSFETs passed the hermeticity and final electrical tests and were delivered to LL.

ACKNOWLEDGMENTS

The chips described in this report were fabricated by commercial CMOS foundries through the efforts of the University of Southern California, Information Sciences Institute, Metal-Oxide-Silicon Implementation Service (MOSIS). The efforts of Vincent Sferrino, Lincoln Laboratory, in providing the opportunity to fly the SEU/TD Radiation Monitor chip and in serving as the interface to the satellite system are gratefully acknowledged. Finally the authors wish to recognize the enthusiasm of Paul Robinson in encouraging the use of his FET probe as a radiation monitor.

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Design and Qualification of the SEU/TD Radiation Monitor Chip

1.0 INTRODUCTION

This document describes the development of a Single-Event Upset (SEU) and Total Dose (TD) Radiation Monitor chip which was delivered to the Massachusetts Institute of Technology's Lincoln Laboratory (LL) by the Jet Propulsion Laboratory (JPL). This chip is scheduled to be flown on the Mid-Course Space Experiment Satellite (MSX) scheduled to launch in 1992.

This chip was developed by JPL's VLSI Technology Group as part of an on-going program devoted to the development of qualification techniques for VLSI circuits. This chip provides a means of establishing the connection between ground test results and space test results. The Group has developed several chips for flight test. The first test chip was delivered in March of 1986. Twelve test chips were delivered to the Air Force Geophysics Laboratory (AFGL) and were included on the Combined Release and Radiation Effects Satellite (CRRES) launched July 25, 1990 [1,2].

Currently a radiation monitor (RADMON) is being developed for flight on the Space Technology Research Vehicle (STRV), which is scheduled for launch in December 1993. It consists of a total dose monitor and a 14 chip, 3-bin particle spectrometer. Our long range goal is to develop the RADMON so that it can serve as a SEU/TD Radiation Monitor on a spacecraft to alert the control system to radiation hazards and to explain radiation-induced system upsets. In addition the data accumulated from these chips will allow mapping of the proton and cosmic-ray environments.

1.1 Overview

The objective of this task is to develop a custom radiation monitor with the same (CMOS) technology used to fabricate the circuitry used in the spaceborne computers and signal processors. Thus the results observed from the radiation monitor can be directly related to the functionality of the spaceborne electronics. The SEU/TD Radiation Monitor will be used to determine the total accumulated dose and SEU rates. These results will be compared to the performance of the signal processor chips developed by Lincoln Laboratory.

The space radiation effects of concern to modern microcircuits are Single-Event Upsets (SEUs) and Total Ionizing Dose (TD). In the SEU effect, cosmic rays and high energy protons, that undergo electronic reactions with the integrated circuits, deposit sufficient charge in memory cells and latches to flip bits and corrupt data. Such events do not induce any physical damage and thus are nondestructive. On the other hand, in the TD effect, gate oxides are charged, which is a permanent change. This shifts transistor threshold voltages and reduces the channel mobility. A change in these parameters degrades the performance of CMOS integrated circuits (ICs) by changing the propagation delay [3].

A photomicrograph of the 28-pin chip is shown in Figure 1 and the pin numbers are listed in Table 1. A block diagram of the chip is shown in Figure 2, where it is seen that the chip contains the following devices: (a) SEU SRAM, (b) standard n-MOSFET, (c) calibrator p-MOSFET, and (d) floating gate p-MOSFET.

The floating gate MOSFET experiences channel-conductance shifts, which are due to radiation-induced gate charge. To monitor total ionizing dose effects, floating gate drain current is measured and compared to the drain current from a calibrator MOSFET so the radiation-induced floating gate charge can be determined.

Table 1. Pinout of the SEU/TD chip.

PIN DESCRIPTION	PIN DESIGNATION	PIN NO.
Power: VDD = 5 V	VDD	5
Ground: 0 V	GND	11
Offset Voltage: Vo = 5 V	Vo	4
SRAM Control:	Ebar	18
	Wbar	19
SRAM Data In:	D0	20
	D1	22
	D2	24
	D3	27
SRAM Data Out:	Q0	21
	Q1	23
	Q2	25
	Q3	28
SRAM Address:	A0	3
	A1	2
	A2	1
	A3	26
	A4	12
	A5	13
	A6	14
	A7	17
	A8	16
	A9	15
n-MOSFET Standard Gate	Gn	9
n-MOSFET Standard Drain	Dn	10
p-MOSFET Calibrator Gate	Gp	7
p-MOSFET Calibrator Drain	Dp	6
p-MOSFET Floating Gate Drain	Dpfloat	8

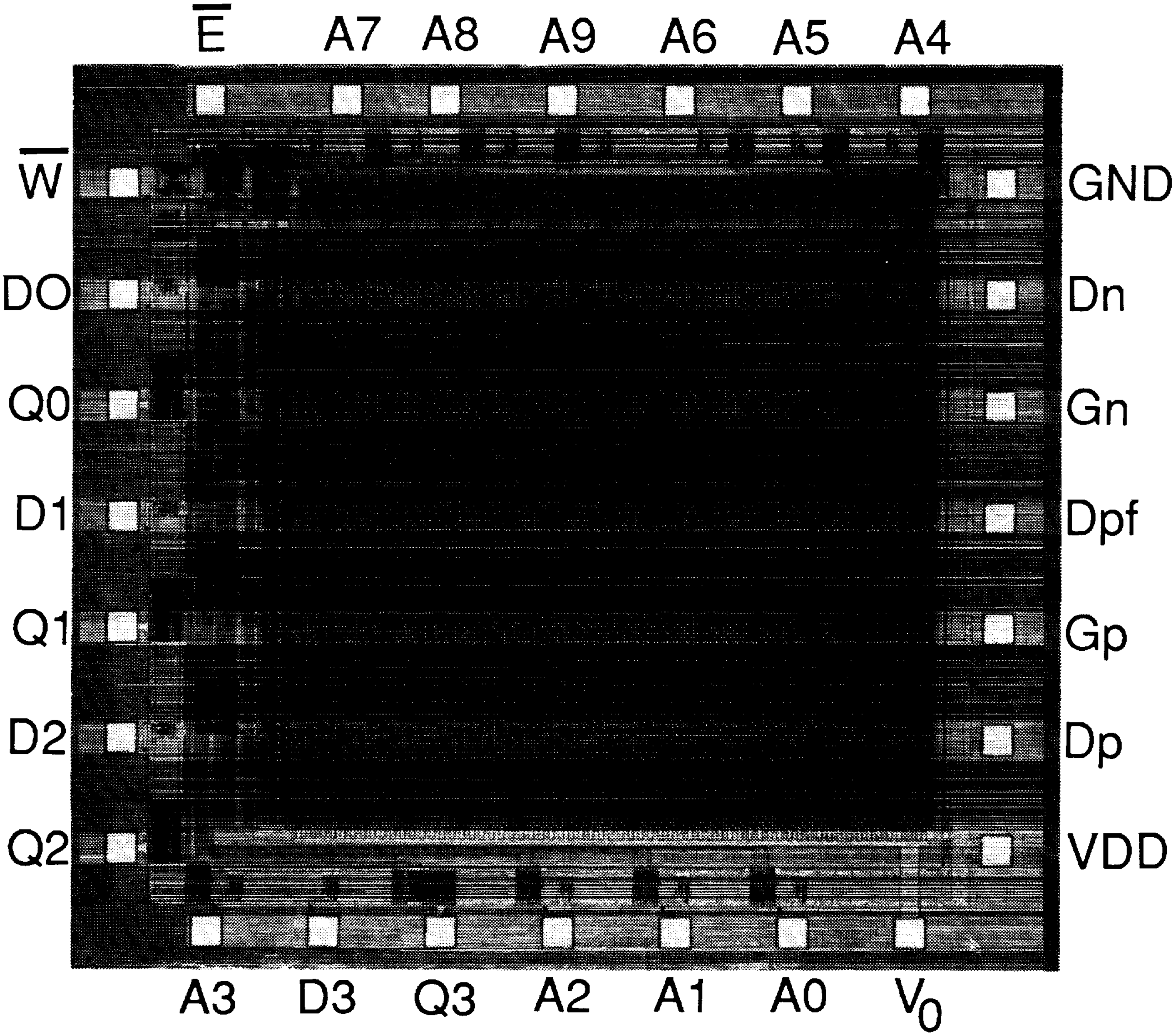


Figure 1. Photomicrograph of SEU/TD radiation monitor chip which is 3.12 mm x 3.29 mm.

The SRAM is a classical six-transistor cell that has been customized as indicated by the cross-sectional diagram shown in Figure 3. The cell was modified by adding an offset voltage, V_0, to one side of the memory cell. This allows the sensitivity of the cell-to-particle upset to be adjusted externally. In addition the drain, Dn2, was enlarged to increase the cell cross-section-to-particle capture. In the LL spacecraft implementation, V_0 is connected to VDD in order to simplify the drive circuitry. Thus the SRAM sensitivity is fixed so that the cells can be upset by particles with a LET (Linear Energy Transfer) in excess of 2.88 $MeV \cdot cm^2/mg$. The V_0 was used in ground tests, however, to select SRAMs with tight initial upset characteristics and to calibrate the cell response with proton and alpha particle radiation.

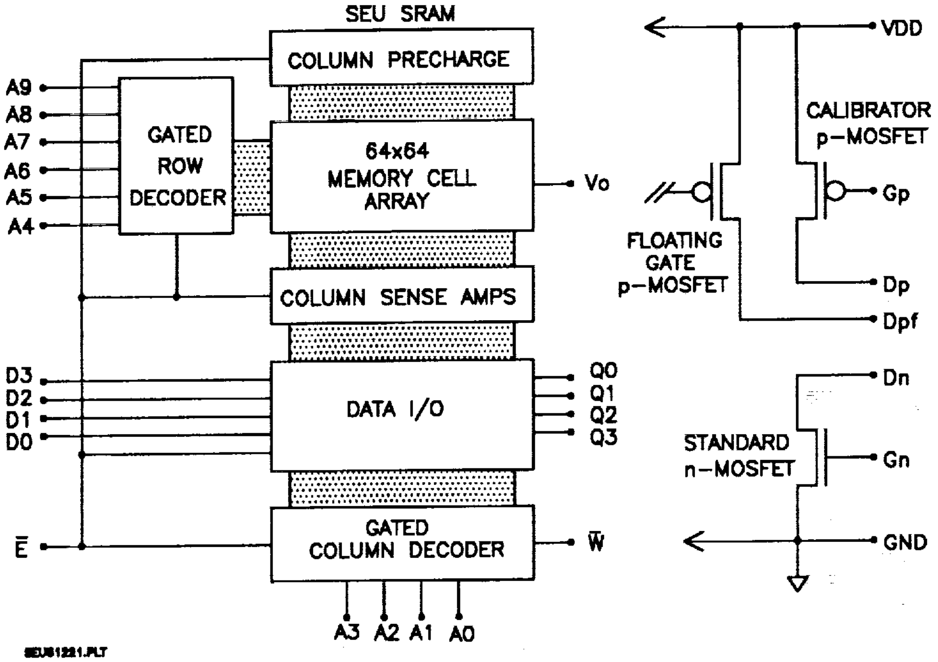

SEU SRAM
COLUMN PRECHARGE
A9
A8
A7
A6
A5
A4
GATED ROW DECODER
64x64 MEMORY CELL ARRAY
Vo
COLUMN SENSE AMPS
D3
D2
D1
D0
DATA I/O
Q0
Q1
Q2
Q3
E
GATED COLUMN DECODER
W
A3 A2 A1 A0
SEU1221.PLT
VDD
CALIBRATOR p-MOSFET
Gp
FLOATING GATE p-MOSFET
Dp
Dpf
Dn
STANDARD n-MOSFET
Gn
GND

Figure 2. Schematic diagram for SEU/TD chip showing the four devices.

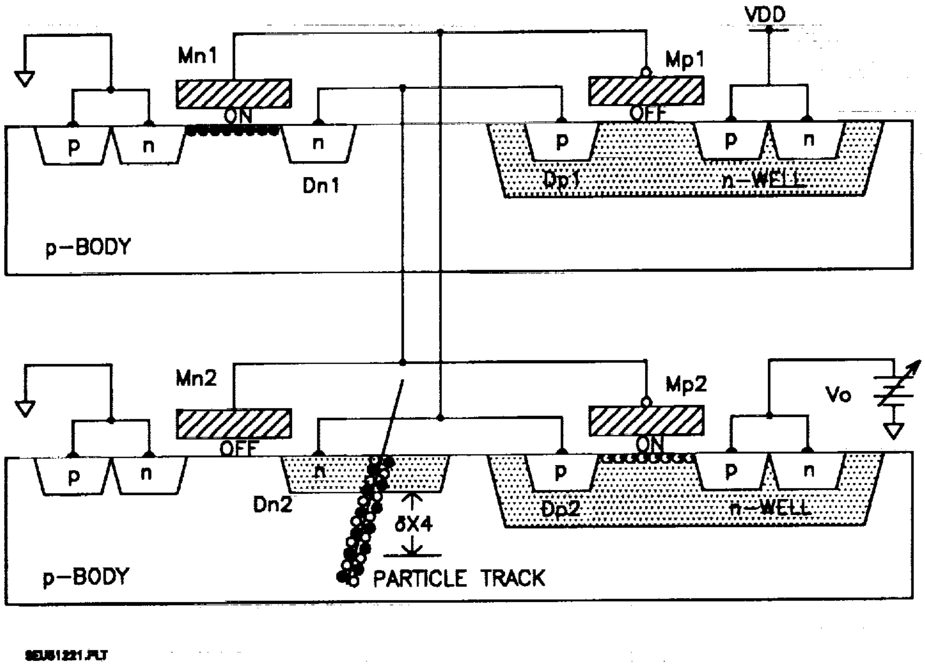

VDD
Mn1
ON
Mp1
OFF
p
n
n
Dn1
p
Dp1
p
n
n-WELL
p-BODY
Mn2
OFF
Mp2
ON
Vo
p
n
n
Dn2
δX4
p
Dp2
p
n
n-WELL
p-BODY
PARTICLE TRACK
SEU1221.PLT

Figure 3. Cross section of SEU SRAM showing a particle track through diode Dn2 which can initiate a bit flip. The n-MOSFETs, Mn1 and Mn2, and p-MOSFETs, Mp1 and Mp2, are also shown in the circuit schematic in Figure 9.

1.2 Scope of Work

This chip was fabricated through MOSIS (Metal Oxide Silicon Implementation Service) in a 1.6-μm double-level metal n-well CMOS process where the p-MOSFETs substrate was doped to $5x10^{14}$ cm^{-3}. The chips were fabricated on 4-inch diameter wafers which contained about 25 complete chips. JPL received three wafers from MOSIS. These wafers were scribed and assembled into 75 packages. Six unscreened parts were delivered to LL for prototyping purposes. Then 50 were hermetically sealed, screened, and 43 parts were delivered to LL. The following scope of work was established between JPL and LL.

1) JPL will design the SEU/TD Radiation Monitor, submit the design to a CMOS foundry for fabrication, and package in 75, 600-mil wide, 28-pin ceramic Dual In-line Packages (DIPs) with lids.

2) JPL will perform initial functional testing of the monitor and deliver 6 unscreened and unlidded parts to LL.

3) JPL will see that the packaged parts are hermetically sealed and will perform screening tests, which are a subset of MIL-STD-883C screening procedures for Class-B devices.

4) JPL will perform final functional testing, monitor grading, and conduct a pre-shipment review.

5) JPL will deliver up to 50 screened parts to LL.

6) JPL will deliver test documentation to LL.

7) JPL will calibrate the monitor as a particle detector.

8) LL will provide JPL with all ground test and satellite data acquired from the monitor in a format convenient for JPL analysis.

9) LL will provide JPL with specific satellite orbital information to allow JPL to correlate the radiation monitor data to known space environmental data.

It should be noted that only 43 screened parts were delivered to LL when 50 were requested. The number of 43 was an acceptable number since only one part was intended for flight. The remaining parts were used by LL for ground radiation tests.

2.0 DIAGNOSTIC TEST CHIPS

A comprehensive set of diagnostic test structures was included with the SEU/TD Radiation Monitor chip as seen in Figure 4. These chips were included on the MOSIS N06J fabrication run and were used to analyze the quality of the fabrication run. As seen in the figure, the diagnostic test chips consist of Process Monitors PM_1 and PM_2, Reliability Chip, the Fault Chip, the Total Ionizing Dose (TD) Chip, and the Single-Event-Upset (SEU) chip. In order to reduce the cost of the fabrication, this run was shared with an ASIC chip and a standard cell (STD CELL) chip. A brief description follows of the test structures and their test results.

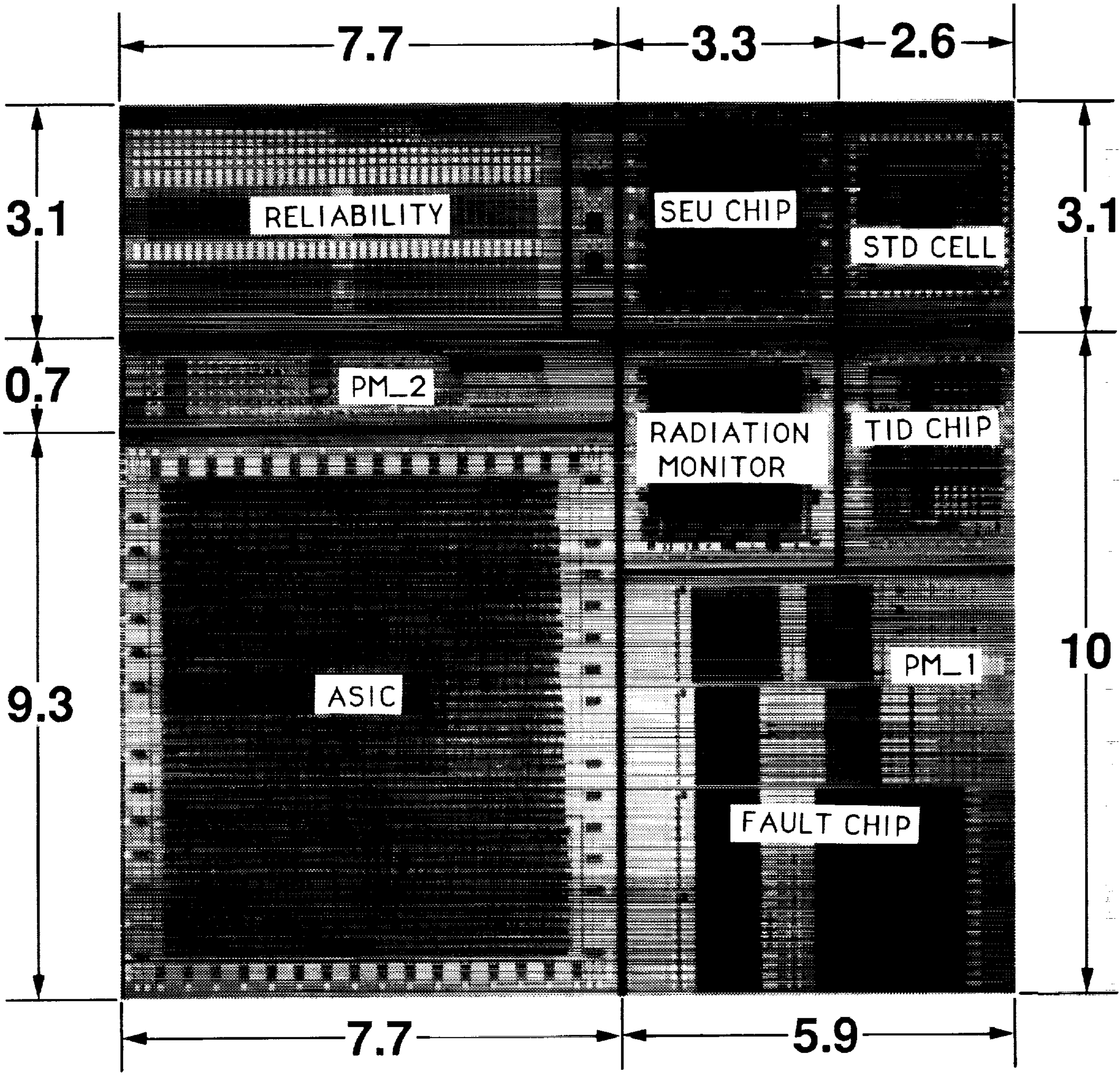

7.7
3.3
2.6
3.1
0.7
9.3
3.1
10
7.7
5.9
RELIABILITY
SEU CHIP
STD CELL
PM_2
RADIATION MONITOR
TID CHIP
ASIC
PM_1
FAULT CHIP

Figure 4. Chips fabricated on MOSIS run N06J. Dimensions in mm.

2.1 Fault Chip

The fault chip consists of a set of test structures which provide statistics on the VLSI defect densities and distributions of component characteristics. The defect densities measured on the fault chip are (a) gate oxide pinholes, (b) Poly-Metal pinholes, (c) Poly-Poly shorts, (d) Metal1-Metal1 shorts, (e) Metal2-Metal2 shorts, (f) Poly wire opens, (g) Metal1 wire opens, and (h) Metal2 wire opens.

A summary of the results obtained from fault chip defect density test structures is given in Table 2. The most troublesome defect is the gate oxide defect. An analysis for the gate oxide defect density follows from the Poisson yield expression:

$$(1) \quad Y = \exp(-DA)$$

where D is the defect density and A is the gate oxide area. The yield can be expressed in terms of the failure rate, F or $Y = 1-F$. For very small failure rates, $D = F/A$. In obtaining this relationship, the approximation $\ln(1-x) \approx -x$ was used. In calculating the gate oxide area, A, the dimensions 1.6 μm by 2.4 μm were used. The defect density for n-pinholes is $D_n = 17$ defects/cm^2 and for p-pinholes $D_p = 5$ defects/cm^2.

These pinhole densities are typical of values previously obtained from MOSIS fabrication runs as seen in Table 3. Such defects should be caught at test time and should represent only a yield loss. Overall the results from the defect density test structures are typical of other CMOS fabrication runs we have analyzed and are acceptable for this application.

The other test structures found on the fault chip are the matrix test structures. These structures are used to assess parameter variability, which is an indicator of the local control obtained in the fabrication process. The structures are: (a) Linewidth/Step Matrix [4], (b) Contact Matrix [5], and (c) Inverter Matrix [6]. The results are listed in Table 4.

A discussion of these results leads to the following conclusions. Results from the Linewidth/Step Matrix reveal that step-coverages are acceptable for the step; resistance percentage is satisfactorily low, being less than 3 percent. Results from the Contact Matrix indicate that the contact resistance standard deviations are high for Metal1-p-Poly, Metal1-n-Poly, and Metal1-n-Diff. Although these standard deviations are high, they are not judged to compromise the devices fabricated on this run.

The standard deviations for the Inverter Matrix [4] are of interest because they are directly related to the variations seen in the offset voltages of the SEU SRAM. The inverter threshold voltage is given by:

$$(2) \quad VT_{inv} = \frac{VDD + VT_n\sqrt{\beta_r} - VT_p}{1 + \sqrt{\beta_r}}$$

where VT_n is the n-MOSFET threshold voltage, and VT_p is the magnitude of the p-MOSFET threshold voltage. The Beta factor is:

$$(3)\quad \beta_r = \frac{\beta_n}{\beta_p} = \frac{KP_n(W_n - \Delta W_n)(L_p - \Delta L_p)}{KP_p(W_p - \Delta W_p)(L_n - \Delta L_n)}$$

where $KP = \mu_o C_{ox}$, μ_o is the channel mobility, C_o is the gate oxide capacitance/area, W and L are the as-drawn channel width and channel length, respectively, and ΔW and ΔL are the deviations from the as-drawn values. The inverter threshold equation is plotted in Figure 5 and shows that for $\beta_r \rightarrow 0$, $VT_{inv} = VDD - VT_p$ and for $\beta_r \rightarrow \infty$, $VT_{inv} = VT_n$.

A useful parameter is the geometry factor, G_{ro}, which is calculated using as-drawn MOSFET dimensions:

$G_{ro} = W_n L_p/(W_p L_n)$. The variance of the inverter threshold voltage is:

$$(4)\quad VT_{inv\sigma}{}^2 = \frac{VT_{p\sigma}{}^2}{(1 + \sqrt{\beta_r})^2} + \frac{\beta_r VT_{n\sigma}{}^2}{(1 + \sqrt{\beta_r})^2} + \frac{\beta_r G(VDD - VT_n - VT_p)^2}{4(1 + \sqrt{\beta_r})^4}$$

where

$$(5)\quad G = \frac{W_{n\sigma}{}^2}{W_{en}{}^2} + \frac{W_{p\sigma}{}^2}{W_{ep}{}^2} + \frac{L_{n\sigma}{}^2}{L_{en}{}^2} + \frac{L_{p\sigma}{}^2}{L_{ep}{}^2}$$

where $W_e = W - \Delta W$ and $L_e = L - \Delta L$. These equations show that for $\beta_r = 0$, $VT_{inv} = (VDD - VT_{p\mu}) \pm VT_{p\sigma}$ and for $\beta_r = \infty$, $VT_{inv} = VT_{n\mu} \pm VT_{n\sigma}$. Thus from Table 4, the standard deviation for $VT_{p\sigma} = 6$ mV and $VT_{n\sigma} = 3$ mV. Also the deviation for the "FAT FET" inverter is 2 mV and this indicates good local control of the ion implantation which controls the threshold voltages. These values are typical of those seen on previous MOSIS runs.

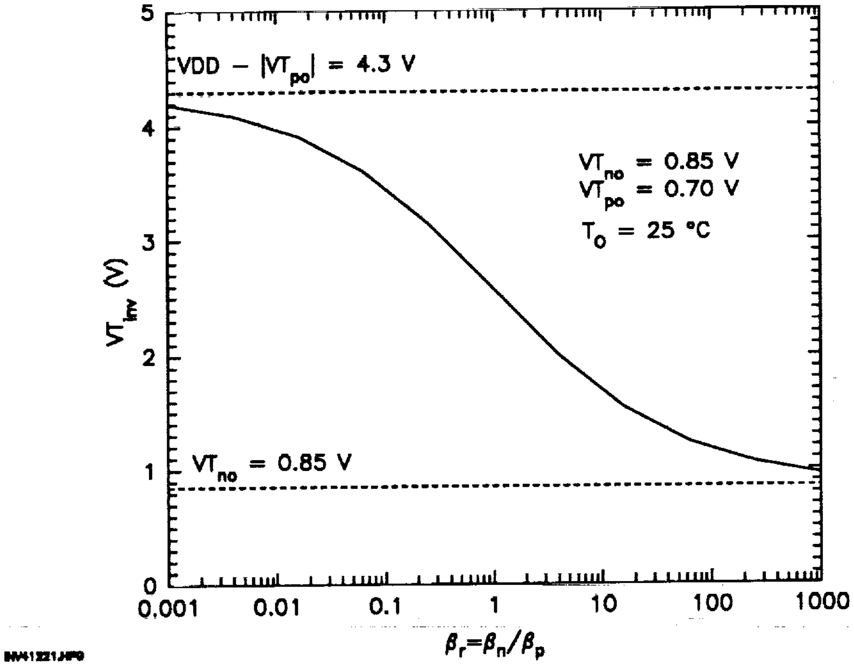


Figure 5. Inverter threshold voltage dependence on the MOSFET geometry factor β_r.

Table 2. Defect density test structure test results

TEST STRUCTURE	DEFECT TYPE	NUMBER DEFECTS	LENGTH meters	NO. MOSFETs MEASURED
COMB RESISTOR	METAL1-METAL1 SHORTS	0	1.8	
	METAL2-METAL2 SHORTS	1	1.5	
	POLY-POLY SHORTS	2	2.7	
SERPENTINE RESISTOR	METAL1 WIRE OPENS	0	9.0	
	METAL2 WIRE OPENS	0	7.6	
	POLY WIRE OPENS	1	13.6	
p-PINHOLE CAPACITOR	METAL1-POLY SHORT	1	75.2	
	GATE OXIDE PINHOLES	3		15.6×10^6 p-MOSFETs
n-PINHOLE CAPACITOR	METAL1-POLY SHORT	0	75.2	
	GATE OXIDE PINHOLES	10		15.6×10^6 n-MOSFETs

Table 3. CMOS gate-oxide pinhole data base.

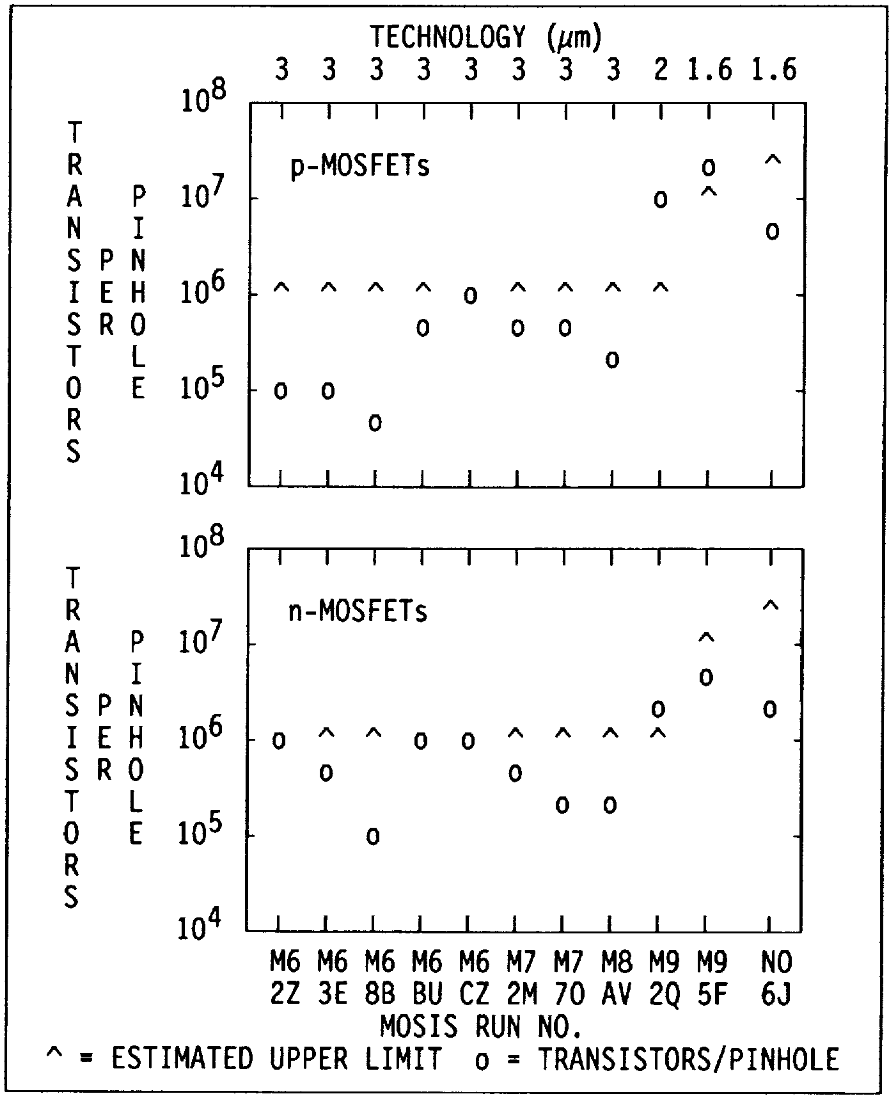


Table 4. Matrix test structure results.

TEST STRUCTURE	UNITS	MEAN±STDEV		TEST POINTS
SIX-TERMINAL CONTACT RESISTOR MATRIX			STDEV(%)	
CONTACT SIZE = 1.6-µmx1.6-µm				
METAL1-p-POLY	Ω	16.3±1.63	10.0	3884
METAL1-n-POLY	Ω	6.1±0.73	11.9	3936
METAL1-p-DIFF	Ω	17.5±0.27	1.5	3992
METAL1-n-DIFF	Ω	25.9±2.58	10.0	3882
LINEWIDTH/STEP MATRIX			STEP RESISTANCE(%)	
METAL1 LINEWIDTH DOWN 2.4 µm	µm	2.27±0.032		1440
METAL1 LINEWIDTH UP 2.4 µm	µm	2.39±0.038		1438
METAL1 LINEWIDTH STEP 2.4 µm	µm	2.26±0.065	1.57	1404
METAL2 LINEWIDTH DOWN 2.4 µm	µm	2.27±0.038		1440
METAL2 LINEWIDTH UP 2.4 µm	µm	2.36±0.043		1440
METAL2 LINEWIDTH STEP 2.4 µm	µm	2.24±0.045	1.69	1440
p-POLY LINEWIDTH DOWN 1.6 µm	µm	1.36±0.036		1440
p-POLY LINEWIDTH UP 1.6 µm	µm	1.39±0.036		1440
p-POLY LINEWIDTH STEP 1.6 µm	µm	1.32±0.039	2.05	1440
INVERTER MATRIX				
W_n L_n W_p L_p G_{ro}		$VT_{inv\mu}$±$VT_{inv\sigma}$		
2.4 6.4 9.6 1.6 µm 0.0625	V	3.50±0.006	◄ $VT_{p\sigma}$=6 mV	44
2.4 1.6 9.6 1.6 µm 0.2500	V	2.86±0.008		132
2.4 6.4 2.4 1.6 µm 0.2500	V	2.76±0.008		44
9.6 6.4 9.6 6.4 µm 1.0000	V	2.08±0.002	◄ FAT FETs	88
2.4 1.6 2.4 1.6 µm 1.0000	V	2.00±0.008		88
2.4 1.6 2.4 6.4 µm 4.0000	V	1.42±0.006		22
9.6 1.6 2.4 1.6 µm 4.0000	V	1.42±0.004		22
9.6 1.6 2.4 6.4 µm 16.0000	V	1.09±0.003	◄ $VT_{n\sigma}$= 3mV	44

2.2 Process Monitor

The JPL process monitor contains split-cross bridge resistors for measuring sheet resistance and linewidth of various layers, contact resistors, circular MOSFET capacitors, MOSFETs and inverters. The process monitor design and data acquisition are described in a JPL Publication [7]. Results from the process monitor are listed in Tables 5 and 6. These results were taken from wafers 2, 11, and 12. The results confirm the observations from the fault chip that the contact resistances for the poly and n-diff contacts have a large spread.

Table 5. Process monitor test results (Part 1).

TEST STRUCTURE LAYER DIMENSIONS	UNITS	MEAN±STDEV
SHEET RESISTANCE		
SAMPLE SIZE = 78		
p-POLY 1.6 µm	Ω/SQ	27.9±1.87
n-POLY 1.6 µm	Ω/SQ	25.6±1.21
p-DIFF 2.4 µm	Ω/SQ	134.7±3.88
n-DIFF 2.4 µm	Ω/SQ	66.6±1.93
METAL1 2.4 µm	mΩ/SQ	55.0±1.1
METAL2 2.4 µm	mΩ/SQ	29.9±1.5
LINEWIDTH		
SAMPLE SIZE = 78		
p-POLY 1.6 µm	µm	1.29±0.03
n-POLY 1.6 µm	µm	1.24±0.03
p-DIFF 2.4 µm	µm	2.04±0.05
n-DIFF 2.4 µm	µm	2.20±0.04
METAL1 2.4 µm	µm	2.37±0.07
METAL2 2.4 µm	µm	2.39±0.25
CONTACT RESISTANCE		
1.6-µmx1.6-µm, SAMPLE SIZE = 79		
METAL1-p-POLY	Ω	16.9±3.39
METAL1-n-POLY	Ω	6.6±1.12
METAL1-p-DIFF	Ω	19.4±1.60
METAL1-n-DIFF	Ω	31.2±6.48
METAL1-METAL2	mΩ	36.0±4.8
TWO CIRCULAR MOSFET CAPACITORS		
R=28.8 µm, ΔR=3.2, 12.8 µm, SAMPLE SIZE = 78		
n-OXIDE THICKNESS	nm	24.800±0.31
n-OXIDE CAPACITANCE	fF/µm^{2}	1.390±0.02
n-OVER-LAP CAPACITANCE	fF/µm	0.085±0.0118
n-ΔL	µm	0.495±0.043
p-OXIDE THICKNESS	nm	25.500±1.19
p-OXIDE CAPACITANCE	fF/µm^{2}	1.358±0.049
p-OVER-LAP CAPACITANCE	fF/µm	0.095±0.0141
p-ΔL	µm	0.475±0.160

The MOSFET threshold voltages for Wafers 2, 11, and 12 are shown in Figures 6 and 7 and the results of a least squares fit to the data are given in Table 7. These figures illustrate that Wafer 2 has a different threshold voltage distribution than Wafers 11 and 12. The variation in threshold voltage is important, for it is the main factor in setting the sensitivity of the SRAMs to particle upset. This correlation will be shown in a later section. Because of wafer-to-wafer variations, it is important to acquire data on a wafer-by-wafer basis in order to identify wafers with uniform characteristics.

Table 6. Process monitor test results (Part 2).

TEST STRUCTURE LAYER DIMENSIONS	UNITS	MEAN±STDEV
FOUR MOSFETs: SAMPLE SIZE = 33 quartets of MOSFETs		
Wn/Ln=2.4/1.6, 7.2/1.6, 7.2/4.8, 2.4/4.8 $\mu m/\mu m$		
$KP_n=\mu_0 C_{ox}$	$\mu A/V^2$	74.73±2.173
$\Delta W_n=W-\Delta W$	μm	0.485±0.074
$\Delta L_n=L-\Delta L$	μm	0.409±0.064
VT_n	V	0.844±0.031
$2\varphi_{fn}$	V	0.731±0.003
γ_{on}	$\sqrt{V}$	0.592±0.019
δ_{on}	$\sqrt{V}$	0.252±0.022
θ_{on}	1/V	0.062±0.021
θ_{bon}	1/V	-0.008±0.021
η_{on}	1/V	-0.051±0.033
ϵ_{on}	1/V	0.083±0.030
λ_{on}	1/V	0.006±0.003
M_{on}	unitless	0.783±0.059
FOUR MOSFETs: SAMPLE SIZE = 70 quartets of MOSFETs		
Wp/Lp=2.4/1.6, 7.2/1.6, 7.2/4.8, 2.4/4.8 $\mu m/\mu m$		
$KP_p=\mu_0 C_{ox}$	$\mu A/V^2$	28.80±0.566
$\Delta W_p=W-\Delta W$	μm	0.780±0.035
$\Delta L_p=L-\Delta L$	μm	0.139±0.028
VT_p	V	0.684±0.025
$2\varphi_{fp}$	V	0.717±0.002
γ_{op}	$\sqrt{V}$	0.530±0.009
δ_{op}	$\sqrt{V}$	0.235±0.008
θ_{op}	1/V	0.132±0.005
θ_{bop}	1/V	-0.089±0.002
η_{op}	1/V	0.021±0.026
ϵ_{op}	1/V	0.058±0.005
λ_{op}	1/V	0.003±0.001
M_{op}	unitless	1.062±0.047
INVERTER: SAMPLE SIZE = 78		
Wn/Ln=2.4/1.6 $\mu m/\mu m$, Wp/Lp=7.2/1.6 $\mu m/\mu m$		
THRESHOLD	V	1.82±0.02
GAIN	-	15.04±0.44
VHIGH	V	5.00±0.00
VLOW	μV	38.00±49.50
NOISE MARGIN	V	2.19±0.02

Table 7. Threshold voltage values for Wafers 3, 11, and 12.

WAFER	MOSFET	$VT_{\mu} \pm VT_{\sigma}$
2	n	0.786±0.037
11	n	0.722±0.014
12	n	0.708±0.022
2	p	0.662±0.023
11	p	0.696±0.029
12	p	0.700±0.036

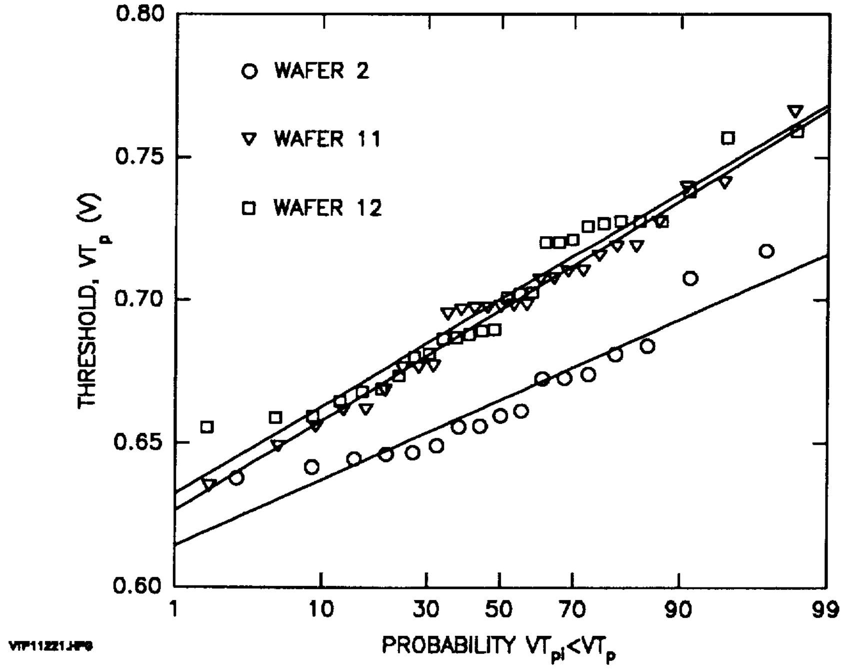


Figure 6. Distribution of p-MOSFET threshold voltage for Wafers 2, 11, and 12.

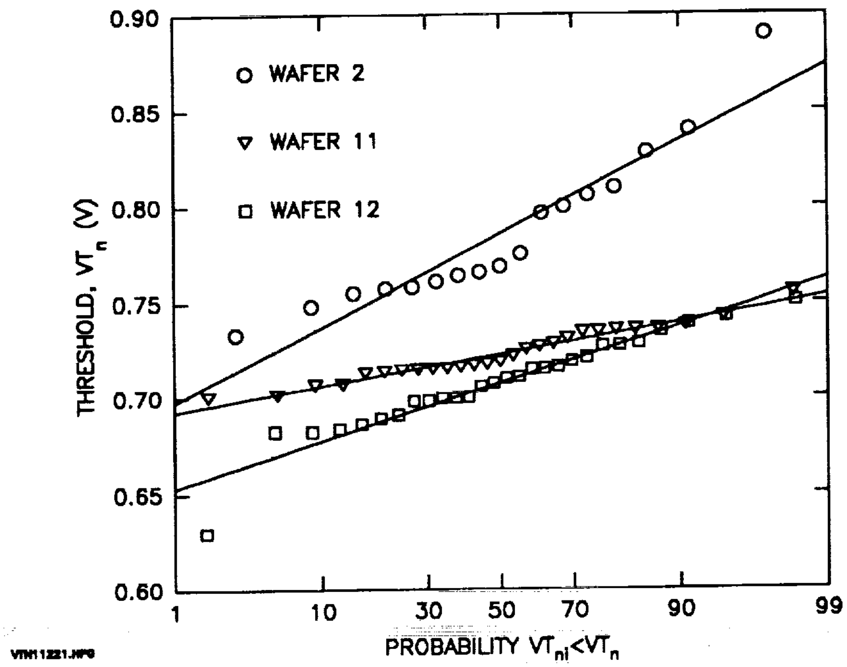


Figure 7. Distribution of n-MOSFET threshold voltage for Wafers 2, 11, and 12.

2.3 Reliability Chip

The reliability chip is intended to be used to characterize electromigration in Metal1, or Metal2, and Metal1 diffusion contacts. Electromigration in metals is a wear-out mechanism found in the interconnects of integrated circuits. This mechanism is accelerated by high temperatures and high current densities. Since Metal2 generally carries the highest current density, it was characterized.

Metal2 electromigration results are shown in Figure 8 for the stress current density, J, and stress temperature, T. The data were fitted to Black's electromigration equation:

(6) $t_{50} = A_{50}J^{-n}\exp(E_a/kT)$

where E_a is the activation energy and n is the current density factor.

The test structures used in this study are Metal2 aluminum wires that have a length L_c = 8 mm. The t_{50} equation parameters are listed in Table 8 under run N06J, Chip No. 18. The results for stress current density, J, and temperature, T, are shown in Figure 8. The parameters listed in Table 8 were used to calculate failures at operating conditions. For $J_{operate}$ = 0.2 MA/cm^2 and $T_{operate}$ = 125°C, t_{50} = 6,014 years and $t_{0.01}$ = 416 years. The $t_{0.01}$ calculation is based on:

(7) $\ln t_{0.01} = \ln t_{50} + \sigma \cdot x$

where σ is the lognormal shape factor, and x = -3.71905 [8] for a cumulative failure percentage of 0.01 percent. At the chip level, the 50 percent failure time is of interest for comparison purposes. The $t_{0.01}$ is taken as the time when the first wire fails.

These electromigration results for this run, N06J, are very encouraging for they indicate that the metal system is robust. The electromigration results for this run are listed in Table 8, where they can be compared to other runs. Two attributes are evident: (a) the t_{50} values are consistent between the two chips tested and (b) the t_{50} results are the highest seen to date except for the M95F run which was erratic.

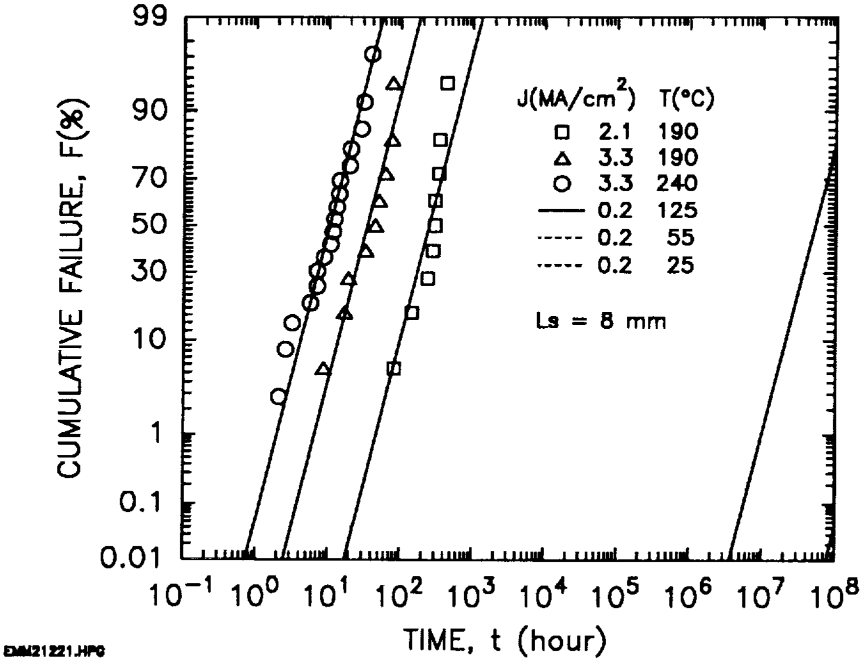


Figure 8. Metal2 electromigration failure rates shown for three stress points and extrapolated to operating conditions for Chip No.18. More results are tabulated in Table 8.

Table 8. Metal2 electromigration data base.

VENDOR TECH. (μm)		RUN NO.	CHIP NO.	E_a (eV)	n	σ	A_{50} hr(MA/cm^2)^n	t_{50} (years) J_{oper}=0.2MA T_{oper}=125°C
3.0	B	M78W	-	0.36±0.05	1.50±0.02	0.32±0.02	0.0660	3.00
3.0	D	M88F	-	0.33±0.02	1.37±0.08	0.18±0.01	0.0039	0.06
2.0	C	M92P	1	0.47±0.02	3.72±0.20	0.37±0.02	0.0326	1300.00
1.6	A	M95F	1	0.50±0.02	1.80±0.10	0.34±0.02	0.0001	0.43
1.6	A	M95F	19	0.19±0.05	6.70±0.30	0.70±0.05	503.6283	700,000.00
1.6	A	M9AD	1	0.54±0.04	3.30±0.21	0.51±0.04	0.0005	77.79
1.6	A	M9AD	10	0.42±0.04	3.09±0.04	0.58±0.03	0.0074	25.00
1.6	A	M06J	18	0.49±0.04	4.36±0.24	0.72±0.04	0.0301	6,014.00
1.6	A	M06J	15	0.50±0.09	4.32±0.50	0.68±0.09	0.0199	4,988.00

2.4 Diagnostic Test Chip Conclusions

Although the standard deviations of p-Poly, n-Poly and n-Diff contact resistance were high, and the oxide pinhole densities were also high, the data collected from the test structures indicated that the MOSIS fabrication was normal for this task. In summary, the measurements uncovered the following:

1) Metal1 had no breaks in 9.0 meters and no metal bridges in 1.8 meters.

2) Metal2 had no breaks in 7.6 meters and no metal1 bridge in 1.5 meters.

3) Poly had 1 break in 13.6 meters and 2 poly bridges in 2.7 meters.

4) Oxide pinhole density for n-type MOSFETs was 17 defects/cm^2 and for p-type was 5 defects/cm^2.

6) Poly, Metal1, and Metal2 step resistances were excellent being less than a few percent.

7) Metal2 electromigration results were excellent with a $t_{0.01}$ = 416 years.

8) Inverter standard deviations ranged between 2 and 8 mV which is excellent.

9) MOSFET threshold voltage for n- and p-MOSFETs was distinctly different for wafer 2. The threshold voltages from wafers 11 and 12 agreed closely.

Thus it is important to acquire data on a wafer-by-wafer basis. The variation in threshold voltage across the wafer from the process monitor MOSFETs is 14 to 37 mV but from the inverter matrix the variation is much less than 10 mV. As will be shown, the latter value is close to the value observed from the SRAM threshold variations. The above results illustrate that across the MOSFET wafer variations are larger than local variations.

3.0 SEU/TD RADIATION MONITOR

The SEU/TD radiation monitor consists of a 4-kbit SRAM and four MOSFETs. The block diagram is shown in Figure 2.

3.1 SEU SRAM Cell

The SEU SRAM, shown in Figure 9, was designed with an offset voltage, V_0, that adjusts the cell critical charge, Q_c, allowing particles that induce a charge greater than Q_c to upset cells. Figure 9 shows the six MOSFETs found in each cell. The pulsed current source, shown in the figure, is used to simulate a particle strike on drain Dn2 when calculating the critical charge of the cell with SPICE.

This cell differs from that of a standard six-transistor SRAM cell in three ways: 1) the source of the p-MOSFET, Mp2, is connected to an adjustable offset voltage, V_0, instead of to VDD to provide control of the cell's critical charge; 2) the drain area of Dn2 has been enlarged by a factor of four over the minimum area to enhance the SEU upset rate, thus reducing measurement time; and, 3) the cell is imbalanced by widening Mn2 over minimum channel width in order to enhance its SEU sensitivity.

In operation the cell is biased and written into the sensitive state, as shown in Figure 9, where the drains Dp1 and Dn2 are reverse biased and susceptible to particle-induced upset. In the sensitive state, $V_0 = 5$ V so that all the memory cells are biased as shown in Figure 9. Thus V_0 is connected to Dn2 through Mp2. Then V_0 is lowered and the memory is in the stare or capture state. The stare state can be very long. In laboratory tests, SEU SRAMs have been held in the stare state for several days. Particles that strike Dn2 and deposit sufficient charge flip the struck cells. Then the read/write cycle is initiated by setting $V_0 = 5$ V. The memory is read to determine which cells have flipped during the stare cycle. Finally the cells are written into the sensitive state and the cycle repeated. The timing diagram for the SEU SRAM is shown in Figure 10. This shows that both V_0 and VDD are lowered during the stare cycle. The rationale behind lowering VDD is discussed below under cell "power requirements".

The upset mechanism depends in part on the charge collection depth, $\delta X4$. The charge collection depth beneath Dn2 is much greater than beneath Dp1 because the n-well truncates the particle-induced charge track. This geometrical effect can be seen in the cell cross section shown in Figure 3. Thus drain Dn2 is bloated as shown in Figure 11, by the dark-line outline, to maximize particle collection and is approximately rectangular being 8.0 μm by 8.8 μm.

The memory cell was designed using the MOSIS scalable CMOS rules and fabricated using 1.6-μm minimum linewidth. Table 9 provides the dimensions of the MOSFETs and their drain areas. The MOSFETs were designed to satisfy the following operating requirements: 1) Read Requirement, 2) Write Requirement, 3) Detector Response Function Requirement, 4) Temperature Requirement, and 5) Power Requirement.

The WRITE REQUIREMENT requires that the cell be forced into the sensitive state. This requires weak pull-up MOSFETs so the bit-line MOSFETs can restore the cells to the sensitive state.

The READ REQUIREMENT requires that the cell pull the appropriate bit line low since the bit lines are charged high. This requires that Mn's be designed to be strong pull downs.

The DETECTOR RESPONSE FUNCTION REQUIREMENT requires that all the cells flip spontaneously. As seen in Figure 12, the SRAMs have a distribution of offset voltages at which the cells flip. This data is replotted in Figure 13 as a cumulative probability plot using:

$$(8)\quad P(V_{0i}>V_0) = 100\cdot(N - 0.5)/N_t$$

where N is the number of flipped cells at V_0 and $N_t = 4096$. The analytical formula that describes the cumulative distribution is:

$$(9)\quad N = N_t\{1 - \mathrm{erf}[(V_{os} - V_{os\mu})/\overline{V}_{os\sigma}\sqrt{2}]\}/2$$

where V_{os} is the offset voltage in the spontaneous flip range, $V_{os\mu}$ is the mean value, and $V_{os\sigma}$ is the standard deviation; erf is the error function.

Devices must be screened carefully for outliers; this point is illustrated in Figure 14. Outliers can appear as cells that flip at high V_o values or as illustrated in the figure as cells that flip at low V_o values. The cumulative distribution plot is particularly useful in highlighting outliers.

The data shown in Figure 13 are listed in Table 10 and indicate that the mean spontaneous offset voltage is approximately 1.8 V and the standard deviation is approximately 10 mV. This behavior is determined by the threshold voltage of inverter #1 (INV#1) and its variance. The $VT_{inv\mu}$ and $VT_{inv\sigma}$ are given by equations in Section 2.1 for the inverter matrix fault chip. That is $V_{o\mu} = VT_{inv\mu}$ and $V_{o\sigma} = VT_{inv\sigma}$. This can be seen in the results listed in Table 11 where the SEU SRAM data falls between the inverter matrix results.

The TEMPERATURE REQUIREMENT requires that the detector function be independent of temperature. This can be achieved by properly sizing the MOSFETs in INV#1. The key to the design follows from the differentiation of the inverter threshold equation given above. It can be shown that β_r is independent of temperature if $(1/\mu_{no})d\mu_n/dT = (1/\mu_{po})d\mu_p/dT$. This relation holds if $\mu_n/\mu_{no} = \mu_p/\mu_{po} = (T/T_o)$^-1.5. The temperature dependence of VT_{inv} is:

$$VT_{iT} = \left.\frac{\partial VT_{inv}}{\partial T}\right|_{T \to T_o} = \frac{\sqrt{\beta_{ro}} \cdot VT_{nT} - VT_{pT}}{\sqrt{\beta_{ro}} + 1} \tag{10}$$

where $VT_{nT} = \partial VTn/\partial T|_{T\to T_o}$, $VT_{pT} = \partial VTp/\partial T|_{T\to T_o}$, and where $\beta_{ro} = KP_{no}W_nL_p/(KP_{po}W_pL_n)$. The inverter threshold voltage is independent of temperature for:

$$\sqrt{\beta_{ro}} = VT_{pT}/VT_{nT}. \tag{11}$$

This is illustrated in Figure 15 for the case where $\beta_{ro} = 1$. For the SRAM INV#1, $\beta_{ro} = 6.67$, which was calculated using W and L from Table 9 and ΔL and ΔW from Table 6. For $\beta_{ro} = 6.67$, $VT_{nT} = -4$ mV/°C, and $VT_{pT} = -4$ mV/°C, the temperature coefficient for the inverter threshold voltage is $VT_{iT} = -1.77$ mV/°C.

The POWER REQUIREMENT is determined by the power available from the system and by self-heating, which causes an increase in the chip temperature. The power consumed by each cell was determined from a SPICE simulation of the cell and plotted in Figure 16 for various VDD and V_o values. For a 4-kbit memory, VDD = 5 V, V_o = 2 V, and ID_{cell} = 40 μA, the P_{chip} = 0.82 W. This power is too high from both system and self-heating standpoints. Thus reducing VDD to reduce chip power is mandatory. For VDD = 3 V, V_o = 1.8 V, and ID_{cell} = 5 μA, the P_{cell} = 61 mW. The reduction in VDD during the stare cycle is shown in the timing diagram given in Figure 10.

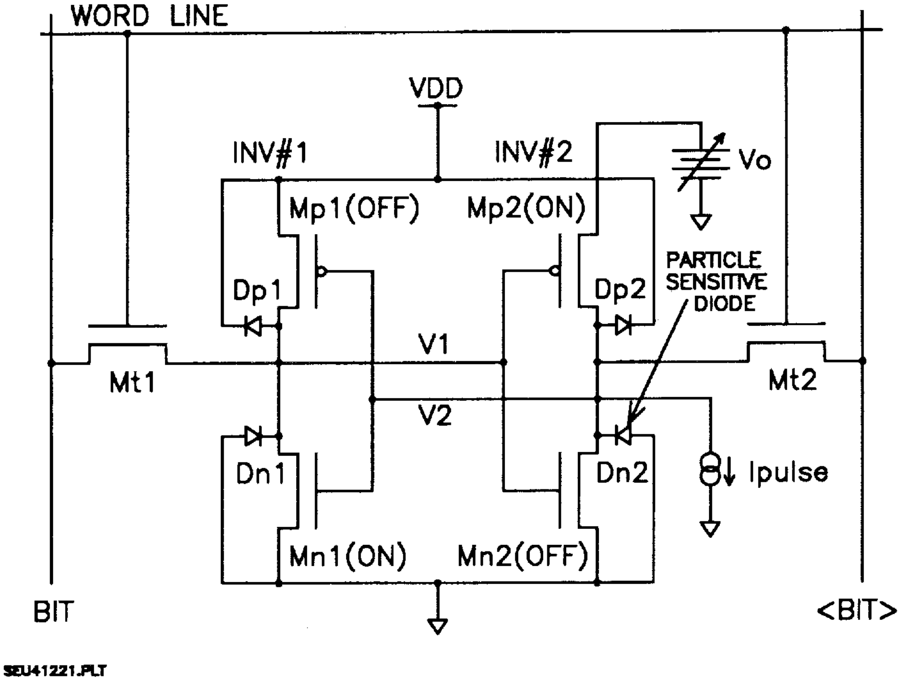

WORD LINE
VDD
INV#1
INV#2
Vo
Mp1(OFF)
Mp2(ON)
PARTICLE SENSITIVE DIODE
Dp1
Dp2
V1
Mt1
Mt2
V2
Dn1
Dn2
Ipulse
Mn1(ON)
Mn2(OFF)
BIT
<BIT>
SEU41221.PLT

Figure 9. The SEU SRAM circuit biased in the sensitive or capture state.

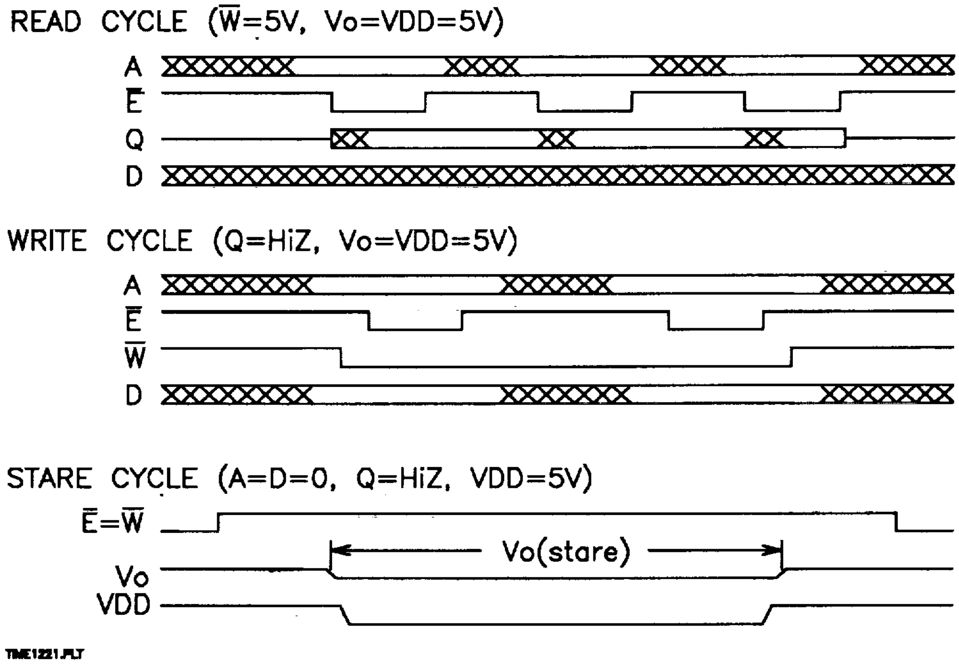

READ CYCLE ($\overline{W}$=5V, Vo=VDD=5V)
A
$\overline{E}$
Q
D
WRITE CYCLE (Q=HiZ, Vo=VDD=5V)
A
$\overline{E}$
$\overline{W}$
D
STARE CYCLE (A=D=0, Q=HiZ, VDD=5V)
$\overline{E}$=$\overline{W}$
Vo(stare)
Vo
VDD
TME1221.PLT

Figure 10. SEU SRAM timing diagram.

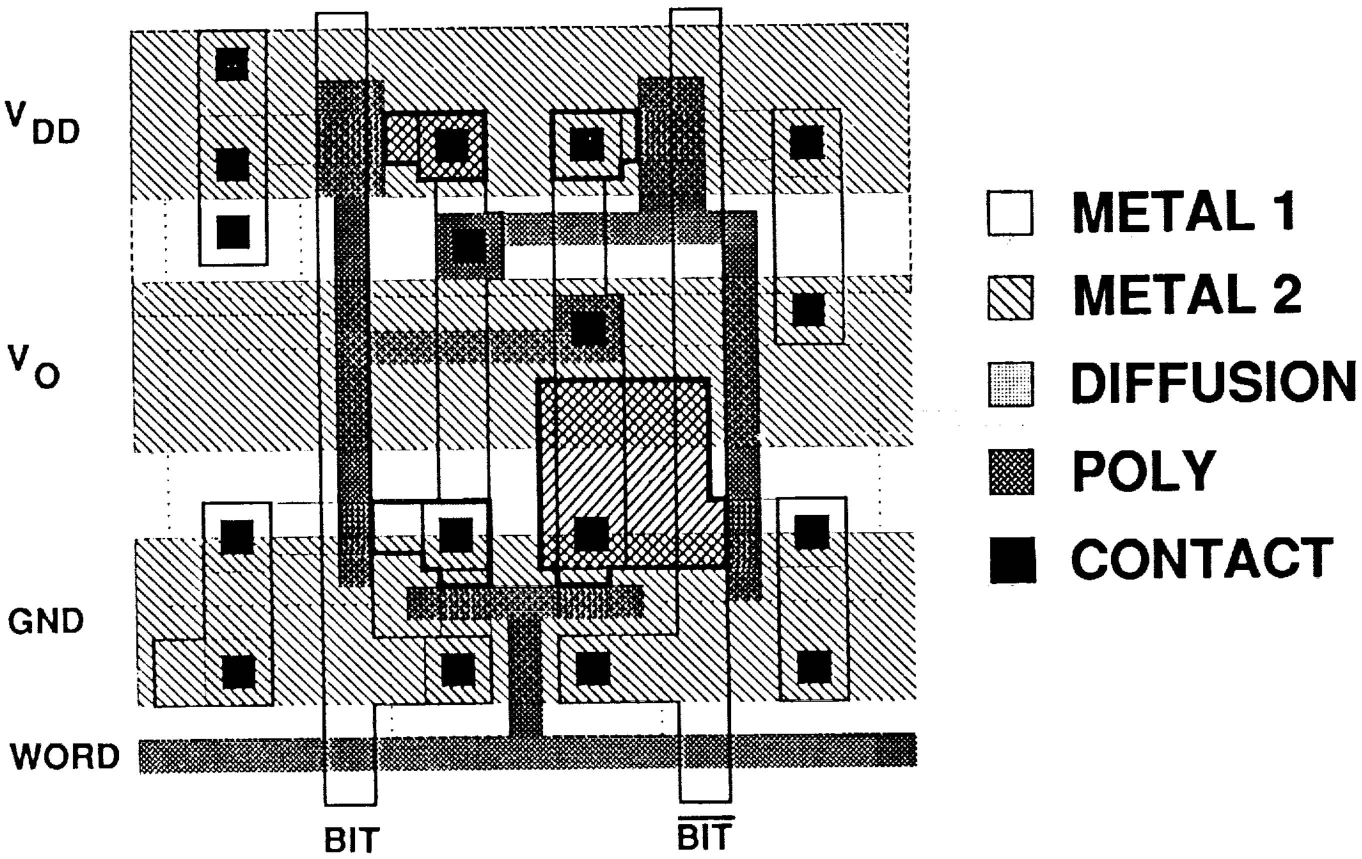

V_DD
V_O
GND
WORD
BIT
B̅I̅T̅
METAL 1
METAL 2
DIFFUSION
POLY
CONTACT

Figure 11. Memory cell layout is 33.6 μm by 36.0 μm.

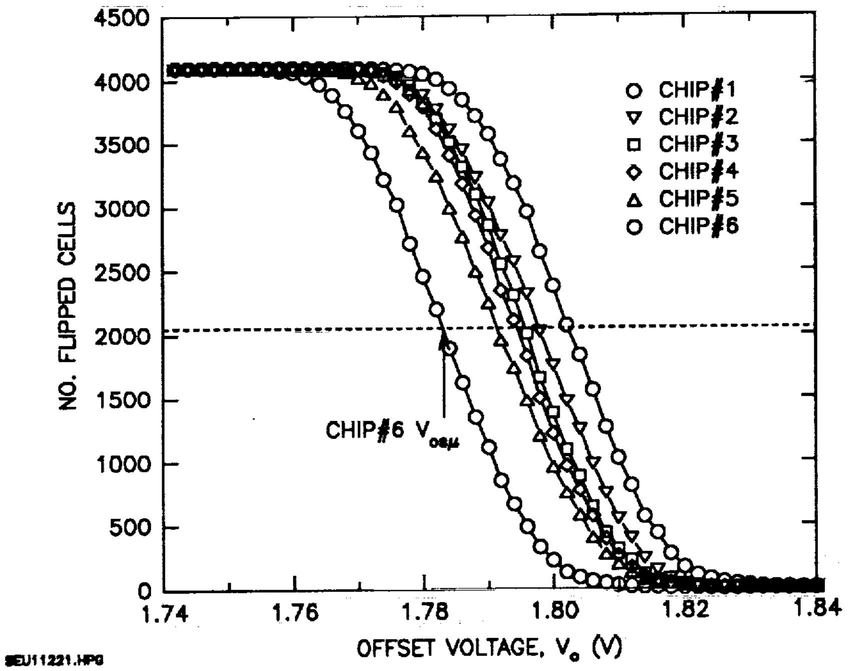


Figure 12. SRAM spontaneous flip response for six SEU SRAMs taken from Wafer 2. This is the detector response function.

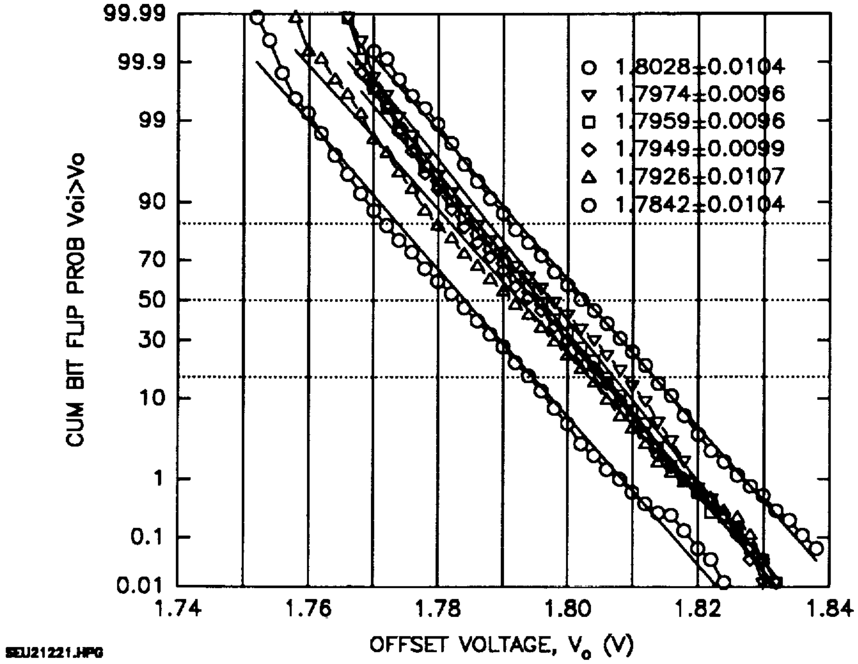


Figure 13. Detector response shown in Figure 12 is shown here as a cumulative distribution allowing the determination of the mean and standard deviation offset voltages.

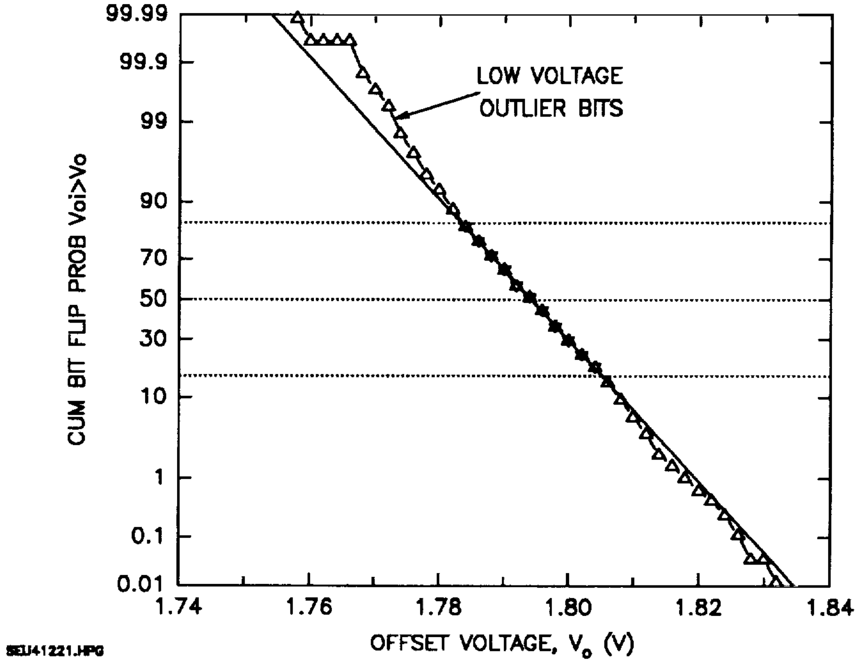


Figure 14. Detector response for Chip #4 shown in Figure 12 where outlier points are included. The line was fitted to points within one sigma of the mean.

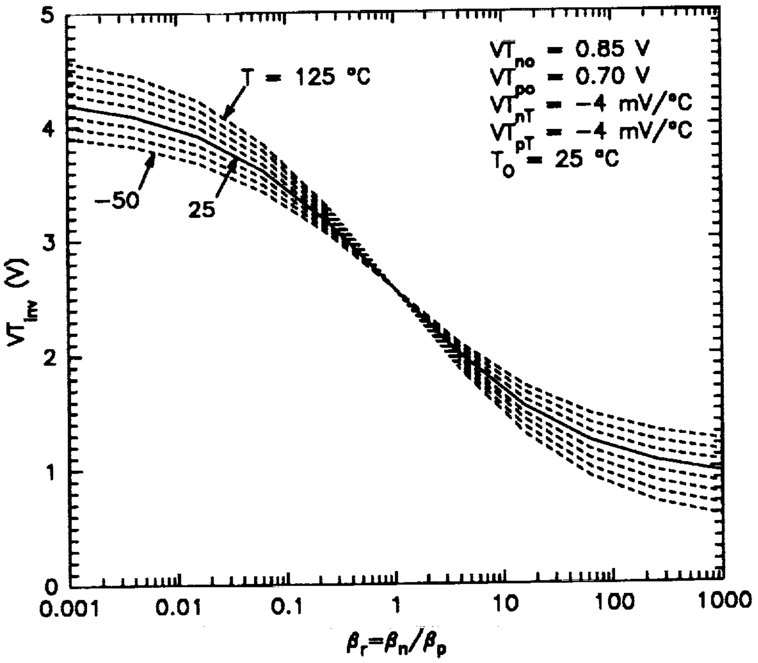


Figure 15. The temperature dependence of the inverter threshold voltage.

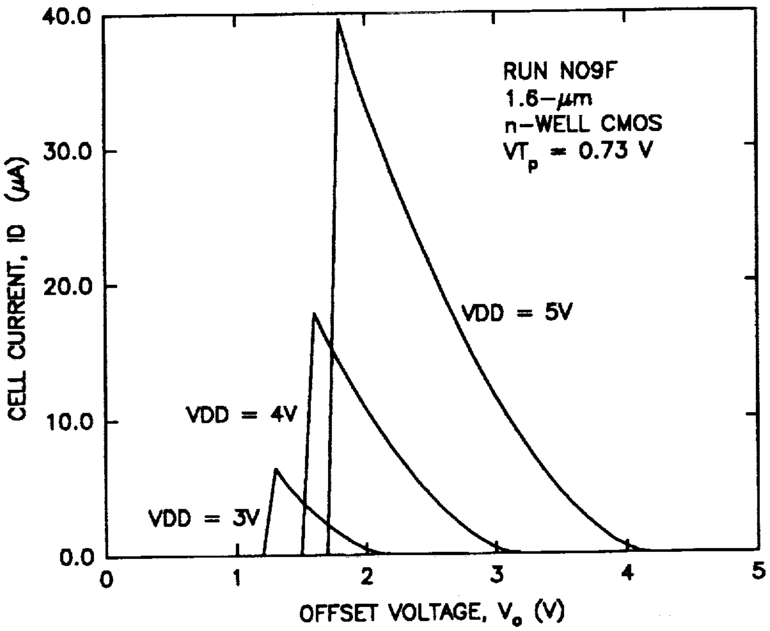


Figure 16. Current drawn by the memory cell.

Table 9. Dimensions of SEU SRAM MOSFETs and drain areas.

DEVICE	L(μm)	W(μm)	Ad(μm^2)
Mn1	1.6	2.4	17.92
Mn2	1.6	3.2	74.88
Mp1	3.2	2.4	14.08
Mp2	3.2	2.4	12.16
Mt1	1.6	2.4	-----
Mt2	1.6	2.4	-----

Table 10. SEU SRAM V_{os} results.

CHIP	$V_{os\mu} \pm VT_{os\sigma}$
#1	1.8028±0.0104
#2	1.7974±0.0096
#3	1.7959±0.0096
#4	1.7949±0.0099
#5	1.7926±0.0107
#6	1.7842±0.0104

Table 11. Inverter matrix and SEU SRAM test result comparison.

W_n	L_n	W_p	L_p	G_{ro}	$VT_{inv\mu} \pm VT_{inv\sigma}$	UNITS	DEVICE
2.4	1.6	2.4	1.6	1	2.00±0.008	V	INVERTER MATRIX
2.4	1.6	2.4	3.2	2	1.80±0.010	V	SEU SRAM (INV1)
2.4	1.6	2.4	6.4	4	1.42±0.006	V	INVERTER MATRIX

3.2 SEU SRAM Analysis

In this section the calibration procedure for the SRAM detector is described. Once calibrated this detector is able to measure protons, alpha particles, and heavy ion environments inside spacecraft computers. The procedure requires determining the detector's overlayer thickness, $\delta X3$, and collection depth, $\delta X4$. These were determined using 0.55 and 1.0 MeV protons from the Caltech Tandem Van de Graaff. The analysis requires a knowledge of the proton charge deposition versus range and this was calculated using particle range physics from TRIM [9,10]. The validity of the analysis was verified with energy straggling measurements. Finally, the SPICE circuit simulation program was used to compute the relationship between the charge deposited in the memory cell and the cell offset voltage [11,12,13]

The critical charge, Q_C, of the SRAM cell was determined as a function of V_O using MOSIS supplied SPICE parameters. The parasitic nodal capacitances were modeled by fixed metal and polysilicon interconnect capacitances and by the drain depletion capacitances using their areas and peripheries. The SPICE simulation used the level-2 model. A triangle current pulse with a 1:19 rise:fall shape was used to upset these cells [14]. The location of the pulse generator in the memory cell is shown in Figure 9. For a given pulse height, the transient simulation was examined at 100 ns where the response was compared to $V_{DD}/2$ to determine if the cell had flipped. The current pulse height was adjusted using a binary search algorithm until the difference in charge (area under current pulse) between successive simulation runs differed by less than 1 fC. These results were found to be invariant with current pulse widths up to 500 ps. Since the proton width is about 200 ps, the response of these circuits exceeds that of the proton current pulse.

SPICE simulations provide the Q_C versus V_O curve shown in Figure 17 which is well approximated by the straight-line relationship:

$$(12) \quad Q_C = C_u(V_O - V_{OS\mu})$$

where $V_{OS\mu} = 1.8$ V is the mean offset voltage in the spontaneous flip range and the slope is the upset capacitance, $C_u = dQ_C/dV_O = 56$ fC/V.

In the SRAM test sequence, all memory cells are written into the sensitive or stare state where Mn2 is turned OFF and Mp2 is turned ON, which connects V_O to the bloated drain, Dn2; see Figure 9. V_O is then lowered from 5 V for a period called the stare time, which can last a few seconds to several days. Thereafter, V_O is returned to 5 V and the cells are read to determine the number of upsets. This cycle is repeated for different values of V_O.

Test results are shown in Figure 18 for protons and alpha particles and compared against the spontaneous flip response. The overall behavior indicates that at high V_O the response curve is determined by particle energy straggling. At intermediate V_O, the response is determined by the collection of particles outside the area of drain Dn2. This is called the peripheral hit region. Finally, at low V_O, the cells flip spontaneously.

3.2.1 Layer Thickness Analysis:

The following analysis is used to determine the SRAM detector Dn2 overlayer material thickness, $\delta X3 = X3 - X2$, and charge collection region thickness, $\delta X4 = X4 - X3$. A schematic view of these layers is shown in Table 12.

The analysis requires the determination of offset voltage, V_{Op}, at the peak of the cell upset distribution. In this technique the cell upset distribution is normally distributed as seen in the cumulative probability plots shown in Figure 19. The analysis follows from the SRAM detector equation:

$$(13) \quad dN/dt = \sigma\phi(N_t - N)$$

where σ is the area of Dn2, ϕ is the flux, N is the measured number of flipped cells, and N_t is the total number of cells in the SRAM. Evaluating for $N \rightarrow 0$

(14) $dN/dt|_{N\to 0} = R_o = \sigma\phi N_t$

The particle flux at diode, Dn2, is described by the Gaussian or normal distribution expressed by the error function:

(15) $\phi = \phi_m\{1 - \mathrm{erf}[(V_{op} - V_{op\mu})/V_{op\sigma}\sqrt{2}]\}/2$

where ϕ_m is the maximum particle flux entering the SRAM, V_{op} is the offset voltage in the vicinity of the upset peak, $V_{op\mu}$ is the mean or peak value, and $V_{op\sigma}$ is the standard deviation for the upset distribution. Note that $\phi = \phi_m/2$ at $V_{op} = V_{op\mu}$, which states that only half the particle flux entering the SRAM can upset cells.

Combining the above equations leads to the following expression for the number of flipped cells in the vicinity of the particle upset distribution:

(16) $N \equiv R_o/\sigma\phi_m = N_t\{1 - \mathrm{erf}[(V_{op} - V_{op\mu})/V_{op\sigma}\sqrt{2}]\}/2$

The probability distribution given in percent and plotted in Figure 19 was determined from:

(17) $P(V_{oi}>V_{op}) = 100\cdot(N - 0.5)/N_t$

where N is the number of flipped cells at V_{op} and for this SRAM $N_t = 4096$ cells.

The calculation of N can take two approaches. The first approach is used when the experimenter knows the beam flux, ϕ_m. In this case, $N \equiv R_o/\sigma\phi_m$ where $\sigma = 68.8\ \mu m$ for Dn2 [12]. The second approach is used when the experimenter knows the beam fluence, F_m, and the number of upsets, N_f, observed during the time the beam is on. That is $N = N_f/\sigma F_m$. This approach is useful when the flux is variable and the fluence can be monitored.

The data points in Figure 19 allow an analysis of the Gaussian nature of the energy dispersion of the particles as they lose energy in the silicon. At the peak of the upset distribution, at the 50 percent point, only half of the particles can deposit sufficient charge to flip the cells. This is defined as Q_{cp} and is given by:

(18) $Q_{cp} = C_u(V_{op\mu} - V_{os\mu})$

where Q_{cp} values for the four curves shown in Figure 19 are listed in Table 13.

The SRAM overlayer thickness, $\delta X3$, was determined using a 0.55 MeV proton beam which stopped within the collection layer. This is crucial for it means that all the charge deposited in the collection layer, $\delta X4$, is collected by the diode Dn2. The charge deposition profile for the 0.55 MeV proton beam is shown in Figure 20. This profile was plotted using TRIM [9]. The analysis for $\delta X3$ begins by determining $V_{op\mu}$ for the 0.55 MeV proton upset data shown in Figure 19; the results are listed in Table 13. Then Q_{cp} is determined from Figure 17. Finally, the Q_{cp} value is subtracted from the End Of Range, EOR, of the charge deposition curve shown in Figure 20. Thus $\delta X3 = 4.32\ \mu m$.

The charge collection thickness, $\delta X4$, was measured with a 1.0 MeV proton beam which has a range greater than X4. The charge deposition profile for the 1.0 MeV proton beam is shown in Figure 21. The analysis begins by determining $V_{op\mu}$ for the 1.0 MeV proton upset data shown in Figure 19. Then Q_{cp} was determined from Figure 17. Finally $\delta X4$ was determined by adding Q_{cp} to the overlayer charge as determined from $\delta X3$; the technique is illustrated in Figure 21. Thus $\delta X4 = 6.64$ μm.

The charge collection depth, $\delta X4$, was also determined for a 4.7 MeV alpha particle beam and a collection depth of 6.33 μm was determined. This value is 0.31 μm smaller than the collection layer thickness determined for the proton beam. This is due to the fact that heavier particles have a smaller range.

The linear energy transfer, LET, in MeV·cm^2/mg for the particles can now be calculated using:

(19) $\mathrm{LET} \equiv \delta E4/\delta X4 = (E3 - E4)/(X4 - X3) = C_u(V_{op\mu} - V_{os\mu})/K\rho\delta X4$

where $K = 44.2$ fC/MeV for silicon, $\rho = 2320$ mg/cm^3 for silicon, C_u is in fC/V, V_o is in Volts, and $\delta X4$ is in cm. LET values are listed in Table 13. The LET value for $V_{op\mu} = 5$ V is 2.88 MeV·cm^2/mg for an estimated $\delta X4 = 6.00$ μm. The conversion factor K is determined from:

(20) $K = 1.602\mathrm{x}10^{-19}(\mathrm{C/e})\mathrm{x}10^{15}(\mathrm{fC/C})\mathrm{x}10^{6}(\mathrm{eV/MeV})/3.62(\mathrm{eV/eh\text{-}pair}) = 44.2$ fC/MeV

where the energy needed to produce a hole-electron pair in silicon is 3.62(eV/eh-pair).

3.2.2 Layer Thickness Dispersion Analysis:

The result of calculating the errors in $\delta X3$ and $\delta X4$, that is, $\delta X3_\sigma$ and $\delta X4_\sigma$, is shown in Table 12. It shows that as the 0.55 and 1.0 MeV protons pass through the various regions that the energy dispersion increases. This leads to an uncertainty in the thickness of each layer. The thickness dispersion is calculated from the energy dispersion. For the overlayer the depth dispersion is:

(21) $\delta X3_\sigma = \delta E3X_\sigma \cdot K \cdot d\delta X3/dQ_d$

where $\delta E3X_\sigma$ is the energy dispersion due to overlayer thickness variations and from Figure 20, $dQ_d/d\delta X3 = 3.85$ fC/μm. The collection layer depth dispersion is:

(22) $\delta X4_\sigma = \delta E4X_\sigma \cdot K \cdot d\delta X4/dQ_d$

where $\delta E4X_\sigma$ is the energy dispersion due to collection depth variations and from Figure 21, $dQ_d/d\delta X4 = 3.125$ fC/μm.

The evaluation of $\delta X3_\sigma$ requires an evaluation of $\delta E3_\sigma$. Since the 0.55 MeV protons stop in the charge collection region, the energy dispersion is determined by the Au scattering foil and the Si overlayer and not the Si collection layer. The energy dispersion for the 0.55 MeV protons is evaluated at the peak of the probability distribution as defined at the 50 percent point in Figure 19; it is calculated from $E_{op\sigma}(0.55) = (C_u/K)V_{op\sigma}(0.55)$. This energy dispersion consists of the following components:

(23) $E_{op\sigma}(0.55) = [(E_{os\sigma})^2 + (E1_\sigma)^2 + (\delta E3_\sigma)^2]^{1/2}$

where $E_{os\sigma} = (C_u/K)V_{os\sigma}$ is the instrument function energy dispersion, $E1_\sigma$ is the source Au scattering foil energy dispersion, and $\delta E3_\sigma$ is

$$(24) \quad \delta E3_\sigma = [(\delta E3S_\sigma)^2 + (\delta E3X_\sigma)^2]^{1/2}$$

where $\delta E3S_\sigma$ is overlayer energy dispersion due to particle straggling and $\delta E3X_\sigma$ is the overlayer energy dispersion due to overlayer thickness fluctuations. The $E1_\sigma = 0.012$ MeV was determined from Rutherford scattering theory for a 1.2-μm thick Au foil. $\delta E3S_\sigma = 0.009$ MeV was determined from Rutherford scattering theory for a 4.32-μm thick overlayer. $\delta E3X_\sigma$ is now calculated from the above two equations and $\delta X3_\sigma = 0.19$ μm was then determined.

The evaluation of $\delta X4_\sigma$ requires an evaluation of $\delta E4_\sigma$. Since the 1.0 MeV protons pass through the charge collection region, the energy dispersion is determined by the Au scattering foil, overlayer and collection layer. The energy dispersion for the 1.0 MeV protons is evaluated at the peak of the probability distribution as defined at the 50 percent point in Figure 19; it is calculated from $E_{op\sigma}(1.0) = (C_u/K)V_{op\sigma}(1.0)$. This dispersion consists of the following components:

$$E_{op\sigma}(1.0) = [(E_{os\sigma})^2 + (E1_\sigma)^2 + (\delta E3_\sigma)^2 + (\delta E4_\sigma)^2]^{1/2}$$

where $\delta E4_\sigma$ is

$$(25) \quad \delta E4_\sigma = [(\delta E4S_\sigma)^2 + (\delta E4X_\sigma)^2]^{1/2}$$

where $\delta E4S_\sigma$ is collection layer energy dispersion due to particle straggling and $\delta E4X_\sigma$ is the energy dispersion due to collection layer thickness fluctuations. The $\delta E4S_\sigma = 0.011$ MeV was determined from Rutherford scattering theory for a 6.64-μm thick collection layer. $\delta E4X_\sigma = 0.025$ MeV is now calculated from the above two equations and $\delta X4_\sigma = 0.36$ μm was then determined.

Table 12. Schematic view of the proton paths from the source to the SRAM.

	Proton source	1.0 MeV	0.55 MeV
X0			
	Au Scattering Foil	$\delta X1$ = 1.20	$\delta X1$ = 1.20
X1		E1 = 1.00±0.01	E1 = 0.55±0.01
	Vacuum	$\delta X2$ = 0	$\delta X2$ = 0
X2		E2 = 1.00±0.01	E2 = 0.55±0.01
	Si Overlayer	$\delta X3$ = 4.32±0.19	$\delta X3$ = 4.32±0.19
X3		E3 = 0.81±0.03	E3 = 0.24±0.03
	Si Collection Layer	$\delta X4$ = 6.64±0.36	--------------
X4		E4 = 0.44±0.04	E4 = 0

δX in μm and E in MeV.

Table 13. $\delta X3$, $\delta X4$, and LET values.

PARTICLE	Q_{cp} fC	$V_{op\mu}$ V	$V_{op\sigma}$ V	$\delta X3$ μm	$\delta X4$ μm	LET MeV·cm^2/mg
0.55 MeV PROTON	10.47	1.99	0.02	4.32	----	----
1.00 MeV PROTON	16.18	2.09	0.03	4.32	6.64	0.24
4.70 MeV ALPHA	50.40	2.66	0.14	4.32	6.33	0.77
OPERATING CONDITION	178.00	5.00	-----	4.32	6.00	2.88
SPONTANEOUS FLIP		$V_{os\mu}$	$V_{os\sigma}$			
		1.80	0.01			

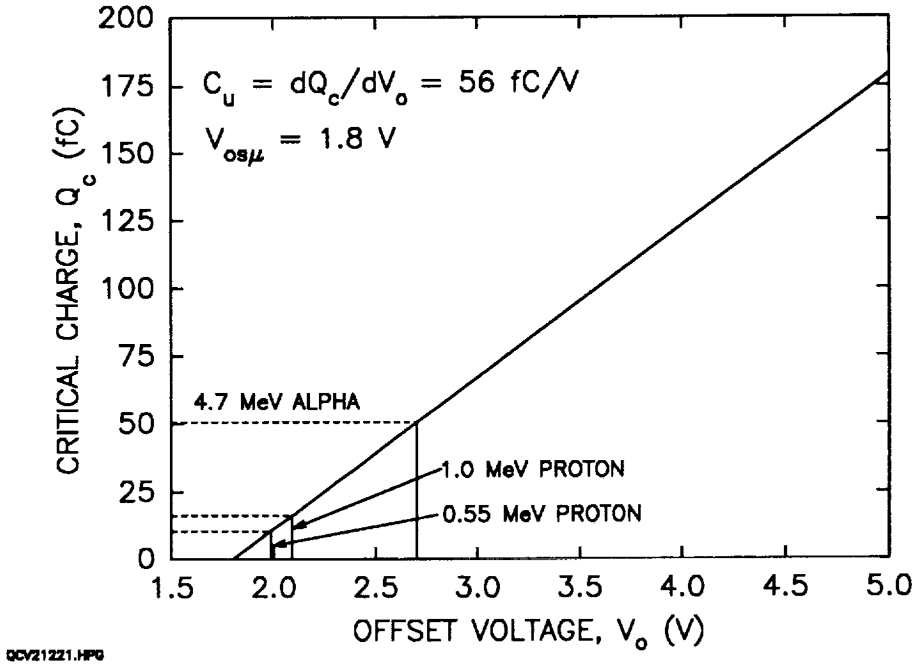


Figure 17. SRAM critical charge response for Node-V2 of Figure 9 calculated using SPICE Level-2.

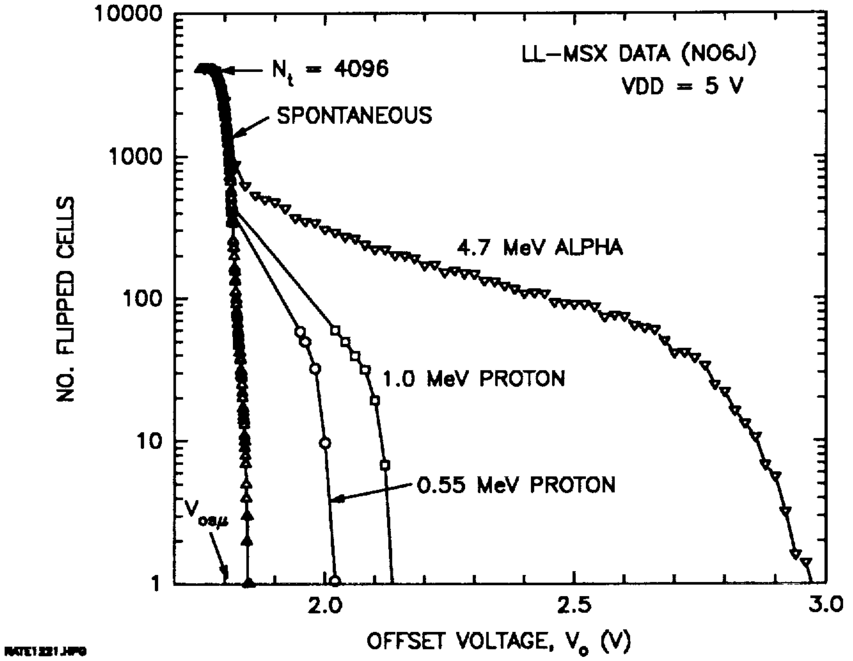


Figure 18. Number of flipped cells for alpha particles and protons shown relative to the spontaneous bit flip response for a stare time of one second.

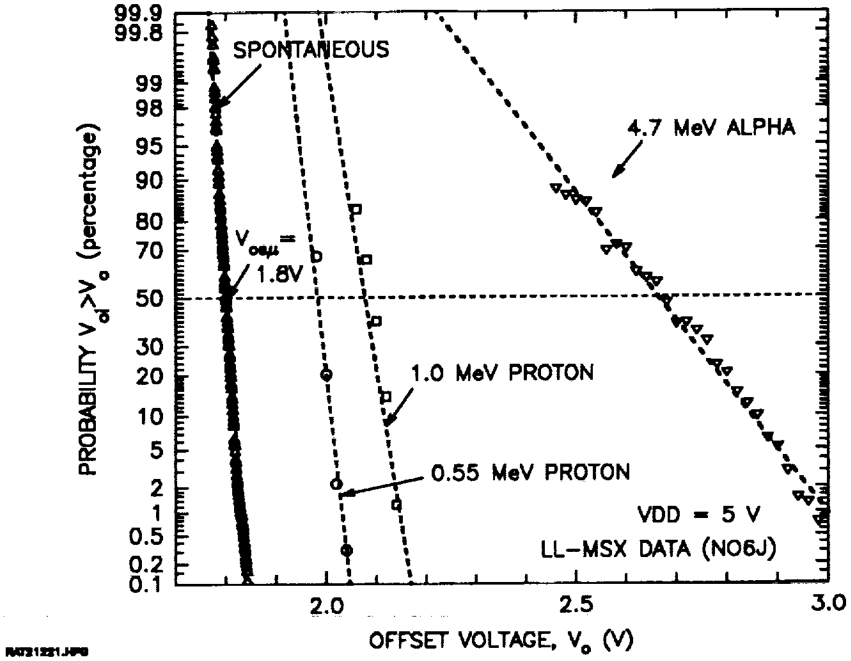


Figure 19. SRAM upset probability distribution for alpha particles and protons shown relative to the spontaneous bit flip response.

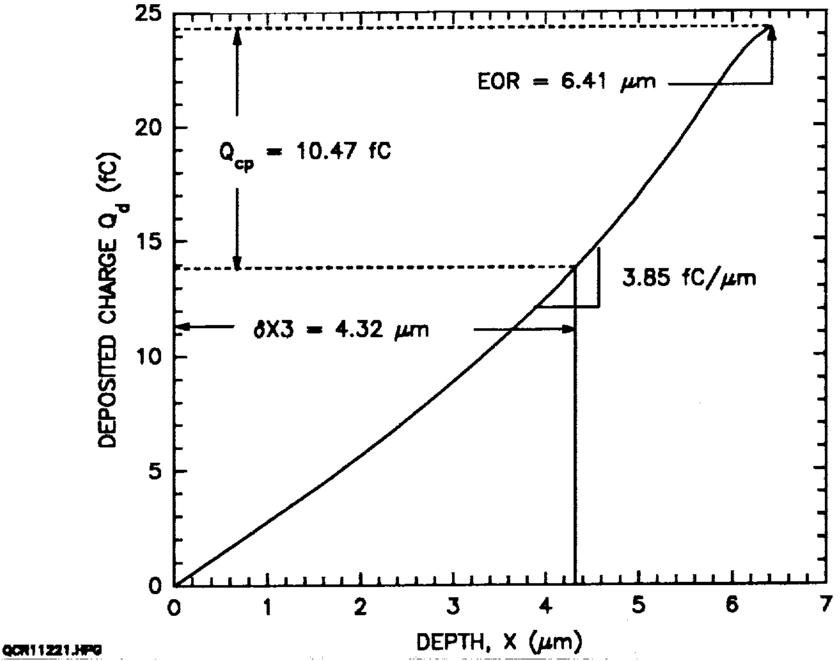


Figure 20. Charge deposited by 0.55 MeV protons in silicon. This charge is used to calculate the overlayer thickness, δX3.

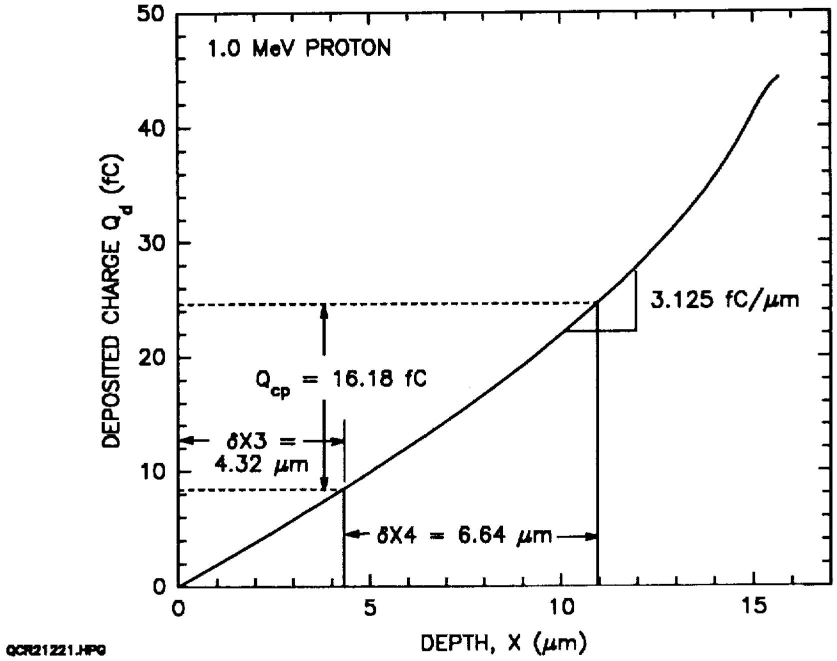


Figure 21. Charge deposited by 1.0 MeV protons in silicon. This charge is used to calculate the collection depth, δX4.

3.3 MOSFET Total Dose Dosimeters

The total dose MOSFETs included on the LL chip consist of a calibrator p-MOSFET, a floating gate p-MOSFET, and a standard n-MOSFET. These devices are intended to monitor total dose by two methods: (a) threshold shift of the n- and p-MOSFETs due to the radiation-induced oxide charge and (b) conductance shift of the floating gate p-MOSFET due to the accumulation of gate charge. The method (a) is a conventional method and method (b) is experimental [15].

The MOSFETs have circuit-like rectangular geometries which are listed in Table 14. The associated measuring circuits are shown in Figures 22 to 24 where the resistor values are fixed at R = 1 kΩ. These circuits are meant to measure the MOSFETs at a single-point in their IV characteristics and provide a rough indication of the total dose degradation. These MOSFETs and circuits have a number of shortcomings; in particular their sensitivity to radiation is low. The sensitivity of the MOSFETs to radiation is analyzed below and in Section 3.4, where an advanced MOSFET dosimeter is introduced which overcomes a number of shortcomings of the current devices and circuits.

3.3.1 Calibrator p-MOSFET Dosimeter

The calibrator p-MOSFET circuitry is shown in Figure 22. This device is used to monitor the radiation-induced charge accumulated in the gate oxide and at the oxide interface. In addition it is intended to provide the threshold voltage needed in the analysis of the floating gate p-MOSFET.

The analysis of the calibrator p-MOSFET uses the saturation region drain current:

(26) $ID_p = \beta_p(VDD - VG_p - VT_p)^2$

where VT_p is the absolute value of the p-MOSFET threshold voltage. A circuit analysis yields $VD_p = VO_p/2$, $ID_p = VO_p/2R$, and $VG_p = VDD/2$. The threshold voltage follows from these relations:

(27) $VT_p = (VDD/2) - \sqrt{VO_p/2\beta_p \cdot R}$

where $\beta_p = \beta_{po}$, the starting value. The sensitivity of the drain voltage, VD, to VT changes is:

(28) $S_p = dVD_p/dVT_p = 2\beta_p R(VDD - VG_p - VT_p)$

where $S_p \approx 0.1$ for the MOSFET values listed in Tables 6 and 13 and the circuit parameters shown in Figure 22.

The amount of VT degradation with dose depends on the bias that is held on the gate during the "soak" state; i.e. when the device is not being measured [16]. For maximal sensitivity to radiation, the gate should be biased so the p-MOSFET is in the OFF state. For the implementation shown in Figure 22, the MOSFET will be maintained in the ON state during the soak state. This will reduce the radiation sensitivity by a factor of two over an OFF state bias. In addition the satellite power down state will place the MOSFET in the OFF state. Thus the dose history will be complicated if the MOSFET is frequently switching between operating states.

3.3.2 Floating Gate p-MOSFET Dosimeter

The floating gate p-MOSFET circuitry is shown in Figure 23 and its gate dimensions are listed in Table 14. The circuitry is intended to provide a measure of the radiation-induced charge that accumulates on the floating gate. This charge will shift the gate potential and hence the channel conduction. This device is designed with the Poly gate connected to Metal1 which is connected to Metal2. The area of the metal sandwich is 8.0 μm by 8.0 μm.

In operation the act of powering up the MOSFET will induce a charge on the floating gate due to displacement currents that flow through the capacitor network formed by the gate overlap capacitances and the gate-well capacitor. Experiments indicate that p-gates have an initial voltage of a few tenths of a volt.

From a circuit analysis of the circuit shown in Figure 23, the gate voltage on the floating gate is given by:

(29) $VG_{pf} = VT_{pf} + \sqrt{VO_{pf}/\beta_{pf} \cdot R}$

where $VT_{pf} = VT_p$, the threshold voltage determined from the calibrator p-MOSFET, and $\beta_{pf} = \beta_{po}$.

As mentioned above, the VT degradation depends on the gate bias history. In this case the gate bias history is unknown, which complicates the analysis. Also recent radiation tests of floating gates, indicate that the polysilicon gates are surrounded by leaky oxides that will not support charge for more than 24 hours.

For the implementation shown in Figure 23, it is recommended that this device be maintained in the power up condition as much as possible and measured periodically. The outcome of this experiment cannot be predicted at this time; however, the results will be viewed with great interest.

3.3.3 Standard n-MOSFET Dosimeter

The standard n-MOSFET circuitry is shown in Figure 24. This device is used to monitor the radiation-induced charge accumulated in the gate oxide and at the oxide interface. The drain current for the n-MOSFET, which is operated in saturation, is:

$$(30) \quad ID_n = \beta_n(VG_n - VT_n)^2$$

and a circuit analysis yields the following expression for the threshold voltage:

$$(31) \quad VT_n = 0.5 \cdot VDD - \sqrt{(2VO_n - VDD/2)/(\beta_n \cdot R)}$$

where $\beta_n = \beta_{no}$, the starting value. The sensitivity of the drain voltage, VD, to VT changes is:

$$(32) \quad S_n = dVD_n/dVT_n = \beta_n R(VG_n - VT_n)$$

where $S_n \approx 0.14$ for the n-MOSFET values listed in Tables 6 and 14 and the circuit parameters shown in Figure 24.

The VT radiation degradation for n-MOSFETs is complicated by the nature of the radiation induced charges. Oxide charge is positive and oxide-silicon interface charge is negative. The VT shift depends on the rate at which these charges accumulate and this process is gate bias dependent.

3.4 Advanced MOSFET Dosimetry

Dosimetry measured via MOSFET threshold voltage shifts is influenced by two second-order effects: (a) the radiation sensitivity of the transconductance factor, KP, caused by radiation-induced mobility, μ, degradation and (b) the temperature sensitivity of KP and VT. The goal in developing an advanced MOSFET dosimeter is to minimize/eliminate or account for both of these effects. In addition, the system operating conditions must be considered in order to obtain accurate dose measurements. The operating conditions are discussed at the end of this section.

The p-MOSFET is operated in the saturation region, which is ensured by connecting the gate to the drain as seen in Figure 25. For this case the drain current is given by:

$$(33) \quad ID = \frac{KP \cdot W}{2L}(VG - VT)^2$$

where VT is the absolute value of the p-MOSFET threshold voltage. This equation is plotted in Figure 26, which shows the temperature effects and the temperature independent point. The above square-law relationship is rewritten in terms of VG:

(34) $VG = VT + \sqrt{2ID \cdot L/(KP \cdot W)}$

where the radiation sensitivity is:

(35) $S = dVG/dVT = 1$

which shows the direct relationship between a change in VT and a change in the measured gate voltage.

The temperature dependence of the p-MOSFET IV characteristics, shown in Figure 26, indicates that the temperature effects can be eliminated by operating the MOSFET at a certain fixed current value, termed ID_O. The analysis uses a Taylor series expansion of the VG expression:

(36) $VG = VG_O + VG_T(T - T_O) + VG_D \cdot D$

where T is the absolute temperature, D is the radiation dose, the VG temperature coefficient is $VG_T = \partial VG/\partial T|_{T \to T_O}$, and the VG dose coefficient is $VG_D = \partial VG/\partial D|_{D \to O}$. The current at the temperature independent point is found by setting $VG_T = 0$ in Eq. (34). This leads to:

(37) $ID_O = 2KP_O{}^3(W/L)[(VT_T/KP_{TO})]^2$

which shows that ID_O is MOSFET geometry dependent. The gate voltage at the temperature independent point is found by substituting ID_O into Eq. (34); that is:

(38) $VG_O = VT_O + 2VT_T \cdot KP_O/KP_{TO}$

which shows that VG_O is independent of the MOSFET geometry.

Further analysis uses a Taylor series expansion of VT and KP:

(39) $VT = VT_O + VT_T(T - T_O) + VT_D \cdot D$

where the VT temperature coefficient is $VT_T = \partial VT/\partial T|_{T \to T_O}$ and the VT dose coefficient is $VT_D = \partial VT/\partial D|_{D \to O}$. For KP:

(40) $KP = KP_O + KP_T(T - T_O) + KP_D \cdot D$

where the KP temperature coefficient is $KP_{TO} = \partial KP/\partial T|_{T \to T_O}$ and the KP dose coefficient is $KP_D = \partial KP/\partial D|_{D \to O}$. The temperature dependence of KP is:

(41) $KP = KP_O(T/T_O)^{-n}$

where n is a constant and $KP_{TO} = \partial KP/\partial T|_{T \to T_O} = -n \cdot KP_O/T_O$.

For $VT_O = 0.7$ V, $VT_T = -2$ mV/°C, $n = 1.5$, $KP_O = 30\ \mu A/V^2$, and $T_O = 300$ K, leads to $KP_{TO} = -0.15\ (\mu A/V^2)/°C$, $ID_O = 19.2\ \mu A$, and $VG_O = 0.7 + 0.8 = 1.5$ V. These values were used to calculate the temperature independent point in Figure 26.

The dose dependence is found by evaluating Eq. (34):

(42) $VG_D = VT_D - VT_T \cdot KP_D/KP_{T0}$

where ID_0 was substituted in the resulting equation. For a p-MOSFET biased in the OFF state [3], VT_D = 3.45 mV/krad(Si) and KP_D = -0.025 (μA/V^2)/krad(Si). Using VT_T = -2 mV/°C and KP_{T0} = -0.15 (μA/V^2)/°C determined above, leads to VG_D = 3.78 mV/krad(Si). Notice that the KP contribution is small, for VG_D is only slightly larger than VT_D. The total dose expression is:

(43) $D = (VG - VG_0)/VG_D$

The above dose expression requires the evaluation of VT_D and KP_D, which is done using Co-60 irradiation. In this evaluation, dose rate effects must be evaluated and then extrapolated to operating dose rate conditions. For p-MOSFETs, dose rate effects are usually minimal.

The p-MOSFET dosimeter operating modes include MEASure, OFF (soak/power down), CALibrate #1 and CALibrate #2. For maximum sensitivity to radiation, p-MOSFETs should be operated in the OFF state during the soak state. In the OFF state the electric field is directed from the gate toward the silicon. This means that during the radiation damage process when the positive oxide charge is mobile, it will be distributed more toward the silicon, which makes the MOSFET harder to turn on. This can be achieved in the implementation shown in Figure 25 by applying zero bias to the gate. This requirement has the advantage that the soak and power down states will be identical and means the MOSFET will be operated in a consistent bias state providing a well-known biasing scenario. The key to this bias requirement is that the n-well be connected to a zero potential and not be biased to VDD as is the normal case in integrated circuit design. Keeping the p-MOSFET's n-well at zero bias will not interfere with SRAM operation whose n-wells are biased to VDD.

The design of the dosimeter requires current flow from source to drain and not via a peripheral leakage path. Thus the device is designed as an edgeless MOSFET where the source completely surrounds the drain. In addition, all junctions are held at zero bias except for the drain junction. The operational amplifier holds the source at zero bias by providing a drain current ID = V1/R. The drain voltage is fixed by the amplifier at VG which, for the case of the p-MOSFET, is negative.

Table 14. Dimensions of total dose MOSFETs

DEVICE	L(μm)	W(μm)
STANDARD n-MOSFET	1.6	3.2
CALIBRATOR p-MOSFET	1.6	3.2
FLOATING GATE p-MOSFET	1.6	3.2

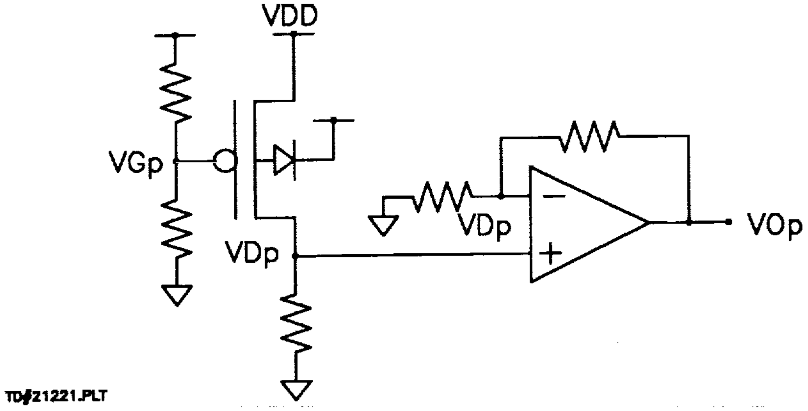

VDD
VGp
VDp
VDp
VOp
TD#21221.PLT

Figure 22. Calibrator p-MOSFET operated as a total dose dosimeter.

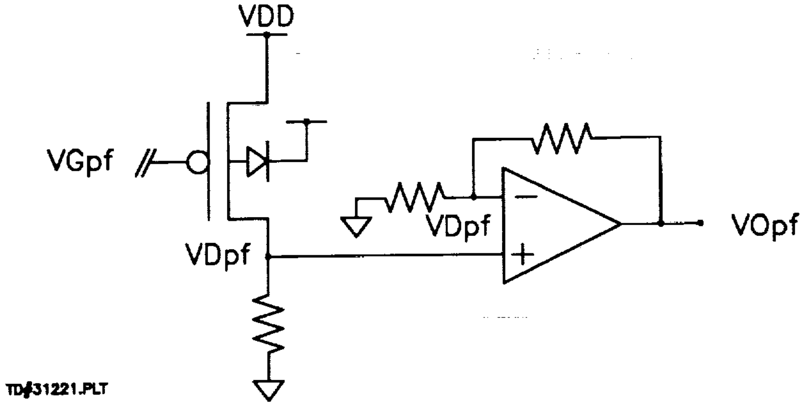

VDD
VGpf
VDpf
VDpf
VOpf
TD#31221.PLT

Figure 23. Floating gate p-MOSFET operated as a total dose dosimeter.

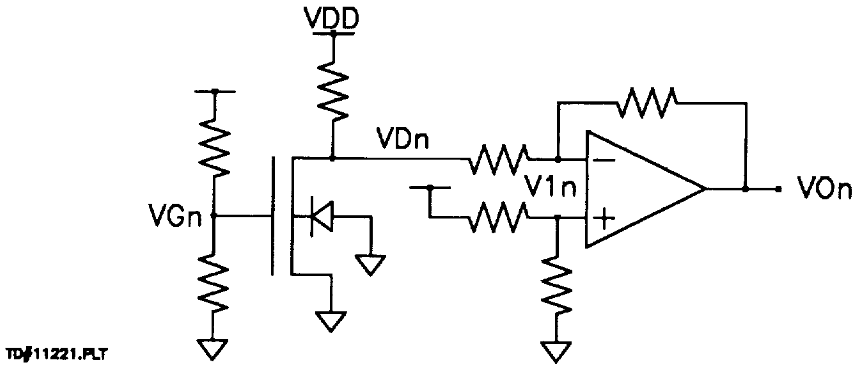
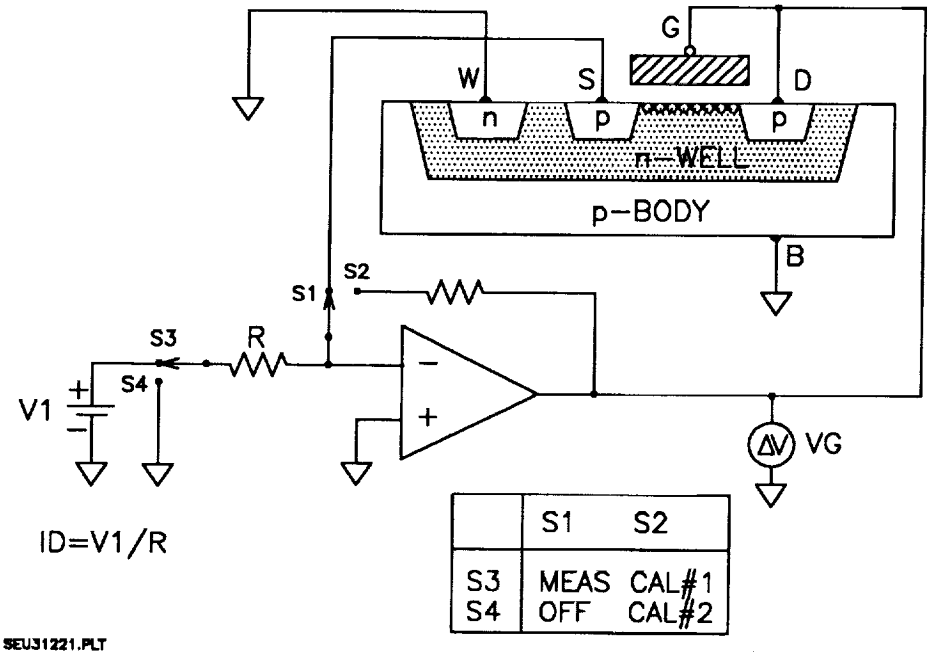

VDD
VDn
V1n
VOn
VGn
TDF11221.PLT

Figure 24. Standard n-MOSFET operated as a total dose dosimeter.


G
W
S
D
n
p
p
n-WELL
p-BODY
B
S1
S2
S3
S4
R
V1
VG
ID=V1/R
SEU31221.PLT

	S1	S2
S3	MEAS	CAL#1
S4	OFF	CAL#2

Figure 25. p-MOSFET operated as a total dose dosimeter where the gate voltage is proportional to the dose. The drain current, ID, is set to minimize temperature variation effects; see Figure 26.

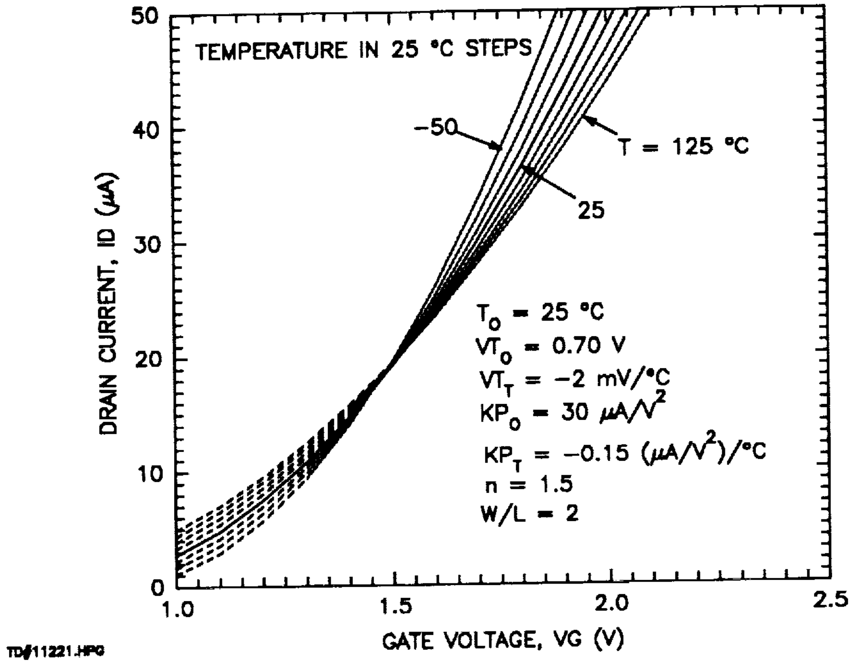


Figure 26. Temperature dependence of the p-MOSFET dosimeter showing the temperature independent point at $ID_0 = 19.2\ \mu A$ and $VG_0 = 1.5$ V.

4.0 SEU/TD RADIATION MONITOR SCREENING PROCEDURES

Once JPL completed the chip design, the design was transmitted electronically to MOSIS, who had the wafers fabricated and the chips packaged in 28-pin DIPs without lids. Once the parts were partly screened, the remaining chips were sent for lidding. The chips for this project came from three wafers: 2, 11, and 12. As is customary at MOSIS, chips are not tested in wafer form. Thus chips that were packaged are untested. The inventory of the chips during functional test, screening, and packaging is listed in Table 15. Table 16 outlines the steps followed in part screening and lists the organization that performed the task.

The screening procedures were conducted according to a subset of MIL-STD-883C screening requirements. The requirements consisted of the following:

1) Non-destructive Bond Pull (Method 2032)
2) Internal Visual Inspection (Method 2010)
3) External (Package) Visual Inspection
4) Pre-Burn-In Static and Dynamic Test
5) Static Burn-In 24 hours at 125°C With All Leads Grounded Except VDD = 5 V
6) Post Burn-In Static and Dynamic Test
7) Post Hermetic Seal Static and Dynamic Test
8) Hermeticity Seal Test (Method 1014)
9) Final External Visual Inspection
10) Pre-Ship Review

The SEU/TD Radiation Monitor chip results showed a functional yield of 94.6 percent. During the test, 71 SRAMs passed the power up, walking ones, checker board, access time, and standby power tests. Fifty (50) SRAMs and 41 complete MOSFET experiments were able to pass a 24-hour burn-in at a temperature of 125 C. During the tests, various failure types were detected which included stuck memory cells, large chip stand-by leakage currents, and large transistor leakage currents. It should be noted that the n- and p-MOSFETs did not have input pad protection to allow an accurate current measurement. Twenty-nine of the devices were lost during the hermetic seal lidding operation. In spite of the best efforts of the assembly house, it appears that the normal ESD prevention practices were not sufficient to protect these devices. Forty-three (43) SEU SRAMs and 14 Total Dose MOSFETs passed the hermeticity and final electrical tests and were delivered to the Lincoln Laboratory. See Table 15 for the chip inventory.

Table 15. Chip Inventory

ACTIVITY	UNLIDDED PACKAGES	LIDDED PACKAGES
CHIPS PACKAGED WITHOUT LIDS...TOTAL	75	
SRAMs FAILING INITIAL TEST-1	4	
PROTOTYPE PACKAGES SENT TO LL	6	
PACKAGES HELD AS SPARES	15	
PACKAGES HERMETICALLY SEALED	50	
PACKAGES HERMETICALLY SEALED...TOTAL		50
SRAMs FAILING TEST-4		7
GOOD SRAMs AND MOSFETs SENT TO LL		14
GOOD SRAMs AND BAD MOSFETs SENT TO LL		29

Table 16. Parts screening procedures

ORGANIZATION	TASK	STEPS
1. VLSI TECH	DESIGN	
2. MOSIS	FABRICATION	
3. ASSEMBLY	ASSEMBLY	A. EUTECTIC DIE ATTACH B. ULTRA-SONIC BONDING
4. VLSI TECH	INITIAL TEST	A. ELECTRICAL TEST-1 1. CHIP LEAKAGE 2. SRAM WALKING ONE/ CHECKER BOARD 3. MOSFET I-Vs
5. VLSI TECH	PROTOTYPE PARTS DELIVERED TO LL	A. 6-PARTS
6. ASSEMBLY	PACKAGE & SCREEN-1	A. PACKAGE SERIALIZATION B. DOCUMENTATION C. NON-DESTRUCTIVE BOND-PULL (2/PACKAGE @ 10 GRAMS) D. VISUAL INSPECTION-1 E. HERMETIC SEAL
7. VLSI TECH	SCREEN-2	A. TEMPERATURE CYCLES (5-60 MIN CYCLES) B. VISUAL INSPECTION-2 C. ELECTRICAL TEST-2 (SEE TEST-1) D. BURN-IN (24 HRS @ 125°C) E. ELECTRICAL TEST-3 (SEE TEST-1) F. VISUAL INSPECTION-3
8. ASSEMBLY	SCREEN-3	A. HERMETIC SEAL TEST
9. VLSI TECH	CHIP GRADING	A. ELECTRICAL TEST-4 (SEE TEST-1) B. DOCUMENTATION REVIEW
10. VLSI TECH	PRE-SHIPMENT REVIEW	A. PROGRAM OFFICE TASK REVIEW
11. VLSI TECH	SCREENED PARTS DELIVERED TO LL	A. 43 PARTS

5.0 SEU/TD SYSTEM INTERFACE CIRCUITRY

The interface circuitry that surrounds the SEU/TD chip is shown in Figure 27. In satellite operation, the SEU/SRAM offset voltage, V_O, is connected to +5 V which makes the chip sensitive to particles with a LET $\geq$ 2.88 MeV$\cdot$cm^2/mg. The SRAM will be monitored periodically for upsets. As seen in the figure, all digital lines have pull-down resistors which force the data lines to ground when the signals from digital chips are in a tri-state condition.

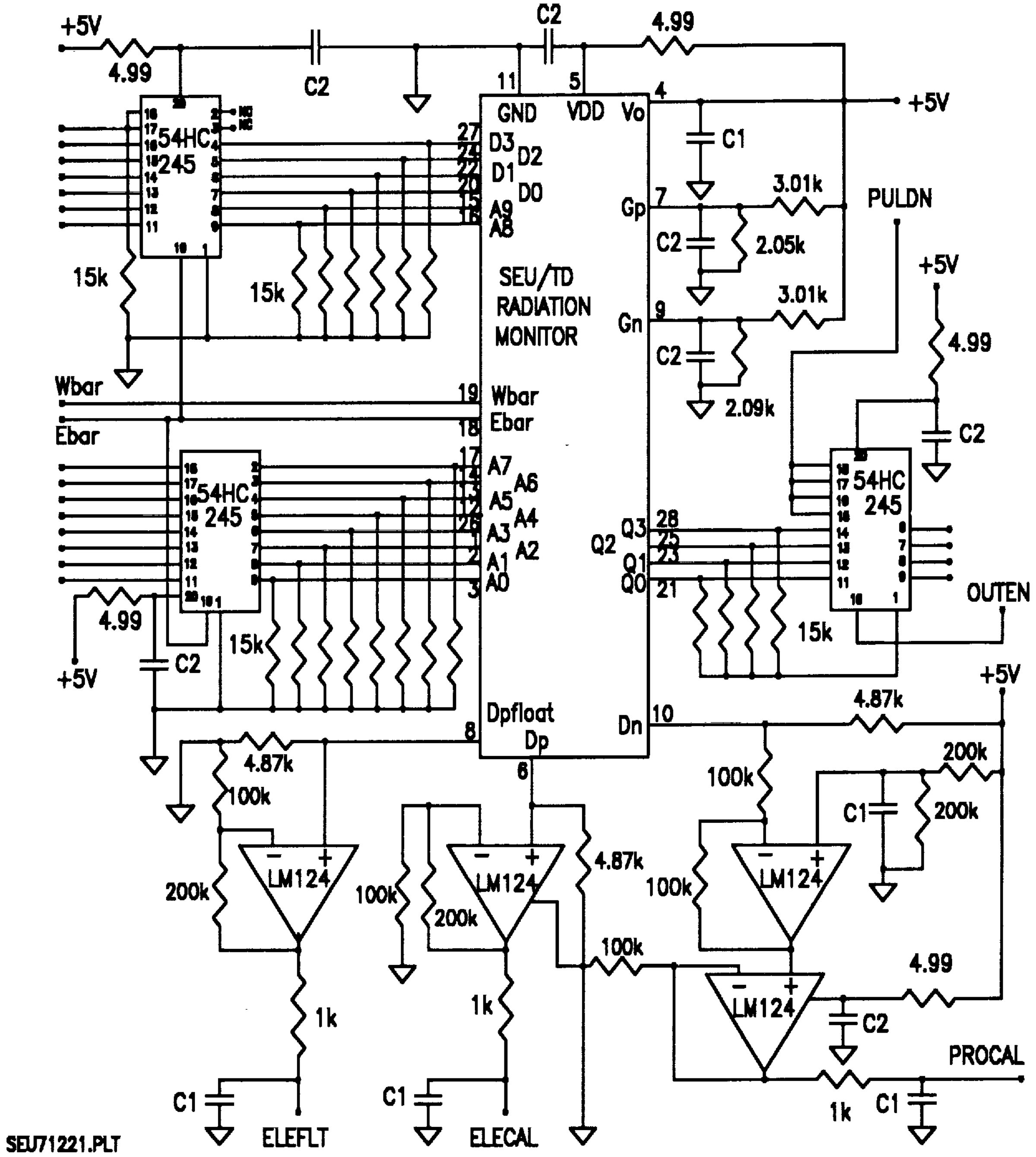

+5V
4.99
C2
C2
4.99
11
5
4
+5V
54HC
245
54HC
245
54HC
245
15k
15k
15k
15k
GND
VDD
Vo
D3
D2
D1
D0
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
27
24
22
20
15
16
17
14
13
12
26
1
2
3
C1
Gp
7
3.01k
PULDN
C2
2.05k
+5V
SEU/TD
RADIATION
MONITOR
Gn
9
3.01k
4.99
C2
2.09k
Wbar
19
Wbar
Ebar
18
Ebar
C2
Q3
Q2
Q1
Q0
28
25
23
21
OUTEN
4.99
+5V
C2
+5V
Dpfloat
Dp
8
6
Dn
10
4.87k
4.87k
100k
200k
LM124
LM124
LM124
LM124
200k
100k
200k
4.87k
100k
100k
200k
100k
4.99
C2
1k
1k
1k
PROCAL
C1
C1
C1
C1
ELEFLT
ELECAL
SEU71221.PLT

Figure 27. Diagram of the MSX Radiation Experiment SEU/TD computer interface electronics. The capacitor values are C1 = 0.01 μF and C2 = 0.1 μF.

The three total dose MOSFETs located on the chip were described in Figures 22 to 24. These MOSFETs are meant to provide a rough indication of the total dose experienced by the chip. There are a number of open issues at this time that concern the operation of the experiment while in orbit. These include:

1) How often will the SEU/TD Chip be measured in orbit? The total dose MOSFETs will change significantly over days or weeks depending on the shielding and solar flare activity. The SEU/SRAM with 4 kbits will experience several upsets per day depending on the orbit and solar flare activity.

2) What is the shielding above the chip? Shielding alters the total dose and shifts the ratio of electrons and protons reaching the chip.

3) What is the bias on the gate of the MOSFETs during non-measurement times? It is well known that the rate of total dose build-up is a function of the gate bias. During periods when the power is off, the chip must be grounded. If the leads are allowed to float, then the chip will be in an unknown state and data will be difficult to interpret.

4) When will the temperature be monitored relative to SEU/TD Chip measurements? This temperature measurement is needed to interpret the dose measurements, for the threshold voltage is temperature sensitive.

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