A Schottky/2-DEG Varactor Diode for Millimeter and Submillimeter Wave Multiplier Applications

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ABSTRACT

A new Schottky diode is investigated for use as a multiplier element in the millimeter and submillimeter wavelength regions. The new diode is based on the Schottky contact at the edge of a 2-dimensional electron gas (2-DEG). As a negative voltage is applied to the Schottky contact, the depletion layer between the Schottky contact and the 2-DEG expands and the junction capacitance decreases, resulting in a non-linear capacitance-voltage characteristic. In this paper, we outline the theory, design, fabrication and evaluation of the new device. Recent results include devices having cutoff frequencies of 1 THz and above. Preliminary multiplier results are also presented.

I. BACKGROUND

Schottky barrier varactor diodes are used as frequency multiplier elements for local oscillator (LO) sources for the millimeter and submillimeter wavelength region. These sources are used in heterodyne receivers for a variety of applications including radio astronomy, atmospheric studies and plasma diagnostics. For space-based receiver systems, the LO source must be compact, lightweight and reliable; and power and cooling requirements must be minimized. While molecular gas lasers have been used as LO sources for airborne radioastronomy measurements at frequencies as high as 2.5 THz [1,2], the stringent requirements for space applications will require the use of a solid-state LO source. Although standard varactor diodes have been used to generate 0.7 mW at 474 GHz [3] and 0.2 mW at 640 GHz [4], these devices will not provide usable amounts of LO power above about 1 THz [5]. Schottky barrier varistor diodes and quantum well oscillators have been proposed as sources of LO power but these technologies will not provide sufficient power to drive the GaAs Schottky barrier mixer diodes used in these receivers [6,7,8]. We report here on a new planar varactor diode in which the Schottky contact is formed at the edge of the 2-dimensional electron gas (2-DEG). This new device, which is essentially the 2-d analog of the standard (3-d) Schottky diode, has unique properties and is a promising candidate for use in millimeter and submillimeter wave multiplier applications [9,10]. In addition, it may be possible to use this device to investigate conduction in a 2-d electron gas at frequencies significantly above 100 GHz.
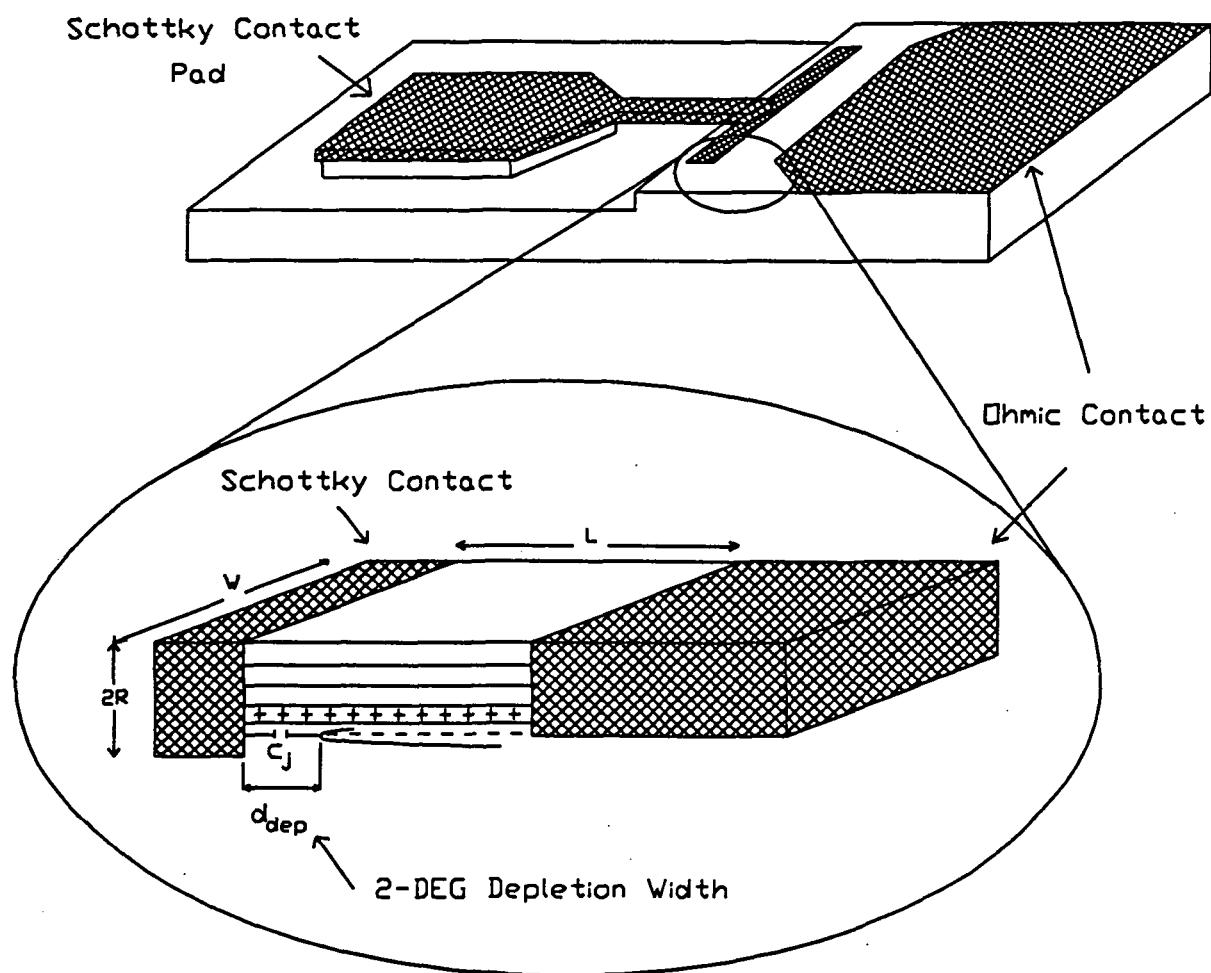
Fig. 1.   Schematic of the planar Schottky/2-DEG varactor diode.

In Section II, the theory of the device and the design for multiplier applications is reviewed. In Section III, the fabrication of the devices is briefly described. The low frequency evaluation is presented in Sections IV and V for the interdigital-type and the "refined prototype" devices, respectively. The preliminary multiplier performance of the "refined prototype" devices are presented in Section VI. Finally, a summary of the work and outlook for future research is presented in Section VII.

II. THE SCHOTTKY/2-DEG DIODE

A. Overview

A sketch of the Schottky/2-DEG diode is shown in Fig. 1. Also shown is an expanded view of the Schottky contact region. The chip dimensions are typically 100 μm by 200 μm by about 50 μm thick. Two device configurations are discussed in this paper. These are the interdigitated contact device (also described in [9,10]) and the "refined prototype" device which is similar to that shown in Fig. 1. The interdigitated devices have been realized in both single and dual anode configurations, the latter being intended for symmetric C(V)
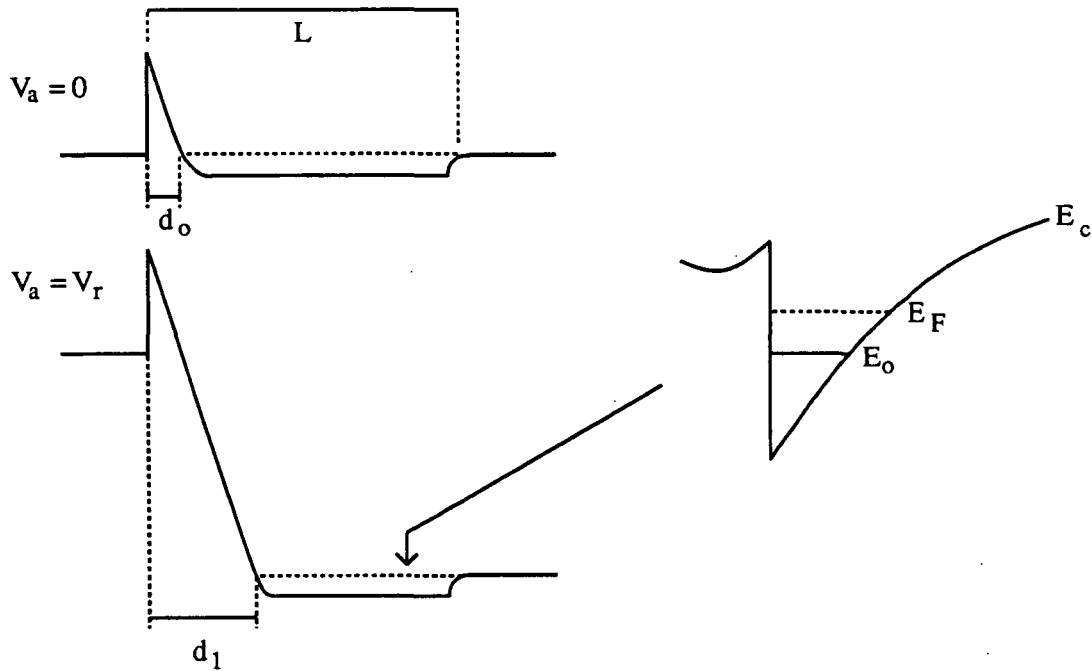
Fig. 2.   Conduction band diagram of the Schottky/2-DEG diode. The 2-DEG is bounded on the left by a Schottky contact and on the right by an ohmic contact. The depletion depths for two applied voltages are shown (left). A qualitative sketch of the potential well in the undepleted channel is shown (right) with the Fermi and lowest sub-band energies indicated.

applications. These devices had Schottky contact widths in the range 150-350 μm. The "refined prototype" devices are single anode devices (whose cathode is an ohmic contact) with widths of about 100 μm. The isolation between pads is achieved by etching through to the semi-insulating GaAs substrate everywhere except in the channel region and beneath the pads. Further details of the fabrication process are outlined in Section III.

B. Physics and Equivalent Circuit

The conduction band diagram of the Schottky/2-DEG diode is shown in Fig. 2. The theory of the metal/2-DEG junction was first considered in [11] and more recently extended in [12]. In [12], the junction capacitance was derived using a conformal mapping technique and by making suitable assumptions about the boundary conditions. The capacitance-voltage characteristic was given by the expression

$$C_j(V) = \frac{W\varepsilon}{\pi}\ln[\frac{(R^2 + d_{dep}^2)^{1/2} + R}{(R^2 + d_{dep}^2)^{1/2} - R}] \tag{1}$$

where W is the width of the contact (see Fig. 1), ε is the permittivity of GaAs and R is the
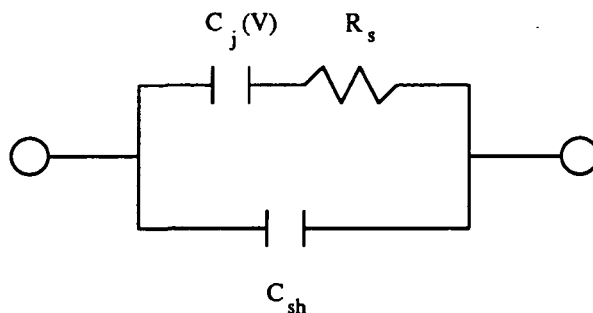
C$_j$(V)   R$_s$

Fig. 3.   A simple equivalent circuit model of the Schottky/2-DEG diode.

half-height of the Schottky metalization. The depletion depth d$_{dep}$ of the 2-DEG is given as

$$d_{dep} = \frac{2\varepsilon(V_{bi} - V_a)}{qn_s}$$ (2)

where V$_{bi}$ is the built-in voltage (0.7-1.0 V), V$_a$ is the applied voltage (which is negative for reverse-bias), and n$_s$ is the 2-DEG sheet charge density. For a 2-DEG sheet charge density of 10^{12} cm^{-2} (10^{13} cm^{-2}) and assuming ε of GaAs, the 2-DEG depletion depth is 3 μm (0.3 μm) at 20V reverse bias. The total capacitance is equal to the junction capacitance in parallel with the shunt capacitance associated with the pad-to-pad fields and anode-to-ohmic fields.

The equivalent circuit is shown in Fig. 3. For simplicity, the junction conductance is neglected. [The skin effect is probably not important for this device since the length and depth of the 2-DEG are small]. Also, the inductive effect of charge carrier inertia is neglected although this effect may be important at cryogenic temperatures due to the long momentum relaxation time of the 2-DEG. The junction capacitance C$_j$ can be estimated using Eq. 1. The series resistance, R$_s$, is composed of the resistance of the undepleted channel and the ohmic contact resistance. The former is given by

$$R_s = \frac{(L - d_{dep})}{q\mu_n n_s W}$$ (3)

where L is the channel length and μ$_n$ is the electron mobility in the undepleted channel. The ohmic contact resistance is simply R$_{OC}$ = r$_{sc}$/W where r$_{sc}$ is the specific contact resistivity (normally specified in units Ωmm) of a HEMT-like ohmic contact, and W is the device width (in mm). The shunt capacitance term C$_{sh}$ includes pad-to-pad capacitance and Schottky-to-ohmic capacitance. For high frequency design, C$_{sh}$ and the R$_s$ must be minimized.

The theory of the junction breakdown has not been fully developed. However, V$_{br}$ in long channel devices is assumed to be caused either by impact ionization or by tunneling. Experimental observations of very large breakdown voltages in prototype devices [9] lead to the conclusion that for short channel length devices, the breakdown voltage was limited by punch-through. In this paper, those devices with channel lengths of 1 μm are probably punch-through limited whereas the 2-3 μm length devices may be limited by impact ionization or

tunneling, or both. The breakdown voltage may also be limited by the geometry of the anode metalization (for example, the half-height R) or by processing and material defects. A more detailed discussion of the breakdown in these devices will be presented in a later paper.

C. Frequency and Power Limitations

Several factors limit the frequency response and power performance of the multiplier. The frequency response may be limited by the dynamic cutoff frequency which is usually defined [13] as

$$v_{co} = \frac{S_{max} - S_{min}}{2\pi R_s}$$ (4)

where S_{max} (S_{min}) is $1/C_{min}$ ($1/C_{max}$), and R_s is the series resistance of the varactor diode. It is desirable for the device to have a v_{co} value much higher than the operating frequency to ensure that the multiplier efficiency is not degraded. To achieve high v_{co}, the series resistance should be as small as possible, the minimum capacitance (near breakdown) should be small and the capacitance modulation ratio C_{max}/C_{min} should be large.

Another important quantity which may limit both the frequency response and maximum output power is the finite velocity of the electrons traversing the modulation region (the epilayer in GaAs diodes or the 2-DEG channel in the Schottky/2-DEG diode). Recently, Kollberg et al [14] showed how the finite electron velocity limited the current in the 6P4 diode used by Erickson [3]. Kollberg argued that the ac displacement current could not exceed the saturation current which in turn is limited by the electron drift velocity. Using Monte Carlo analysis, the effective velocity and the saturation current in the 6P4 diode were estimated (in [14]) to be 2.4×10^7 cm/s and 44 mA, respectively. At input powers beyond that which causes the current to saturate, the diode's rf impedance increases (since the current cannot). Kollberg used this analysis to simulate the roll-off in efficiency with input power, which was observed by Erickson.

The velocity saturation current is written here for the 2-d case as

$$I_{vs} = qn_s v_{eff} W$$ (5)

where n_s is the 2-dimensional sheet charge density, W is the contact width and v_{eff} is the effective velocity of the electrons in the channel. As will be shown, a Schottky/2-DEG diode with $W = 100\,\mu m$ and $n_s = 1.85 \times 10^{12}\,cm^{-2}$ has roughly the same characteristics as the 6P4 diode. Assuming the same effective velocity as was used for the 6P4, namely $v_{eff} = 2.4 \times 10^7$ cm/s, I_{vs} is about 70 mA.

The finite electron velocity may also limit the frequency response if the transit-time for electrons traversing the modulation region is comparable to the period of the LO frequency. The transit-time corner frequency has been proposed [10] as a useful design parameter for the diode's frequency response, and is defined as

$$v_{tt} = \frac{v_{eff}}{2\pi L}$$ (6)

where L is the channel length (or the epilayer thickness in the standard diode). Note that the

frequency given by Eq. 6 is a corner frequency since, as the frequency increases beyond this value, the maximum rf modulation length shortens, resulting in a smaller capacitance ratio and thus to a roll-off in the multiplier efficiency. For example, assuming an effective electron velocity of 2.4×10^7 cm/s (as was used in [14]), a varactor diode with input frequency of 80 GHz will have a maximum modulation length of about 0.48 μm. In comparison, the 6P4 diode, which is often used at this frequency, has an epilayer thickness (and maximum dc modulation length) of about 1.0 μm. Thus, both standard and 2-DEG diodes should be designed to achieve a large capacitance modulation ratio within the length given by Eq. 6.

Having outlined the equations for the capacitance, resistance, punch-through voltage (Eq. 2 with $d_{dep} = L$), the dynamic cutoff and the transit-time frequencies and the saturation current, the Schottky/2-DEG diode may be designed for particular applications. This procedure is simplistic but is similar to the design of the state-of-the-art varactors currently in use. This design procedure was used for the "refined prototype" devices whose results are given in Section V. Before presenting the device results, the fabrication will be briefly reviewed.

III. FABRICATION

The prototype Schottky/2-DEG devices discussed here were fabricated on a pseudomorphic $Al_{.25}Ga_{.75}As/In_{.15}Ga_{.85}As/$ GaAs structure shown in Fig. 4. This structure was grown by MBE and analyzed using the Van der Pauw method to determine the mobility and sheet charge density. The electron sheet charge density at both 77 K and 300 K was 1.85×10^{12} cm^{-2} and the electron mobilities were 31,400 cm^2/V-s and 6640 cm^2/V-s at 77 K

Layer			
1	GaAs	5×10^{18} cm^{-3}	40 Å
2	$Al_{0.25}Ga_{0.75}As$	5×10^{17} cm^{-3}	300 Å
3	Si Atomic Plane	5×10^{12} cm^{-2}	--
4	$Al_{0.25}Ga_{0.75}As$	--	50 Å
5	$In_{.15}Ga_{.85}As$	--	150 Å
6	GaAs	--	5000 Å
7	SI GaAs Substrate		

Fig. 4.   AlGaAs/InGaAs/GaAs heterostructure used for the devices discussed here.
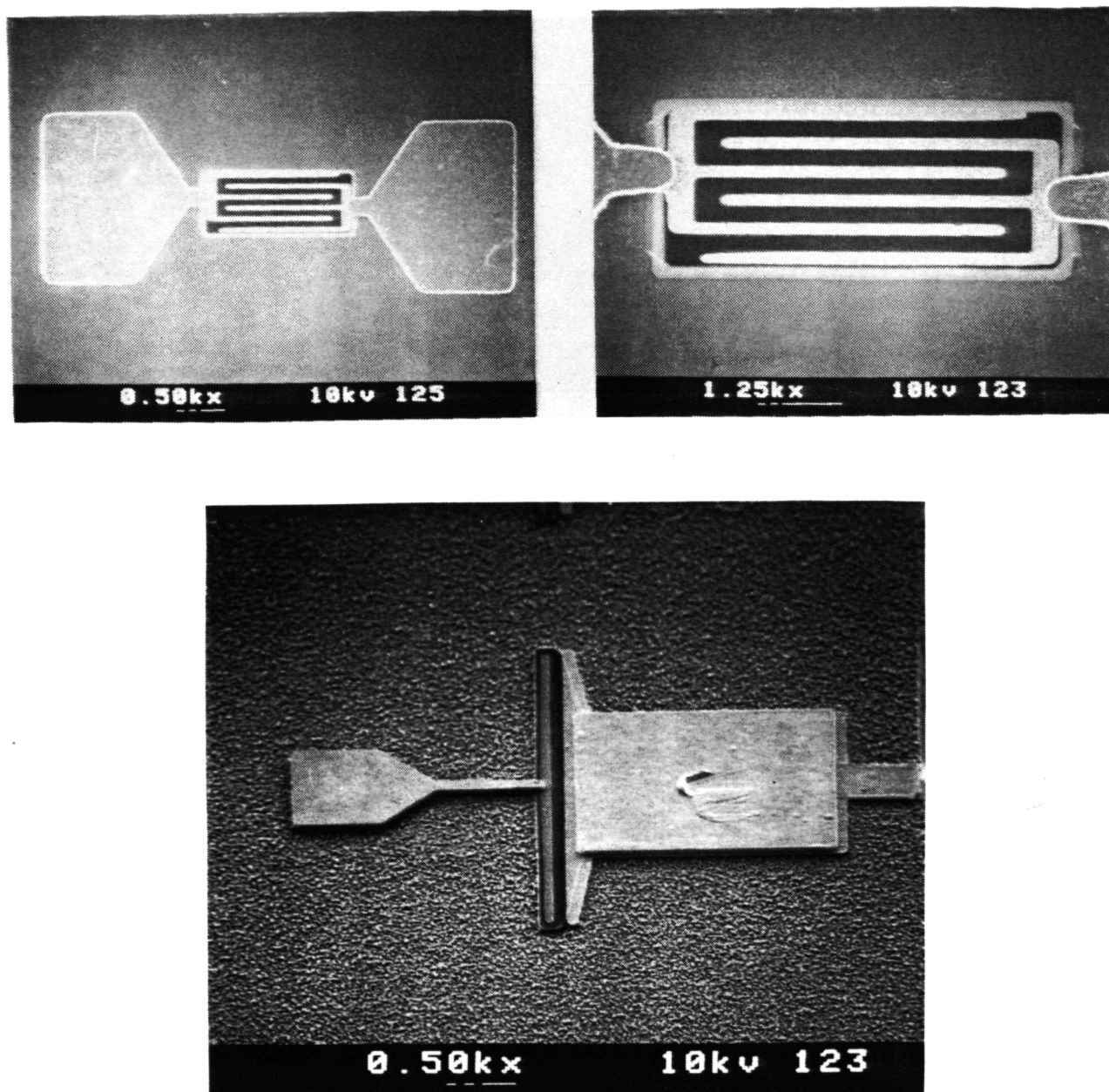
Fig. 5. *Scanning electron micrographs of Schottky/2-DEG devices. The interdigitated device (top) has anode width of 250 μm and channel length of 2 μm. The "refined prototype" device (bottom) shown here is similar to the devices discussed in Section V. Here, the anode width is 100 μm and the channel length is 5 μm.*

and 300 K, respectively. The supply and cap layers are substantially depleted to the 2-DEG and/or the surface, to minimize parallel conduction. The ohmic contact consists of an electroplated SnNi/Ni/Au trilayer which is alloyed at about 380°C. To form the Schottky contact, a trench is etched through the 2-DEG layer and a Pt/Au contact is electroplated into the trench. Next, the contact pads are plated and finally a 2-3 micron deep $NaOH:H_2O_2$ etch to the SI-GaAs substrate is performed to isolate the two pads. All lithography levels are performed using a Karl Suss MJB-3 (405 nm). An SEM photo of the interdigitated device is shown in Fig. 5 (top). A sketch of a "refined prototype" is also shown (bottom). The rough surface of this device was due to the isolation etch, performed using chlorine reactive ion etching. A subsequent wet chemical etch reduced the surface roughness considerably.

IV. LOW FREQUENCY EVALUATION OF INTERDIGITATED DEVICES

The dc evaluation of the Schottky/2-DEG diodes include I(V), C(V) and reverse breakdown voltage measurements. First, the interdigitated device results are presented (these results were also presented in [10]). The forward and reverse I(V) of a single Schottky/2-DEG device is shown in Fig. 6 (top), measured at room temperature. The exponential diode characteristic is seen as the linear portion of this semi-log I(V) plot, in the range 0.35 - 0.7 V. The "knee" voltage (at 1 μA) was 0.512V. The ΔV values for the current intervals 0.1 - 1.0μA, 1.0 - 10.0μA and 10.0 - 100μA are 74mV, 74mV and 81mV, corresponding to inverse slope parameters, V_o, of 32.1mV, 32.1mV and 35.2mV, respectively. This corresponds to a diode ideality factor of 1.26. The series resistance of this device was determined to be 56Ω. The expected 2-DEG channel resistance at room temperature is 6 Ω. Allowing for a pessimistic value of the ohmic contact resistivity, r_{sc} of 2.5 Ωmm, the total series resistance expected for this device was about 16 Ω. The remaining 40 Ω series resistance is most likely due to insufficient plating of the ohmic contacts, as was substantiated by inspection using scanning electron microscopy. The dual anode devices have no ohmic contact resistance. In these devices, the I(V) is dominated by the characteristic of the reverse-biased junction and a series resistance measurement cannot be made. However, using Eq. 3, the L = 2μm, W = 250μm device resistance is about 4 Ω at 295K and about 1.0 Ω at 100 K due to the increase in mobility upon cooling.

The C(V) curves of the single and dual anode interdigitated devices are shown in Fig. 6 (bottom). The channel length (gap between fingers) is 2 μm (3 μm) for the dual (single) Schottky device. The anode widths were 250 μm for both devices. As expected, the dual Schottky device has a nearly symmetric C(V) characteristic and it's zero-bias capacitance is about half that of the single anode device. Subtracting the pad-to-pad capacitance which was measured to be 4 fF, this symmetric C(V) device had a dynamic cutoff frequency of about 1 THz at 295K and about 4 THz at 100 K. The velocity saturation current (Eq. 5 using $v_{eff} = 2.4 \times 10^7$ cm/s) is 178 mA. Also, the transit-time corner frequency of the 2 μm channel length device is about 19 GHz, calculated using Eq. 6. The capacitance levels of the dual anode device is probably too high for most multiplier applications. Nevertheless, multiplier testing of these devices will be performed in the near future.
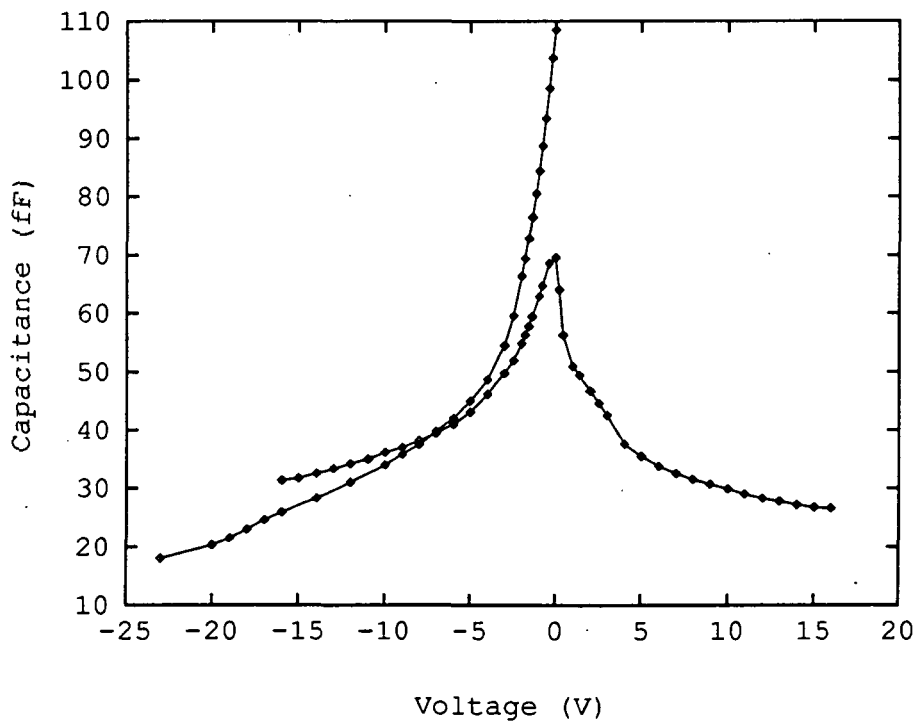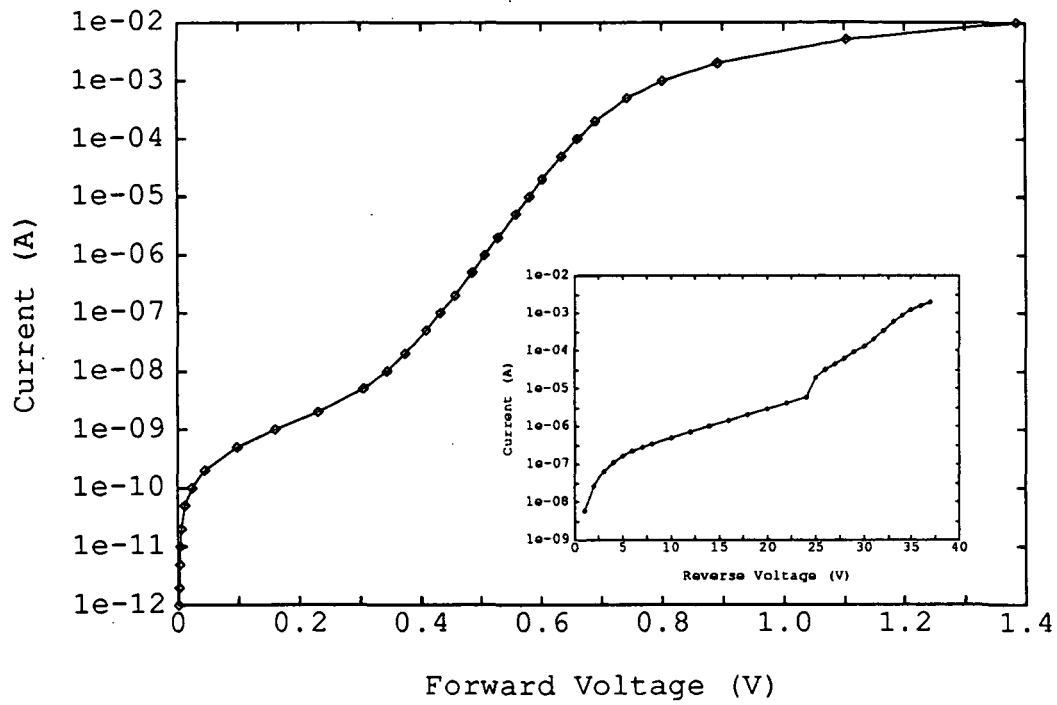
Fig. 6. *Forward and reverse I(V) of single anode interdigitated device (top) with*
W = 250 μm *and* L = 3.0 μm. *C(V) characteristics (bottom) of* L = 3.0 μm *single and*
L = 2.0 μm *dual anode interdigitated devices of width 250 μm.*
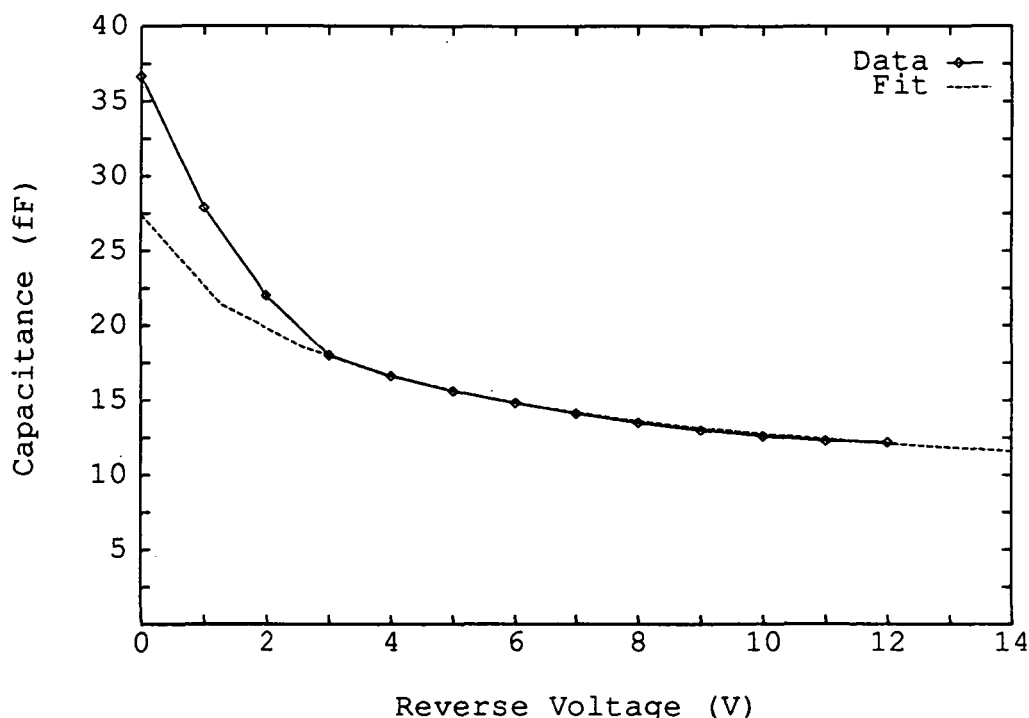
Fig. 7.   *C(V) of refined prototype device A. Also shown is a fit (Eq. 1) using* R = 0.75 μm,
C_{sh} = 8.0 fF, V_{bi} = 0.7 V and W = 90 μm.

V. LOW FREQUENCY EVALUATION OF REFINED PROTOTYPE DEVICES

The refined prototype devices had two anode width/channel length combinations. The "A" devices had anode widths of 90 μm (on average) and channel lengths of 2.5 μm while the "B" devices had anode widths of 80 μm and channel lengths of 3.0 μm. The C(V) characteristic of device A is shown in Fig. 7. The theoretical capacitance, shown fitted to the data, agrees well with the data except near zero-bias where the fit is lower than the data. The fit assumed a reasonable value of the anode metal half-height (R = 0.75 μm) and a shunt capacitance of 8.0 fF. This value of C_{sh} is higher than expected since the pad-to-pad capacitance was measured to be about 2 fF. The additional shunt capacitance may be due in part to fields between the anode and ohmic metals. This contribution to the capacitance is not easily determined and is also not substracted for the v_{co} calculations. The difference between the theory and the data near zero-bias is either due to inaccuracy of Eq. 1 for the geometry of this device or to effects related to the leakage current at low bias. We are currently investigating a more general theory of the junction capacitance for devices of various geometries.

The forward I(V) as a function of temperature of device A is shown in Fig. 8. As the temperature decreased, several changes occured. First, the entire I(V) curve shifted to higher voltages, as expected due to the temperature dependence of the saturation current (the theory of the thermionic saturation current of the Schottky/2-DEG junction is being investigated [15]). At lower currents, the "leakage" current which has been routinely observed at room temperature is seen to decrease substantially so that, at 220 K, it is much less than one nanoamp. Finally, the strong temperature dependence of the series resistance is evident at high currents.
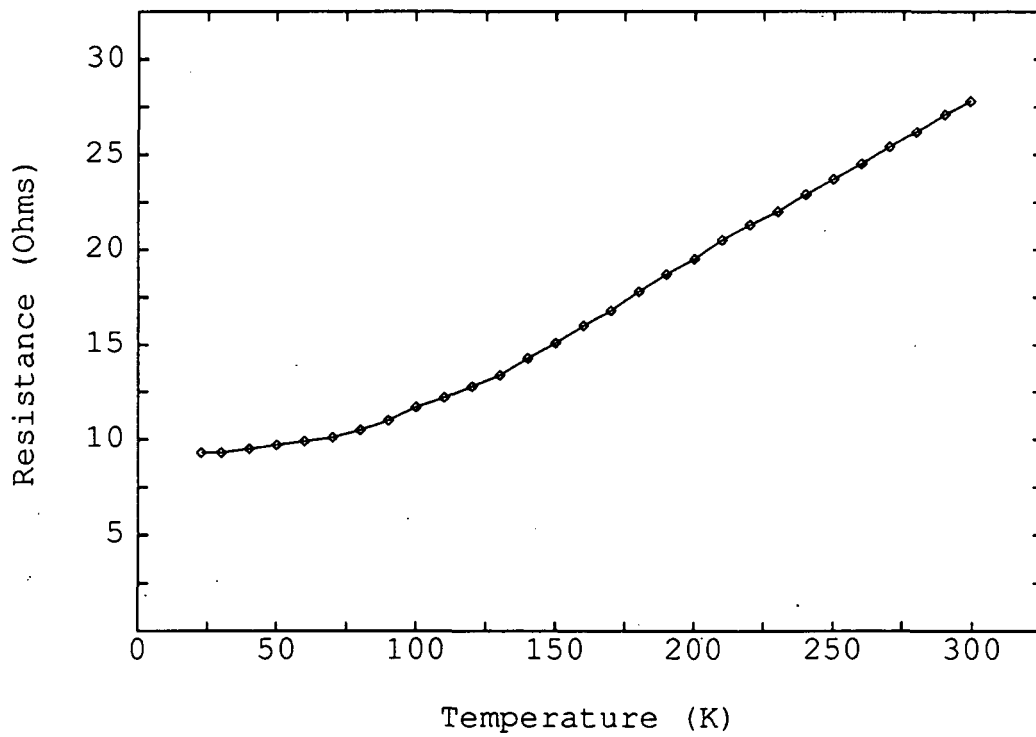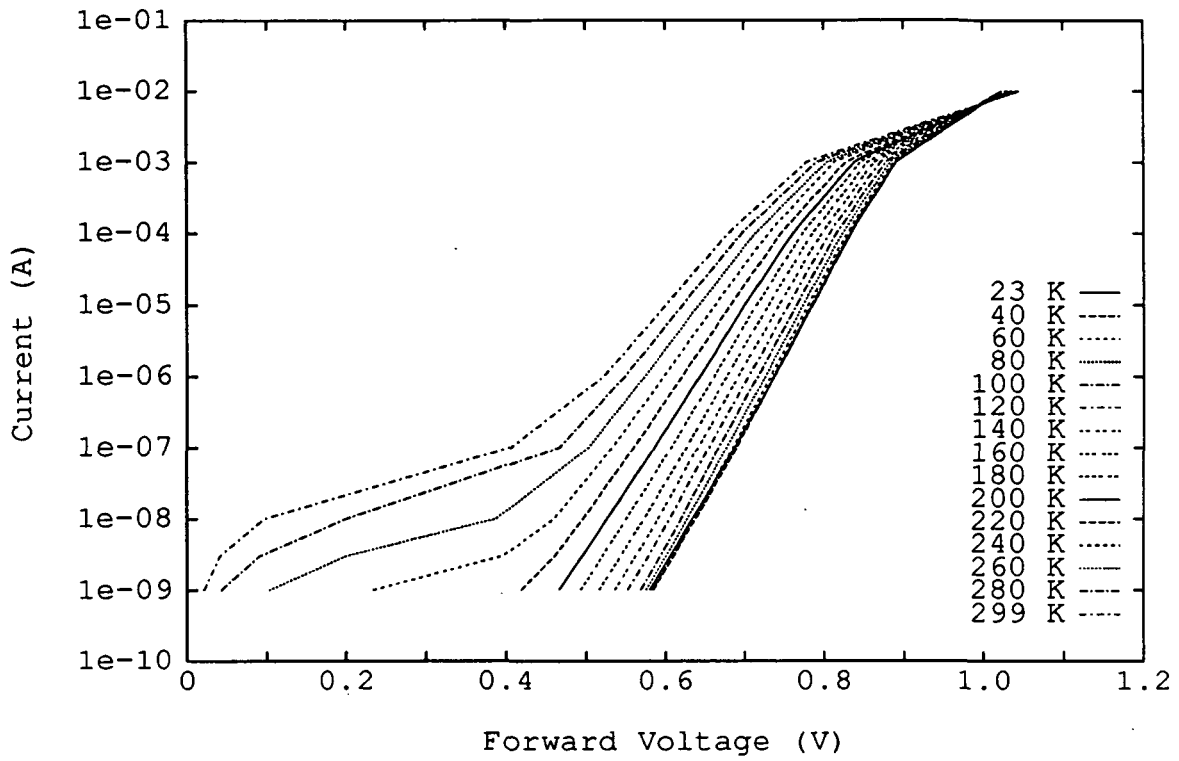
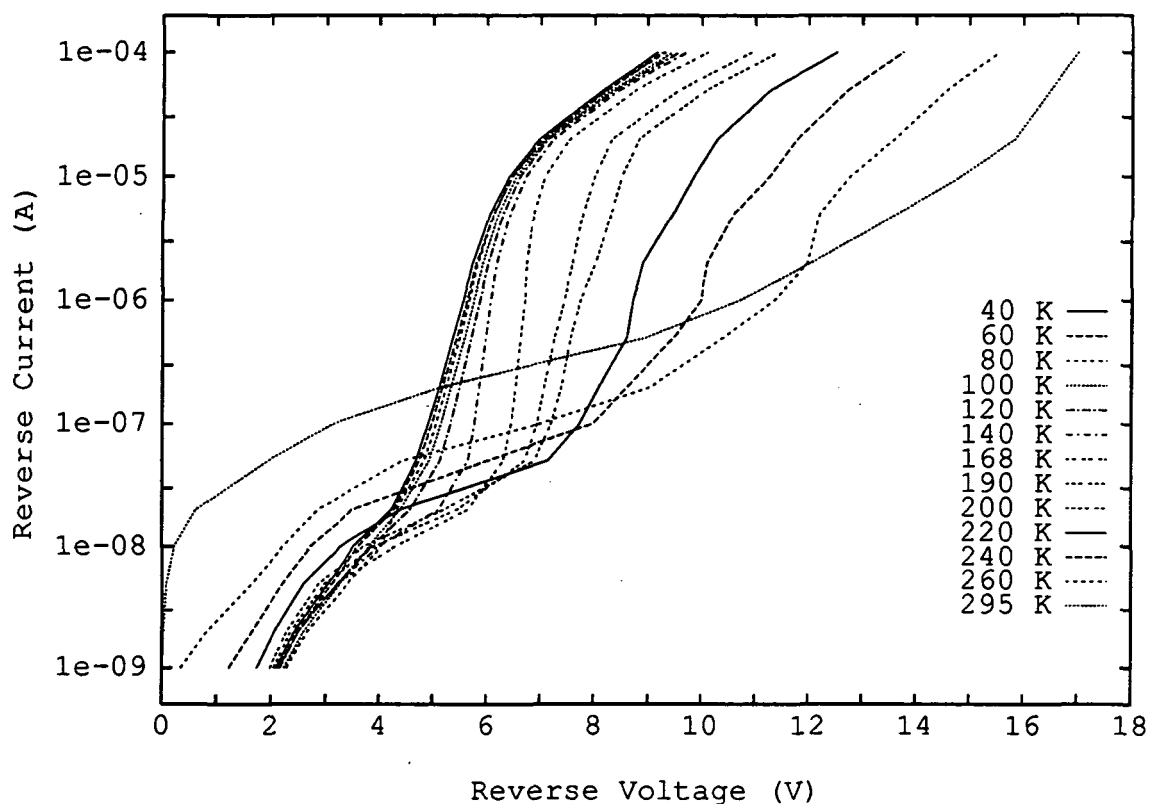*Fig. 8.   Forward I(V) (top) and series resistance (bottom) versus temperature of device A.*

Fig. 9.   Reverse I(V) versus temperature of device A.

The measured series resistance of device A is plotted as a function of temperature in Fig. 8 (bottom). The resistance decreased nearly linearly from 19.9 Ω at 300 K to 10.5 Ω at 130 K, and the resistance at 77 K was 8.9 Ω. The 2-DEG resistances calculated using Eq. 3 with the low field mobility values at 300 K and 77 K are 14.1 Ω and 3.0 Ω, respectively. Thus, the ohmic contact resistivity (for the width 90 μm) is estimated to be about 0.6 Ωmm. This value of r_{sc} is much lower than was achieved on the earliest Schottky/2-DEG devices. The improvement is probably a consequence of the higher doping at the heterostructure surface and an improved ohmic plating and alloying procedure. Further reduction of r_{sc} (perhaps to 0.1 Ωmm) should be possible using evaporated Ni/Ge/Au ohmic contacts.

The reverse I(V) of device A was measured as a function of temperature and is shown in Fig. 9. As in the forward I(V), the leakage current is seen to decrease upon cooling. At the highest reverse current (100 μA), the reverse voltages decreased with temperature from 17 V at 300 K to about 9 V at 40 K. This temperature dependence of the breakdown voltage is qualitatively consistent with impact ionization theory. Since the mean free path for electron phonon interactions increases with decreasing temperature, the electrons can achieve higher kinetic energies before phonon scattering occurs. Consequently, as the temperature decreases, electrons reach the impact ionization energy at lower field strengths (lower reverse voltages) and the breakdown voltage decreases.
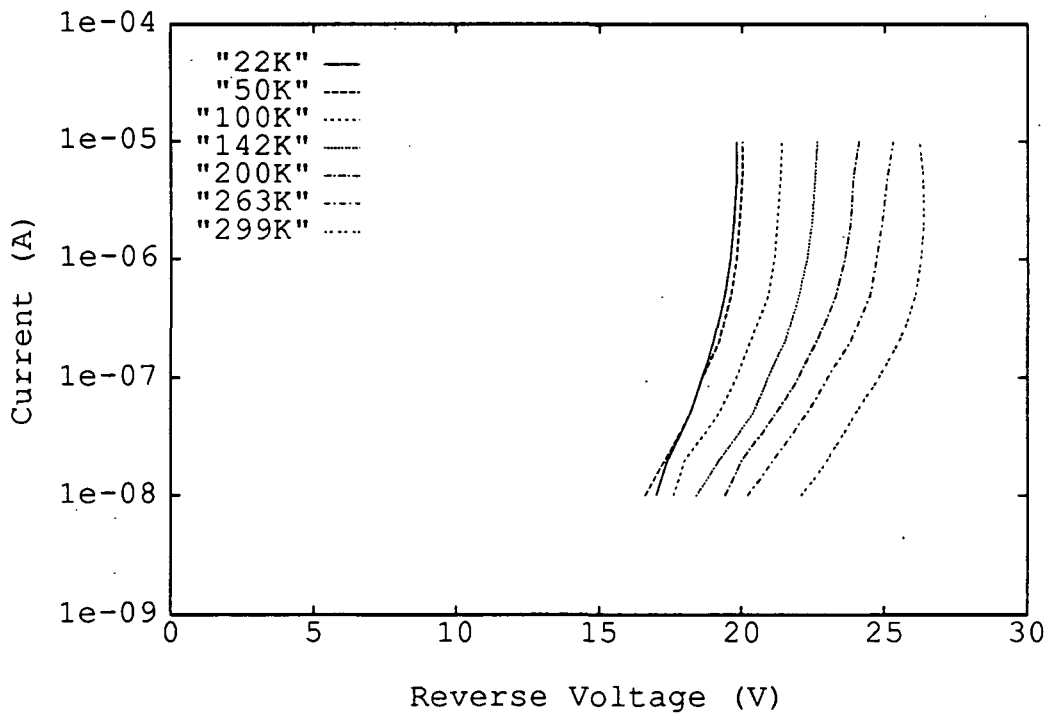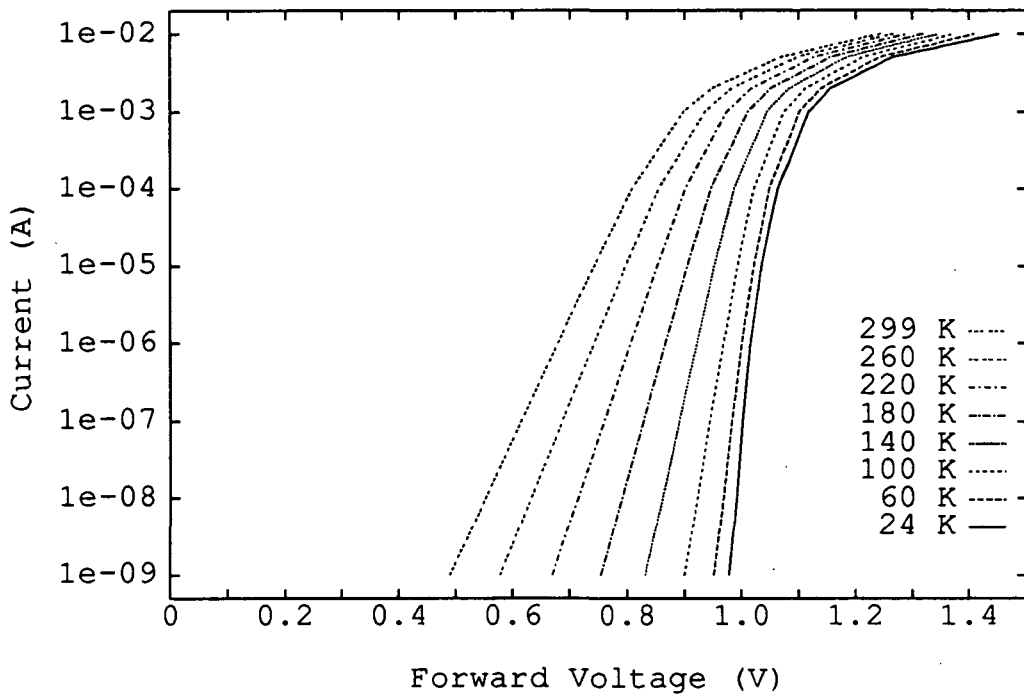
Fig. 10. Forward I(V) (top) and reverse I(V) (bottom) vs. temperature of planar GaAs Schottky diode SC6T1.

The temperature dependence of the breakdown voltage of the Schottky/2-DEG diode raised the question of whether the breakdown voltage in standard GaAs varactors had a similar temperature dependence. To investigate further, the I(V) of several planar GaAs varactor diodes (UVA-SC6T1) were measured as a function of temperature. The doping concentration and anode diameter for this diode were 2×10^{16} cm^{-3} and 6 μm, respectively, compared to the respective values 3×10^{16} cm^{-3} and 6 μm for the whisker-contacted UVA-6P4 diode. The forward and reverse I(V) of one device is shown in Fig. 10. The forward I(V) is typical for a low doped diode. Here, the knee voltage increased from 0.678 V at 299K to 1.015 V at 24K. The inverse slope parameter decreased from 28.7 mV at 299 K to 12.7 mV at 24 K. The series resistance was constant and equal to 30 Ω (± 1 Ω) over the range 24-299 K. The reverse I(V) was measured from 10 nA to 10 μA. The breakdown voltage characteristics are all very sharp. Of the three SC6T1 diodes tested, all had breakdown voltages of 18-19 V at 24K, although the room temperature breakdown voltages were 26 V, 29 V and about 30 V. Thus, the average reduction in V_{br} was about 35 percent upon cooling, compared to a reduction of about 50 percent for the Schottky/2-DEG diode. A decreasing breakdown voltage in these devices upon cooling may impact the low temperature multiplier performance. On the other hand, the large decrease in the series resistance of the 2-DEG upon cooling should result in higher multiplier efficiency.

Finally, the saturation drift current of device A was calculated, using Eq. 5 with $v_{eff} = 2.4 \times 10^7$ cm/s, to be 64 mA. This may be a conservative estimate since higher velocities may be possible in the 2-DEG than in bulk GaAs. In any case, the Schottky/2-DEG diode of roughly equivalent properties as those of the 6P4 diode has a significantly higher saturation current (at least 64 mA) than does the 6P4 diode (44 mA according to [14]).

VI. PRELIMINARY MULTIPLIER RESULTS

The first rf measurements of a Schottky/2-DEG diode were performed at the National Radio Astronomy Observatory using a modified NRAO tripler which was designed [16] for whisker contacted diodes (such as the UVA-6P4). The Schottky/2-DEG diode chip was soldered across the output waveguide. A klystron was used as a source and two power meters were used to measure the power at the input and output ports of the multiplier. Further details of the measurement setup may be found in [17].

The preliminary measurements were of device A having chip width and length dimensions of 100 μm and 180 μm. The chip thickness was about 60 μm. After soldering, the clearance between the back of the chip and the waveguide wall was estimated to be only 2-3 μm, due in part to the thick solder "bump". The I(V) of the device was checked after soldering and found to be the same as before soldering. The room temperature R_s and V_{br} of this device were 20 Ω and 12 V, respectively.

The first multiplier test was to determine the optimum frequency. Using 50 mW input power, the multiplier tuners and dc bias were optimized for maximum output power at several frequencies over the range 70-79 GHz. The result is shown in Fig. 11 where the input power was 50 mW. The best performance was obtained at 75 GHz where P_{out} was 160 μW at 225 GHz. The input return loss was measured at 75 GHz to be about -20 dB so the input tuning was relatively well optimized. Next, the output power at 225 GHz was measured as a function of
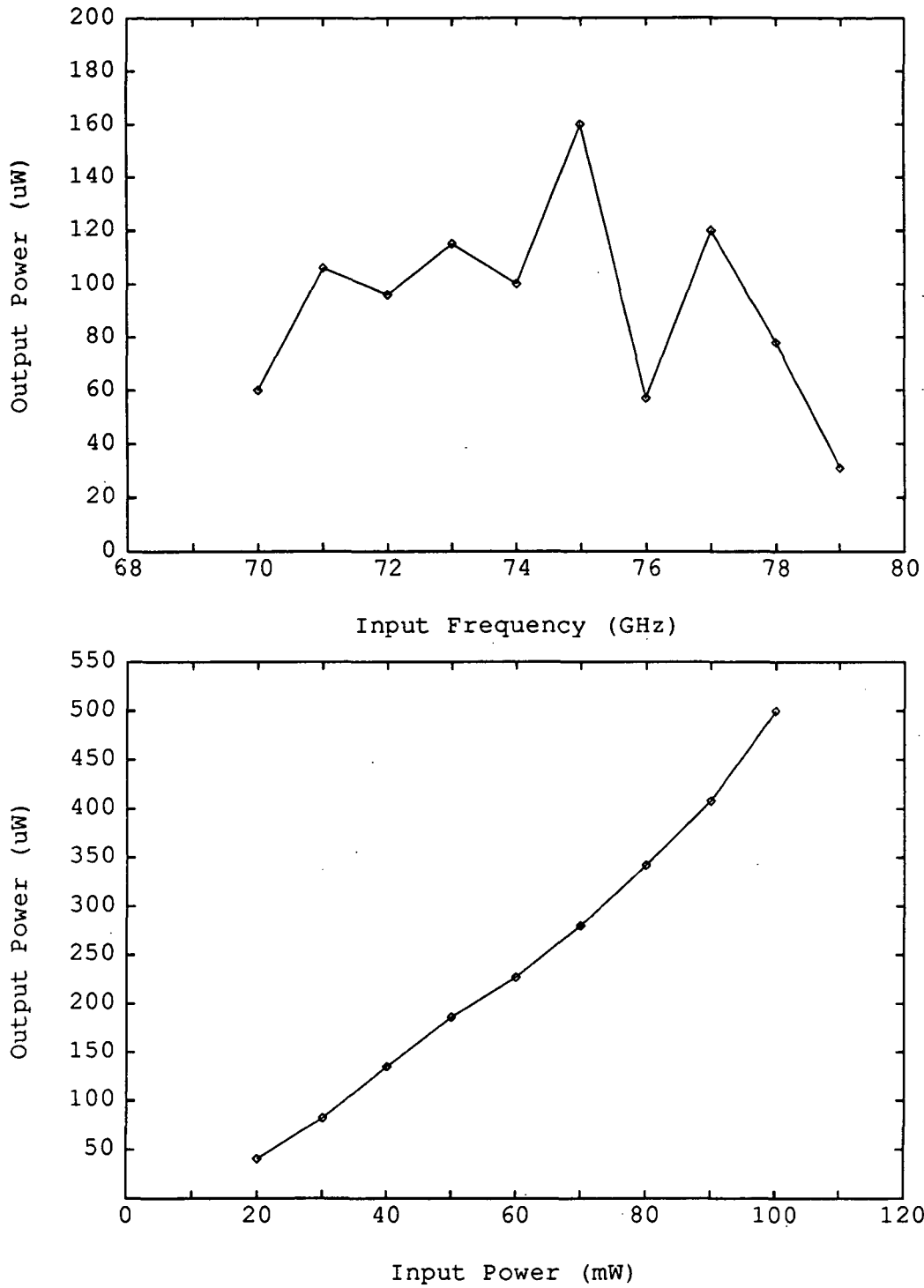
Fig. 11. Tripler output power versus input frequency (top) with $P_{in} = 50$ mW and output power versus input power (bottom) for tripling to 225 GHz.

the input power, as shown in Fig. 11 (bottom). P_{in} was varied over the range 20 -100 mW. As the input power increased, the output power increased, reaching a maximum value of 500 μW at 100 mW at the input. This corresponds to an efficiency of 0.5 percent. In comparison, Bradley [17] used this multiplier with a planar GaAs varactor of doping 1.1×10^{17} cm^{-3} and diameter 7 μm and obtained 3.7 mW output power and 4.1 percent efficiency at 219 GHz. This first multiplier measurement of the Schottky/2-DEG diode is encouraging but much higher performance should be possible. Even the current devices should yield higher multiplier efficiencies if they are thinned to 25 μm or less and if a thinner solder layer is used to reduce the shunt capacitance between the chip and the waveguide wall.

VII. SUMMARY AND FUTURE RESEARCH

In summary, we have reported on the recent progress in the research of a novel Schottky/2-DEG varactor diode. Observations of reduced breakdown voltages upon cooling in both the standard GaAs and the novel Schottky/2-DEG diodes were in agreement with the theory of impact ionization. The problem of current saturation was discussed and the Schottky/2-DEG diode of width 90 μm was found to have a significantly higher saturation current than the comparable GaAs 6P4 varactor. Recent improvements to the design and fabrication procedures have resulted in devices having lower series resistance and lower capacitance. Both single anode and dual anode (with symmetric C(V)) devices have been investigated. The cutoff frequency of the dual anode device was estimated to be 1 THz (4 THz) at 300 K (100 K), whereas the single anode device had cutoff frequency of about 0.6-1.0 THz, depending on the temperature. Preliminary multiplier measurements of a single anode device were encouraging, resulting in 500 μW output power at 225 GHz with 0.5 percent efficiency. Ongoing research will include more extensive multiplier testing of both the single anode and the symmetric C(V) devices. Also, shorter channel length devices with Ni/Ge/Au ohmic contacts will be fabricated to achieve much higher cutoff and transit-time frequencies. In addition, AlInAs/InGaAs/InP heterostructures will be investigated. Finally, the theories relating to the junction capacitance and breakdown are being developed and the current transport in these devices will be investigated using Monte Carlo simulations.

ACKNOWLEDGEMENTS

REFERENCES

[1] H. P. Röser, "Heterodyne Spectroscopy for Submillimeter and Far-Infrared Wavelengths From 100 μm to 500 μm," Infrared Physics, Vol. 32, pp. 385-407, 1991.

[2] J. Zmuidzinas, A.L. Betz, and R.T. Boreiko, "A Corner-Reflector Mixer Mount for Far Infrared Wavelengths," Infrared Phys., Vol. 29, No. 1, 119-131, 1989.

[3] N. Erickson, "High Efficiency Submillimeter Frequency Multipliers," The 1990 IEEE MTT-S Int. Microwave Symposium, Dallas, TX, May 1990.

[4] P. Zimmermann, private communication, March and May 1990.

[5] T. W. Crowe, W.C.B. Peatman, and E. Winkler, "GaAs Schottky Barrier Varactor Diodes for Submillimeter Wavelength Power Generation," Microwave and Optical Tech. Lett., Special Issue: Space Terahertz Tech., Vol. 3, No. 1, January 1991.

[6] K. Benson and M.A. Frerking, "Theoretical Efficiency for Triplers Using Nonideal Varistor Diodes at Submillimeter Wavelengths," IEEE Trans. Microwave Theory Tech., Vol. MTT-33, No. 12, 1367-1374, Dec. 1985.

[7] C. Kidner, I. Medhi, J. East, G. Haddad, "Performance Limitations of Resonant Tunneling Diodes," The First Int'l. Symposium on Space Terahertz Technology, Ann Arbor, MI, March 1990.

[8] H. Rothermel, T.G. Phillips, J. Keene, "A Solid-State Frequency Source for Radio Astronomy in the 100 to 1000 GHz Range," Int. J. Infrared and Millimeter Waves, Vol. 10, No. 1, 83-100, 1989.

[9] W. C. B. Peatman, T. W. Crowe and M. Shur, "Design and Fabrication of Heterostructure Varactor Diodes for Millimeter and Submillimeter Wave Multiplier Applications," Proc. IEEE/Cornell Conf. on Advanced Concepts in High Speed Semic. Dev. and Circuits, Ithaca, NY, 1991.

[10] W.C.B. Peatman, T.W. Crowe and M. Shur, "A Novel Schottky/2-DEG Diode for Millimeter and Submillimeter Wave Multiplier Applications," *IEEE Electron Device Lett.*, Vol. 13, No. 1, pp. 11-13, January 1992.

[11] S.G. Petrosyan and A. Ya Shik, "Contact Phenomena in a two-dimensional electron gas," Soviet Physics Semicond., 23 (6), pp. 696-697, June 1989.

[12] B. Gelmont, M. Shur and C. Moglestue, "Theory of Junction Between Two-Dimensional Electron Gas and P-Type Semiconductor," to be published, IEEE Trans. Electron Devices, Vol. 39, No. 5, May 1992.

[13] P. Penfield and R. Rafuse, Varactor Applications, MIT Press, 1962, p. 86.

[14] E. Kollberg, T. Tolmunen, M. Frerking and J. East, "Current Saturation in Submillimeter Wave Varactors," Proc. Second Int'l. Symp. Space Terahertz Technology, Pasadena, CA, pp. 307-322, 1991.

[15] B. Gelmont, M. Shur (unpublished).

[16] J. Archer, "An Efficient 200-290 GHz Frequency Tripler Incorporating A Novel Stripline Structure," IEEE Trans. Micrwave Theory and Tech., Vol. 32, No. 4, pp. 416-420, 1984.

[17] R. Bradley, Ph.D. Thesis, University of Virginia, pp. 42-65 May, 1992.