# Rapid Thermal Processing (RTP) of Semiconductors in Space

Progress Report
for 12 Month
Period Ending March 31, 1993

NAG5-1809

Submitted by:

T.J. Anderson (P.I.)
Department of Chemical Engineering

and

K.S. Jones (Co-P.I.)
Department of Materials Science and Engineering
University of Florida
Gainesville, FL 32611

## Introduction and Objectives

This report summarizes the progress achieved under the subcontract No. 375-558-1 to Grant No. NAG5-1809; a subcontract between Clarkson University and the University of Florida. The project is entitled "Rapid Thermal Processing of Semiconductors in Space" and the grantee is Goddard Space Flight Center. The period covered for this report is the 12 month period of activity ending March 31, 1993.

The activity of this group is being performed under the direct auspices of the ROMPS program. The main objective of this program is to develop and demonstrate the use of advanced robotics in space with rapid thermal process (RTP) of semiconductors providing the test technology. Rapid thermal processing is an ideal processing step for demonstration purposes since it encompasses many of the characteristics of other processes used in solid state device manufacturing. Furthermore, a low thermal budget is becoming more important in existing manufacturing practice, while a low thermal budget is critical to successful processing in space.

A secondary objective of this project is to determine the influence of microgravity on the rapid thermal process for a variety of operating modes. In many instances, this involves one or more fluid phases. The advancement of microgravity processing science is an important ancillary objective.

The University of Florida team also provides connectivity between the ROMPS program and the Clarkson CCDS (Center for Commercial Crystal Growth in Space). The objectives of this Center (W.R. Willox, Director) are :

1) To expand industrial support of crystal growth in space.
2) To demonstrate the advantage of space by flying intelligent experiments as often as practical.
3) To develop the technology and capability necessary to grow crystals in space.
4) To develop marketable patents.
5) To develop other marketable products and services.

6) To serve as a user friendly interface to NASA and the space community in order to facilitate commercialization.

Since the semiconductor industry already operates in an environment of high automation with large value-added products, commercialization of space processing will necessitate demonstration of both automation and microgravity processing advantages. Connection with the Clarkson CCDS will permit utilization of their existing commercialization structure. In addition, several companies not involved with this CCDS will provide samples for the program.

The University of Florida team will ground-base and flight process a variety of samples which have an ultimate application in solid state electronics. This industry is the single largest one in the United States. The factory sales of electronics in the U.S. is in excess of $100 billion dollars per year, while the sale of integrated circuits alone exceeds $10 billion dollars. The level of automation in the electronics industry has significantly increased in the past 10 years. The processing of an integrated circuit involves the batch processing of multiple wafers (typically 100-150 wafers) in a sequence of steps. Each batch process is highly automated though the linkages between processing steps is still largely manual. Rapid thermal processing is a specific type of processing step used in this industry and its use has significantly increased in recent years. The technique is used for a variety of purposes; the most common one is to anneal ion implantation damage.

## Ground Base Research and Sample Preparation

A variety of samples will be tested in this project. These samples were chosen to test a wide range of processing conditions (temperature, vapor pressure, etc.), to test a variety of materials (Si, Si-Ge, III-V compound semiconductors, II-VI compound semiconductors), and to test a set of potential microgravity advantages (mainly centered about reduced buoyancy driven convection). The set of samples to be investigated is given in Appendix I. This set and the processing conditions are subject to change, based on the results of ground base testing. One of the positive aspects of this contribution is that the PI's have other research support for many of

these sample preparations. Thus, the funding under this project is highly leveraged and the quality of science and samples can be improved. A short summary of progress in each area is given below.

**Project 1. Closed Space Vapor Deposition of InAs Hall Generators**

Discrete Hall effect devices are presently being fabricated commercially for a broad range of applications including gaussmeters, wattmeters, limit switches and motor commutation. One of the world's largest producers of such devices is F.W. Bell, a small business based in Orlando. Of the many semiconductor materials available for Hall generators, InAs appears to have the best combination of electron mobility (33,000 $cm^2/V \cdot sec$ at room temperature) and temperature coefficient (0.1%/°C at 20°C).

The company currently deposits InAs thin films on $Al_2O_3$ substrates by a closed space vapor deposition process. This process uses $AsCl_3$ as a chemical transport in a rapid thermal, proximity-type growth chamber. Polycrystalline InAs pieces are placed in the recessed area of a bottom quartz plate while the $Al_2O_3$ substrate is placed in the recessed area of a top quartz plate. The source and substrate are separated by a vapor space 1 mm in distance which contains a $H_2/AsCl_3$ mixture. Growth is achieved by rapidly heating the chamber to approximately 850°C for a few minutes. At growth temperature, the $AsCl_3$ thermally decomposes to give HCl which reacts with the polycrystalline InAs to produce volatile InCl and $As_x$. These species then transport to the cooler $Al_2O_3$ substrate and deposit InAs.

The performance and yield of the Hall generators are largely determined by the background carrier concentration, thickness uniformity and microstructure of the deposited film. In addition, drift in the device is determined by the quality of the contacts. The deposition process relies on the heat and mass transfer characteristics of the vapor gap and thus low gravity processing could influence these processes. Similarly, contacts are Cu-based and rapid thermal annealing has been shown to influence the series resistance and subsequent drift characteristics of the device.

It is proposed to investigate the potential of depositing InAs on $Al_2O_3$ by rapid thermal processing in space. The variables to be investigated include processing temperature and $H_2/AsCl_3$ molar ratio. Deposited films will be characterized for impurity content (Hall effect, SIMS, EMPA, SAM, CV profiling), thickness uniformity (SEM after KOH staining) and microstructure (TEM, XRD, Raman spectroscopy). Films will be processed into devices and tested by F.W. Bell. Additionally, contacted Hall generators will be rapidly thermally annealed at a variety of temperatures and tested for drift.

Using the F.W. Bell process, we have grown over 150 films of InAs on alumina. In these growths, the temperature, deposition time, purge time, $AsCl_3$ partial pressure and source material have been varied. We are now in the process of characterizing the films in terms of electrical properties and thickness. The data to date indicate that the films deposited by the Bell process have poor thickness uniformity, with thickness variations as large as 50%. These thickness variations directly lead to variations in the performance of the device. The data also suggest that the background impurity levels vary across the film, producing changes in the electron mobility. Possible causes for the thickness variations include non-uniform heating and buoyancy driven flows. This latter mechanism should be influenced by space processing. A preliminary design for the ROMPS CVD reactor have been given to Ed Aaron.

## Project 2. Rapid Thermal Annealing of Ion Implanted and In-situ Doped ZnS ACTFEL Devices

Alternating current thin film electroluminescent (ACTFEL) devices are used as "cold-light" emitting displays. The largest producer of such devices in the U.S. is Planar Systems, Inc. The device is based on a metal-insulator-semiconductor-insulator-metal (MISIM) type layered structure. The semiconductor of choice is ZnS since it exhibits a large room temperature bandgap (3.54 eV), making it an ideal host for both the electroluminescent impurities and the "hot" electrons necessary for electroluminescence. "Hot" electron injection into the ZnS is

believed to result in electron impact excitation of the impurities (typically rare earths) with a subsequent radiative emission upon deexcitation.

The major problem with full color ACTFEL devices is the inability to fabricate a high brightness device with dominant electroluminescent emission in the blue region of the visible spectrum. The factors which affect the brightness of these devices include the concentration and distribution of the luminescent impurities, the thickness and microstructure of the active semiconductor layer, the applied voltage, the semiconductor/insulator interface and the point defect concentration in the active layer. It has been shown that rapid thermal annealing of structures after deposition of the semiconductor layer improves the efficiency of the devices.

It is proposed to grow ZnS layers on glass/ITO/$BaTaO_5$ substrates by MOCVD. The films will be doped with electroluminescent impurities (e.g., Mn or Tm) and coactivators (e.g., Cl or F) by ion implantation or in-situ doping. Rapid thermal annealing will be used to repair the implant damage and "activate" the luminescent centers. An ambient (Zn or S over pressure) must be maintained above the ZnS to control the concentration of point defects. In addition to the ambient composition, the anneal temperature and time will be studied in an effort to optimize the electroluminescent properties. The annealed films will be characterized for microstructure (TEM, SEM, XRD), composition (SIMS, SAM, EDS) and optical properties (PL, CL). Actual devices will then be fabricated and tested by Planar Systems, Inc.

We have been depositing ZnS by MOCVD onto both Si single crystal and glass-based (Planar supplied) substrates using DEZn and $H_2S$ as the main element precursors. These samples are now being characterized. One issue that we hope to evaluate is the necessity for supply an over pressure of Zn or S during RTP.

Our activities in the ACTFEL device area have greatly expanded in the past 12 months. In addition to the continuing collaboration with Planar, we have developed 3 new interactions through external grants. In particular, we have been working with the David Sarnoff laboratory of the Stanford Research Institute (SRI) on modulation doped and superlattice device structures. These structures consist of alternating regions of undoped host (e.g., ZnS) and doped

luminescent materials. The thermal stability of these structures upon RTP is an issue. T.J. Anderson has been working with Spire exploring ion implantation as a means to incorporate luminescent centers. RTP is required to activate these centers. Finally, ARPA has recently informed us that they intend to fund our proposal to establish a Center of Excellence in Phosphors. This center will be based at the University of Georgia and address a broad range of issues in both particle and thin film phosphors.

**Project 3. Impurity Induced Disordering in Superlattices**

Impurity induced layer disordering (IILD) has been studied on superlattice structures constructed with III-V compound semiconductors and, to a lesser extent, with II-VI materials. The IILD process involves the selective intermixing of superlattice layers in areas containing significant impurity incorporation. The technique can therefore be used to spatially alter the composition of a structure (e.g., produce a change in bandgap energy). The disordering results from the increased self-diffusion rates due to a locally high concentration of dopant. In compound semiconductors, there exists several models to explain this phenomenon, yet it is still not clear how the self-diffusion rates are enhanced.

One main problem with IILD is that the region of disorder is diffuse. This diffuse region is a result of isotropic diffusion profiles being established during thermal processing. One possible solution is to exploit a dopant with anisotropic diffusivities. Another possible method to improve pattern delineation is to apply an electric field in a manner to impede lateral diffusion or enhance vertical diffusion. Since many point defects are ionized at elevated temperature, transport rates should be affected by an electric field. Field assisted diffusion is well known, though it has not been applied to IILD. Additionally, the diffused region profile can be controlled by adjusting the temperature profile since intermixing is strongly temperature dependent. Rapid thermal processing offers a method of establishing non-uniform temperature profiles and therefore non-uniform intermixing. A vertical temperature profile is naturally

established while horizontal gradients can be established by the insulating characteristics of patterned masks.

It is proposed to examine this latter method with RTA in a microgravity environment. Since buoyancy driven convective heat transfer is greatly reduced in microgravity, the heat transfer characteristics should be altered. Superlattice structures consisting of alternating layers of lattice matched InGaAs and InP or GaInP and GaAs or Si and SiGe will be doped by either ion implantation or diffusion through a patterned $Si_3N_4$ mask. The mask will be left on the surface to serve as an insulator and the extent of intermixing will be studied as a function of anneal temperature and time. The degree of intermixing will be measured by TEM, and SAM or SIMS on bevel-lapped samples. These results will then be compared to ground processed samples.

We have been growing InGaAs/InP and InGaP/GaAs superlattices by MOCVD. We also have received MBE grown Si-SiGe superlattices from Texas Instruments. It is hoped to investigate the use of an electric field to assist in the impurity induced disordering in these materials.

**Project 4. Solid Phase Epitaxial Regrowth of $Si_xGe_{1-x}$ on Si**

$Si_{1-x}Ge_x$ alloys have been used in high performance optical and electronic device applications, such as heterojunction bipolar transistors and avalanche photodiode detectors. Such pseudomorphic layers result in bandgap reductions in the base region of bipolar devices. This reduction provides several potential advantages, including higher emitter injection efficiency, lower base resistance, shorter base transit time, and superior low temperature operation. Bandgap reductions of $Si_{1-x}Ge_x$ alloys are proportional to the Ge content and are dependent on the strain in the layers. However, the Ge content directly affects the strain and the critical thickness of the layers.

Strained $Si_{1-x}Ge_x$ alloys, which are grown by MBE or CVD, contain a low density of 60° misfit dislocations. The relaxation of $Si_{1-x}Ge_x$ strained layers may occur by intermixing or by

formation of additional misfit dislocations during thermal annealing. Unlike pseudomorphic III-V layers, the onset of relaxation of the $Si_{1-x}Ge_x$ alloy is gradual. It has been shown that samples with few dislocations present initially relaxed predominantly by intermixing due to stress enhancement, while those with a high initial dislocation density tended to relax mainly by forming additional dislocations.

Solid phase epitaxy (SPE) is a well characterized phenomenon in ion implanted semiconductors. The epitaxial regrowth occurs typically by a 2-dimensional growth mechanism in <100> elemental semiconductors (e.g., Si). Since lattice sites in $Si_{1-x}Ge_x$ alloys are randomly occupied by Si and Ge atoms, intermixing of strained layers and reduction of threading dislocation densities may be feasible by SPE. The SPE can be also applied in devices which are locally implanted by dopants as well.

In this work, SPE regrowth of amorphous $Si_{0.7}Ge_{0.3}$ layers on (100) Si will be studied as a function of annealing time and temperature. The $Si_{0.7}Ge_{0.3}$/Si structures will be provided by Texas Instruments. Ar ion implantation of the samples will be carried out at room temperature (dose ~$10^{15}/cm^2$) to generate an amorphous layer; the depth being adjusted by the energy of the implant. The SPE regrowth rate will be studied as a function of annealing temperature (525-650°C) and time (15-120 min.). The extent of regrowth will be measured from cross-sectional TEM analysis and compared to samples processed on the ground.

In addition, liquid phase epitaxy of $Si_xGe_{1-x}$ layers on Silicon will be investigated. These experiments will focus on the effect of microgravity on the liquid phase epitaxial regrowth process. The goal is to determine the effect of reduced convection currents on the final point defect and extended defect morphologies and the Ge segregation.

We have been investigating solid phase epitaxial regrowth of amorphized SiGe alloys. A short description of the progress is given in Appendix I.

**Project 5. Solidification of Silicon Polycrystalline Thin Films for Photovoltaic Applications**

The effect of microgravity on the solidification of thin films of polycrystalline silicon for photovoltaic applications will be studied. Silicon films will be made on earth by the melting and solidification of semiconductor grade silicon pellets and/or powders onto suitable substrates (quick release or permanent). Rapid thermal processing of the presolidified silicon films will be carried out both on earth and in space to compare the relative grain sizes and impurity segregation. These films will be subsequently processed into solar cells and their efficiencies compared to samples processed in ground based studies.

## Other Activities

The PI's have been involved in a variety of other activities associated with the program. These activities are summarized below:

1) The PI's assisted in the preparation of the Payload Plan.
2) The PI's participated in the interim review (IR).
3) The PI's have assisted in the design review.
4) The PI's have been discussing the design of the RTP furnace with Dr. Eric Cole (George Mason University), Ed Aaron (ITE), D. Bugby (Swales) and Lloyd Purves (GSFC).
5) The PI's have been assisting in the design of the sample holder with the personnel listed in (4).
6) The PI's have participated in the design of the ROMPS Preliminary Investigator's Interface with the developers at the Space Automation and Robotics Center.

## Summary

As discussed previously, this program will develop and demonstrate a fully automated rapid thermal processing capability on a variety of samples. As such their are 3 components to this program:

1) Advances in automation could provide useful products to semiconductor equipment manufacturers.
2) Rapid thermal processing equipment is still somewhat rudimentary. Current issues include temperature uniformity and control, temperature measurement, and control of cool-down rates. The first two issues will be addressed in this program in the design of the equipment and could lead to improved processing equipment.
3) The materials being examined have a wide range of applications in electronic, optoelectronic and optical components. The microgravity science component of this project could lead to new understanding of phenomena important in RTP and to the production of benchmarks.

The PI's have been actively involved in the design of the furnace and sample holder. Questions remain in regard to the temperature uniformity and the gas phase contaminant. The current design does not appear to be capable of achieving better than ± 40°C uniformly at 1200°C over a 1 $cm^2$ surface. The PI's have primarily been engaged in the preparation of samples and the development of the ground-base data from which space processing operating parameters can be determined. During this period, 2 graduate students are being supported in this project, one in Chemical Engineering and one in Materials Science and Engineering.

## Experiment Samples

| Sample No. | Experiment | Sample Material | Substrate Material | Temp. Range Degrees °C | Time in sec, |
|---|---|---|---|---|---|
| 1 | Improve Uniformity of CVD | InAs (wafer) | $Al_2O_3$ (wafer) | 820 | 180 |
| 2 | | | (reactants: $AsCl_3$ (vapor), | 820 | 180 |
| 3 | | | $H_2(g)$) | 820 | 180 |
| 4 | | | | 820 | 180 |
| 5 | | | | 820 | 180 |
| 6 | Improve Uniformity of CVD | InAs (wafer) | $Al_2O_3$ (wafer) | 700 | 180 |
| 7 | | | (reactants: $AsCl_3$ (vapor), | 740 | 180 |
| 8 | | | $H_2(g)$) | 780 | 180 |
| 9 | | | | 820 | 180 |
| 10 | | | | 860 | 180 |
| 11 | Improve Uniformity of CVD | InAs (wafer) | $Al_2O_3$ (wafer) | 820 | 30 |
| 12 | | | (reactants: $AsCl_3$ (vapor), | 820 | 70 |
| 13 | | | $H_2(g)$) | 820 | 110 |
| 14 | | | | 820 | 150 |
| 15 | Rapid Thermal Annealing of | ZnS | ZnS on $BaTaO_5$ on | 760 | 30 |
| 16 | ZnS Based Devices | | ITO on $SiO_2$ (62 mil) | 760 | 30 |
| 17 | | | (reactants: Zn, S) | 760 | 30 |
| 18 | Rapid Thermal Annealing of | ZnS | ZnS on $BaTaO_5$ on | 750 | 30 |
| 19 | ZnS Based Devices | | ITO on $SiO_2$ (62 mil) | 750 | 30 |
| 20 | | | (reactants: Zn, S) | 750 | 30 |
| 21 | Rapid Thermal Annealing of | ZnS | ZnS on $BaTaO_5$ on | 500 | 30 |
| 22 | ZnS Based Devices | | ITO on $SiO_2$ (62 mil) | 590 | 30 |
| 23 | | | (reactants: Zn, S) | 690 | 30 |
| 24 | | | | 850 | 30 |
| 25 | Rapid Thermal Annealing of | ZnS | ZnS on $BaTaO_5$ on | 750 | 5 |
| 26 | ZnS Based Devices | | ITO on $SiO_2$ (62 mil) | 750 | 25 |
| 27 | | | (reactants: Zn, S) | 750 | 45 |
| 28 | | | | 750 | 65 |
| 29 | | | | 750 | 85 |
| 30 | | | | 750 | 120 |

| Sample No. | Experiment | Sample Material | Substrate Material | Temp. Range Degrees C | Time in sec, |
|---|---|---|---|---|---|
| 31 | Order-Disorder of Active Layer | InGaAs | InP | 700 | 120 |
| 32 | | $Si_3N_4$ (capped with | | 745 | 120 |
| 33 | | | | 785 | 120 |
| 34 | | | | 830 | 120 |
| 35 | | | | 875 | 120 |
| 36 | | | | 916 | 120 |
| 37 | | | | 950 | 120 |
| 38 | Order-Disorder of Active Layer | InGaAs | InP | 850 | 30 |
| 39 | | Si3N4 (capped with) | | 850 | 175 |
| 40 | | | | 850 | 320 |
| 41 | | | | 850 | 465 |
| 42 | | | | 850 | 610 |
| 43 | | | | 850 | 755 |
| 44 | | | | 850 | 900 |
| 45 | Impurity Induced Disordering | SiGe | Si | 525 | 1800 |
| 46 | | | | 550 | 1800 |
| 47 | | | | 575 | 1800 |
| 48 | | | | 600 | 1800 |
| 49 | | | | 625 | 1800 |
| 50 | | | | 650 | 1800 |
| 51 | Impurity Induced Disordering | SiGe | Si | 625 | 900 |
| 52 | | | | 625 | 2160 |
| 53 | | | | 625 | 3420 |
| 54 | | | | 625 | 4680 |
| 55 | Liquid Phase Epitaxy | SiGe | Si | 1275 | 40 |
| 56 | | | | 1275 | 80 |
| 57 | | | | 1275 | 120 |
| 58 | | | | 1275 | 180 |
| 59 | | | | 1275 | 240 |
| 60 | Liquid Phase Epitaxy | SiGe | Si | 1150 | 60 |
| 61 | | | | 1250 | 60 |
| 62 | | | | 1350 | 60 |
| 63 | Liquid Phase Epitaxy | SiGe | Si | 1380 | 60 |
| 64 | Vary Ge Content | | | 1380 | 60 |
| 65 | | | | 1380 | 60 |

| Sample No. | Experiment | Sample Material | Substrate Material | Temp. Range Degrees C | Time in sec, |
|---|---|---|---|---|---|
| 66 | Liquid Phase Epitaxy of SiGe Superlattices | SiGe | Si | 1275 | 5 |
| 67 | | | | 1275 | 70 |
| 68 | | | | 1275 | 120 |
| 69 | | | | 1275 | 240 |
| 70 | LPE of Superlattices Vary Spacing | SiGe | Si | 1275 | 60 |
| 71 | | | | 1275 | 60 |
| 72 | | | | 1275 | 60 |
| 73 | LPE of Superlattices | SiGe | Si | 1250 | 60 |
| 74 | | | | 1300 | 60 |
| 75 | | | | 1350 | 60 |
| 80 | Liquid Phase Processing of Si PV | Si | BN or graphite | 1425 | 5 |
| 81 | | | | 1425 | 60 |
| 82 | | | | 1425 | 120 |
| 83 | | | | 1425 | 180 |
| 84 | | | | 1425 | 300 |
| 85 | Liquid Phase Processing of Si PV | Si | BN or graphite | 1415 | 60 |
| 86 | | | | 1435 | 60 |
| 87 | | | | 1455 | 60 |
| 88 | | | | 1475 | 60 |
| 89 | Liquid Phase Processing of Si PV Vary Thickness | Si | BN or graphite | 1425 | 60 |
| 90 | | | | 1425 | 60 |
| 91 | | | | 1425 | 60 |
| 92 | | | | 1425 | 60 |
| 93 | Reflow in SIMOX | O Implanted Si | Si | 1380 | 60 |
| 94 | | | | 1380 | 400 |
| 95 | | | | 1380 | 800 |
| 96 | | | | 1380 | 1200 |
| 97 | Amorphous Films | a:Si:H, a:Si:F (Amorphous Si) | Au (0.1μ) on $SiO_2$ (7 mil) | 1275 | 30 |
| 98 | | | | 1350 | 30 |
| 99 | | | | 1450 | 30 |
| 100 | | | | 1450 | 5 |
| 101 | | | | 1450 | 10 |
| 102 | | | | 1450 | 20 |

| Sample No. | Experiment | Sample Material | Substrate Material | Temp. Range Degrees C | Time in sec. |
|---|---|---|---|---|---|
| 103 | Poly CdTe, CdS | Poly CdTe or CdS | ITO | 800 | 60 |
| 104 | | (Paste) | (conductive) | 400 | 60 |
| 105 | | | | 800 | 10 |
| 106 | | | | 800 | 30 |
| 107 | Poly CdTe, CdS | Poly CdTe or CdS | $SiO_2$ | 800 | 60 |
| 108 | | (Paste) | (nonconductive) | 400 | 60 |
| 109 | | | | 800 | 10 |
| 110 | | | | 800 | 30 |
| 111 | Poly CdTe, CdS | Poly CdTe or CdS | Metal Stainless Steel | 800 | 60 |
| 112 | | (Paste) | Metal Stainless Steel | 400 | 60 |
| 113 | | | Metal Mo | 800 | 10 |
| 114 | | | Metal Cu | 800 | 30 |
| 115 | Poly CdTe, CdS | Poly CdTe or CdS | ITO | 800 | 60 |
| 116 | | (Electrodeposition) | (conductive) | 400 | 60 |
| 117 | | | | 800 | 10 |
| 118 | | | | 800 | 30 |
| 119 | Poly CdTe, CdS | Poly CdTe or CdS | $SiO_2$ | 800 | 60 |
| 120 | | (Electrodeposition) | (nonconductive) | 400 | 60 |
| 121 | | | | 800 | 10 |
| 122 | | | | 800 | 30 |
| 123 | Poly CdTe, CdS | Poly CdTe or CdS | Metal Stainless Steel | 800 | 60 |
| 124 | | (Electrodeposition) | Metal Stainless Steel | 400 | 60 |
| 125 | | | Metal Mo | 800 | 10 |
| 126 | | | Metal Cu | 800 | 30 |
| 127 | Poly CdTe, CdS | Poly CdTe or CdS | ITO | 800 | 60 |
| 128 | | (Spray pyrolysis) | (conductive) | 400 | 60 |
| 129 | | | | 800 | 10 |
| 130 | | | | 800 | 30 |
| 131 | Poly CdTe, CdS | Poly CdTe or CdS | $SiO_2$ | 800 | 60 |
| 132 | | (Spray pyrolysis) | (nonconductive) | 400 | 60 |
| 133 | | | | 800 | 10 |
| 134 | | | | 800 | 30 |

| Sample No. | Experiment | Sample Material | Substrate Material | Temp. Range Degrees C | Time in sec, |
|---|---|---|---|---|---|
| 135 | Poly CdTe, CdS | Poly CdTe or CdS | Metal | 800 | 60 |
| 136 | | (Spray pyrolysis) | | 400 | 60 |
| 137 | | | | 800 | 10 |
| 138 | | | | 800 | 30 |
| 139 | High Temperature | YBCO or BISCO | $SrTiO_3$ | 950 | 50 |
| 140 | Superconductors | (Thin Film Poly Material) | | 800 | 50 |
| 141 | | | | 950 | 5 |
| 142 | High Temperature | YBCO or BISCO | $Al_2O_3$ | 950 | 50 |
| 143 | Superconductors | (Thin Film Poly Material) | | 800 | 50 |
| 144 | | | | 950 | 5 |
| 145 | High Temperature | YBCO or BISCO | SrTiO | 950 | 50 |
| 146 | Superconductors | (Thick Film) | | 800 | 50 |
| 147 | | | | 950 | 5 |
| 148 | High Temperature | YBCO or BISCO | $Al_2O_3$ | 950 | 50 |
| 149 | Superconductors | (Thick Film Poly Material) | | 800 | 50 |
| 150 | | | | 950 | 5 |
| 151 | Calibration Sample | TC | $Al_2O_3$ | 950 | 50 |
| 152 | Calibration Sample | TC | $Al_2O_3$ | | |
| 153 | Calibration Sample | TC | $Al_2O_3$ | | |
| 154 | Calibration Sample | TC | $Al_2O_3$ | | |

## Appendix I

# Kinetics of Solid Phase Epitaxial Regrowth in Amorphized $Si_{0.88}Ge_{0.12}$ Measured by Time-Resolved Reflectivity

K. S. Jones, M. J. Antonell, C. Lee and T. E. Haynes*

Department of Materials Science and Engineering
University of Florida, Gainesville, FL 32611 USA
* Solid State Division ORNL Oak Ridge, TN 37831 USA

## ABSTRACT

Time-resolved reflectivity has been used to measure the rate of solid phase epitaxial regrowth (SPER) in situ during annealing of strained $Si_{0.88}Ge_{0.12}$ epilayers on Si preamorphized by implantation of Si. The SPER velocities were measured over more than two orders of magnitude at temperatures from 503° to 603°C. The results confirm that the average SPER velocity in thin, strained $Si_{0.88}Ge_{0.12}$ layers is less than that in pure Si. Furthermore, these real-time measurements demonstrate that the SPER rate for strained $Si_{0.88}Ge_{0.12}$ alloys is not a constant during the regrowth at a fixed temperature but varies systematically by as much as a factor of 2 as a function of the position of the amorphous-crystalline interface, reaching a minimum after regrowth of approximately 800Å of the alloy layer. The activation energy barrier of SPER in strained $Si_{0.88}Ge_{0.12}$ is higher than that in pure Si and is also a function of interface position, ranging from 2.94 to 3.11 eV. Cross-section transmission electron microscopy shows that strain-relieving defects are introduced during SPER primarily in the stage of regrowth coinciding with the minimum regrowth rate and maximum activation energy.

## 1. Background, Motivation and Objectives

Intensive research effort has been directed toward the applications of SiGe alloys in high performance electronic and optical devices, such as high electron mobility transistors [1] and photodetectors [2]. The advantages of SiGe alloys include higher mobilities and smaller bandgaps, compared with Si. In conventional silicon IC processing, amorphization during dopant implantation and subsequent SPER are critical steps for improving activation, minimizing channeling tails, and reducing the densities of extended defects. On the other hand, although Ge is presumed to be completely soluble in Si, SPER in SiGe alloys results in poor quality layers [3]. Furthermore, the SPER rate of strained SiGe alloys is reportedly smaller than that of pure Si, while the activation energy is larger [3-5]. Thus, the reduction in the velocity and increase in the activation energy of SPER processes in SiGe relative to Si have been attributed to the existence of strain, although the mechanisms have not been determined. The relationship between strain and SPER rate deserves further study.

## 2. Experimental Results

The technique of time-resolved reflectivity (TRR), as described by Olson and others [6,7], permits real-time measurement of the interface position and regrowth velocity during SPER. Besides, TRR measurements are efficient and rapid, do not require extensive sample preparation, and allow continuous, real-time monitoring of SPER over a large temperature range. In this letter, the first extensive set of TRR measurements of the SPER kinetics in SiGe epilayers on Si is described. In addition to confirming and extending previous results obtained by cross-section transmission electron microscopy (XTEM) and ion channeling [3-5,8], this letter reports the discovery of a previously overlooked phenomenon, namely that the SPER velocity varies systematically with interface position in these strained layers and that this variation is correlated with the formation of strain-relieving defects during regrowth.

Strained $Si_{1-x}Ge_x$ layers were grown on p-type, 5-20 Ω-cm, 4-inch (100) Si wafers at 550°C by molecular beam epitaxy at Texas Instruments, Inc. Rutherford backscattering spectrometry and XTEM showed the $Si_{1-x}Ge_x$ layer had Ge fraction $x = 0.12$ and a thickness of ~2000Å, which is less than the critical thickness for this composition. This $Si_{0.88}Ge_{0.12}$ epilayer was amorphized to a depth of 3000Å (including 1000Å of the Si substrate) by dual-energy implantation of $6 \times 10^{14}/cm^2$ $Si^-$ at -100°C at energies of 75 and 150 keV. As-implanted and partially regrown layers were characterized by XTEM (using a JEOL 4000FX with point-to-point resolution of 1.95Å) and <100>-axial ion channeling (2 MeV $He^+$ at a 160° scattering angle).

The technique of TRR has been described extensively elsewhere [6,7]. Briefly, the phase difference between the components of laser light reflected from the surface and from the (crystalline-amorphous) *c/a* interface changes continuously during SPER due to the advance of the *c/a* interface, leading to interference fringes in the reflected light intensity which are used to monitor the progress of the interface position. In these experiments, a He-Ne laser ($\lambda$ = 6328Å) source was used, with two Si photodiodes to measure the incident and reflected laser power. Samples were mounted on a low-mass molybdenum holder using a heat-conducting paint, and this holder was then wedged into a larger, heated stage which had been preheated to the annealing temperature in an Ar-filled chamber. The sample temperature was measured by a thermocouple embedded in the sample holder. The sample reached the annealing temperature in less than 1 min. after insertion. The temperature was quite stable, with variations of less than ±1°C after an initial settling period of ~1 min., thus permitting TRR measurements over time scales from several minutes to tens of hours. In several samples, SPER was interrupted and the thicknesses of the partially regrown layers measured by ion channeling and XTEM, in order to verify the thicknesses determined from TRR.

Figure 1 shows an example of the time-dependence of the reflectivity during regrowth of $Si_{0.88}Ge_{0.12}$/Si at 562°C. The film thickness increment, $\Delta z$, between each successive interference maximum and minimum is $\lambda/4n$, where $n = 4.65$ is the refractive index of this a-

$Si_{0.88}Ge_{0.12}$ layer, as measured by spectroscopic ellipsometry. The SPER rate $v(z)$ is defined as $v = \Delta z/\Delta t = \lambda/(4n\Delta t)$, where $\Delta t$ is time interval between successive extrema. (Thus $v$ is actually the average rate during the time interval, $\Delta t$.) As the *c/a* interface moves toward the surface, the absorption decreases and consequently the amplitude of the reflectivity oscillations is expected to increase. This behavior is observed during regrowth of the Si substrate (Stages 7-8 in Fig. 1) but not in the strained $Si_{0.88}Ge_{0.12}$ epilayer (Stages 2-5), where the amplitude instead decreases slightly. A similar reduction of the interference amplitude has been reported during SPER in GaAs, where it is caused by interface roughening during regrowth [9]. Thus, the reduction of the amplitude in the present SiGe layers is ascribed to the existence of a nonplanar interface, as observed by Paine [3] and confirmed below for these samples. In the case of a nonplanar interface, TRR still reliably measures the mean interface depth (i.e., the interference fringes are not shifted), so long as the roughness is not a strong function of interface position [9]. It is shown below that this condition is satisfied in these alloy layers.

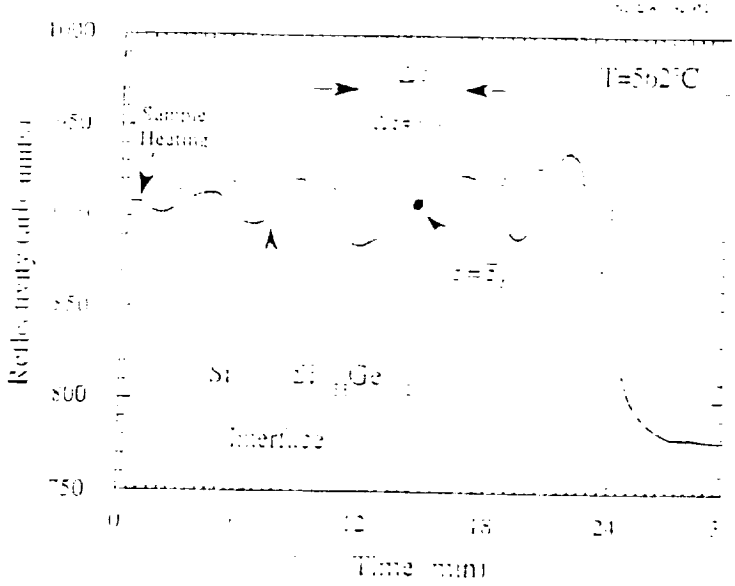


Figure 1. Time-dependence of the reflectivity during regrowth of $Si_{0.88}Ge_{0.12}/Si$ at 562°C. Numerals label sections of the curve corresponding to regrowth Stages 1-8 referred to in the text.

Previous reports have suggested that the SPER rate in strained SiGe alloys is constant [3-5]. However, the present results demonstrate that v depends on the *c/a* interface depth. This can be seen immediately in Fig. 1, where $\Delta t$ varies for different stages, e.g., $\Delta t_1 > \Delta t_2$. A plot of velocity versus *a/c* interface depth is presented in Fig. 2. Below 2000Å, including Stage 7 and part of Stage 6, SPER is occurring only in the Si substrate. As the interface moves into the $Si_{.88}Ge_{.12}$ alloy away from the Si substrate, the velocity first decreases in Stages 5 and 4 to a minimum at ~1200Å deep, and then increases in Stages 3 and 2. The interface velocity appears to decrease again in Stage 1, but this is at least partly due to the roughness of the *c/a* interface, which simulations have shown induces a long tail on the last interference fringe [9]. The uncertainties in the measured regrowth rates vary between 3% and 9%. As Fig. 2 clearly shows, there is a very significant difference, as much as a factor of two, between the regrowth rates in Stage 2 and Stage 4 and at all annealing temperatures. Earlier reports did not detect these variations in SPER rate due to experimental uncertainties. However, in retrospect, evidence for such variations might be inferred from the data exhibited in Fig. 4 of Ref. 3 and Fig. 2 of Ref. 4.

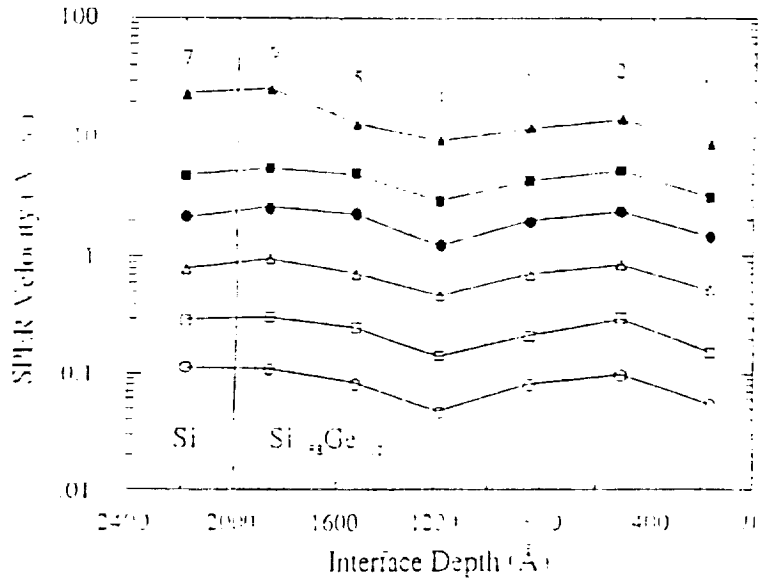


Figure 2. The SPER rate as a function of a/c interface depth at various temperatures (top to bottom: 603°, 580°, 562°, 543°, 523°, and 503°C respectively). The vertical line marks the Si/SiGe interface.

An Arrhenius plot of the SPER velocity for Stages 2-4 in strained $Si_{0.88}Ge_{0.12}$ is shown in Fig. 3. At any given position in Stages 1-5, Arrhenius-type behavior is observed with a single activation energy. It should be noted that the SPER rates reported in Ref. 5 for a similar alloy composition are bounded by the lines shown in Fig. 3 for Stages 2 and 4. The activation energy determined from the fits in Fig. 3 varies from 2.94 to 3.11 eV as a function of interface depth. The dependence of activation energy on depth is shown in Fig. 4. It reaches its maximum in Stage 4, where the SPER rate is a minimum. At all other depths, the activation energy barrier is approximately constant at 2.97 eV, to within the experimental uncertainty. This value is 0.3 eV larger than in pure Si (2.68 eV[6]) and is consistent with values reported earlier for strained SiGe epilayers [3-5]. Based on an analysis of the experimental errors and quality of the Arrhenius fits, we believe that the difference of the measured activation energy in Stage 4 as compared to the other stages is significant. Similarly, the pre-exponential factor of the interface velocity also varies most strongly in Stage 4.

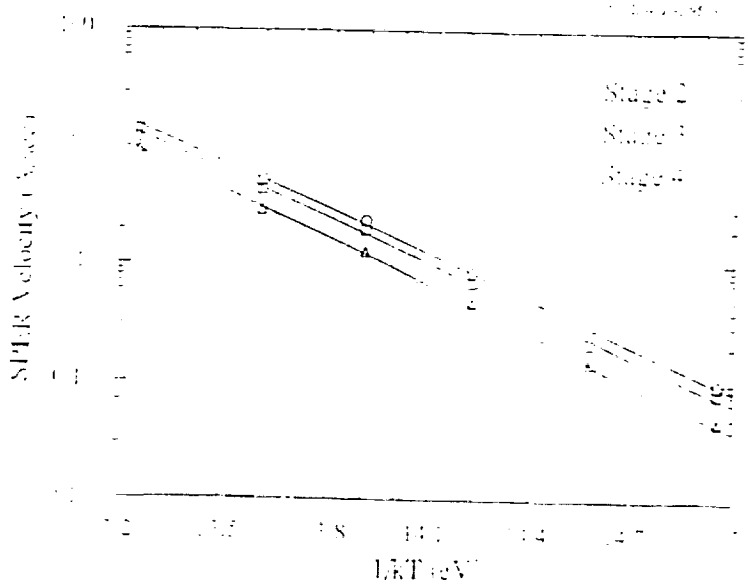


Figure 3. An Arrhenius plot of the SPER velocity for Stages 2-4 of regrowth in strained $Si_{0.88}Ge_{0.12}$.

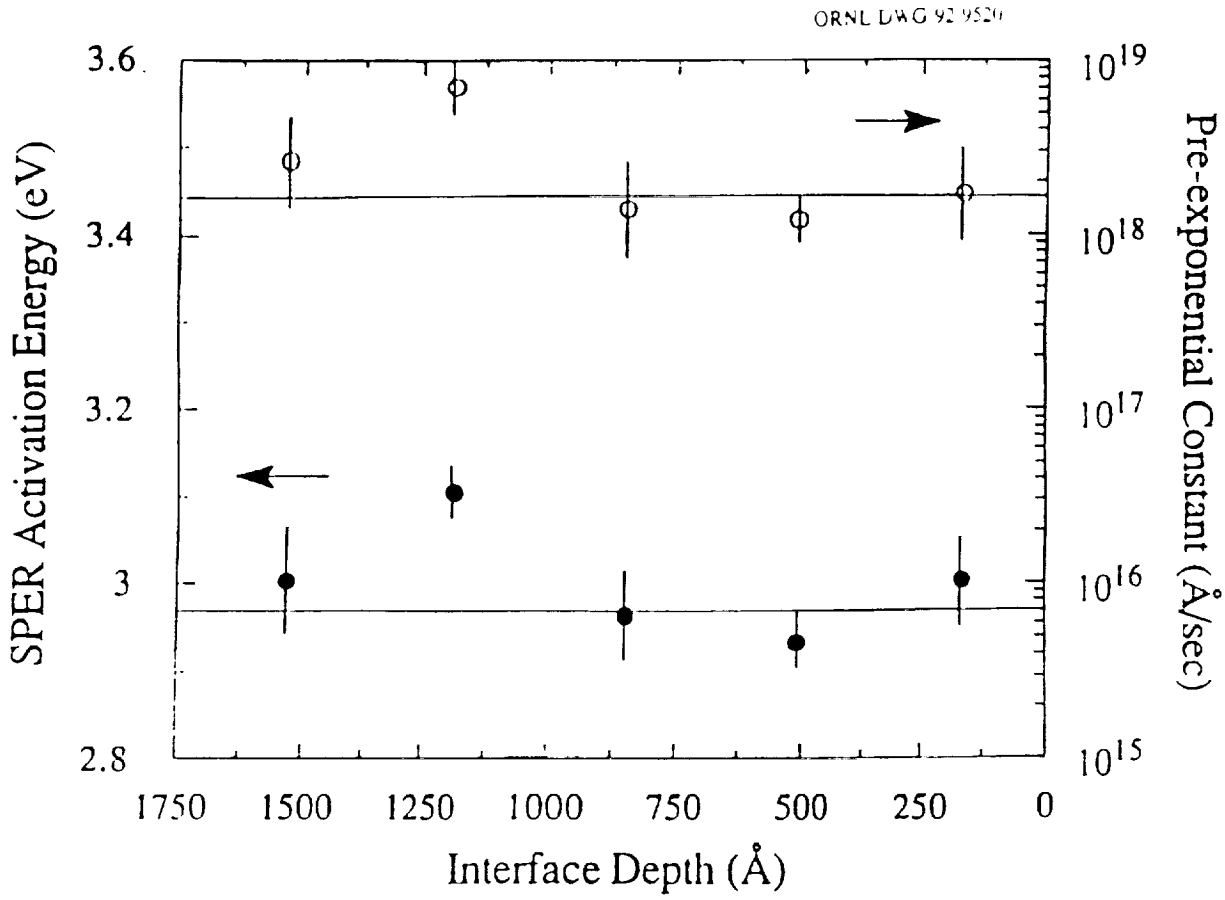


Figure 4. Activation energy and pre-exponential factor of SPER velocity as function of the a/c interface position. Error bars represent the standard error of the Arrhenius fits shown in fig. 3.

## 3. Discussion

Cross-section TEM has been used to investigate the relationship between the variable SPER rate and microscopic features of the *a/c* interface. Samples were annealed at 562°C, and SPER was interrupted at selected stages during TRR measurements. Figure 5(a) shows a cross-section micrograph of such a sample interrupted in Stage 2. This figure illustrates (1) the roughness of the *a/c* interface; (2) coherent, relatively defect-free regrowth of the first 300Å of the alloy near the Si interface; and (3) defects such as stacking faults and dislocations in the region from the *a/c* interface down to ~300Å from the Si/SiGe interface. Such defects form in order to relieve strain in these lattice-mismatched epilayers [5]. That they do not

appear in the 300Å of SiGe nearest the Si SiGe interface is in good agreement with the critical thickness calculations in Ref. 5. Careful examination of a number of micrographs indicated that most such defects originated in the range between 300 and 1000Å from the Si/SiGe interface, while only a few intersect this interface. This observation was confirmed by ion channeling on the same partially-regrown samples, illustrated in Fig. 5(b). The channeling spectra exhibit a peak due to scattering from defects in the range between 500 and 1000Å from the Si/SiGe interface (1000–1500Å from the surface), indicating that the largest concentration of defects is indeed found at this depth. Note that this corresponds to the mean depth of the *a/c* interface in Stage 4 of the regrowth, where the velocity is a minimum. In the channeling spectra of Fig. 5(b), the large peaks on the right correspond to the residual amorphous layer, and the slopes of the left edges of these peaks are indicative of the roughness of the *a/c* interface. Comparison of the spectra (2) and (4) shows that the interface roughness is similar in Stages 2 and 4. Furthermore, XTEM also showed that the *a/c* interface was already nonplanar in Stage 5 before the interface velocity reached its minimum value. These results have led us to conclude that the primary cause of the lower SPER rate and higher activation energy during Stage 4 of the regrowth of these strained $Si_{0.88}Ge_{0.12}$ epilayers is most likely related to the nucleation of strain-relieving defects.

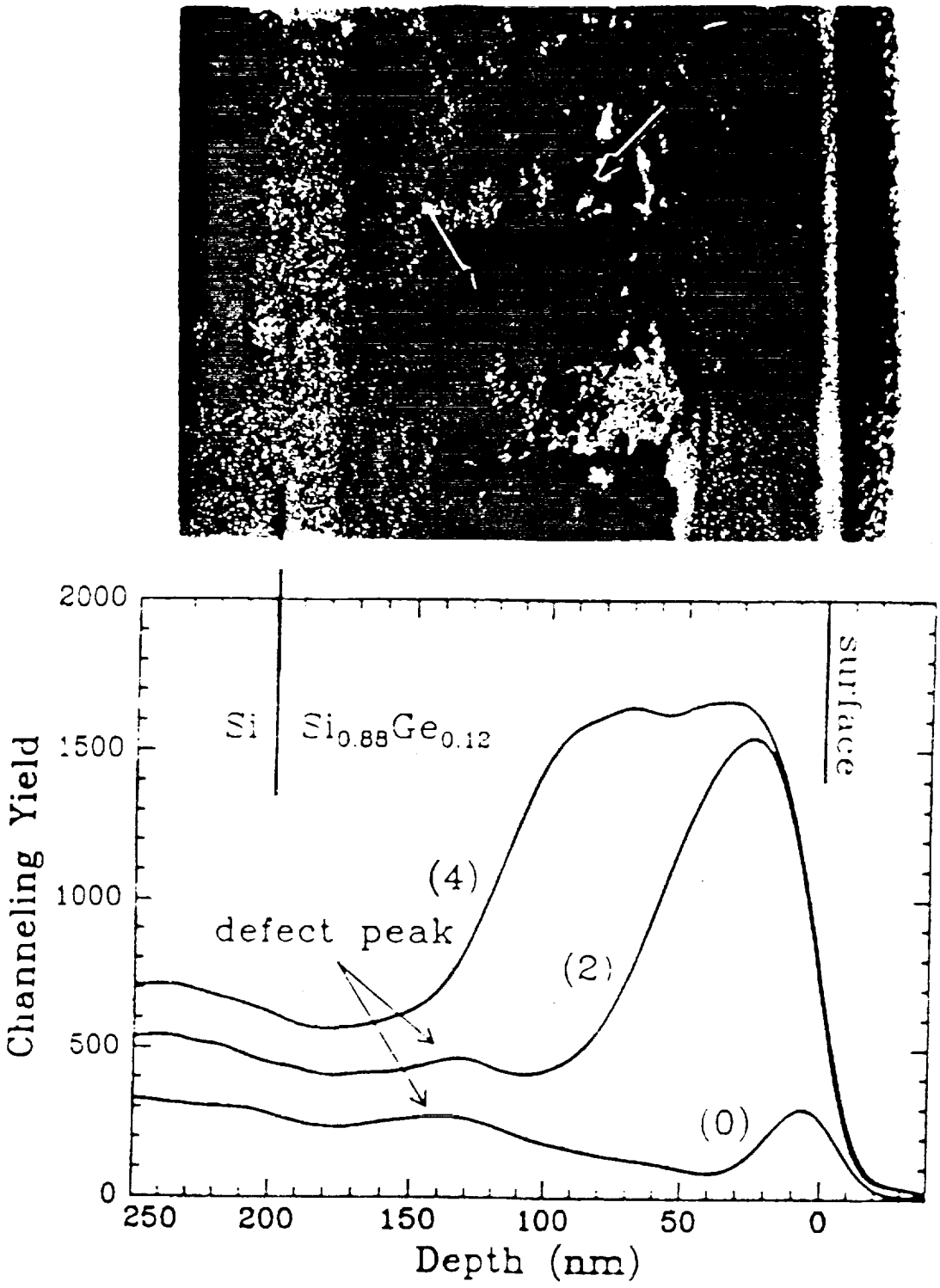


Figure 5. (a) Cross-section TEM micrograph of a partially regrown layer interrupted during Stage 2 at 562°C, showing dislocations (*dis*, dark contrast) and stacking faults (*sf*); (b) ion channeling spectra of a fully regrown layer (0), and partially regrown layers interrupted in Stage 2 (2) and Stage 4 (4). Depth scales in (a) and (b) are identical.

## 4. Conclusions

In summary, the first extensive set of measurements of the SPER kinetics in SiGe epilayers on Si has been reported. The main observation from these measurements is that the SPER velocity of strained $Si_{0.88}Ge_{0.12}$ alloys is not a constant, but varies with interface position during regrowth at a fixed temperature. The SPER rate reaches a minimum after regrowth of approximately 800Å of SiGe. This depth corresponds to the region where the majority of strain-relieving defects nucleate. Therefore, the introduction of these defects is believed to retard the SPER process in these mismatched epilayers and contribute to an apparent ~0.15 eV increase in the activation energy in that stage of regrowth. Accordingly, the lower activation energy barrier measured in Stages 1-3 is thought to be characteristic of SPER in $Si_{0.88}Ge_{0.12}$ epilayers after relaxation of the misfit strain.

## 5. Future Work

This study will continue further with the characterization of SiGe alloys of higher content and will attempt to discern if $C^-$ implantation can be used to compensate for the strain in the $Si_{1-x}$ $Ge_x$ layers and contribute to defect free SPER in the thinner SiGe layers. From our previous work varying Ge concentration ($0<x<.45$) it has been observed that the regrowth velocity reaches a minima and its activation energy a maxima in the 12% Ge alloys. It is unknown why this maxima occurs although there is some theoretical speculation that this can be attributed to bonding (i.e. Ge-Ge vs. Si-Ge) at the amorphous crystalline interface. No studies of the higher Ge content ($x>.45$) have been published. Both strained and unstrained

$Si_{1-x}Ge_x$ layers of varying composition have been grown on (100)Si. Higher Ge concentrations ($x > .5$) have been grown on Ge substrates by SPIRE Corporation to reduce lattice mismatch strain. SPER of the higher Ge concentrations will be studied after Ge amorphization to determine the affect of Ge concentration on the SPER kinetics and how the activation energy for SPER varies with Ge content.

Recently $C^+$ implants have been shown to induce a state of tension in Si. $C^+$ implantation of thin SiGe layers (which result in poor quality SPER) can be compensated and the quality of SPER improved. This may help us better understand what limits the SPER process. In addition, liquid phase epitaxy (LPE) is being studied in order to determine the affect of a micro-gravity environment on the kinetics of regrowth and subsequent defect formation. Single composition $Si_{1-x}Ge_x$ layers growth on Si as well as some SiGe super-lattice structures will be melted at different temperatures and regrown. After LPE, the samples will be characterized and compared to the normal values that are expected to be seen with LPE done in ground-based experiments. These results will also be compared to solid phase epitaxy data obtained from the ground-based experiments. To date, test samples have been cut and a glue for holding the samples to the substrates has been found. These samples have been sent to Ed Aaron for testing of the temperature control in the furnace.

## 6. Conference Proceedings and Publications

Support from NASA has been cited in the following presentations and Publications listed below.

Conference Presentation:

(1) C . Lee. K.S. Jones and T.E. Haynes. "Time Resolved-Reflectivity Study of Solid Phase Epitaxial Regrowth in Relaxed and Strained $Si_{1-x}Ge_x$ Epilayers." in the Symposium on Semiconductor Heterostructure for Photonic and Electronic Applications. Fall MRS Meeting Boston. Mass.. Nov. 30 - Dec. 3 1992.

Publications:

(2) C. Lee, T.E. Haynes and K. S. Jones. "Kinetics of Solid Phase Epitaxial Regrowth in Amorphized $Si_{0.88}Ge_{0.12}$ Measured by Time-Resolved Reflectivity," Accepted by Applied Physics Letters, to be published in early 1993.

(3) C. Lee. K.S. Jones and T. E. Haynes. "Time-Resolved Reflectivity Study of Solid Phase Epitaxial Regrowth in Relaxed and Strained $Si_{1-x}Ge_x$ Epilayers." Semiconductor Heterostructure for Photonic and Electronic Applications. eds. D.C. Houghton. C.W. Tu and R.T. Tung, Proceedings Materials Research Society Volume 283. 1993.

(4) C. Lee. T.E. Haynes and K.S. Jones. "Effect of Ge Concentration on Solid Phase Epitaxial Regrowth Kinetics in Amorphized SiGe Alloys," being submitted to Applied Physics Letters.

## 7. Collaborations and Spin-Offs

This work has resulted in an interest by E. Kasper at Daimler-Benz, in Ulm Germany they have given us sample devices processed with SiGe for sample characterization. Also, this work has sparked study of Interface Morphology by the Electron Microscopy Group - Solid State Division ORNL, D.E. Jepson.

## 8. Acknowledgments

The authors would like to thank G.E. Jellison, Jr. and H. H. Burke for measuring optical constants of the amorphous SiGe layers. Research performed at Oak Ridge National Laboratory sponsored by the Division of Materials Sciences, U.S. Department of Energy under contract DE-AC05-84OR21400 with Martin Marietta Energy Systems, Inc., with additional funding from NASA and through the SURA/ORNL Summer Cooperative Research Program in Materials Science.

## REFERENCES


1. C. Smith and M.E. Jones, Mater. Res. Soc. Proc. 91, Pittsburgh, PA (1987), pp. 277.

2. H. Temkin, A. Antreasyan, N.A. Olsson, T.P. Pearsall, and J.C. Bean, Appl. Phys. Lett. 49, 809 (1986).

3. D.C. Paine, D.J. Howard, N.G. Stoffel, and J.A. Horton, J. Mater. Res. 5, 1023 (1990).

4. Q.Z. Hong, J.G. Zhu, J.W. Mayer, W. Xia, and S.S. Lau, J. Appl. Phys. 71, 1768 (1992).

5. D.C. Paine, N.D. Evans, and N.G. Stoffel, J. Appl. Phys. 70, 4278 (1991).

6. G.L. Olson and J.A. Roth, Mater. Sci. Reports 3, 1 (1988).

7. G. Q. Lu, E. Nygren, M.J. Aziz, J. Appl. Phys. 70, 5323 (1991).

8. B.T. Chilton, B.J. Robinson, D.A. Thompson, T.E. Jackman, and J.M Baribeau, Appl. Phys. Lett. 54, 42 (1989).

9. C. Licoppe, Y.I. Nissim, C. Meriadec, and P. Krauz, J. Appl. Phys. 60, 1352 (1986).