A VLSI Implementation for Synthetic Aperture Radar Image Processing

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Abstract – **A simple physical model for the Synthetic Aperture Radar (SAR) is presented. This model explains the one dimensional and two dimensional nature of the received SAR signal in the range and azimuth directions. A time domain correlator, its algorithm and features are explained. The correlator is ideally suited for VLSI implementation. A real time SAR architecture using these correlators is proposed. In the proposed architecture, the received SAR data is processed using one dimensional correlators for determining the range while two dimensional correlators are used to determine the azimuth of a target. The architecture uses only three different types of custom VLSI chips and a small amount of memory.**

1 Introduction

Modern real time signal and image processing demands high speed computing hardware and large memory. The availability of low cost, high density, high speed, very large scale integrated circuits enables the design of massively parallel processors which can exceed supercomputers in calculation speeds. This makes special purpose parallel processors attractive for real time signal processing.

Synthetic Aperture Radar (SAR) is an imaging system dominated by signal processing algorithms. Signal processing algorithms use techniques like convolution, correlation and filtering. The major processor requirement in these techniques is the need to multiply a data value by a coefficient and add it to a sum. Hence, digital processors implementing these signal processing functions are specialized arithmetic computers optimized to do multiplications, additions and logical operations. Most of the signal processing algorithms are highly repetitive and possess properties such as regularity, recursiveness, etc. These properties make the signal processing architecture less complex to build [1,2].

In this paper, a physical model for SAR is presented. An architecture for the SAR processor is also is presented. This architecture for SAR uses a new correlator chip. This paper also describes the correlator, its application to two dimensional imaging and the features of the SAR architecture.

2 SAR Principles

Synthetic Aperture Radar is an imaging system in which a return pulse from a object target is detected and processed using convolution techniques. SAR differs from normal aperture radar in that the beam aperture in the direction of motion of the radar (Azimuth direction) is synthetically increased by processing carrier phase history (Doppler phase history) information in the returned radar signal. In this way, a sharply focussed beam is synthesized from a normal length antenna and a high azimuth resolution is achieved. In a SAR, the area to be mapped (Swath) is in a direction perpendicular to the azimuth direction (Range direction). Processing the received data in a SAR is a 2-D operation. However, with suitable corrections and compensations, this 2-D operation can be considered as two 1-D operations. A simple physical model explaining the principle on which this separation is done is explained in the following subsection.

2.1 A Physical Model for SAR

First, it is helpful to visualize a two dimensional array of all the data collected from the target during the time the target in under the influence of the beam (dwell time). The signal processing that will be developed [3] is easily understood by referring to this data array. This array never really exists as a whole, but is used here as a conceptual aid in the presentation that follows.

The radar signal is a swept linear FM pulse of a fixed duration and the pulses are repeated at the Pulse Repetition Frequency, PRF. Between the pulses, the transmitter is turned off and the antenna and electronics become a receiver system. The reflected signal from a single pulse is collected, digitized and stored as a range line in the memory. The length of the range line is dependent on the width of the area to be imaged.

Let a be the number of samples in each range line. After several range lines, say b, have been received, the signal memory array is formed and the array contains $a \times b$ data points. The coordinates of the signal memory are the slant range and the azimuth. A single sample in the signal memory array contains contributions from a large number of point targets (ground reflectors) in the area to be mapped. By the above principle, the received signal from a single point reflector on the ground will be spread through a large area in the signal memory array. Let p and q be the number of samples along the range direction and azimuth directions over which this spread in the signal memory array takes place. It is valid to assume that the energy contribution from a point target beyond this area is negligible.

Assuming for a moment, that the transmitted pulses are continuous in nature, the received data will exhibit a carrier phase history proportional to the slant range rate. It is this carrier phase history on which the SAR principle is based. An analysis of the satellite and point target motion shows that the slant range rate varies, approximately, linearly with time. This means that the received carrier phase history varies linearly with time or has a linear FM modulation. As the radar transmitted signal is pulsed and itself is a swept linear FM waveform, this carrier phase history is manifested as a changing phase angle in

the received carrier signal. There is a large disparity in range and the azimuth FM rates in the received signal and hence, can be decoupled with correction. Thus the point target response in the signal memory array consists of two linear FM waveforms, one in the range and the other in the azimuth directions.

The function of the SAR signal processor is to focus or compress the energy of each point target which is spread in the signal memory array in the manner described above, into single points in the image. In actuality, a two dimensional compression using a two dimensional reference function is needed to compress the energy into a point target, since the spread is in two dimensions. A two dimensional correlator of $a \times b$ multipliers will image the point targets comprising the swath.

A closer look at the received data reveals that the data collected from point targets from a single transmitted pulse are all the same except that the data from each point target may have a different amplitude and time shift. This time shift is the delay associated with the received signals from point targets at different locations. Since, only p samples contribute to the energy for a point target in the range direction, it is enough if only p multipliers are used in the range direction. It is also sufficient for the range reference function to use only p samples. A similar argument is true in the azimuth direction. The azimuth phase history is similar for all the point targets at different azimuth coordinates, but shifted in time. Hence, only q multipliers are needed in this direction, since the spread in the energy of a point target extends only over q samples in the memory. Figure 1 shows the total image data in the signal memory array and the two dimensional correlator with p and q multipliers in the range and azimuth directions respectively. The other point targets can be imaged by sliding this $p \times q$ correlator along and across the range direction.

The effect of the correlation operation is to slide the two dimensional correlator along the data and whenever a two dimensional match is obtained with the two dimensional reference function, a point is imaged. This, in effect, reduces the number of multipliers to be used in the two dimensional correlator. If no range migration (RM) is assumed, then the two dimensional operation along the range and the azimuth directions can be performed independently, since there is no cross coupling between the data in the two directions. The range compressed data lies parallel to the azimuth axis. Azimuth compression of the range processed data with an azimuth reference function results in the point target being imaged. Because of the forward motion of the radar platform and the Earth's rotation, the range of a point target response, however, varies with each transmitted FM pulse. This is because the instantaneous slant range from the satellite radar antenna to the point target on the ground varies appreciably during the total period over which the pulses are transmitted. Hence, the spread in the energy due to a single point target is nonlinear and is in two dimensions. So, when the data is compressed in the range direction, the path taken by the compressed data in the signal memory array is two dimensional in nature. Hence, if a one dimensional compression in the azimuth direction is to be done, then a correction has to be applied to align the data parallel to the azimuth axis. However, if a two dimensional azimuth compression is done, a two dimensional azimuth reference function is needed. This 2-D azimuth reference function should also take into account the satellite parameters such as pitch, yaw and roll.
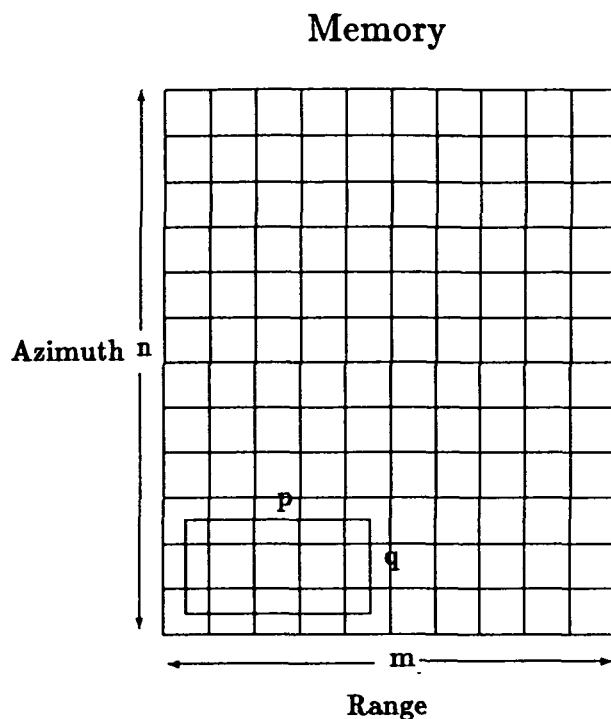
Memory

Figure 1: Total Image Data collected and a Two Dimensional Correlator with $p \times q$ Multipliers

3   Correlator

In signal processing, discrete time sequences and systems are extensively encountered. A common practice is to process discrete time sequences using discrete time systems. The discrete time system produces an output given by the convolution operation as:

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \tag{1}$$

where $x(k)$ and $h(k)$ are the input sequence and the impulse response of the system respectively.

The preceding 1-D signal processing operation can be extended to 2-D applications. In image processing, since the input data is inherently 2-D, the convolution and correlation operation will also be 2-D. The 2-D correlation expression is as follows:

$$y(n_1, n_2) = \sum_{k_1=-\infty}^{\infty} \sum_{k_2=-\infty}^{\infty} a^*(k_1, k_2)b(n+k_1, n+k_2) \tag{2}$$
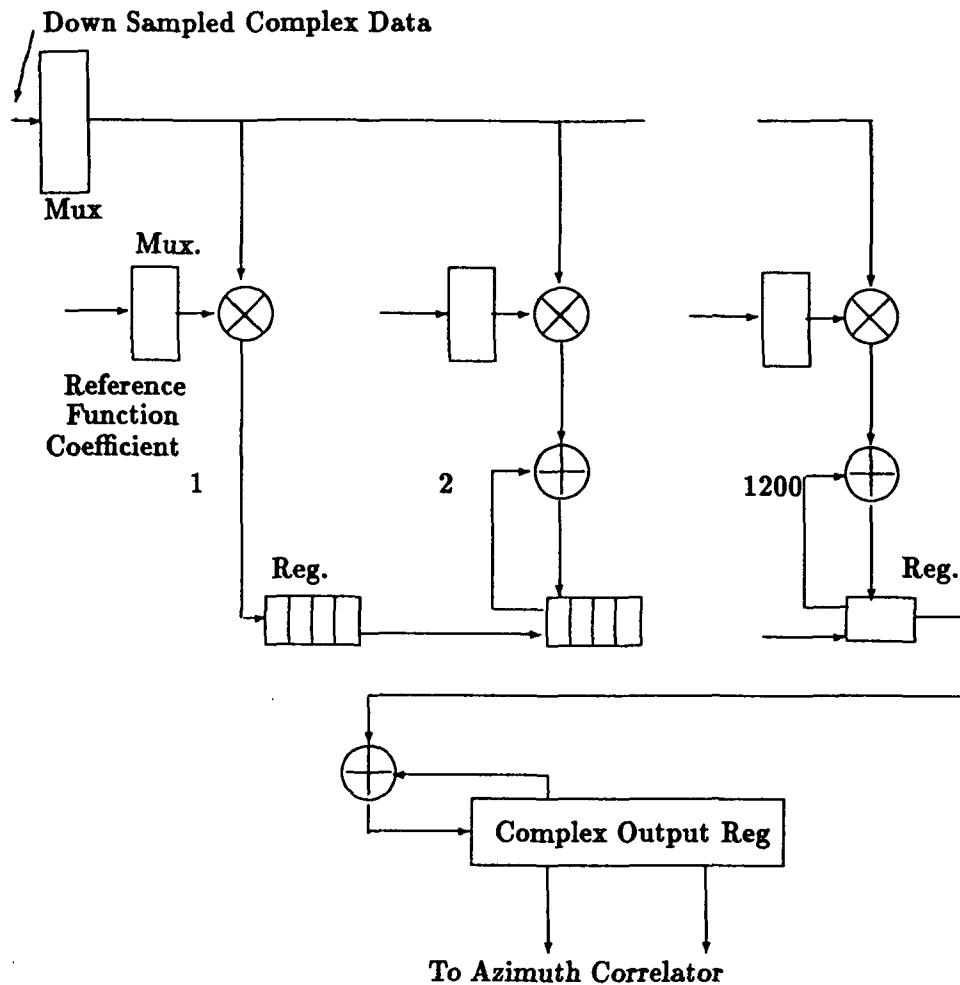
Figure 2: Block Diagram of the Correlator Circuit

3.1   Correlator Architecture

The one dimensional correlator architecture consists of a series of multipliers operating in parallel as shown in Figure 2. The multiplicand and the multiplier are in general both complex sequences. The multiplier operates at four times the speed of the data rate, since one multiplier is used to do the complex multiplication. The one dimensional correlation algorithm is implemented according to Equation 1.

The circuit shown above can be easily extended to the two dimensional correlation operation. For two dimensional correlation, the input data is an $n \times m$ array of complex numbers. Theoretically, the number of multipliers needed is equal to the number of elements in the array, i.e., $n \times m$ multipliers. However, a smaller number of multipliers can be used and correlation can be achieved if the reference function has many zero sample values. Then, the number of multipliers needed is equal to the number of non-zero samples in the reference function.
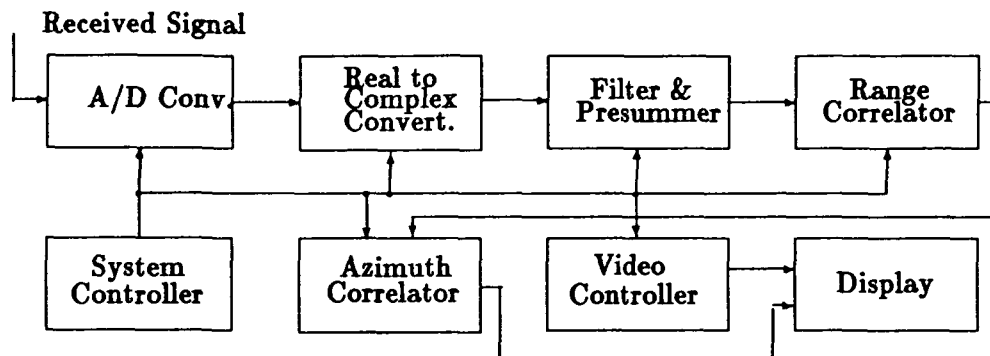
Received Signal

Figure 3: Block Diagram of SAR Processing Architecture

3.2 Significant Features of the Correlator

1. The architecture performs the two dimensional correlation with one data clock period latency.

2. The architecture is ideally suited for two dimensional correlation especially when there are a large number of zero coefficients in one of the functions being correlated.

3. Correlation output appears every data clock period.

4. A CMOS VLSI chip containing 64 multipliers configured as a correlator is possible.

4 A Real Time SAR Architecture

Processing SAR images involves compression techniques using correlation operations. The similarity in both range and azimuth processing enables similar hardware to be used for both operations. Using the correlator architecture described above, it is possible to implement the correlation operation with VLSI chips in the time domain. Hence, a time domain implementation is discussed in the following sections. This example is based on the SEASAT system parameters [4]. A block diagram of the time domain architecture is shown in Figure 3. The data received from the target area is sampled and converted to digital form by an A to D converter. The digitized data is converted to real and imaginary form to extract both the reflectivity and the phase information. The following sections briefly describe the block diagram.

4.1 Filter and Presummer

The azimuth time-bandwidth product required for the desired resolution is much lower than what is available in the received signal. In order to reduce the memory requirements

of the system and the processing data rates, the received data is filtered in the azimuth direction and then down sampled.

4.2   Range Correlator

Range correlation compresses the image in the range direction. The one dimensional range correlator uses the filtered and down sampled data and a reference function with 1200 samples. Each processor chip has 64 multiplier cells. Each multiplier cell has its own complex multiplier operating at $16MHz$, an adder and a 4 word register. With 1200 samples in the reference function, 20 such chips must be connected in parallel to perform real time correlation. The reference function samples are stored in buffers.

4.3   Azimuth Correlator

The azimuth correlation is performed on the range compressed data. The reference function is two dimensional in nature for the reasons explained in Section 2. The reference function depends on various parameters of the spacecraft and hence, has to be computed. 64 samples are usually needed in the reference function. Hence, a two dimensional correlator consisting of 64 by 64 multipliers is needed to compress the range correlated data. However, in the array of multipliers, all the coefficients except 64 are zero. Hence, only 64 multipliers are needed in the azimuth processor. The multipliers are loaded with the samples corresponding to a reference function that follows the range migration path of the target under consideration. The partial products obtained after every multiplication are stored in the memory according to the position of the 64 non-zero coefficients. The storage operation is performed by the video controller in conjunction with the video memory. Each location in the video memory corresponds to a pixel in the image. The azimuth two dimensional correlation is achieved by a single multiplier chip and the video memory.

4.4   Video and System Controllers

The video controller is a microcontroller which performs the complex function of retrieving processed data stored in the memory after every time the azimuth processor does a multiplication operation. The video controller also restores the summed data from the azimuth correlator in the original video memory location.

The system controller is a microcomputer coordinating the functions of all the subsystems of the architecture. It computes the reference functions based on the attitude parameters of the spacecraft and updates the coefficients in the corresponding units. The system controller also supervises the operation of the video control processor and the video output device.

4.5   Video Output

This is the final interface for the image. The data stored in the video memory comprises the final focussed image which can be transmitted or displayed.

4.6 Expected System Performance

The system is efficient, fast and uses no corner turn memory. Also, since a two dimensional azimuth processing is used, no explicit range migration circuitry is needed. The presummer and filter circuit reduce the data rates by a factor of 8. With the high speed multipliers and low data rates, the images, like those from SEASAT, can be processed in real time. Since CMOS VLSI chips are used, the size and power consumption are small and hence, ideally suited for on board space applications. Except for the three custom built ICs, the rest of the chips are available commercially. The memory used in the video processor are either video or BICMOS memories [5].

5 Conclusion

The theory behind the SAR signal processing has been discussed and a physical model is presented. A time domain correlator has been discussed. A real time SAR architecture using these correlators for processing SAR data has been presented. This architecture uses only a small amount of memory and performs no corner turn. The architecture is fast and efficient and uses three custom VLSI chips for its implementation.

References

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