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Phase Aligner for the Electronically Scanned Thinned Array Radiometer (ESTAR) Instrument

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Abstract: *A prototype Phase Aligner (PA) for the ESTAR (Electronically Scanned Thinned Array Radiometer) instrument has been designed and tested. Implemented in a single Xilinx XC3042PC84-125 Field Programmable Gate Array (FPGA), it is a dual-port register file which allows independent storage and phase coherent retrieval of antenna array data by the Central Processing Unit (CPU). It has dimensions of 4 X 20 bits and can be used at clock frequencies as high as 25 MHz.*

1. Introduction

ESTAR (Electronically Scanned Thinned Array Radiometer) is a passive synthetic-aperture radiometer designed to sense soil moisture and ocean salinity in L-band. It is being developed as an earth probe mission intended for launch in the late 1990's as part of the Earth Observing System (EOS).

A recent feasibility study [1] of the ESTAR concept recommended that a two-dimensional prototype be built in order to study further the design issues involved. Grand Valley State University Professor William A. Chren, Jr. was awarded NASA JOVE Grant NAG 8-226 to design and build four subsystems that will be part of the digital data subsystem (DDS) in this prototype. The third of these four subsystems, the Phase Aligner (PA), has been completed and is the subject of this memorandum. Two previous memoranda [2,3] presented the specifications of the first two of the subsystems, called the Output Data Formatter (ODF) and Walsh Function Generator (WFG).

Section 2 is a presentation of background information about the ESTAR. Subsequent sections present the details of the PA.

2. ESTAR Background

The synthetic aperture sensing technique employed by ESTAR is a method whereby the high spatial resolution and sensitivity of a large dish antenna can be duplicated with a small, lightweight cross-shaped array of dipole antennas (see Figure 1).

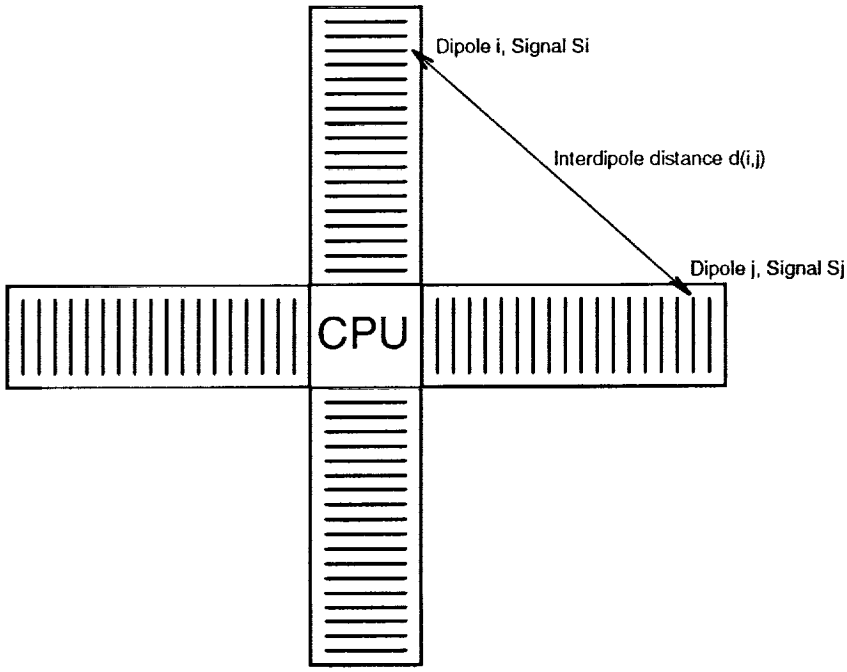


Figure 1: Dipole Antenna Locations on ESTAR Instrument

Such a duplication yields size and weight advantages which make it attractive for use on earth-sensing spacecraft. It is made possible by the calculation, for all pairs (i,j), of the pairwise complex correlation between dipole signals S_i and S_j using the formula

$$< S_i, S_j >= \frac{1}{T}\int_0^T S_i(t)S_j^*(t)dt, \qquad (1)$$

in which "*" denotes the complex conjugate and T is a suitably chosen integration period. It can be shown that each of these correlations is a sample, in frequency space, of the spatial Fourier Transform of the brightness temperature distribution over the field-of-view (FOV) of the antenna. Consequently, the visibility function in the FOV can be computed by inverting the sampled transform. Furthermore, the location of the sample in frequency space is determined only by the inter-dipole distance and not by the absolute locations of the dipoles themselves [4].

The data processing system on ESTAR will compute, in real time, these correlations for each dipole pair (i,j). Sensitivity and resolution specifications dictate that 145 dipoles (73 on each leg of the cross) must be used for a full ESTAR mission, or 73 (37 on each leg) for a reduced mission [5]. The correlations will be done digitally at a centrally located processing unit called the CPU, as shown in the figure. The results will then be sent to earth where the inverse transform will be computed. Necessary dipole signal preprocessing, including down-mixing and A/D conversion, will be done at each dipole by circuitry contained in a "Front End Module" (FEM).

2.1 Major Digital Data Subsystem Components

At the functional level, the digital data subsystem (DDS) consists of six major components [6]. The first of these, the Digitizer, must convert the FEM data to digital form before sending it to the CPU. This will be done by an A/D converter in each FEM. The second, the Data Bus, must transport the digitized data from the FEMs to the CPU. The third, the CPU, must compute the correlations for each pair of FEMs. It is also responsible for overall control of the DDS. Furthermore, it must interface with the Small Explorer Data System (SEDS), which is a software and hardware "operating system" on the space vehicle. Among other tasks, SEDS performs overhead functions such as data error immune encoding and transmission to earth, earth command processing and system test. The CPU must pass the correlation products to SEDS for transmission to earth. The fourth component, the System Clock, is necessary to ensure that dipole data samples are generated synchronously by all FEMs. In effect, the Clock signals the FEMs to generate data samples at the same instant of time. The fifth part, the Phase-Aligner (PA), removes the phase differences between FEM samples when they arrive at the CPU. These differences are caused by unequal data propagation times to the CPU from distant and nearby FEMs. The PA must hold the early-arriving data until the late-arriving data is available. Only when all FEM data for a particular sample time have arrived at the CPU will the PA signal the CPU that the data is ready for correlation. The sixth component, the Walsh Function Generator (WFG), generates a unique

Walsh function signal for each FEM. This signal is used to cancel low frequency noise generated by the analog circuitry in the FEM.

These six components fit together as shown in Figure 2. Note that the Phase Aligner completely surrounds the CPU so as to effect phase adjustment for all four legs of the array. As will soon be discussed, the CPU must generate a single data retrieval clock signal which will access simultaneously the phase-aligned data from all four sections of the PA.

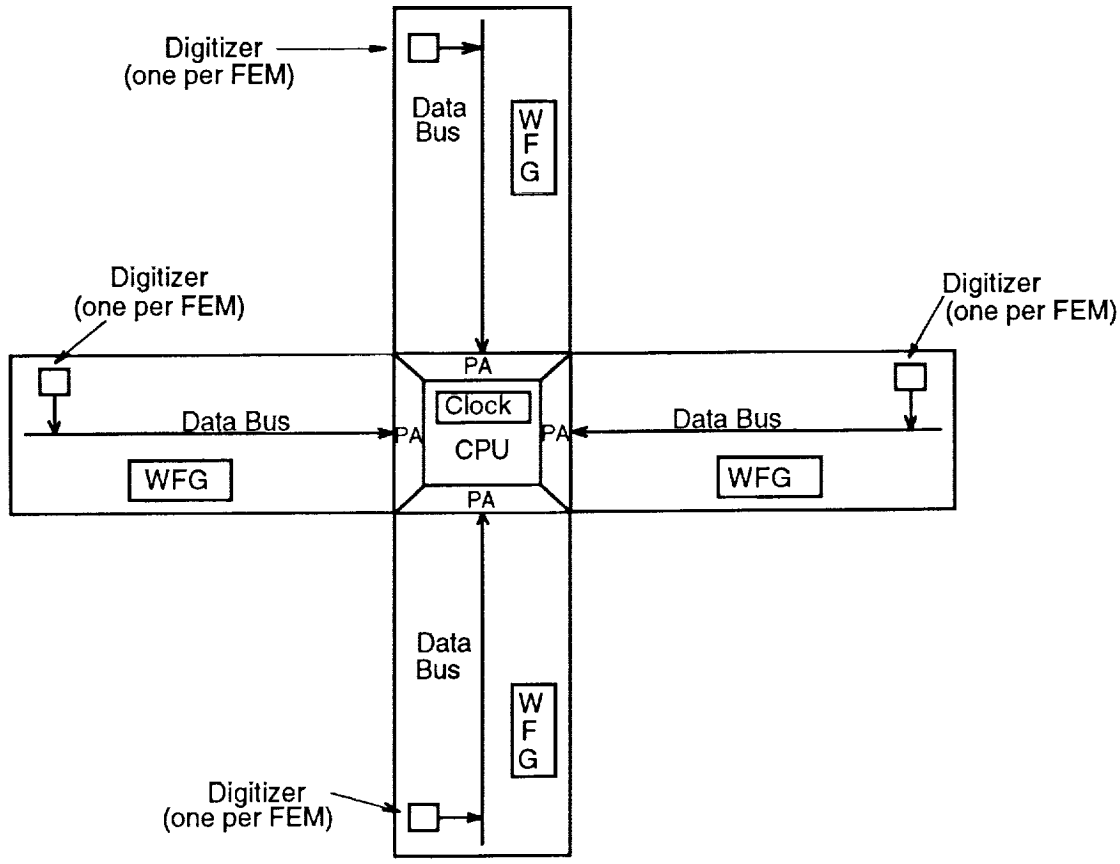


Figure 2: Six Major Components of the DDS

2.2 Phase Aligner Requirements

As mentioned above, the Phase Aligner must store early FEM data until late data can arrive. Typically, the device used for such applications is a synchronous First-In First-Out (FIFO) stack. It is essentially a dual port static RAM with two separate and independent addressing and data ports [7]. The output data is read in the order it was stored. It allows an "upstream" device to store data independently of a reading "downstream" device. The stored data can be read at any time. As long as the average input and output data rates are equal the FIFO will not overflow. Extra circuitry is included on chip to monitor capacity and set external "empty" and "full" flags.

Each of the four parts (one for each leg of the cross in Figure 2) of the PA must be wide enough to accommodate the Data Bus outputs. The Data Bus will be implemented using

differential coaxial cable and some number of 1.2 Gbaud transmitter/receiver chips called *G-Taxis*. These chips, from Vitesse Semiconductor, implement all the communication link overhead such as error detection/correction, data packing/unpacking and formatting. Each G-Taxi transmitter has 40 parallel data input and output pins. Every FEM produces digitized quadrature data encoded in two bits/channel, and therefore one G-Taxi chipset is needed for every ten FEMs. In the full (reduced) ESTAR deployment, we will therefore need 4 (2) G-Taxis per leg, and consequently each of the four legs of the Phase Aligner must be 160 (80) inputs wide. Figure 3 shows the number of inputs to the Phase Aligner for a full ESTAR deployment.

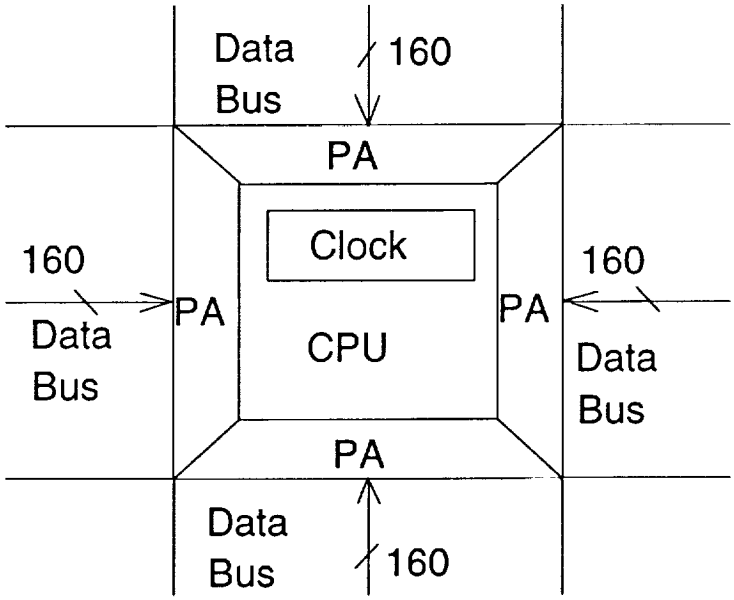


Figure 3: Phase Aligner Inputs for a Full ESTAR Deployment

The depth of the PA FIFO must be computed from the worst case travel time for data to traverse one leg of the cross. The legs are 5m (2.5m) long in the full (reduced) versions. Assuming a worst case propagation velocity of 5 nsec/meter for the FEM data, we conclude that the worst case transit time for the data is 25 (12.5) nsec. The prototype is to be operated at a maximum frequency of 25MHz, and therefore the transit time is equal to a maximum of .63 (.32) clock periods. Consequently, we require a storage depth of at least 1 in both full and reduced versions of the PA. In order to allow for design expansion, the Phase Aligner FIFO was implemented with a depth of 4 so that higher clock speed versions of the ESTAR can be built. With a depth of 4 the maximum clock frequency that can be used in the full ESTAR deployment is

$$f_{max} = \frac{4}{25} = 160 \text{ MHz},$$

although the PA prototype has been designed for a maximum frequency of 25 MHz. Figure 4 summarizes the input/output and depth requirements of the Phase Aligner. Note that

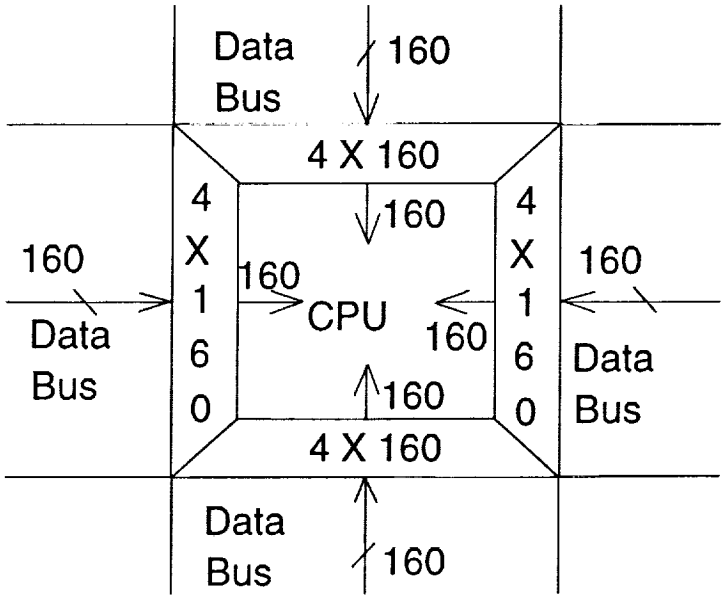


Figure 4: Phase Aligner Inputs, Outputs and Depth for a Full ESTAR Deployment

a partial ESTAR deployment would halve the number of input and output lines.

3. Phase Aligner Design

3.1 General Description

The Phase Aligner will be built using 32 of the 4 X 20 FIFO prototypes depicted in Figure 5. As can be seen in the figure, the prototype has separate, independent input and output

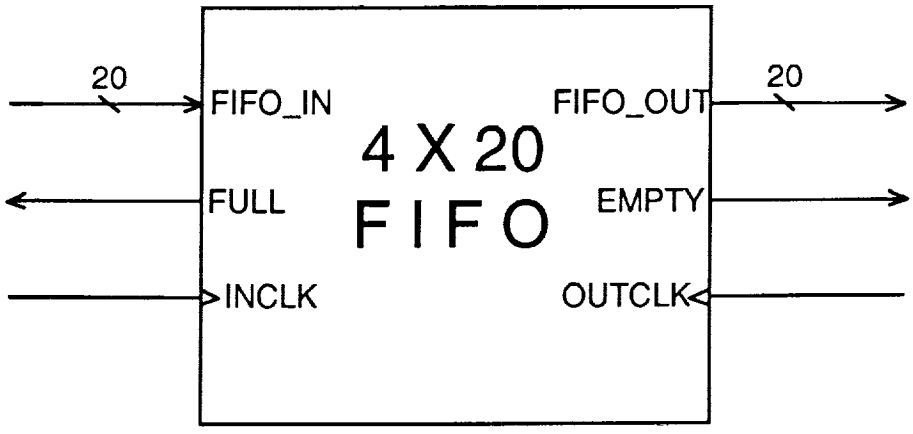


Figure 5: Phase Aligner FIFO Input/Output Configuration

leading edge clocking which will be controlled by the Data Bus and CPU respectively. The positive logic FULL and EMPTY outputs indicate to the Data Bus and CPU controller,

respectively, that the appropriate condition has occurred. The Data Bus and Controller will be designed to cease further clocking under this condition, until it no longer exists. The 20 input and output lines are positive logic and are fully buffered.

Operation of the prototype is as follows. A positive-going transition on INCLK strobes the data on the FIFO_IN lines into one of four internal 20-bit data registers. A positive-going transition on OUTCLK causes the data stored in one of the internal data registers to be placed on the output lines FIFO_OUT. Which of these four internal 20-bit wide data registers receives the input data or is the source of the output data is determined by internal address registers whose operation will be discussed below. The FULL flag is asserted when four transitions on INCLK occur in a row, without an intervening transition on OUTCLK. This corresponds to the situation where all four internal data registers have been filled with input data. The EMPTY flag is asserted when four transitions on OUTCLK occur in a row, without an intervening transition on INCLK. This corresponds to the situation where all four internal data registers have had their data strobed onto the FIFO_OUT lines.

Figure 6 depicts the internal structure of the FIFO prototype. In the figure, the Input and

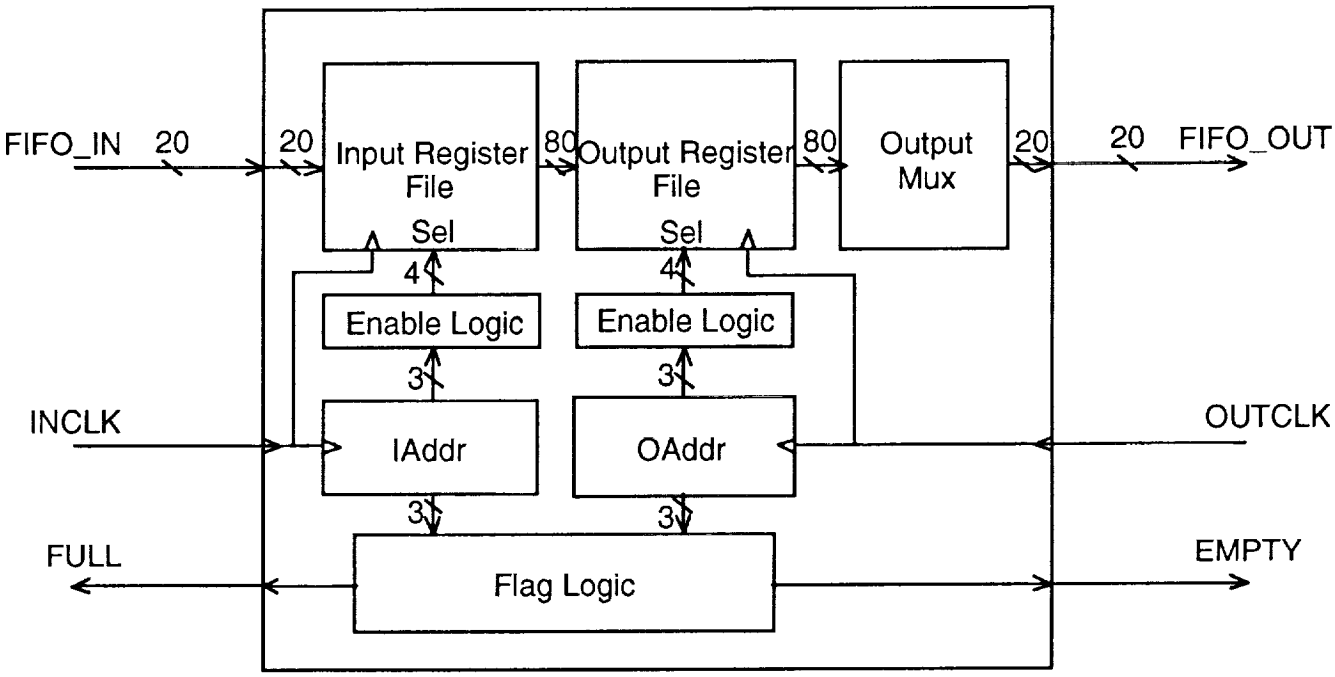


Figure 6: Phase Aligner Prototype Internal Architecture

Output Register Files are identical banks of four 20-bit wide registers whose internal architecture is shown in Figure 7. From the latter figure, it can be seen that the Input

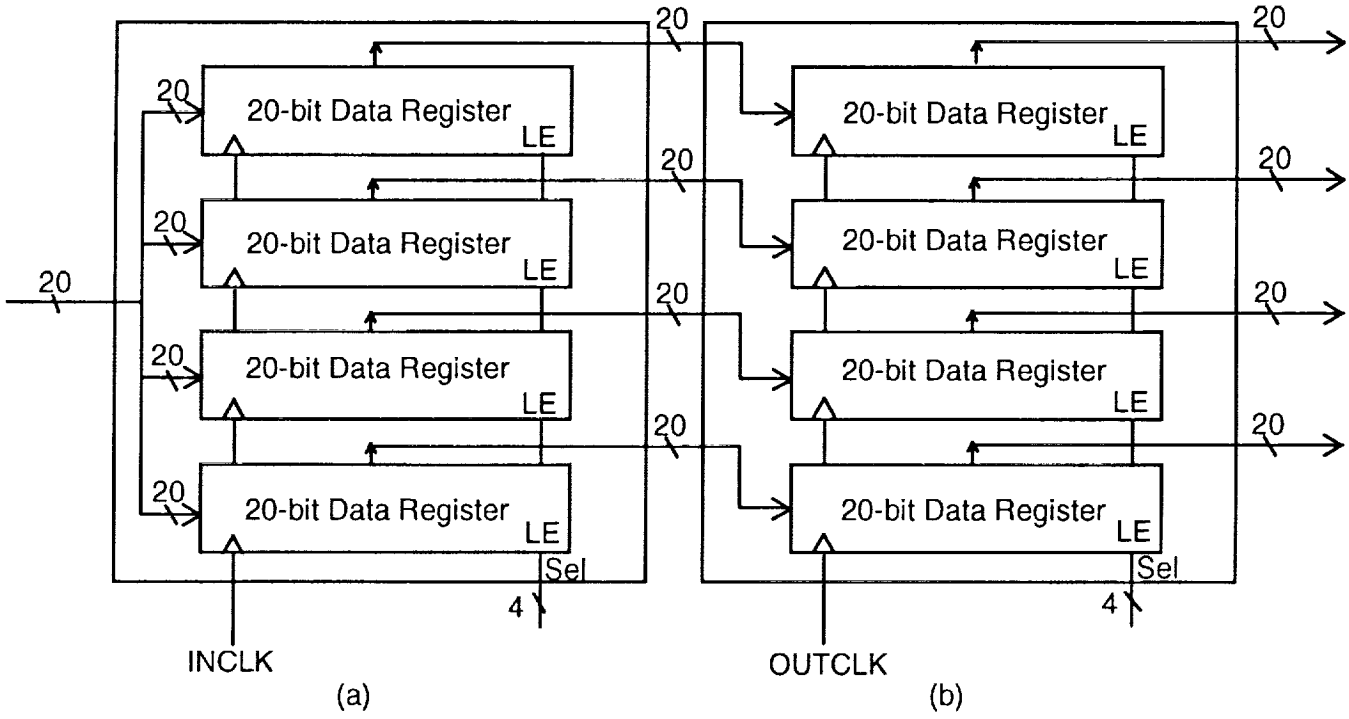


Figure 7: a) Input and b) Output Register File Internal Architecture

Register File, clocked by the INCLK, has all of its stored data (80 bits) fed to the Output Register File, which is clocked by the OUTCLK. The four Sel lines determine which of the four registers in each file responds to the clock signal. These lines are encoded using a "one hot" code so that only one register is enabled at any time. The outputs of the others are zero. The dual file structure was chosen because it allowed independent assertion of the clock inputs while not requiring any clock gating.

From Figure 6 it can also be seen that the 80-bit output from the Output Register File is input to the Output Mux, which selects the proper register data for the FIFO_OUT data lines. Note that the proper output register is selected by the four Sel lines, which are encoded using the "one hot" code mentioned above. Note that no "select" inputs are needed for the Output Mux because only one of the Output Register File registers is enabled at any time. This fact allows the Output Mux to be implemented using an array of twenty 4-input OR gates.

The clocking signals INCLK and OUTCLK are also fed into identical 3-bit address registers IADDR and OADDR, which perform data storage management. At any time, IADDR contains the address of the next register in the Input Register File that is available for input data storage. Similarly, the OADDR register points to the next register in the Output Register File whose data is to be output. The counting sequence of these address registers is the 3-bit Gray code shown in Table 1. In the table, the present count value is denoted by the unstarred state

Table 1: Counting Sequence for Address Registers IADDR and OADDR

Present State			Next State		
Q_0	Q_1	Q_2	Q^*_0	Q^*_1	Q^*_2
0	0	0	1	0	0
1	0	0	1	1	0
1	1	0	0	1	0
0	1	0	0	1	1
0	1	1	1	1	1
1	1	1	1	0	1
1	0	1	0	0	1
0	0	1	0	0	0

variables. The Gray code was used rather than the binary code because its sequence adjacency property minimizes the possibility of count glitches when the design is placed and routed on the FPGA.

The output of the IADDR and OADDR registers is fed to two different subsystems, as can be seen in Figure 6. One of these, the Enable Logic, is a decoder which converts the Gray code to a "one hot" code for use as the select inputs for the register files. The internal architectures of the Enable Logic blocks are identical, and are a straightforward decode function.

The other type of subsystem in Figure 6 is the Flag Logic, which produces the active high outputs FULL and EMPTY. The Flag Logic asserts the EMPTY flag when the addresses in the IADDR and OADDR are the same. This corresponds to the situation where there is no data stored in the FIFO. The Full flag is asserted when the addresses are separated by four transitions on INCLK (i.e., loosely speaking, when the "IADDR address exceeds the OADDR address by 4"). This corresponds to the state when four consecutive INCLK transitions have been received. It is the responsibility of the external circuitry to avoid asserting INCLK when FULL is asserted, and OUTCLK when EMPTY is asserted.

The architecture of the Flag Logic is a straightforward implementation of the equations

$$\text{EMPTY} = (Q_0^I \oplus Q_0^O)' (Q_1^I \oplus Q_1^O)' (Q_2^I \oplus Q_2^O)'$$

$$\text{FULL} = (Q_0^I \oplus Q_0^O)' (Q_1^I \oplus Q_1^O)(Q_2^I \oplus Q_2^O)$$

where superscripts denote bit membership in either IADDR or OADDR, and ' denotes complementation. These expressions can be shown to be minimal implementations of the full and empty conditions discussed above.

3.2 Circuit Operation

Initialization or Reset

Input Storage/Output Retrieval

Positive-going transitions on INCLK strobe the 20-bit data words on the FIFO_IN lines into successive internal 20-bit data registers. Positive-going transitions on OUTCLK cause the data stored to be placed on the output lines FIFO_OUT in the same order in which it was strobed in. Which of the four internal 20-bit wide data registers receives the input data, or which becomes the source of the output data is determined by internal address registers IADDR and OADDR. The former always points to the next register available for strobing data into, and the latter always points to the next register whose data is to be strobed out. Active high output flag FULL is asserted when four transitions on INCLK occur in a row, without an intervening transition on OUTCLK. This corresponds to the situation where all four internal data registers have been filled with input data. Active high output flag EMPTY is asserted when four transitions on OUTCLK occur in a row, without an intervening transition on INCLK. This corresponds to the situation where all four internal data registers have had their data strobed onto the FIFO_OUT lines. It is the responsibility of the external controlling circuitry to avoid asserting INCLK (OUTCLK) when the FULL (EMPTY) flag is asserted.

4. Specifications

The schematic diagram of the Phase Aligner prototype FIFO is shown in Figure 8.

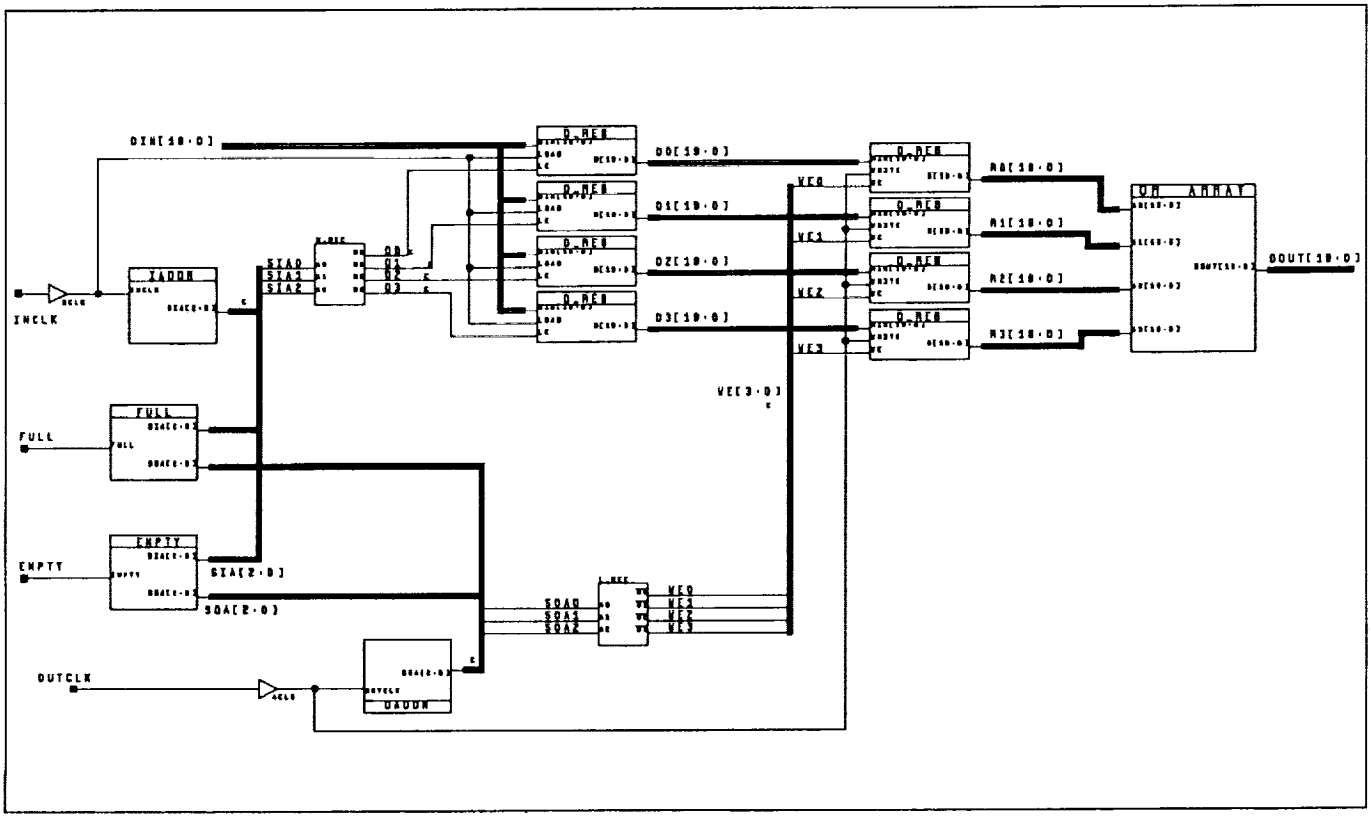


Figure 8: Phase Aligner FIFO Prototype Schematic Diagram

4.1 Electrical Specifications

Maximum Absolute Ratings:

Symbol	Description	Value	Units	Conditions
V_{cc}	Supply Voltage	-.5 to +7.0	V	
V_{in}	Input Voltage	-.5 to Vcc + .5	V	
V_{TS}	Tri-state applied voltage	-.5 to Vcc + .5	V	
T_{STG}	Storage Temperature	-65 to +150	Degrees Centigrade	
T_{SOL}	Max. Soldering Temperature	+260	Degrees Centigrade	
T_J	Junction Temperature	+125	Degrees Centigrade	

Recommended Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{cc}	Supply Voltage 0°C to 70°C	4.75	5.25	V	
V_{IHT}	TTL High-Level Input	2.0	Vcc	V	
V_{ILT}	TTL Low-Level Input	0	0.8	V	
V_{IHC}	CMOS High-Level Input	70%	100%	V	
V_{ILC}	CMOS Low-Level Input	0	20%	V	
T_{IN}	Input Transition Time		250	ns	

DC Characteristics Over Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
V_{OH}	High-Level Output Voltage	3.86		V	I_{OH}= 4.0mA V_{CC} min
V_{OL}	Low-Level Output Votage		.32	V	I_{OL}=4.0 mA V_{CC} max
V_{CCPD}	Power-Down Supply Voltage	2.3		V	
I_{CCPD}	Power-Down Supply Current		120	µA	V_{CC} max T max
I_{IL}	Input Leakage Current	-10	+10	µA	
C_{IN}	Input Capacitance		10	pF	Sample Tested

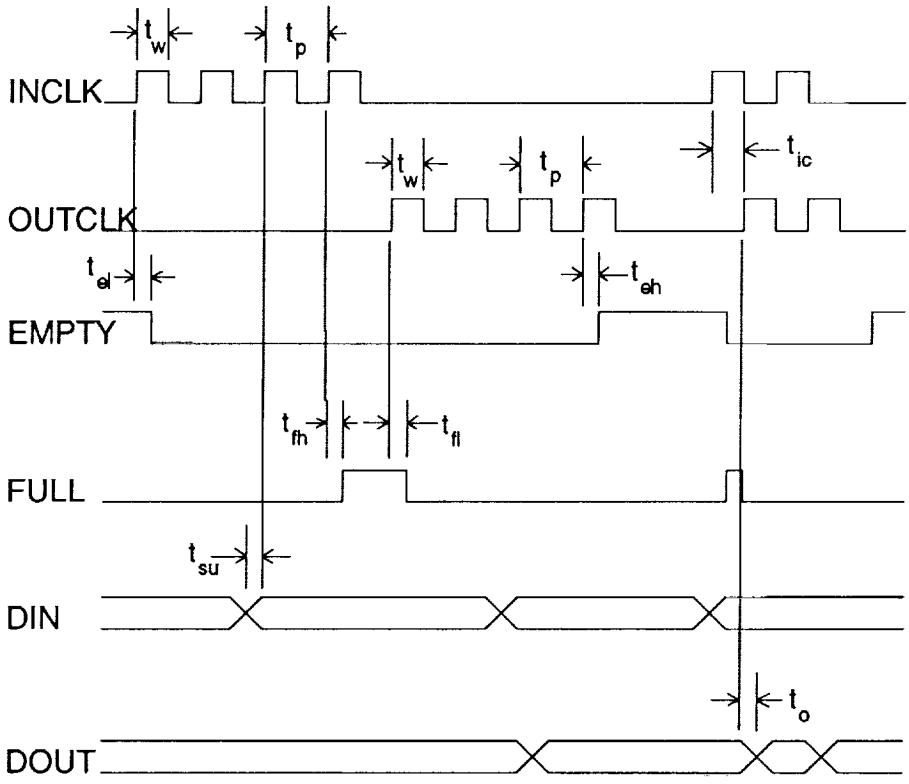
AC Electrical Characteristics Over Operating Conditions:

Symbol	Description	Min	Max	Units	Conditions
t_{rise}	Input rise time		250	ns	Worst case[1]
t_{fall}	Input fall time		250	ns	Worst case[1]
t_w	High time INCLK and OUTCLK	3		ns	Worst case[1]
t_p	Period INCLK and OUTCLK	40		ns	Worst case[1]
t_{ic}	Interedge time INCLK and OUTCLK	0[2]		ns	Worst case[1]
t_{el}	Time to valid EMPTY from INCLK		28	ns	Worst case[1]
t_{eh}	Time to valid EMPTY from OUTCLK		37	ns	Worst case[1]
t_{fh}	Time to valid FULL from INCLK		32	ns	Worst case[1]
t_{fl}	Time to valid FULL from OUTCLK		30	ns	Worst case[1]
t_{su}	Setup time for FIFO_IN data from edge of INCLK		17	ns	Worst case[1]
t_o	Positive-going OUTCLK edge to FIFO_OUT valid		34	ns	Worst case[1]
f	CLOCK frequency		25	MHz	Worst Case[1]

Notes:

1) 70^0 C and 4.75 volt supply.
2) Does not allow EMPTY and FULL to become valid.

Timing Diagram:



5. Signal Descriptions

5.1 Control Inputs

OUTCLK	Strobes data out of the FIFO on leading edge
INCLK	Strobes data into FIFO on leading edge

5.2 Control Outputs

EMPTY	Active high denotes no data stored
FULL	Active high denotes no more data can be stored

5.3 Data Inputs

FIFO_IN[19:0]	20 data bits to be stored on assertion of INCLK

5.4 Data Outputs

FIFO_OUT[19:0]	20 data bits of stored data retrieved on assertion of OUTCLK

6. Package Type

The WFG is implemented in a 84-pin PLCC package with a speed grade of 125 MHz (part number XC3042PC84-125). The FPGA gate density is 73% (105/144 available CLBs used); the pin density is 60% (44/74 available IOBs used).

7. References

[1] Levine, D. M., Hilliard, L., et. al., 1990, *Electronically Scanned Thinned Array Radiometer (ESTAR) Earth Probe Concept: An Engineering Feasibility Analysis*, Goddard Space Flight Center, page 9.

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[5] Levine, D. M., Gatlin, J., et. al., *Peer Review of LaRC Six-Month Study of "ESTAR" Small S/C Mission*, Langley Research Center/Goddard Space Flight Center internal document, 10/9/92.

[6] *A Digital Data Subsystem Design for an L-band ESTAR Instrument: A Summary of Research Performed in the JOVE Fellowship Program, 6/1/91 through 11/30/91*, page 5, Appendix A of *ESTAR Digital Data Subsystem Development*, Chren, W. A., Jr., Grand Valley State University, 12/15/91.

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13. ABSTRACT *(Maximum 200 words)*

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14. SUBJECT TERMS

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