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COMPACT DISC ERROR MEASUREMENTS

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OBJECTIVES

The objectives of this project are as follows:

Provide hardware and software that will perform simple, real-time, high resolution (single-byte) measurement of the error burst and good data gap statistics *seen by a photoCD player read channel* when recorded CD write-once discs of variable quality (i.e., condition) are being read (9/93);

Extend the above system to enable measurement of the hard decision (i.e., 1-bit error flags) and soft decision (i.e., 2-bit error flags) decoding information that is produced/used by the Cross-Interleaved-Reed-Solomon-Code (CIRC) block decoder employed in the photoCD player read channel (1/94);

Construct a model that uses data obtained via the systems described above to produce meaningful estimates of output error rates (due to both uncorrected ECC words and misdecoded ECC words) when a CD disc having specific (measured) error statistics is read (completion date to be determined); and

Check the hypothesis that current adaptive CIRC block decoders are optimized for pressed (DAD/ROM) CD discs. If warranted, do a conceptual design of an adaptive CIRC decoder that is optimized for write-once CD discs (completion date to be determined).

BACKGROUND

Equipment that determines whether a given CD disc conforms with the Phillips "Red Book" error specifications is commercially available. To make this determination, however, this equipment does not monitor data read from the disc, i.e., it does not directly measure disc errors. Instead, it monitors pin outputs on its CIRC block decoder chip (i.e., the VLSI circuit that performs the decoding of the C1 and C2 ECC words) that indicate when either a one-byte, or two-byte error is corrected, or when an error of length greater than two-bytes is detected, by either the C1 or the C2 ECC decoder. The equipment averages the results of this pin monitoring activity over one-second intervals before reporting them. Although this is adequate for a "yes/no" determination of the disc's conformance to the Red Book error specifications, it is not adequate for high resolution (single byte) mapping of a disc's errors. To see that this is true, consider that at the nominal CD playback scan velocity of 1.3 m/s, one second represents, on average, five full spiral turns of the 120 mm diameter disc, i.e., a surface area of 2.08 mm² (since

the nominal track-to-track spacing on a CD disc is $1.6 \mu\text{m}$). This should be compared to the disc real estate occupied by a single byte; one byte occupies a length of $5.1 \mu\text{m}$ along the disc's spiral track, which corresponds to a surface area of $8.16 \times 10^{-6} \text{ mm}^2$ on the disc. The coarseness of error event measurements delivered by commercial CD disc evaluation equipment, together with the fact that such equipment does not directly "look at" the data being read from the disc, diminishes the usefulness of this commercial equipment for certain applications. Activities such as disc manufacturing process development/control and disc aging/degradation studies require the observation of small changes in the type and number of errors residing on a disc.

The system identified in the first of the four project goals listed above, which will be completed this summer, will provide high resolution (single-byte) measurement of the error events on specially recorded CD discs (i.e., discs that have a repetitive 24-byte data pattern written to them using the CD-Audio format) that are played on a Phillips Model CCD-461 CD-ROM player. The fact that a particular data pattern must be present on the disc is not a limitation since this system is meant for use with (i.e., studies of) write-once CD discs which can have any specified data written on them for experimental purposes. (Note: we have determined that our hardware could be adapted to high resolution measurement of errors on CD discs containing arbitrary data, e.g., pressed CD-ROM discs.)

PROGRESS

To understand the following description of the CD error measurement system that we are developing, one must know how the various CD data structures, such as C1 and C2 codewords and EFM frames, are organized on (i.e., recorded on) a CD disc. This background information is contained in Appendix I ("Determining the Locations of the Various CIRC Recording Format Information Blocks [User data blocks, C2 & C1 word and EFM frames] on a Recorded Compact Disc"). It is recommended that those interested in the details of our CD error measurement system read that Appendix to facilitate their understanding of what follows.

The scheme we are using to perform high resolution measurement of the errors on CD discs is enabled by the architecture of the Phillips CD3A CIRC block decoder, which is a VLSI circuit that performs data detection, channel data demodulation and C1 & C2 ECC decoding. It is the latest generation CIRC block decoder; it features adaptive data detection, intelligent channel clock synchronization, and soft decision ECC decoding. This chip's C1 ECC decoder will determine how to handle a given received C1 codeword based on the calculated syndrome for that word *and* whether any 1-bit erasure flags are attached to any of the bytes of the word (by the eight-to-fourteen channel data demodulator); its C2 decoder chooses how to treat a given received C2 word based on the calculated syndrome for the word *and* the distribution of 2-bit soft-error flags that accompany the word (a 2-bit flag

is attached to every C2 word byte when the byte is output by the C1 decoder). The CD3A chip is used in the Phillips CCD-461 CD-ROM player as well in the Kodak PhotoCD player.

A high level diagram of the CD3A chip is given as Fig. 1. The aspect of this chip's architecture that we exploit is the fact that data are clocked from the chip itself to an external RAM, and back, as illustrated in Fig. 1. This is done to implement the de-interleaving that is required to obtain C1 codewords from the EFM frames that are sequentially read from the disc, and to obtain C2 codewords from the data blocks that are output by the C1 decoder. By monitoring the data traffic marked as "write 1" in Fig. 1 we intercept the serial data stream recovered from the disc after eight-to-fourteen channel data demodulation has occurred, but before any ECC decoding. After appropriate synchronization is obtained, this data stream is organized into individual EFM frames.

Phillips CD3A Decoder

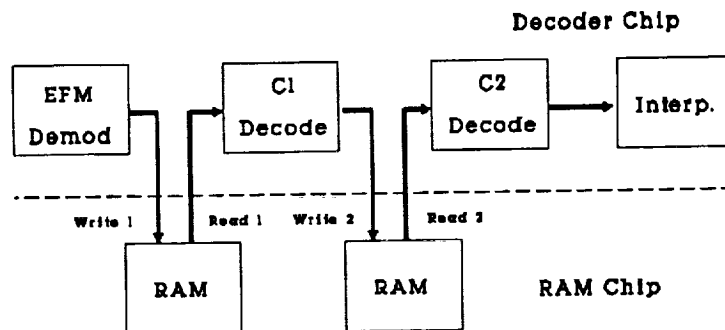


Figure 1.

If a given 24-byte block of user data is repetitively recorded on the disc being read, the lower 32 bytes of each of the recovered EFM frames will be identical, assuming that there are no errors in the block (cf., Appendix I). Therefore, by comparing each recovered EFM frame, byte by byte, with the exact 32-byte pattern that would be present in each EFM frame in the absence of errors, any error that is contained in an EFM frame can be located. Fig. 2 illustrates this; the block labeled "error detector" in that figure represents the 32-byte comparator. This logic element outputs 32 bits in response to each EFM frame comparison operation; a "zero" is output if two compared bytes are identical, a "one" is output if they are not. The hardware will be developed in two phases (versions). Phase I will produce one output byte for each EFM frame in which an error is detected and the output byte will specify the number of erroneous bytes in the contaminated EFM frame. The Phase I hardware will provide intermediate resolution error measurements, i.e., error counts will be averaged over a spatial disc track segment that corresponds to a single EFM frame, which nominally occupies a distance along the track of about 0.176 mm (this distance includes EFM frame overhead). An advantage of the Phase I system

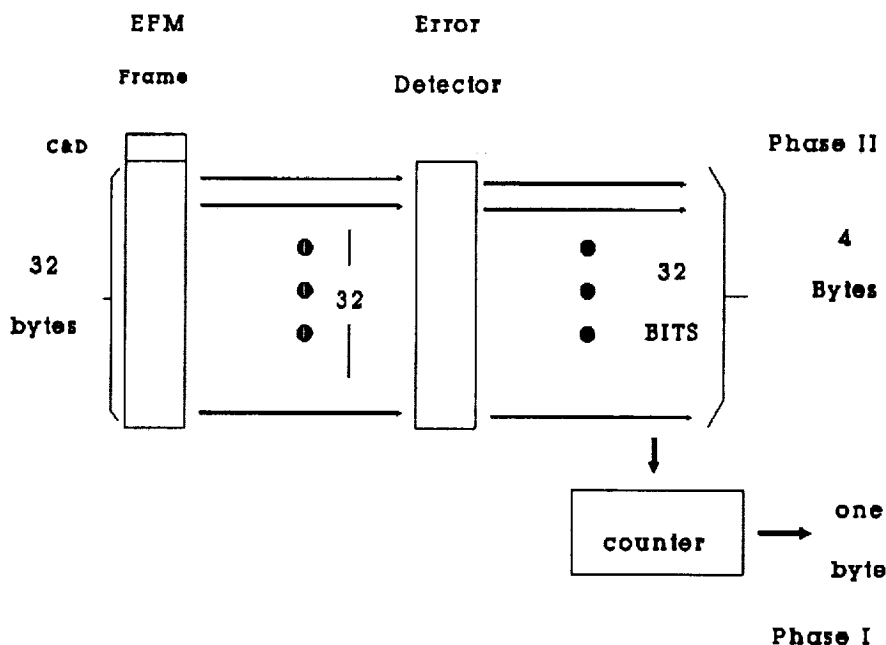


Figure 2.

is that its output data can be processed in real time and we plan to provide polar graph visualizations of the measured error statistics. Phase II hardware, which will produce 4 output bytes for each EFM frame comparison, will provide high resolution (single-byte) error burst and good data gap length measurements. Output data from this system will be stored for post processing.

As an extension to this project, we plan to extend the Phase II hardware's functionality to the collection of the 1-bit erasure flags that are generated by the eight-to-fourteen demodulator in response to channel data run-length violations (cf., the second project goal listed at the beginning of this report). These flags are passed across the CD3A CIRC block decoder RAM interface along with the EFM frame data (cf., Fig. 3). We also will study the possibility of collecting the 2-bit soft decision flags that are generated by the C1 decoder and passed to the C2 decoder for its use in selecting an error handling strategy. These 2-bit flags appear on the CD3A RAM interface at the point labeled "write 2" in Fig. 1.

During the past quarter we have determined the sequencing used for writing and reading both data and error flags to/from the CD3A RAM; we have devised a method of obtaining EFM frame block synch; we have worked out a scheme for relating measured error events to a geometrical location on the disc; and we have completed a high (logical block) level design of the CD error measurement hardware. We are currently designing/constructing the functional system subblocks and writing the system control software.

Phase II Hardware

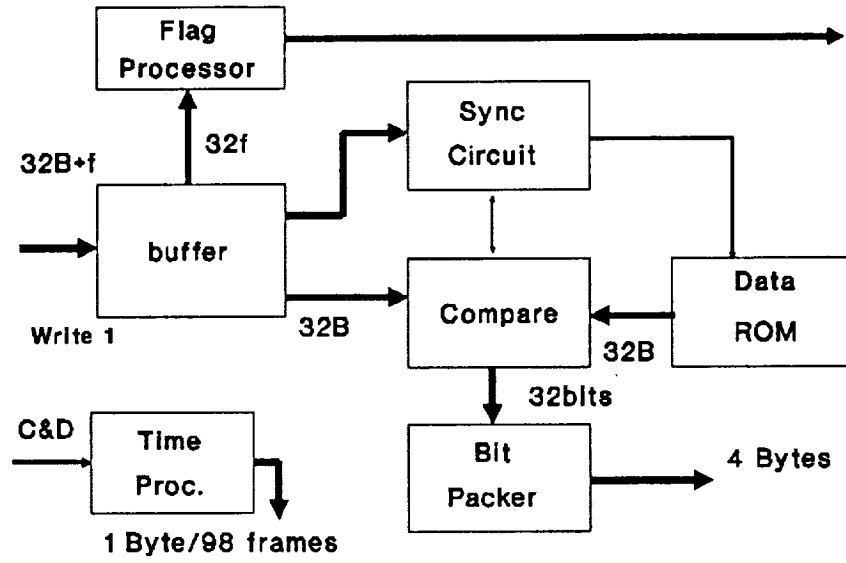
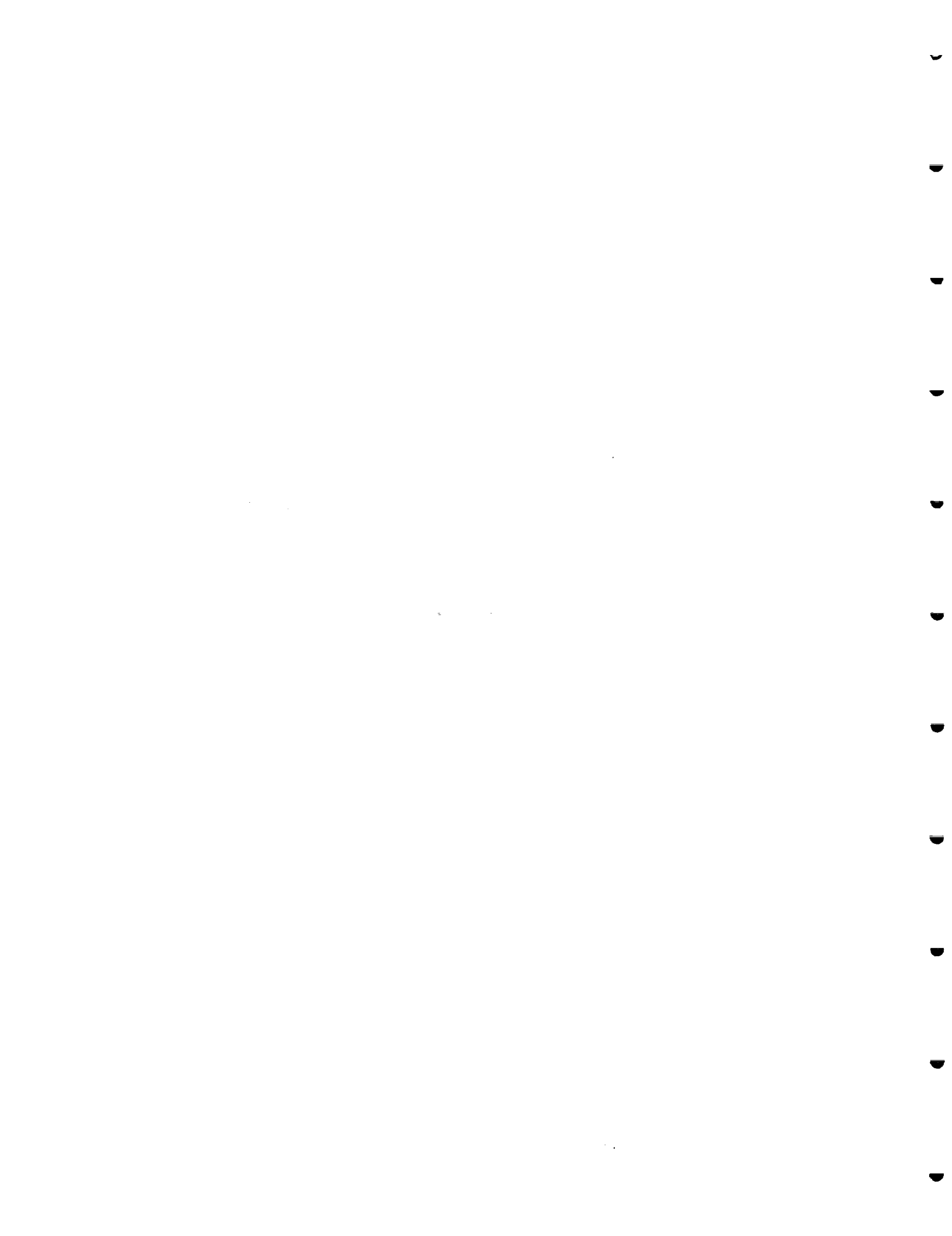


Figure 3.



SECTION 2. APPENDICES

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APPENDIX A

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