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**NASA Space Engineering Research Center for
VLSI Systems Design
University of New Mexico/University of Idaho
Grant NAGW-3293**

Proposal and Annual Review

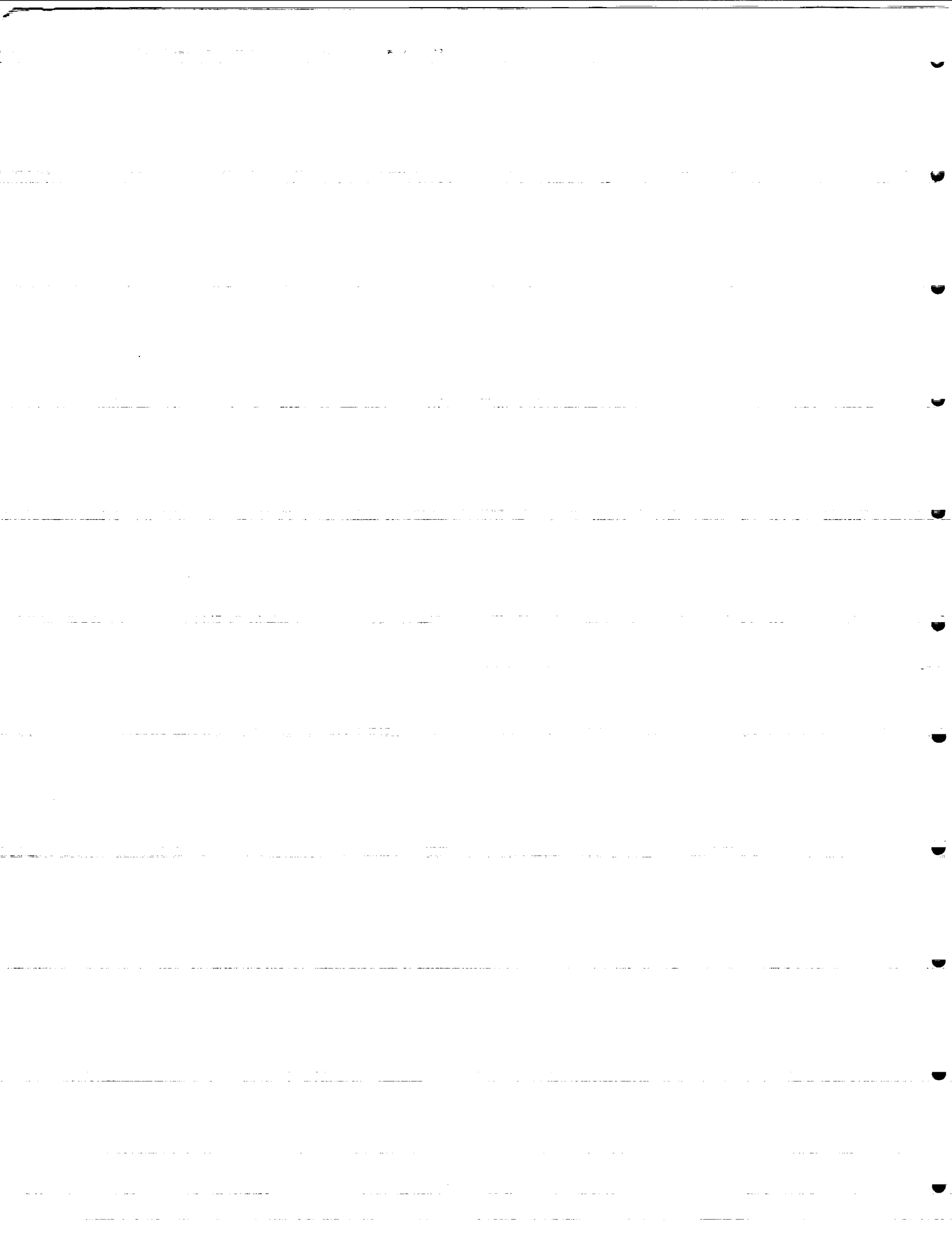
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VLSI SYSTEM DESIGN Proposal and
Annual Review (New Mexico Univ.)
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1 Summary

1.1 Introduction

This annual report outlines the activities of the past year at the NASA SERC on VLSI Design. Highlights for this year include:

- A significant breakthrough was achieved in utilizing commercial IC foundries for producing flight electronics.
- The first two flight qualified chips were designed, fabricated, tested and now being delivered into NASA flight systems.
- A new technology transfer mechanism has been established to transfer VLSI advances into NASA and commercial systems.

1.2 Published Papers

A summary of all referred papers that have been published in conferences and journals is given in Section 3. The number of papers published per year is shown in Table 1.

Year	Number of Papers
1989	14
1990	19
1991	41
1992	25
1993	14

Table 1: Paper Summary

Data covering the four symposia on VLSI Design is provided in Section 4. Table 2 presents a summary of papers presented at the four symposia. Next years symposium will be held in Albuquerque on November 4 and 5, 1993. Greater attendance is anticipated being closer to national laboratories.

	Date	SERC Authors	Outside Authors	Total Papers
1st Symposium	Jan 1990	18	7	25
2nd Symposium	Nov 1990	19	16	35
3rd Symposium	Oct 1991	23	23	46
4th Symposium	Oct 1992	17	27	44

Table 2: Symposium Summary

1.3 Research Technology Transfer

Technology transfer from the laboratory to NASA is a high priority SERC activity. Table 3 shows a list of projects that have been or are being transferred to space data systems.

Project	Mission	Application
Flight CCSDS Encoder	XTE TRMM ACE	Communication
Bus Controller	XTE TRMM HST	Microprocessor Controller
Lag Correlator	Arecibo, Greenbank	Science
Data Compression	Landsat 7	Communication

Table 3: Processors In NASA Systems

- **Flight CCSDS Encoder** The encoder is a custom processor designed with UTMIC flight qualified electronics. The chip was delivered to GSFC and JPL in September 1992, tested in NASA systems, radiated at Brookhaven National Laboratories, and approved for flight use. The chip is being fabricated and qualified for use in XTE, TRMM and ACE.
- **Bus Controller** The microprocessor bus controller is a custom processor designed with UTMIC flight qualified electronics. The chip was delivered to GSFC in October 1992, tested in NASA systems, and approved for flight use. The chip is being fabricated and qualified for use in XTE, TRMM and HST.
- **Lag Correlator** This chip contains over a million transistors, realizing a 1024 lags, is scheduled for astro physics use at the radio telescopes at Arecibo and Greenbank. This project was funded by the SERC program, NRL, NIAC and NRAO. The chip is in fabrication.
- **Lossless Data Compression** The flight qualified lossless data compression processor is being designed and is in the critical path for Landsat 7. The chip is scheduled for release to fabrication in August 1993.

Processors in research and development include:

1. Flight Reed Solomon CCSDS Decoder
2. Lossy Data Compression
3. High Performance Flight Viterbi Decoder
4. Flight A/D Converter
5. High Performance Auto Correlator
6. Flight hardware using Navy's SOS foundry
7. CCSDS Packetizer

1.4 Commercial Technology Transfer

The working relationship with NASA toward developing new technology is described next.

- **Chip Development** NASA scientists and engineers develop the fundamental algorithms and identify the system needs. The SERC and the NASA center jointly develop the chip specification. The SERC designs and has the chip fabricated and tested; testing normally takes place at the SERC facilities. NASA integrates the tested prototype into a system and tests the complete system.
- **Flight Parts** After the chip has been tested and proven to meet system requirements, flight parts need to be obtained. There are several ways.
 1. **Commercial Companies** - Must develop internal expertise, which often times they do not wish to do for market reasons.
 2. **GFE to Contractors** - This sometimes presents a problem for the government to furnish equipment to contractors.
 3. **Separate Company** - An option that was exercised in New Mexico.
- **New Company Solution** The University of New Mexico started a new company with the following goals:
 - Establish Company to Support SERC Technology
 - Contract Fabrication/Testing/Qualification to Government Certified Sources
 - Provide long term technical support for SERC developed technology.
- **New Mexico Company - Integrated Circuit Solutions** This company has been formed in Albuquerque. It is currently supplying 2 chips to GSFC.

1.5 Technical Support

The SERC has provided technical support to NASA GSFC on two projects.

1. **VLSI ASIC Design Review** Dr. Kelly Cameron attended 3 design reviews in California to identify problems with the Mickelson Doppler Interferometer instrument. Dr. Cameron accompanied Steve Pszcolka, David Langjahr and James Shannon of GSFC as a VLSI expert. He helped identify problems in the design of the ASIC chip.
2. **Analog to Digital Converter** Sipex is building an analog to digital converter which is an integral part of the of the Fine Pointing Sun Sensor in the International Solar-Terrestrial Physics Project. Sipex supplies the ADC to Adcole, who builds the Fine Pointing Sun Sensor for NASA, who is sharing the technology with ESA. The Sun Sensor ADC is a Sipex standard product with a special linearity specification and a slightly lower conversion rate. The ADC is a hybrid module consisting of a

rad hard gate array, a Harris 12-bit Digital to Analog Converter (DAC), an 8-bit DAC, an opamp, a counter, and various discrete components. The DAC's are used together with a comparator and a successive approximation register in the gate array to form a successive approximation ADC. The 12-bit Harris DAC is laser trimmed by Sipex so that the ADC meets the 16-bit linearity specifications.

The problem is that the linearity of the ADC no longer meets the specification after the part is burned in. The most likely place for the problem is in the Harris 12-bit DAC, since DAC linearity in a successive approximation ADC directly affects ADC linearity. A residual gas analysis found the moisture content inside some of the hybrid ADC's to be above specification by almost a factor of two, but this is still very dry, and probably not the problem.

The purpose of the meeting was to determine what should be done next to solve the shifting linearity problem. Suggested were made by Don Thelen of the SERC staff. The end result is unknown.

1.6 Student Involvement

Education is a key element in the SERC activities. Student involvement remains high and includes the following:

- Three Ph.D students graduated in Electrical Engineering in the last year. Nine Master of Science students graduated in Electrical Engineering and Computer Engineering in the last year. These are listed in Section 6.1.
- Thirty seven undergraduate students are currently involved in the NASA program. The NASA Scholars are listed in Section 6.3.
- Nine Master of Science students are currently pursuing advanced degrees and research in Electrical and Computer Engineering. These graduate students are listed in Section 6.2.
- Five Ph.D students are currently pursuing advanced degrees in Electrical Engineering. These graduate students are listed in Section 6.2.
- Sixteen new high school teachers were exposed to digital logic design SERC NASA program this year.
- Ten high school teachers designed their own VLSI chip with the chips being fabricated at NSF's MOSIS foundry this year.

1.7 Outside Support

\$2,509,597 in non-SERC contracts are in force this year to support the SERC activities. These are itemized in Section 5.

1.8 Research Results

Research summaries and proposed research activities are described in Section 7 and Section 8. The major result is summarized here.

- **Low Cost High Performance Flight Electronics** A new breakthrough has been achieved in producing flight electronics with commercial foundries. For years it has been believed that flight electronics could only be produced with specialized foundries. It has been demonstrated that now flight electronics can be realized with commercial foundries.

Significance

- Produce flight electronics with commercial non-radiation hard foundries
 - Reduce Cost of flight electronics by one or two orders of magnitude.
 - Design with latest IC technologies to produce faster more dense ICs
 - No government investment needed to develop new IC processes (follow and use commercial foundries)
- **Test Results** Test cells were designed and processed using the Hewlett Packard 1.0 micron CMOS commercial process. The cells were tested at Brookhaven National Laboratory for single event upset (SEU) and single event latchup (SEL). NASA accepts an LET = 40 as sufficient for flight electronics. The test cells demonstrated an LET greater than 120 and in fact did not upset or latchup under any conditions.

Following is an example illustrating the difference today in producing flight electronics using special foundries and commercial foundries. The SERC was asked to provide a high performance EDAC for future NASA solid state recorders. A total of 55 chips were required to be delivered. The comparison is shown next with a savings of approximately \$500,000.

Item	Current Solution	New Solution
Engineering	\$122,000	\$104,400
Fabrication	556,750	190,000
Total	\$893,500	\$400,000

1.9 Space Experiment

Microelectronic and Photonic Test Bed A new test bed is being proposed to continue experimentation initiated in the CRRES program. The sponsors for the new space test bed are:

1. Defense Nuclear Agency
2. Naval Research Laboratory
3. USAF Phillips Laboratory

The test bed program consists of:

- Joint Space "Piggy back" Experiment
- Assess Device Performance in Space Radiation Environment
- Modeled after 1990-91 CRRES Space Experiment
- Launch in 1996

The NASA SERC has been asked to provide special purpose processors to be used in this test bed.

1.10 Outreach Program

The one week digital logic program was repeated this year with 16 new teachers. The teachers left with great enthusiasm. This program will be continued in Albuquerque.

The four week VLSI design project was conducted again this year. Five chips were designed by the teachers. The teachers had to master the following skills - logic specification, logic design with VLSI standard cells, logic simulation, layout, design rule check and verification. This experience had a remarkable effect on the teachers. A great deal of publicity should result since each teacher will present his experiences at regional meetings. It is likely that these are the only high school teachers in the country to design a VLSI chip. Moreover, they may now have more VLSI skills than many graduates from EE programs. They left feeling very proud and highly motivated. Details can be found in Section 10.

A third phase is completed. The teachers feel that the introduction of digital electronics to public schools can have a major impact, not only on the high achievers, but on the broad spectrum of students. Vocational education can greatly benefit from knowing this technology. The teachers feel that the information gained at this workshop can affect the entire country. Therefore, they would like to try to design a curriculum, write a proposal for funding and investigate delivery mechanisms. A proposal was written to US Army Research Office for funding next year. The goal is to transfer digital electronics and CAD systems into the high school programs. Text book material needs to be created.

2 VLSI Project Status

2.1 Chip Summary

Chip Project	Status	Expected Date	Application
Flight CCSDS Encoder	Delivered	Sept 1992	XTE TRMM ACE
Bus Controller	Delivered	Oct 1992	XTE TRMM HST
Hewlett Packard ECC	Delivered	Nov 1992	Disc Drives
Flight Custom CCSDS Decoder	Initial Stage		EOS
1024 Lag Correlator	Design	Aug 1993	Arecibo, Greenbank
High Performance Correlator	Design	Jan 1994	MIT Haystack
Flight Lossless Data Comp	Design	Nov 1993	Landsat 7
Lossy Data Compression	Initial Stage		
Flight A/D	Test Cells In Fab		
CCSDS Packetizer	Design	January 1994	
Viterbi Decoder	Specification		
Hewlett Packard uP	Design	Dec 1993	Commercial

2.2 Project Description

- **Bus Controller** A bus controller for several missions, including XTE, TRMM and HST, was designed using a UTMIC space qualified gate array. This chip is part of the system that contains the new flight qualified Mongosse microprocessor realized by Harris and GSFC.
- **Flight CCSDS Encoder** A low speed flight Reed Solomon encoder was designed with a UTMIC space qualified gate array. It operates at 200 Mbits/second. The interleaving depth is programmable up to 8. This processor is being ordered for the XTE, TRMM and ACE flight projects. Fully tested and qualified flight parts should be delivered to GSFC July 1993.
- **Hewlett Packard ECC** High performance Error Correction Module designed in HP's 0.8 micron process that should be installed in future disc drive products. The layout of this design used an automatic tiling system to assemble the base cells.
- **High Performance Correlator** A 100 MHz 1024 channel time-lag correlator is being developed. The chip will contain SEU immune circuitry.
- **Flight Lossless Data Compression** An enhanced version of the military grade compression is being designed for flight use. The data rate is specified up to 200 Mbits/sec and it has enhanced features for data compression performance. It is being implemented to meet the specific needs of Landsat.

- **Lossy Data Compression** New algorithms and chip architectures are being investigated to produce a variable rate lossy data compression system.
- **Flight A/D Converter** The goal is to design a 18 bit 50 Khz sampling A/D converter which can be used in a low earth orbit. This processor is designed to be immune to SEU and SEL radiation impacts. The test cells have been sent for fabrication.
- **CCSDS Packetizer** The CCSDS packetizer will accept variable length, variable word width instrument data. Input data rates are specified to be 20 Mbits/second. The packetizer will output CCSDS packets and MPDU data formats.
- **High Performance Viterbi Decoder** An initial design has been completed on the realization of a constraint length 15 Viterbi decoder. The final system is estimated to have up to 128 chips, each chip having 4096 processors.
- **Hewlett Packard uP** A general purpose microprocessor that can be used in disc drives is being designed in accordance with specifications given by HP. This processor is exceedingly flexible and should yield a competitive commercial advantage to HP.

3 Published Papers

J. Sarker and J. Purviance, "Yield Sensitivity Study of AlGaAs/ GaAs High Electron Mobility Transistor," *International Journal of Microwave and Millimeter-Wave Computer Aided Engineering*, Vol. 2, No.1, January, 1992.

M. Beale and H. Demuth, "Training Functions in a Neural Network Design Tool", Proceedings of the Workshop on Neural Networks, Auburn University, Auburn, Alabama, Feb. 10-12, 1992.

M. Beale and H. Demuth, "Building a Neural Network", Scientific Computation and Automation, May, 1992, pp. 19-21.

H. Demuth and M. Beale, "Neural Network Users Guide", The Mathworks, Natick, Massachusetts, approx. 300 pp., June, 1992.

M. Meehan and J. Purviance, "Statistical Performance Sensitivity - A Valuable Measure for Manufacturing Oriented CAD," *1992 IEEE Microwave Theory and Techniques International Microwave Symposium*, June, 1992.

J. Sarker and J. Purviance, "Yield Sensitivity of HEMT Circuits to Process Parameter Variations, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 40, No. 7, July, 1992.

N. Liu and S. Whitaker, "Low Power SEU Immune CMOS Memory Circuits", *IEEE Conference on Nuclear and Space Radiation Effects*, New Orleans, LA, PA7, July 1992.

M. Beale and H. Demuth, "Preparing Controllers for Nonlinear Systems," *AI Expert*, July 1992, pp. 42-46.

K. Cameron, J. Canaris and S. Whitaker, "A Video Image Processor for Real-time Centroid Calculation", *Proceedings of the IEEE ASIC Conference and Exhibit*, Rochester, NY, pp. 201-204, Sept. 1992.

S. Whitaker and G. Maki, "Self Synchronized Asynchronous Sequential Pass Transistor Circuits", *IEEE Transactions on Computers*, vol. 41, no. 10, pp. 1344-1348, Oct. 1992.

G. Maki, "Special Purpose High Performance VLSI: Impacts on Mission Strategies", *Space Exploration Science and Technologies Research: ASME, AD-Vol. 31*, pp 43-48, November 1992.

N. Liu and S. Whitaker, "Low Power SEU Immune CMOS Memory Circuits", *IEEE Transactions on Nuclear Science*, vol. 39, no. 6, pp. 1679-1684, Dec. 1992.

J. Venbrux, Pen-Shu Yeh, and M. N. Liu, "A VLSI Chip Set for High Speed Lossless Data Compression", *IEEE Transactions on Circuits and Systems for Video Technology*, December 1992.

M. Liu, K. Liu, G. Maki and S. Whitaker, "Automated ILA Design for VLSI Synchronous State Machines", *IEEE 35th Midwest Symposium on Circuits and Systems*, Washington, DC, pp. 851-854, Dec. 1992.

G. Maki, J. Gibson, J. Gambles, J. Canaris, S. Whitaker and J. Venbrux, "NASA Secondary Teacher VLSI Program", *1992 Annual Conference Proceedings of the American Society for Engineering Education*.

M. Meehan and J. Purviance, "Yield and Reliability in Microwave Circuit and System Design," ARTECH, Inc., 1992.

D. Janson and J. Frenzel, "Application of Genetic Algorithms to the Training of Higher Order Neural Networks," *Journal of Systems Engineering*, Vol. 2, pp. 272-276, 1992

J. Young, "A time-domain weighted residual formulation of Maxwell's equations," 31st American Institute of Aeronautics and Astronautics (AIAA) Symposium, Reno, Nevada, January, 1993.

J. Canaris, "A VLSI Architecture for the Real Time Computation of Discrete Trigonometric Transforms", *The Journal of VLSI Signal Processing*, January 1993.

M. Shamanna and S. Whitaker, "A Carry Select Adder with Conflict Free Bypass Circuit", *Proceedings of the 6th International Conference on VLSI Design*, Bombay, India, pp. 363-366, Jan. 1993.

E. Ingermann and J. Frenzel, "Sensitivity Analysis of a Radiation Immune CMOS Logic Family under Defect Conditions," *Proceedings of the 11th IEEE VLSI Test Symposium*, pp. 355-357, April 1993.

D. Lamet and J. Frenzel, "Defect-Tolerant Cache Memory Design," *Proceedings of the 11th IEEE VLSI Test Symposium*, pp. 159-163, April 1993.

J. Gambles and P. Windley, "Reasoning About the Standard Logic Package Signal Data Type", *CHDL '99: The IFIP Conference on Hardware Description Languages and their Applications*, Ottawa, Canada, April, 1993.

D. Wiseman, J. Canaris, N. Liu, S. Whitaker, K. Liu, J. Venbrux, K. Cameron, K. Arave and L. Arave, "Design and Testing of SEU/SEL Immune Memory and Logic Circuits in a Commercial CMOS Process", accepted for publication at the IEEE NSREC. May 1993

G. Maki, S. Whitaker, J. Gambles, J. Canaris and J. Venbrux, "NASA High School Teacher VLSI Program", accepted for publication in the Proceedings of the *10th Bienial University/Government/Industry Microelectronics Symposium*. May 1993

P. Windley, "A Theory of Generic Interpreters," Proceedings of the 1993 Conference on Correct Hardware Design Methodologies (CHARME), Arles, France, 1993.

P. Windley, "Abstract Theories in HOL," Proceedings of the 1992 International Workshop on the Higher-Order Logic Theorem Proving and its Applications, L. J. M. Claesen and M. J. C. Gordon, editors, North-Holland, 1993.

J. Frenzel and P. Windley, "Microprocessor Applications," *The Electrical Engineering Handbook*, Chapter 76.2, CRC Press. (*in publication*)

J. Frenzel, "Supply Current Diagnosis of VLSI Circuits," *IEEE Transactions on Reliability*. (*accepted for publication*)

David J. Janson and James F. Frenzel, "Training Product Unit Neural Networks with Genetic Algorithms," *IEEE Expert Magazine*. (*accepted for publication*)

J. Young, "Characterizing radio wave interactions with ionized fluids using a weighted residual, time-domain method." A conference abstract has been accepted for presentation at the Progress in Electromagnetic Research Symposium.

4 NASA Symposium on VLSI Design 1992

- Waleed K Al-Assadi, Y. Malaiya and A. Jayasumana, "Detection of Feed-Through Faults in CMOS Storage Elements," Fourth NASA VLSI Design Symposium, 1992.
- Kari Arave, John Canaris, Lowell Miles and Sterling Whitaker, "Schematic Driven Layout of Reed Solomon Encoders," Fourth NASA VLSI Design Symposium, 1992.
- Grant Beagles, Kel Winters and A.G. Eldin, "Bit-Systolic Arithmetic Arrays Using Dynamic Differential Gallium Arsenide Circuits," Fourth NASA VLSI Design Symposium, 1992.
- V. Bobin, S. Whitaker, and G. Maki, "Links between N-Modular Redundancy and the Theory of Error-Correcting Codes," Fourth NASA VLSI Design Symposium, 1992.
- Lowell Campbell and John Purviance, "Interpolative Modeling of GaAs FET S-parameter Data Bases for Use in Monte Carlo Simulation," Fourth NASA VLSI Design Symposium, 1992.
- John Canaris, "NASA SERC Digital Correlator Projects," Fourth NASA VLSI Design Symposium, 1992.
- Kumar Chandra and William J. Wilson, "Low Power, CMOS Digital Autocorrelator Spectrometer for Spacebourne Applications," Fourth NASA VLSI Design Symposium, 1992.
- A.G. Eldin, "A DRAM Compiler Algorithm for High Performance VLSI Embedded Memories," Fourth NASA VLSI Design Symposium, 1992.
- Arai Eshraghi, Terri Fiez, Kel Winters and Thomas Fischer, "Design of a New Squaring Function for the Viterbi Algorithm," Fourth NASA VLSI Design Symposium, 1992.
- Joseph J. Feeley and Daniel Ahlstrom, "A New Eddy Current Model for Magnetic Bearing Control System Design," Fourth NASA VLSI Design Symposium, 1992.
- Jody W. Gambles and Phillip J. Windley, "HDL to Verification Logic Translator," Fourth NASA VLSI Design Symposium, 1992.
- J.A. Gunawardena, "A Novel Cache Mechanism," Fourth NASA VLSI Design Symposium, 1992.
- David K. Probst and Hon F. Li, "A Simple Modern Correctness Condition for
- Jon Hagen, "Applications of Correlator Chips in Radio Science," Fourth NASA VLSI Design Symposium, 1992.

- K. Hebbalalu, S. Whitaker and K. Cameron, "On the Decomposition of Synchronous State Machines Using Sequence Invariant State Machines" Fourth NASA VLSI Design Symposium, 1992.
- Erik H. Ingermann and James F. Frenzel, "Defect-Sensitivity Analysis of an SEU Immune CMOS Logic Family," Fourth NASA VLSI Design Symposium, 1992.
- Byung Wook Jeon and Chidchanok Lursinsap, "A Statistical-based Scheduling Algorithm in Automated Data Path Synthesis," Fourth NASA VLSI Design Symposium, 1992.
- Byung Wook Jeon and Chidchanok Lursinsap, "Micro-rollback and Self-recovery Synthesis," Fourth NASA VLSI Design Symposium, 1992.
- S. Kamath, Doug Lynn and Sterling Whitaker, "A VLSI Implementation of DCT Using Pass Transistor Technology," Fourth NASA VLSI Design Symposium, 1992.
- James D. Kinnison, "Single Event Phenomena: Testing and Prediction," Fourth NASA VLSI Design Symposium, 1992.
- Dan Lamet and James F. Frenzel, "A Set-Associative, Fault-Tolerant Cache Design," Fourth NASA VLSI Design Symposium, 1992.
- John Lenell, Steve Wallace and Nader Bagherzadeh, "A 20MHz CMOS Reorder Buffer for a Superscalar Microprocessor," Fourth NASA VLSI Design Symposium, 1992.
- Xueqin Li and H.D. Cheng, "A Novel Visual Hardware Behavioral Language," Fourth NASA VLSI Design Symposium, 1992.
- Priscilla L. McKerracher, Russel P. Cain, Jon C. Barnett, William S. Green and James D. Kinnison, "Design and Test of Field Programmable Gate Arrays in Space Applications," Fourth NASA VLSI Design Symposium, 1992.
- T.R. McKnight, D.E. Rodriguez, J.C. Barnett, and C.R. Valverde, "System Development Using VLSI for Space Applications," Fourth NASA VLSI Design Symposium, 1992.
- Sankaran M. Menon, Yashwant K. Malaiya and Anura P. Jayasumana, "Behavior of Faulty Double BJT BiCMOS Logic Gates," Fourth NASA VLSI Design Symposium, 1992.
- Gulam Mohamed, Tan Han Ngee and Chng Chew Lye, "A Heuristic-Based Scheduling Algorithm for High Level Synthesis," Fourth NASA VLSI Design Symposium, 1992.

- Bruce Offord, "Fully Depleted Silicon-on-Sapphire and Its Application to Advanced VLSI Design," Fourth NASA VLSI Design Symposium, 1992.
- Ramesh Panwar and Leon Alkalaj, "Low Energy CMOS for Space Applications," Fourth NASA VLSI Design Symposium, 1992.
- A. Benjamin Premkumar and T. Srikanthan, "A Real Time Correlator Using Distributed Arithmetic Principles," Fourth NASA VLSI Design Symposium, 1992.
- David K. Probst and Hon F. Li, "A Simple Modern Correctness Condition for a Space-Based High-Performance Microprocessor," Fourth NASA VLSI Design Symposium, 1992.
- Jogendra Sarker and John Purviance, "Dimension Scaling Effects on the Yield Sensitivity of HEMT Digital Circuits," Fourth NASA VLSI Design Symposium, 1992.
- E. Thomas Schubert, "A Mechanized Process Algebra for Verification of Device Synchronization Process," Fourth NASA VLSI Design Symposium, 1992.
- Manju Shamanna and Sterling Whitaker, "On Fast Carry Select Adders," Fourth NASA VLSI Design Symposium, 1992.
- Donald C. Thelen, "An 18 Bit 50 kHz ADC for Low Earth Orbit," Fourth NASA VLSI Design Symposium, 1992.
- C. Timoc, T. Tran and J. Wongso, "A 1 GHZ Sample Rate, 256-Channel, 1-Bit Quantization, CMOS, Digital Correlator Chip," Fourth NASA VLSI Design Symposium, 1992.
- M. Kemal Unaltuna and Vijay Pitchumani, "A Mean Field Neural Network for Hierarchical Module Placement," Fourth NASA VLSI Design Symposium, 1992.
- Paul Vincent and Jea Park, "Analog/Digital pH Meter System I.C.," Fourth NASA VLSI Design Symposium, 1992.
- Larry Volkening, "Teaching VLSI in High School," Fourth NASA VLSI Design Symposium, 1992.
- Abdul Wahab, S.S. Erdogan and A.B. Premkumar, "Evaluation of Floating Point Sum or Difference of Products in Carry Save Domain," Fourth NASA VLSI Design Symposium, 1992.
- K.C. Wang and D.T. Cheung, "Heterojunction Bipolar Transistor Technology for Data Acquisition and Communication," Fourth NASA VLSI Design Symposium, 1992.

- Phillip J. Windley, "Instruction Set Commutativity," Fourth NASA VLSI Design Symposium, 1992.
- Don R. Wiseman and Sterling Whitaker, "A High Speed CMOS A/D Converter," Fourth NASA VLSI Design Symposium, 1992.
- Gregory C. Zweigle and Roberto Bamberger, "Reduction of Blocking Effects for the JPEG Baseline Image Compression Standard," Fourth NASA VLSI Design Symposium, 1992.

5 Contracts

Title	P.I.	Funding Agency	Amount
VLSI Bus ASIC	S. Whitaker	NASA GSFC	\$146,750
Space Qualified Reed Solomon Codex	S. Whitaker	NASA GSFC	300,000
RS1 and RS3 Encoder Macrocell	S. Whitaker	HP DMD	107,000
Radiation Hardened VLSI Electronics	S. Whitaker	NASA GSFC	212,500
RAD Testing of Lossless Data Comp	J. Venbrux	NASA GSFC	154,150
Flight Data Compression	J. Venbrux	NASA GSFC	130,000
Lossy Data Compression	K. Cameron	NASA GSFC	100,000
High Performance Correlator	J. Canaris	MIT	215,227
High Performance Correlator	J. Canaris	NRL	30,000
High Performance Correlator	J. Canaris	NAIC	30,000
High Performance Correlator	J. Canaris	NRAO	30,000
Correlator Chip Testing	J. Canaris	Aerojet	2,062
EDAC Microprocessor	K. Cameron	HP DMD	300,000
Hardware Verification	P. Windley	Boeing	14,938
Hardware Verification	P. Windley	NSF	34,818
Hardware Verification	P. Windley	NSA	41,150
Test Pattern Generation	J. Frenzel	UoI Research Grant	6,000
SEU-Immune State Machines	J. Frenzel	Idaho Space Grant	5,000
Research Center Support	J. Feeley	State of Idaho	100,000
Research Center Support	G. Maki	UNM	550,000
Total			\$2,509,597

6 Students

6.1 Graduated Graduate Students

Student	Degree	Year	Thesis Title
Vijay Bobin	PhD EE	1992	Application of the Theory of Linear Codes to Modular Redundancy.
Kristen Chen	MS CE	1992	Pulse Mode VLSI Asynchronous Sequential Circuits.
Lowell Campbell	PhD EE	1992	Interpolative Modeling for MonteCarlo Simulation of GaAs FETs.
Jody Gambles	MS CE	1992	Incorporating Formal Verification into VLSI Design Methodology.
Ganesh Gursuswamy	MS EE	1992	A Modified Reconfigurable Data Path Processor.
Kumar Hebbalalu	MS EE	1992	The Decomposition of Synchronous Sequential Machines in VLSI Controllers.
Seetaram Kamath	MS EE	1992	A VLSI Implementation of Discrete Cosine Transform (DCT) Using Pass Transistor Logic.
Jiasui Li (Gary Lee)	PhD EE	1992	Parallel Algorithms and Processors for Optimization and Optimal Control.
George Niederaer	MS EE	1992	An Efficient Fuzzy Control Algorithm.
John Pendleton	MS EE	1992	SEU Immune Data Compressor.
Don Wiseman	MS EE	1992	High Speed CMOS A/D Converter.
Fang Zhuo	MS CS	1992	A Comparison of Software Maintainability Indices.

6.2 Current Graduate Students

Student	Degree	Year	Thesis Title
Mark Beale	MS CE	IP	
Michael Coe	MS CS	IP	
John Canaris	PhD EE	IP	Single Event Upset Immune Circuit Design Techniques for CMOS VLSI Memory and Logic Circuits.
Mike Dallabetta	MS EE	IP	
Jon Gibson	PhD EE	IP	Delay Analysis of Combinations of Pass Transistors and Classical Logic Gates.
Nabeel Ijaz	MS EE	IP	
Erik Ingermann	MS EE	IP	
Kraig Kaiser	MS EE	IP	
Navid Madani	MS CE	IP	Behavioral Model Simulation Encoder.

Noman Rangwala	MS EE	IP	
Manjunath Shamanna	PhD EE	IP	VLSI Hardware Acceleration.
Don Thelen	PhD EE	IP	Integrated CMOS Analog Design Tech- niques for Space Applications.
Feng Yu	MS EE	IP	Testing of ILA VLSI Circuits
Greg Zweigle	PhD EE	IP	Lossy Data Compression

6.3 Undergraduate Students

NASA Scholars supported by SERC:

Clinton Alter	B.S.	Computer Science
Amy Anderson	B.S.	Computer Science
Matthew Baca	B.S.	Electrical Engineering
Eric Cameron	B.S.	Computer Engineering
Brandon Carlson	B.S.	Electrical Engineering
Kenneth Chapman	B.S.	Electrical Engineering
Dee Lee Chou	B.S.	Electrical Engineering
James Clough	B.S.	Computer Science
Brenda Daniel	B.S.	Chemical Engineering
Michael Fisch	B.S.	Electrical Engineering
Brad Fitzgerald	B.S.	Electrical Engineering
Cade Greenup	B.S.	Computer Engineering
Chad Hale	B.S.	Electrical Engineering
Brian Haler	B.S.	Computer Science
Eric Hewitt	B.S.	Electrical Engineering
Sheryl Hoene	B.S.	Computer Science
Kirk Kludt	B.S.	Electrical Engineering
Vernon Koehler	B.S.	Computer Science
Matt Langenbahn	B.S.	Electrical Engineering
Walter McNall	B.S.	Electrical Engineering
Shad Miller	B.S.	Architecture
James Morasch	B.S.	Computer Engineering
Savanah Partridge	B.S.	Electrical Engineering
Teresa Ratts	B.S.	Computer Engineering
Emily Rehwinkel	B.S.	Civil Engineering
Jason Rubero	B.S.	Electrical Engineering

NASA Scholars supported by SERC:

Aimee Schmidt	B.S. Computer Science
Robert Schoeffing	B.S. Computer Engineering
Brett Shelton	B.S. Computer Engineering
Nathan Shiflet	B.S. Electrical Engineering
Eben Sutton	B.S. Computer Engineering
Tammy Teuscher	B.S. Electrical Engineering
Dan Tintzman	B.S. Electrical Engineering
Chad Vandemeer	B.S. Computer Engineering
Shannon Wade	B.S. Computer Science
Wendy Wahl	B.S. Electrical Engineering
Lance Wasem	B.S. Electrical Engineering

6.4 Minority Outreach

The University of New Mexico is identified as a Minority Institution defined by the requirements of the Higher Education Act of 1965 (20 U.S.C 1058) and FAR 252.226-7001.

The Idaho Science Camp is organized in the college of engineering to attract minorities into science and engineering professions. The Science Camp consists of mostly junior high school Native Americans who come to campus during the summer for a one week program.

The SERC is pursuing a longer term program through building an infrastructure among the high school science teachers. Over forty teachers are already part of this structure who are active in helping to recruit good science students. The teachers have been on campus and understand the NASA SERC program and activities.

7 University of New Mexico Research Report and Proposed Research

7.1 Test Results for SEU and SEL Immune CMOS Memory Circuits

Don Wiseman, John A. Canaris, Sterling R. Whitaker,
Jack Venbrux, Kelly Cameron, Kari Arave, and Larry Arave

Abstract - Test results for three recently proposed SEU logic/circuit hardened CMOS memory circuits verify upset and latch-up immunity for two configurations to be in excess of $120 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ using a commercial, non-radiation hardened CMOS process.

Summary

It is well known that special radiation resistant integrated circuit (IC) processes exist that are designed to provide protection against single event latch-up (SEL) and single event upset (SEU) phenomena. An experiment is reported in this paper which demonstrates that it is possible to provide a high degree of SEL and SEU immunity using a commercial, non-radiation hardened, CMOS process.

A test IC was designed consisting of five shift registers. Three of the shift registers utilized memory cells designed to be tolerant of SEU's through three different logic/circuit design hardening techniques [2,3,4]. The other two were normal shift register designs to be used for comparisons. All of the structures were built using latch-up hardening techniques. The IC was hardened against single event induced latch-up through guard barring, layout techniques, and the use of a starting material with an epitaxial layer. The test samples were processed through MOSIS in Hewlett Packard's commercial $1\mu\text{m}$ double metal CMOS (CMOS34) process at the Corvallis, Oregon facility.

Tests to determine the SEU susceptibility of the specially designed memory cells were conducted at Brookhaven National Laboratories (BNL) on January 13, 1993. The objective was to determine the threshold linear energy transfers (LETs) and cross-sections for SEU and latch-up due to heavy ions. The Single Event Upset Test Facility (SEUTF) utilizes a Tandem Van De Graaff accelerator for providing various ions and energies. The ion beam is directed at a test board mounted inside a vacuum chamber. The facility provides a computer-driven monitor and control program for the ion beam and test board setup.

Four of the test chips were placed on a wire-wrapped board, along with additional control logic, and mounted into the radiation test chamber at BNL. Three of the chips, with their die exposed, were placed in a heavy ion beam and individually irradiated. The outputs of the part being irradiated were compared in real time with the outputs of the fourth chip; the fourth chip acted as a control unit. Counters were placed at the output of the board to record differences between the outputs of the chip being irradiated, and

the outputs of the control chip. In this manner, upsets due to the heavy ion beam could be observed and quantified. The data sent through the shift register was comprised of an equal number of 1's and 0's. However, at any given time, different data patterns were sent through each register, to illuminate possible data dependent effects.

The current drawn by the chips was continuously monitored during the tests. Also, a current limit was placed on the voltage source such that if latch-up occurred in any of the parts, the power would be removed from the entire test board. The test board and chips were running at 1 MHz with a 5 volt supply. The board drew a total of 10 mA of current while operating under these conditions. The test board also included circuitry that would emulate upsets. By using this circuitry, the counters could be calibrated, and the functionality of the entire test set-up could be verified.

Experiments were conducted using Cl-35 at 206 MeV, Ni-58 at 265 MeV, I-270 at 320 MeV, and Au-197 at 350 MeV ions, beamed at various angles. The LET was steadily increased from 20 to 120 over the course of the experiment. The ion used for the beam was changed whenever the depth of the beam for the desired LET would be less than 20 μm . The non-hardened designs exhibited upsets under every condition. One of the hardened designs [3] exhibited an SEU threshold of $\text{LET}=35$ while the threshold of the other two designs [2,4] exceeded 120 $\text{MeV} \cdot \text{cm}^2/\text{mg}$. No latch-up was observed in any of the 10 parts subjected to radiation, demonstrating an SEL threshold in excess of 120 $\text{MeV} \cdot \text{cm}^2/\text{mg}$. A previous run of the same test chip without guard barring and SEL hardening layout techniques showed an SEL threshold of approximately 31 $\text{MeV} \cdot \text{cm}^2/\text{mg}$. Table 1 summarizes the experimental data for one of the test chips. Sec. 1 is the hardened design based on [4], Sec. 2 and 3 are the non-hardened designs. Sec. 4 was based on [3] while Sec. 5 was based on [2].

This paper would review the memory cell designs, describe the measurement techniques and report the results of the SEU testing. This would be the first report of actual test results for the new design techniques and demonstrates the possibility of designing circuits for space applications using high density, high performance commercial processes. Additional test ICs are currently in various stages of design and fabrication, including an adjustment of device sizes in the shift register based on [3] which should improve the present $\text{LET}=35$ threshold. These results should also be available by the conference and any additional information will be included in the poster presentation. As long as follow on test chip experiments confirm this data, this is a major break through.

The implications of the data taken in this experiment should not be underestimated. The data implies that standard, high density, commercial CMOS processes can achieve SEU and SEL protection equal to or better than expensive radiation hardened processes for space applications.

Ran	Ion	Energy MeV	Depth um	LBT ¹	Time sec	Flux #/cm2/sec	Fluence #/cm2	Upsets Sec. 1	Upsets Sec. 2	Upsets Sec. 3	Upsets Sec. 4	Upsets Sec. 5
1	Cl-35	206	35.8	20.0	132.3	8.853E+04	1.171E+07	0	21	40	0	0
2	Cl-35	206	35.8	20.0	134.5	8.786E+04	1.182E+07	0	25	51	0	0
3	Cl-35	206	35.8	20.0	118.6	9.932E+04	1.178E+07	0	21	40	0	0
4	Cl-35	206	31.8	22.5	120.6	8.300E+04	1.001E+07	0	28	50	0	0
5	Cl-35	206	31.8	22.5	112.7	8.893E+04	1.002E+07	0	21	42	1	0
6	Cl-35	206	31.8	22.5	131.6	7.614E+04	1.002E+07	0	22	78	0	0
7	Cl-35	206	28.6	25.0	150.9	7.814E+04	1.179E+07	0	25	55	0	0
8	Cl-35	206	28.6	25.0	133.4	7.513E+04	1.002E+07	0	23	57	0	0
9	Cl-35	206	26.0	27.5	138.5	7.230E+04	1.001E+07	0	30	62	0	0
10	Cl-35	206	26.0	27.5	137.1	7.306E+04	1.002E+07	0	34	64	0	0
11	Cl-35	206	23.9	30.0	153.7	6.513E+04	1.001E+07	0	28	83	0	0
12	Cl-35	206	23.9	30.0	147.4	6.783E+04	1.001E+07	0	39	76	1	0
13	Cl-35	206	23.9	30.0	147.9	6.772E+04	1.002E+07	0	38	78	0	0
14	Cl-35	206	22.0	32.5	166.5	6.015E+04	1.001E+07	0	29	71	1	0
15	Cl-35	206	22.0	32.5	161.5	6.198E+04	1.001E+07	0	40	68	0	0
16	Cl-35	206	22.0	32.5	164.2	6.095E+04	1.001E+07	0	36	76	1	0
17	Cl-35	206	20.4	35.0	175.8	5.695E+04	1.001E+07	0	38	115	2	0
18	Cl-35	206	20.4	35.0	174.8	5.726E+04	1.001E+07	0	29	87	1	0
31	Ni-58	265	32.1	35.0	30.9	3.260E+05	1.007E+07	0	40	97	4	0
32	Ni-58	265	32.1	35.0	30.7	3.277E+05	1.006E+07	0	45	79	2	0
33	Ni-58	265	32.1	35.0	31.6	3.182E+05	1.006E+07	0	46	78	8	0
34	Ni-58	265	28.1	40.0	38.0	2.645E+05	1.005E+07	0	45	107	12	0
35	Ni-58	265	28.1	40.0	39.7	2.529E+05	1.004E+07	0	43	105	13	0
36	Ni-58	265	24.9	45.0	42.7	2.353E+05	1.005E+07	0	63	146	28	0
37	Ni-58	265	24.9	45.0	43.7	2.298E+05	1.003E+07	0	60	134	17	0
38	Ni-58	265	22.4	50.0	49.6	2.028E+05	1.004E+07	0	84	145	19	0
39	Ni-58	265	22.4	50.0	50.1	2.006E+05	1.005E+07	0	75	135	18	0
40	Ni-58	265	20.4	55.0	55.5	1.809E+05	1.004E+07	0	93	162	45	2
41	Ni-58	265	20.4	55.0	56.6	1.774E+05	1.004E+07	0	87	164	40	0
42	Ni-58	265	20.4	55.0	57.6	1.743E+05	1.004E+07	0	88	154	39	1
64	I-127	320	31.0	55.0	57.1	2.054E+05	1.173E+07	0	86	162	17	0
65	I-127	320	31.0	55.0	49.7	2.021E+05	1.004E+07	0	72	143	12	0
66	I-127	320	28.4	60.0	58.8	1.705E+05	1.003E+07	0	66	154	16	0
67	I-127	320	28.4	60.0	60.1	1.668E+05	1.002E+07	0	79	136	25	0
68	I-127	320	26.2	65.0	67.9	1.479E+05	1.003E+07	0	69	154	25	0
69	I-127	320	26.2	65.0	69.3	1.447E+05	1.003E+07	0	87	153	26	0
70	I-127	320	24.3	70.0	74.9	1.359E+05	1.003E+07	0	94	153	30	0
71	I-127	320	24.3	70.0	74.5	1.345E+05	1.002E+07	0	111	147	27	0
72	I-127	320	22.7	75.0	100.2	9.996E+04	1.002E+07	0	113	159	23	0
73	I-127	320	22.7	75.0	84.3	1.189E+05	1.002E+07	0	126	175	32	0
74	I-127	320	21.3	80.0	78.6	1.276E+05	1.003E+07	0	116	159	33	0
75	I-127	320	21.3	80.0	75.2	1.334E+05	1.003E+07	0	121	160	30	0
76	I-127	320	20.0	85.0	78.9	1.372E+05	1.004E+07	1	136	154	32	0
77	I-127	320	20.0	85.0	81.4	1.240E+05	1.009E+07	0	134	162	35	0
78	I-127	320	20.0	85.0	80.6	1.243E+05	1.002E+07	0	143	185	35	0
111	Ar-197	350	27.5	85.0	19.0	6.891E+05	1.309E+07	0	121	186	31	0
112	Ar-197	350	27.5	85.0	14.6	6.926E+05	1.011E+07	0	86	119	21	0
113	Ar-197	350	26.0	90.0	16.1	6.296E+05	1.014E+07	0	96	131	23	0
114	Ar-197	350	26.0	90.0	15.4	6.611E+05	1.018E+07	0	92	119	22	0
115	Ar-197	350	24.6	95.0	15.8	6.424E+05	1.015E+07	0	110	122	22	0
116	Ar-197	350	24.6	95.0	16.8	6.019E+05	1.011E+07	0	110	104	15	1
117	Ar-197	350	24.6	95.0	17.6	5.768E+05	1.015E+07	0	92	128	18	0
118	Ar-197	350	23.4	100.0	16.6	6.103E+05	1.013E+07	0	100	150	20	1
119	Ar-197	350	23.4	100.0	16.6	6.065E+05	1.012E+07	0	98	145	25	1
120	Ar-197	350	23.4	100.0	16.4	6.170E+05	1.012E+07	0	98	131	21	0
121	Ar-197	350	21.3	110.0	18.6	5.450E+05	1.014E+07	0	122	135	18	0
122	Ar-197	350	21.3	110.0	18.5	5.466E+05	1.011E+07	0	123	158	24	2
123	Ar-197	350	21.3	110.0	18.5	5.476E+05	1.013E+07	0	128	171	33	0
124	Ar-197	350	19.5	120.0	20.9	4.830E+05	1.009E+07	0	124	146	38	0
125	Ar-197	350	19.5	120.0	20.3	4.984E+05	1.012E+07	0	138	155	31	0

¹ MeV · cm²/mg

7.2 Proposed Radiation Hard Electronics

Task Objective and Deliverables

- Demonstrate that radiation hard CMOS can be produced in a non-radiation hard commercial foundry.
- Deliver commercially fabricated radiation hard CMOS gate array.

- Demonstrate new gate array technology is as radiation hard as gate arrays produced in special flight foundries.
- Deliver full custom radiation hard VLSI.

Technology Description

There are three radiation effects to consider:

1. Single event upset (SEU). SEU tolerance is achieved through electronic non-resistor feedback in the proposed designs. This technology was developed at the SERC during the past two years.
2. Single event latchup (SEL). SEL is achieved through specialized layout techniques, as demonstrated in recent tests.
3. Total dose. Total dose tolerance is achieved through IC fabrication. Many commercial foundries produce high total dose levels.

Initial developments have been made that show it is possible to produce radiation hard CMOS in a non-radiation hard foundry. Test cells have demonstrated an LET greater than 120. The proposed development will be to bring this technology to maturity.

User Needs and Benefits

The ability to produce radiation hard electronics with commercial foundries would yield:

1. One or two orders of magnitude reduction in flight electronics. The reason for this saving is that government electronics would represent only a small part of the product from a given line.
2. NASA can design with latest IC technologies to produce faster more dense ICs.
3. No government investment is needed to develop new IC processes. The commercial companies will bare this burden within their own programs.

Current Status

Initial test cells have been fabricated and tested at Brookhaven National Laboratories. The January 1993 test has shown that the "hard" cells are SEU and SEL immune for LET > 120.

State of Technology

The fundamental electronics is understood and has been demonstrated. The SEU technology was developed over the last two years and published in the NASA Symposium on VLSI Design. The SEL technology is a recent discovery and has been demonstrated at BNL in January 1993.

Technical Approach

- Refabricate and test 1.0 micron CMOS test cells.
- Redesign, fabricate and test 0.8 micron CMOS test cells.
- Repeat test with second commercial foundry.
- Design full custom chip. Likely candidates are a 1024 channel correlator or the RS16 decoder.
- Design gate array hardware.
- Design gate array software to interface with Mentor tools.
- Implement gate array designs to compare with UTMC/Honeywell designs. Likely candidates are the Reed Solomon encoder and the flight data compression chip.

Potential Commercial Benefits

The commercial benefits are primarily to NASA where low cost high performance VLSI can be obtained with commercial foundries.

Milestones

Level	No	Date	Planned Accomplishment
3	1	8/01/93	1.0 micron test cells
3	2	11/01/93	0.8 micron test cells
3	3	3/15/94	Gate Array Hardware
3	4	10/30/94	Radiation testing of gate array
4	5	3/15/95	Full custom design complete
6	6	6/15/95	CAD software complete
6	7	6/15/95	Gate array designs complete

7.3 Flight Lossless Data Compression

Jack Venbrux

Abstract

This work will complement the activity being conducted in current research. A new architecture is being formulated to implement a new lossless data compression algorithm. While simulations and theoretical deductions can verify the results of the new work, the final proof of concept will be the fabrication and radiation testing of a space qualifiable component. Electronic protection against errors due to single event upsets (SEUs) is critical to the performance of the lossless compression algorithm since a single bit error can invalidate a large amount of data.

The new investigation will examine the impact of space radiation impacts on the VLSI architecture that realizes a powerful lossless data compression algorithm. The VLSI architecture that is being designed under current research is proposed to be fabricated and tested. The results of the radiation testing will demonstrate the viability of the new architecture for space applications.

Lossless Data Compression

The major objective for designing and fabricating the chip set is to provide real time lossless compression for satellite imagery. In order to compress satellite imagery it must adapt rapidly to changing scene statistics and compress image data over a wide entropy range.

The Rice algorithm is a lossless compression method that is rapidly adaptive and efficient over a wide range of entropy conditions. The structure of the algorithm can best be understood through the following argument. Assume that a particular encoder has, for example, 11 different Huffman codes to choose from. Each Huffman code is designed for a particular entropy range. The first codebook might be designed for an expected codeword length of 2 bits, while the next one might be designed for an expected codeword length of 3 bits, and so on in integer increments of one bit. By applying each of the 11 codebooks to the same data block of size J , and then choosing the codebook that produced the best compression would allow the coder to cover a wide entropy range: approximately 1.5 bits through 12.5 bits. By deciding which coder was the winner on a block by block basis, the coder would be adaptive to changes in data entropy.

One of Robert F. Rice's accomplishments was develop a compression algorithm that requires *no codebooks* [15], yet provides equivalent performance to the multiple Huffman codebook approach just described. The equivalence is only true for sources that have a Laplacian distribution. Fortunately, for many types of sampled data, especially imagery, the output from DPCM can be well modeled as a Laplacian distribution. The Rice algorithm has been shown mathematically to provide equivalent performance to using multiple, parallel Huffman codes, this was supported by extensive simulations [16]. An intuitive feel for this equivalence can be obtained by understanding two major components of the algorithm: a comma code Rice calls the Fundamental Sequence (FS), and sample splitting.

For low entropy data, direct coding of the data, without sample splitting, would pro-

duce the fewest number of coded bits. Higher entropy data will be more efficiently coded by using sample splitting. This reaffirms the assumption that as entropy increases the randomness (or information content) in the k least-significant bits prohibits compression. Therefore, using successive split bits combined with FS coding is equivalent to using Huffman codebooks that are designed for successive integer steps in entropy. Due to the simple structure of the FS code, however, no actual codebook is necessary for each code option.

Encoder

The encoder has a fully pipelined architecture. After 64 clock cycles, data is available for output. It can continuously accept new data and process every sample in one clock cycle.

The chip architecture and the generic Rice architecture differ in three ways. First, on the chip, the DPCM and mapper functions were implemented in one hardware block. Second, the winner select section was broken up into two sections for the chip: the bit counts section and the winner select section. The bit counts section is the largest single block on the chip. It calculates the number of bits that will be required to code the input block (16 samples) for each of the 12 coding options. The winner select block selects which of the options will produce the smallest number of coded bits and also performs calculations needed for the coding sections. The final difference between the VLSI implementation and the generic architecture is sharing of hardware among 12 coding options: only 2 hardware blocks are necessary (FS and K/Default). Control is distributed throughout the chip, but is mainly found in the input control section and in the two coding blocks.

The data formatter concatenates the split bits with FS coded bits. It also prepends the 4 ID bits that specify which code option performed the coding. The output of the chip is a 16 bit parallel output with an asserted signal to flag the presence of data. The design reflects the requirements from NASA to output a contiguous block of compressed data that begins with a header word to specify the length of the block. An external packetizer should be used for concatenating the specified number of blocks to form a large data packet.

Proposed Research

The current encoder compression chip was not designed with the space environment in mind. Specifically, it is subject to negative impacts due to Single Event Upsets (SEU). It is proposed to perform the following:

- Analyze the current architecture to identify impacts of SEUs on the current architecture and identify the critical areas.
- Identify solutions to provide SEU tolerance. Potential solutions involve the following:
 - Selecting an IC foundry that is capable of producing flight qualified parts.
 - Design all logic in SEU tolerant electronics.

- Design architecture with redundancy and necessary control circuitry such that the total system is tolerant of SEUs.

Enhancements

Features that the new architecture will have are:

- **Low Entropy Improvements:** Include a zero-run and a low-entropy option to yield improved performance for low entropy data.
- **More Efficient Coding at Small Quantizations:** Provide an optional 3-bit ID to improve coding performance for data that is quantized to less than 9-bits per sample. (The present design uses a fixed 4-bit ID independent of quantization.)
- **Block Size Options:** Besides the present 16 samples per block, allow coding an 8 sample block. This should allow more efficient entropy coding and rate control for coding outputs from lossy algorithms such as the frequency bins of a Discrete Cosine Transform.
- **Study Impact of Decision Regions:** Using decision regions is a method of choosing the winning code option using approximations instead of having to use exact counts. The present design uses exact counts which results in maximum performance but at a cost of using more chip area than if decision regions were used. This portion of the study would help answer the question, "What is the performance penalty for using decision regions versus using exact counts?"

Proposal

The chief goal of this study will focus on the following elements:

1. Have the VLSI test structure which implements lossless data compression with SEU immune electronics fabricated.
2. Pursue functional and electrical testing over the space radiation range to carefully analyze any performance impacts. The new cells with SEU immunity must not have significant impact in performance.
3. Perform radiation testing to measure the effects of total dose immunity and SEU's.

The current status is:

- A lossless algorithm with enhanced features to cover a larger entropy range has been proposed and tested for a large variety of images.
- A VLSI architecture is being designed with flight electronics that possess SEU immunity and is latchup free.

USE vs USES

Following are the differences between the flight and commercial foundry data compression chips. Some of the larger feature changes include and increased entropy range and prediction modes. USES is able to perform 2 dimensional and multispectral data compression.

Metric	USE	USES
Foundry Type	Commercial	RAD Hard, Level S parts
Technology	1.0uM custom	1.2 uM Gate Array
Package Type	84 Pin PLCC	144 Pin flat-pack
Quantization	4-14	4-15 bits/sample
Entropy Coverage	1.5-12.5	0-14.5 bits/sample
Prediction Modes	near. neighbor+external	also 2D, Multi-spectral
MSamples/Sec	25 at MIL spec	est. 18 at MIL spec
Variable ID	no, fixed 4bit	3bit ID if 8bits or less
Input Data	positive only	positive or bipolar
Block Sizes	16	8, 10, 16 samples
Output Format	individual blks	concatenated packets
Entropy Coding	Set XP=0+ext. pred.	pin selectable
Packetizing Mode	NO	Yes. User selects packet size
Ref-to-Ref diff	NO	Can Compress references

7.4 N-Modular Redundancy using the Theory of Error Correcting Codes

V. Bobin, S. Whitaker and G. Maki

Using redundancy is basic to fault-tolerant computing. N-Modular Redundancy (NMR) is in some ways analogous to the use of a repetition code where an information symbol is replicated as parity symbols in a codeword. Linear Error-Correcting Codes (ECC) use linear combinations of information symbols as parity symbols to generate syndromes for error patterns. In this paper, ECC theory has been applied to derive redundant circuits which tolerate faults in both the modules and checkers. Circuits using comparators for diagnosis are derived with a non graph theoretic approach. Coding theoretic principles are applied directly to NMR, so that extensive diagnosis of the fault-tolerant system is achieved. Links between NMR and the theory of linear codes are also investigated.

In a repetition code, the information symbol is replicated as parity symbols for the purpose of error detection and correction. An NMR system with voting has a similar purpose, to tolerate failures in some modules. In an NMR system, voting can be replaced by Galois Field (GF) arithmetic operations to identify the good and failed modules, just as GF arithmetic operations are used to identify and correct the erroneous symbols in a received codeword, provided the number of errors or failed modules is within the correction

Failed Unit	Comp. Outputs			Corresponding Error Pattern						
	C_1	C_2	C_3	Information				Parity		
	p_1	p_2	p_3	i_1	i_2	i_3	i_4	p_1	p_2	p_3
M_1	1	1	0	1	0	0	0	0	0	0
M_2	1	0	1	0	1	0	0	0	0	0
M_3	1	1	1	0	0	1	0	0	0	0
M_4	0	1	1	0	0	0	1	0	0	0
C_1	1	0	0	0	0	0	0	1	0	0
C_2	0	1	0	0	0	0	0	0	1	0
C_3	0	0	1	0	0	0	0	0	0	1

Table 4: Relation to (7,4) Hamming Code

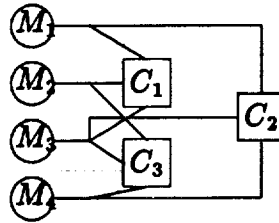


Figure 1: (7,4) Hamming Code Example

capability of the code. This paper attempts to adapt some results from coding theory for use in fault tolerance using modular redundant systems.

Consider a (7,4) binary Hamming code to illustrate these principles. The i 's represent information bits and the p 's represent parity bits. Note that a Hamming code has single error correction capability. We are trying to isolate a single faulty element. The parity bits are generated as follows.

$$p_1 = i_1 + i_2 + i_3$$

$$p_2 = i_1 + i_3 + i_4$$

$$p_3 = i_2 + i_3 + i_4$$

Notice that the parity bits are composed of an odd number of information bits. This is allowed since we are considering the fault-free modules to be represented by the additive identity of GF(2). Let the modules being checked be represented by the information bits. Let bus-bus comparators be connected at the outputs of the modules according to the way the parity bits are generated; ie., one three-way comparator compares the outputs of modules M_1, M_2 , & M_3 , a second comparator compares the outputs of M_1, M_3 , & M_4 , and a third comparator compares M_2, M_3 , & M_4 . The relations are summarized in Table 4 given. The system is shown in Figure 1.

The special feature of this implementation is that the comparators roughly correspond to the parity bits. Thus the comparators are also included as part of the code. The outputs of the comparators indicate which element is faulty. Notice that when a module is faulty, the outputs of the comparators indicate the syndrome of the fault pattern (or the error pattern in the equivalent code). For example, when the module M_1 is failed, the comparators output the vector $[1\ 1\ 0]$. This vector corresponds to the syndrome of the error pattern $[1\ 0\ 0\ 0\ 0\ 0\ 0]$ in a (7,4) Hamming code, where the first four positions represent the information bits which are the modules in the equivalent NMR system, and the last three represent the parity bits which are the comparators. Since 1 represents a failed element, module M_1 , corresponding to the first information bit is the failed element. As another example, consider the case where comparator C_1 is failed. Now the comparators output the vector $[1\ 0\ 0]$, which is the same as the syndrome of the error pattern $[0\ 0\ 0\ 0\ 1\ 0\ 0]$. This error pattern indicates that the first parity bit is in error, or in the equivalent NMR system, the first comparator is failed. Similarly, all possible single element failures are uniquely identified by this system.

In this research, we explored the links between the use of N-Modular Redundancy for hardware fault tolerance, and the use of linear Error-Correcting Codes. We showed how NMR is an application of a (N,1) repetition code, and also showed how special encoding structures can be designed to cover failures in the checker units themselves. We adapted some well-known results from coding theory for use in NMR for fault tolerance. The rich mathematical theory that finds application in error-protection techniques in digital data communication has faces that touch other subjects. The use of modular redundancy for hardware fault tolerance is one of them.

7.5 Flight High Speed Reed Solomon Encoder

Sterling Whitaker and Jody Gambles

General Description of Part

This project represents the first flight qualified IC designed by an SERC. This chip is a Rad-Hard gate-array implementation of a CCSDS Reed Solomon (RS) encoder. An RS code is a powerful cyclic symbol error correcting code. This code is useful in obtaining correct data through a burst error channel and thus has potential applications in communication systems and in digital systems where burst error conditions could exist. Under normal operation, the code is a (255,223) code. Due to the flexible nature of the algorithms being implemented, the circuit will support the encoding of shortened, as well as full length RS codes. Specifically, the codes which are supported are of the form: $(255 - i, 223 - i)$, where i can be any integer from 0 to 222.

The code is defined over the finite field $GF(2^8)$. The field defining primitive polynomial is $p(x) = x^8 + x^7 + x^2 + x^1 + x^0$ and the generator polynomial is given by:

$$G(x) = \prod_{i=112}^{143} (x - \beta^i)$$

where $\beta = \alpha^{11}$. The encoder represents data in the Dual Basis defined by the following transforms:

$$\begin{aligned} [z_0, z_1, \dots, z_7] &= [u_7, u_6, \dots, u_0] \\ [u_7, u_6, \dots, u_0] &= [z_0, z_1, \dots, z_7] \end{aligned}$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$\begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 \end{bmatrix}$$

where $[z_0, z_1, \dots, z_7]$ is the symbol represented by the dual basis and $[u_7, u_6, \dots, u_0]$ is the symbol represented by the normal basis.

The coder circuit has data input and output ports. Data is input at a constant rate, and output with a fixed latency. The latency of the encoder is one clock. Data is input in a byte serial fashion and with only one clock delay, is output byte serial. After the information bytes have been output, the next 32 output bytes are the RS check bytes. The output data rate for the chip is 200 Mbits/sec when clocked at a rate of 25 MHz.

The encoder can be programmed to interleave the data at depths of one, two, ... or eight. Interleaving of two or more encoded messages allows higher burst error correction capabilities. The interleaving depth, I , is controlled by external pins, S_0 , S_1 and S_2 .

Circuit Process Information

The encoder has been fabricated using the United Technologies Microelectronics Center (UTMC) UTE-R Radiation-Hardened double metal gate-array process. The UTE-R processes feature submicron effective channel lengths (0.9μ leff, 1.2μ drawn) in a twin-tub, P-well epitaxial bulk CMOS technology. The process is reported to be tolerant of total dose radiation levels exceeding 1 Mrad. In addition, the chip is designed to provide protection against Single Event Upsets (SEU) in two ways. First, the process and gate array cells

are reported to be hardened against errors to less than 1.0×10^{-10} errors/bit-day. Second, the control structure and data path are configured to completely reset after each message insuring that an SEU of the data registers will effect at most one encoded message.

The prototype parts were delivered on September 3, 1992. Heavy Ion Experiment testing was conducted at Brookhaven National Laboratories jointly by MRC and Goddard Space Flight Center personnel on December 3, 1992. The LET threshold was found to be approximately 38 with the 10% threshold approximately 58. The test report concludes that the RS parts are usable for all LEO missions. UTMIC is listed on QPL-38510 and the double metal process has been qualified for JAN class S production.

7.6 High Performance Lossy Data Compression System

Kelly Cameron and Jack Venbrux

Abstract

Lossy data compression is a critically important technology for NASA as instrument data rates become greater. There are several algorithms that have been produced that appear to help solve this problem, but there are no high performance processors that could be employed in NASA missions to operate on real time data. It is proposed to study high performance architectures along with a specific algorithm that will implement variable rate lossy data compression.

This work seeks to research and develop a lossy data compression system that has moderate high rate capabilities and can be used by scientists and engineers to experiment with data compression for high rate instruments. Such a system will allow one to identify the critical parameters needed for effective lossy data compression.

Introduction

Data compression can be categorized into two general areas: lossless and lossy. Lossless data compression can generally achieve a compression ratio less than a factor of 10, depending on the data characteristics [15,8,16,13]. A high performance encoder/decoder chip set has been implemented under NASA contract to implement lossless data compression [10] at data rates in the hundreds of Mbits/sec.

Significant benefits for data compression include:

- Reduce the number of ground communication stations that are needed as a backup to a potential failure in the Tracking Data Relay System (TDRS).
- Increase the amount of science that can be gathered, assuming that a large amount of insignificant data is compressed out and the useful science data remains.

- Increase the observation times since data compression will allow more observation before the storage tapes are filled. Moreover, access to the downlink channel is not as critical therefore increasing observation time.
- Decrease the demand on the downlink channel.

In many advanced instruments, sensor pointing control and the selection of viewing geometry can be greatly assisted by examining a snap shot of the high rate sensor data, sometimes referred to as "quick look" data. This usually requires real-time high rate compression of the sensor data for near real-time transmission to either onboard control or a ground station. There will also be instances when real-time video monitoring of scientific experiments dictate the use of data compression of a factor greater than achievable with lossless compression. In such situations, a high rate lossy data compression scheme is necessary to provide needed information through available communication channels.

Lossy data compression will lose information in the compression and decompression process. The question concerning how much data can be or should be lost is not an easy one to answer. Factors such as image information content, available transmission bandwidth, buffer size, and availability of the downlink channel play important roles in the answer to this question. Ideally one would like to have a variable rate high performance data compression system (chip set). This proposal seeks to discover such a system.

High Performance Data Compression

Adaptive compression techniques have been proposed for over twenty years[11,12]. One goal of researchers is to find a compromise between system complexity and performance[11]. Many compromises however ignore the advances that have been or can be made with VLSI. System complexity that requires a large amount of computational power can sometimes be easily achieved with VLSI. The lossless VLSI data compressor work accomplished under NASA contract is one such example [10].

The general system diagram of the proposed system is shown in Figure 2. A popular modern approach to lossy data compression involves the Discrete Cosine Transform (DCT). A DCT module is to be utilized in the system here. The DCT produces a two-dimensional array of transform coefficients. This technology is well known. However, commercial processors that meet the needs of NASA are not available, even ignoring space qualification issues.

With the basic system, the array of transform coefficients is quantized and coded using a zonal coding strategy. The lowest spatial frequencies generally possess the greatest energy. These are quantized most finely, while the highest spatial frequency coefficients are quantized more coarsely. The quantization levels are encoded in some general manner and output to a buffer. This transform method is reported to work well for natural scenes [12]. The Quantizer in Figure 2 in general performs this task. However, the proposed Quantizer will do more.

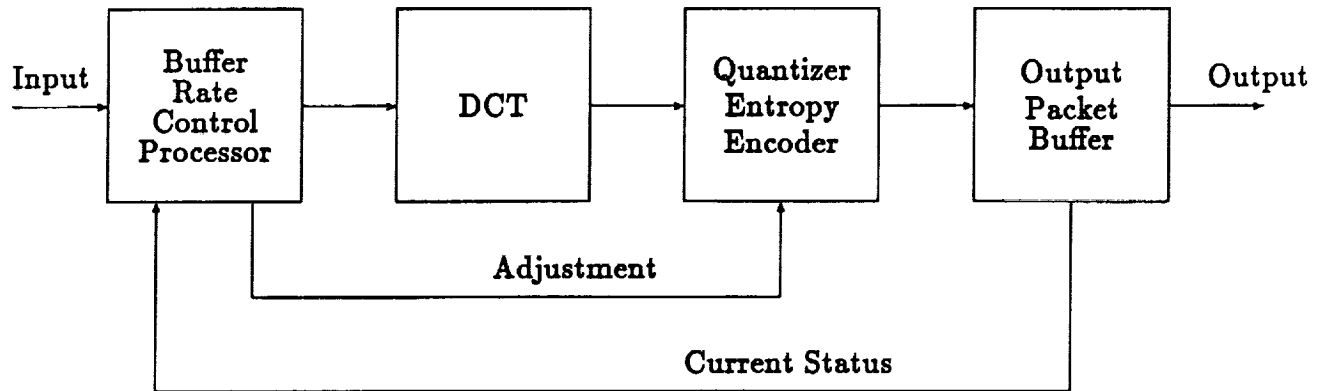


Figure 2: Block Diagram Lossy Compressor

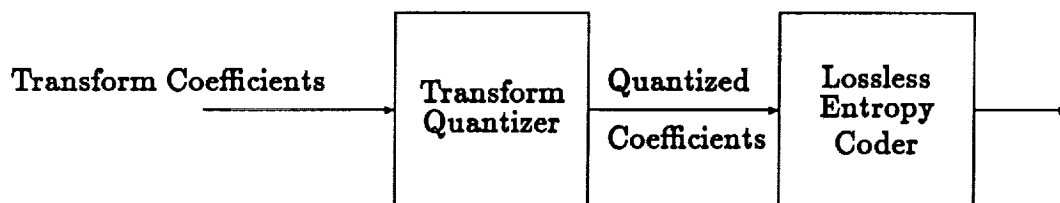


Figure 3: Quantizer Block Diagram

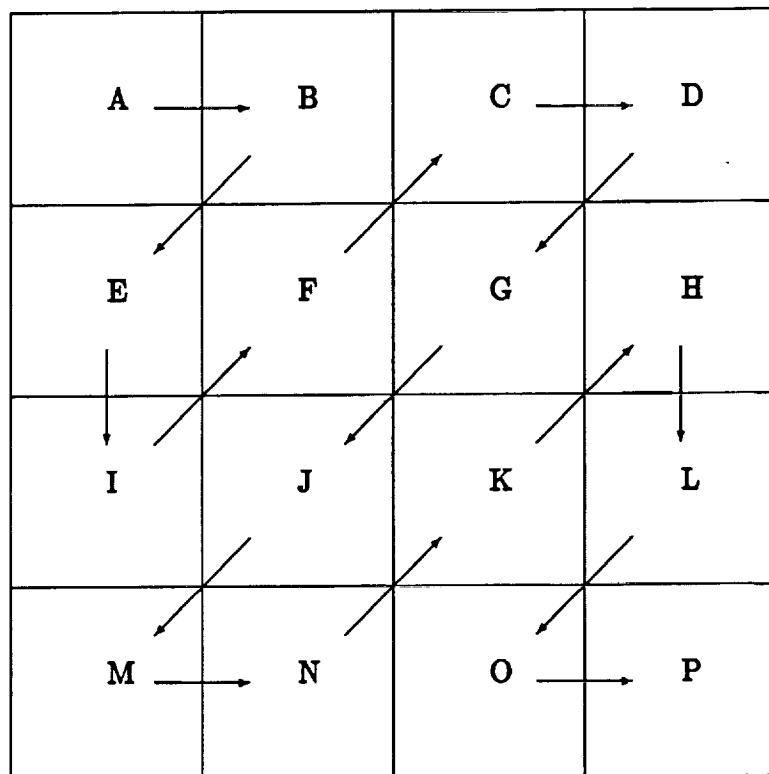


Figure 4: Energy Components from DCT

The proposed Quantizer will perform an additional task. The block diagram of the Quantizer is shown in Figure 3. The Transform Quantizer performs the task of selecting the frequencies with the most energy. Let the DCT produce an output of the cosine transform coefficients as depicted in Figure 4. The order which the data is produced is sequentially is depicted in Table 5. However, the desired order that the data ought to be scanned is also depicted in Table 5 and shown in Figure 4. The function of the Transform Quantizer is to scan the coefficients in the desired order and to select the n components with the greatest amount of energy. The number of components that are kept will be a variable in this structure. One possible architecture for implementing this function is a variable length sorter. Only the desired frequency components are retained and transmitted. All others are not transmitted and hence the information contained in these frequency components is lost.

The lossless entropy encoder has been designed and will be used in the system [10].

The feedback control portion of the system will determine the block statistics and

Sequence	DCT Out Sequence	Desired Scan Sequence
1	A	A
2	B	B
3	C	E
4	D	I
5	E	F
6	F	C
7	G	D
8	H	G
9	I	J
10	J	M
11	K	N
12	L	K
13	M	H
14	N	L
15	O	O
16	P	P

Table 5: Zigzag Data Sequencing

calculate the adjustment needed to control the Quantizer. Data will be received from the input images and the output packet buffer. The desired compression is then calculated. One parameter passed to the Quantizer is the number n that denotes the number of frequency components to be retained by the Transform Quantizer.

The overall system is depicted in Figure 5. The lossy data compression system is controlled by the user through a microprocessor. This allows one to identify the critical parameters in satellite imagery.

Proposed Research

The final goal is to investigate and design a high performance test system for lossy data compression that achieves the following:

- Identify critical lossy data compression parameters
- Demonstrate variable data rate compression
- Provide an experimental tool for various data compression strategies

The approach to achieving this goal is:

1. Study and propose architectural solutions for each individual module in the system as depicted in Figure 2.

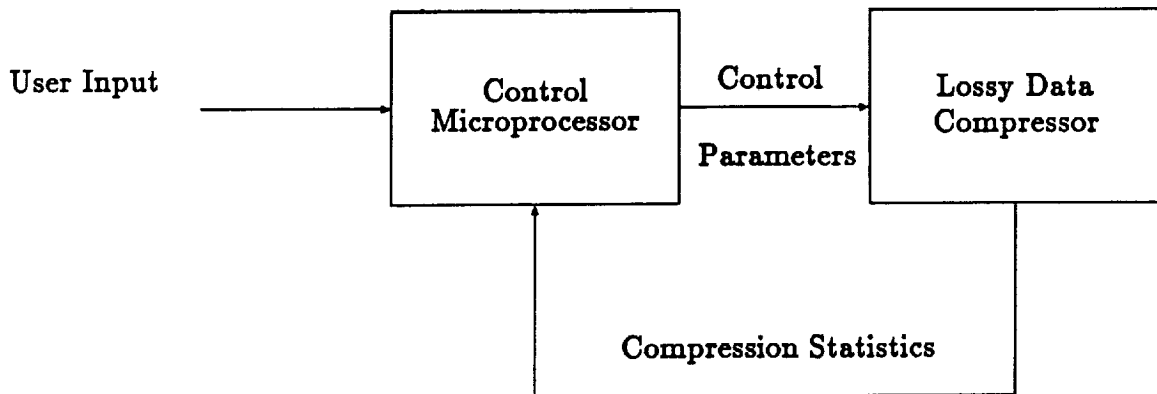


Figure 5: Overall System

2. Design and have fabricated proposed architectures for the final system. A close working relationship with NASA engineers is critical to the success of this effort since VLSI expertise (available at the University of Idaho) and data compression expertise (present at GSFC) need to jointly specify the final system.
3. Integrate the components together to provide the test system as depicted in Figure 5. The actual proof that a given solution is viable occurs when a test system is completed and demonstrated. This new area requires such a demonstration.

It is likely that only objective 1 and a start on objective 2 will be achieved in the first year of effort.

Digital Modules

High performance modules that are flexible to allow for experimentation will be studied.

- **DCT Features** that are needed in a real time satellite compression system include speed and accuracy. Commercial DCT modules are not fast enough, and they typically only accept 8-bit samples. A much faster architecture will be advanced that accepts up to 16-bit samples.
- **Transform Quantizer** This is a new architecture that is not currently available commercially. The new processor will need to identify and store the transform coefficients generated by the DCT in a manner that will allow variable rate compression. The Entropy Encoder has already been designed and is available.
- **Feedback Control** This module will be the most challenging component in the system for it contains the intelligence for determining the variable rate. Block statistics need to be calculated. An intelligent controller is needed to be incorporated to make decisions based on the statistics and current state of the output buffer.

After the study phase is complete and their feasibility demonstrated, and if it is deemed appropriate by NASA, the above components will be fabricated subject to available resources. The technologies that will be considered for implementation range from gate array ASICs to full custom VLSI. IC foundries can range from MOSIS to a fully space qualified line such as Honeywell. Foundry decisions will be made by NASA. Commercial components such as the DCT will be employed whenever possible and practical.

7.7 High Performance Correlator

John Canaris

Science Objective

A revolutionary architecture and design of a high performance digital correlator VLSI chip is proposed that will have applications in many science projects. Such a correlator would have applications in astrophysics, geodynamics, and atmospherics. Following are entities interested in this project to advance science:

Agency	Project	Contact
NAIC, NASA	Planetary Radar Decoder	Mike Davis
NSF	Radio Astronomy Spectrometer	Mike Davis
NASA GSFC	ESTAR	Jim Shannon
NRL, NASA	Orbiting HF Radio Interference Monitor	Kurt Weiler
JPL	Microwave LIMB Sounder for EOS/MLS	William Wilson
JPL	Submillimeter Intermediate Mission SMIM	William Wilson

Specific science objectives include:

- Determine improved ionospheric models for geolocation from space
- Characterize man-made/natural RFI in the near-earth environment
- Quantify ionospheric shielding against RFT
- Study solar and planetary bursts for astrophysics
- Plan for future radio imaging arrays in space
- Radio astronomy spectrometer
- Planetary radar decoder
- Precise pulsar timing analysis

Technical Objective

A High performance digital correlator will be designed to the following specifications:

- 1024 digital lags
- 100 Msamples/sec
- 32 bit accumulator stages
- 3 level input

The largest available digital correlator chip, suitable for these applications, contains 32 lags and operates at 25 Msamples/sec. The new correlator requires in excess of 785,000 gate equivalents. The largest known commercial gate array can realize 100,000 gate equivalents. Therefore, the proposed correlator will represent a major advance in digital correlator technology.

7.8 Flash Analog-to-Digital Converter

The purpose of this work was to design a high speed A/D converter for use at the NASA Space Engineering Research Center. The Center was in need of an A/D converter that could be used as a cell in high performance signal processing ASIC's for NASA. Therefore, the converter was specified to be high speed and be designed in a standard CMOS digital process. After reviewing the possible architectures for analog to digital conversion, it was decided that only a flash A/D converter offered the required performance.

The converter was designed using a novel comparator circuit. The comparator is a clocked, precharged circuit that offers very fast operation with a minimal offset voltage (2 mV). This comparator was shown to out perform more traditional comparators, and thus increases the speed of the converter.

Additionally, a novel "waffle" transistor architecture is used in the digital encoding ROM. This ROM could have been a speed limiting circuit had it not been for the use of this novel transistor along with precharged logic to encode the digital output.

The converter will function at 100 MHz under worst case conditions with typical parts functioning at 200 MHz. Hewlett Packard's CMOS-34 process was selected to use with this design. CMOS-34 is a 1 micron, double metal, single poly process and is considered a standard digital CMOS process.

The converter was designed with 7 bits of resolution and should have one half LSB accuracy. The converter was drawn to fit into a space of only 2,244 microns by 3,972 microns. It has separate power supplies for the analog and digital circuitry, and has a pipelined architecture to enable it to function at high speeds.

Currently, NRaD (Navy) is fabricating the converter in their CMOS-34 mask compatible SOS process. If successful, a radiation hard converter would be available.

7.9 BUS ASIC

The BUS ASIC was designed to control the flow of information throughout the SEDS/RPP (Small Explorer Data System/Recorder, Processor, Packetizer) system. Additional responsibilities include the generation of control functions (selects, read and write pulses, etc.) and the incorporation of extraneous glue logic. Also, all data stored in memory flows through the EDAC (Error Detection and Correction) circuitry that is contained in the BUS ASIC.

This chip was designed using Mentor Graphics CAD tools and fabricated at the UTMIC radiation hard foundry. Prototype chips were delivered in the fall of 1992 and tested at GSFC. The chip is being integrated into the flight programs. When the chip comes back from the SOS foundry, it will be tested to examine its flight quality.

7.10 Viterbi Decoder

Introduction

Let the received code word be

$$r = r_i, r_{i+1}, r_{i+2}, \dots$$

where r_i is a codeword. In a block code, each r_i is a set of symbols; for example for the CCSDS Reed Solomon code, each r_i consists of 255 8-bit symbols [6]. In a rate 1/2 convolutional code, each r_i is a 2-bit symbol.

Block codes use a "hard decision" methodology in the decoding process [5] where a decision is made based on the information in one r_i . A "soft decision" methodology uses a sequence of codewords, each symbol used in many error calculations to identify an error. For each received codeword r_i , the most likely transmitted message codeword m_i is determined by the sequence of received codewords $r_i, r_{i+1}, r_{i+2}, \dots, r_{i+t}$ [5].

Convolutional codes use soft decision decoding [5]. A common widely used means to decode convolutional codes is known as the Viterbi decoding algorithm [5]. While this algorithm is relatively straightforward and easy to implement in a general purpose computer, no known hardware exists to decoder larger constraint length (greater than 14) that operates in the 10 Mbits/second range. To achieve faster data rates, a parallel or pipelined architecture is needed. Though the computing requirements are quite large, the interconnect problem associated with a parallel implementation is severe, and constitutes the main problem.

The goal of this research is to investigate a VLSI solution to producing a high speed (10 Mbit/sec) Viterbi architecture for a large constraint length convolution code. It is proposed to identify a unique architecture that minimizes the interconnect problem.

Proposed Work

Considerable work has already been done to formulate the proposed solution, which is now felt to be practical. Much simulation and preliminary design effort has been spent

verifying key pieces of the proposed architecture.

The first task that we will perform relative to the project once funding arrives is to generate a detailed specification for NASA and NMSU to review.

The next task would probably be to create a detailed functional simulation of the decoder system for NMSU and NASA to review so as to ensure that the performance of the system is what NASA and NMSU expect.

Here is a list of technical properties of the decoder:

1. Implements a Viterbi Decoder (maximum likelihood) for the rate 1/2 code:

$$G(d) = \frac{1 + d^2 + d^3 + d^4 + d^6 + d^7 + d^8 + d^{10} + d^{14}}{1 + d + d^5 + d^6 + d^7 + d^8 + d^{11} + d^{13} + d^{14}}$$

2. System consists of 128 or fewer identical chips operating in parallel.
3. Each chip will have approximately 276 I/O pins. A tentative signal pin summary is given below. Power pads will be added as available and required.

Pin Name	Count	Description
M	256	Metric and Traceback Signal Paths. Input/Output.
S	10	Winning metric Select. Some Input/Some Output.
Clock	1	System Clock. Input.
Q	2	Data Out. Tri-State.
ResetN	1	System Reset and Initialization Control. Input.
D	3	Data Input. Input.
NoLock	1	Data Sync Not Acquired. Output.
Config	2	Configuration Serial Data path.

4. The maximum data rate for chip to chip communication will be 35-45MHz.
5. The system clock for the decoder will be 35-45MHz.
6. Input data will be supplied at a 20MHz rate, three bits at a time. Incoming data is encoded in normal binary coding to represent eight quantization levels (0-7). It is assumed that 0 corresponds to a noiseless logical ZERO and 7 corresponds to a noiseless logical ONE.
7. Individual branch metrics are calculated as the absolute value of the difference between the expected noiseless values and the actual received values. These are three bit quantities.
8. The effective size of the history buffer for path traceback will be 70 or more bits deep.

9. The smallest metric encountered will be calculated for purposes of metric re-normalization and signal lock determination.
10. The decoder will automatically determine the proper bit lock based upon the metric values.
11. The individual metrics will be represented as 10-12 bit quantities. Attention will be paid to arithmetic circuitry to insure overflow cannot occur.
12. Maximum supported Information rate of: 10 Mbits/Second.

7.11 Data Compression

Greg Zwegle

Lossy data coding research at the MRC has centered on developing waveform based coding techniques. Algorithms under consideration include the discrete cosine transform (DCT), discrete wavelet transform (DWT), and maximally decimated multirate filter banks (MFBs). The wavelet transform and multirate filter banks are known to outperform the discrete cosine transform by reducing coding artifacts in decoded data. However, the DCT is a very well understood algorithm that can be implemented in hardware with a relatively low cost. The DWT and MFBs are still in the research stage and in general have higher hardware implementation costs.

The research has developed new rate distortion results for realizable MFBs (which can be used to compute the DWT), giving insight into how they can be designed for best performance. These results are under consideration for publication. The research has also developed new techniques for hardware implementation of all three coding algorithms. An area of work involving the Rice algorithm is in the use of Rice with adaptive differential pulse code modulation (ADPCM). This may be incorporated in the USES chip to provide a fixed bit rate when needed.

Future Directions

The data compression research will continue to explore the theory and implementation of modern waveform coding techniques. Theoretical tasks ahead include applying these algorithms to lossless data compression and incorporating the Rice algorithm with adaptive versions of these coders for lossy data compression. ADPCM is being implemented for USES with the intent of providing a fixed bit rate and is not optimized for best compression ratio. A higher compression ratio can be attained at the expense of a variable bit rate. Research into this use of ADPCM with Rice and minimizing the variable bit rate problem is planned. Finally, research will continue looking at VLSI implementation issues for all of these coders. These ideas are also well suited for video data, if there are needs for this.

The current American National Standard Data Format for the Interchange of Fingerprint Information is using a symmetric wavelet transform. I am not sure if the standard

is finalized or if it is still in development. The expertise we have here at the MRC in lossy data compression could be used to implement this standard or help develop it.

7.12 Analog Conditioning of Digital Images

Greg Donohoe

The goal of this effort is to dynamically map an analog video signal into an 8 bit digitized image using a uniform A/D converted in such a way that the entropy of the digitized image is maximum. If done well, this should allow us to construct digital imaging systems that work with fewer digital bits that would otherwise be required for reliably detecting objects in the image. This is an ill-posed problem, but we have found several approaches that seem to work well. One is based on a programmable linear gain block with clipping; another is based on a programmable, piecewise linear amplifier.

So far, we have implemented the linear system using commercial video digitizing equipment from Datacube. With this implementation, we have been able to dynamically increase the entropy of a raw video signal from about 5.5 bits/pixel to around 7 bits/pixel; this can make a dramatic difference in the ability to detect things in the images. In order to do better than this, and to handle more difficult cases, we will have to use more degrees of freedom: this is the motivation for the piecewise linear system. We can only simulate the piecewise linear system at this time.

In order to make further progress, both in terms of theory and in moving towards realizing useful systems, we need to build our own hardware. Even with the linear solution, commercial hardware is less than ideal, since it was not designed with this application in mind. Listed below are the proposed development stages:

1. Implement the programmable linear gain function at the breadboard level, with bit switches to provide the gain and offset functions. This will give us some experience handling video signals.
2. Add an A /D converter and some memory, and interface a PC to automatically generate the gain and offset functions. At this point we could spin off development of a small, self-contained demo unit.
3. Implement the piecewise linear gain function in analog, with the adjustment algorithm running in the PC. We will probably want a second student at this point.
4. Build a black box, eliminating the PC and moving the entire algorithm into one self-contained module.

As this work progresses and the real-world constraints become clearer, the algorithm work will crystallize.

7.13 Nonlinear Prediction for Image Data Compression

Greg Donohoe

Linear prediction is a well-known image data compression technique. This method treats the image as a 2-D sequence, scans the sequence and predict future pixel samples from past samples. If the image is perfectly predictable, the prediction error is zero. If the predictor is invertible, we can exactly reconstruct the image by running the predictor backwards; we only need to store a description of the predictor algorithm, some starting values, and a prediction error sequence. We hope that the error sequence will have a lower entropy than the original image; then an entropy code like the Huffman code can produce a code with a smaller average word length. The method can be extended to lossy compression by adding a quantizer.

The Wiener predictor is known to be the optimal linear predictor in the mean squared error sense. The Wiener predictor gives disappointing results for several reasons. One is that many sequences are not easily predicted by linear predictors, but may yield to nonlinear predictors such as multilayer perceptrons. Another approach to improving the performance of predictors is to make them locally adaptive. Finally, with trainable predictors, we can seek improved training rules: instead of minimizing the variance, which is only loosely related to entropy in real images, we can seek to minimize the entropy directly.

The desired result of this work is a better understanding of predictive coding, generate a set of computer programs for implementing predictive coding, and a paper for the NASA VLSI Design Symposium.

7.14 SOS VLSI

Sterling Whitaker

Silicon on Sapphire (SOS) as a technology has natural immunity to some radiation effects. Total dose radiation does not significantly change the threshold voltage of the transistors at the radiation levels experienced in most NASA missions. In addition, due to the reduction of junction area SOS is fairly immune to Single Event Upsets (SEU). Therefore, SOS is an ideal candidate for VLSI design.

When Hewlett Packard first announced an SOS foundry capability, there was a great deal of interest generated in pursuing SOS VLSI. SOS has attractive advantages, such as improved speed, which appealed to commercial industry. Initial results were promising, but a basic limitation to the scalability of the process was encountered at about the 2 micron level. Without the ability to continue to scale the process and with continuing yield problems, it became unacceptable to Hewlett Packard to maintain a viable commercial production and the SOS foundry was discontinued. Since Hewlett Packard's exit from the SOS foundry business, very few new commercial firms have initiated SOS foundry activity. The scaling problem is a crystalline defect occurring at the silicon sapphire interface preventing the epitaxial layer from being reduced below about 5000 Å. This prevented the

implementation of transistor with features smaller than 2 microns. Therefore, the current SOS process lines are several generations old relative to the density available in modern bulk CMOS processes.

The Navy at NaRAD in San Diego has solved the defect problem and now is able to produce SOS devices with 0.75 micron geometries. This process, with two layers of metal, is expected to be fully operational near January 1994.

It is proposed that the NASA SERC work with NaRAD to investigate using SOS as a technology for flight electronics. The joint activities would include:

- Designing special test cells to be included in the fabrication runs as NaRAD develops the new manufacturing line. This amounts to free process runs through their foundry. Test cells to be designed are those common to Reed Solomon and data compression VLSI.
- Design a Reed Solomon CCSDS encoder in SOS as a test chip.
- Investigate the SEU immune properties of SOS.
- Incorporate SOS design rules into the CAD system.
- Develop electronic design CAD tools needed for SOS.

The SERC has delivered two test designs to NaRAD: the lossless data compressor and an 10 bit A/D. The lossless data compressor chip is being made ready for fabrication. The masks were made in April 1993 and complete fabrication is scheduled for completion in August 1993.

7.15 The Decomposition of Synchronous Sequential Machines Using Regular and Repetitive Structures

K. Hebbalalu, J. Frenzel, D. Lynn and S. Whitaker

Most digital Very Large Scale Integrated (VLSI) circuits currently designed contain controllers based on synchronous state machines which coordinate and control activities occurring both inside and outside the chip. Depending on the complexity of the control required, these synchronous sequential machines can be large. While it is possible to design these machines as single composite units, a large number of state variables can result in unwieldy design equations. The layout process for these composite, large machines can become complicated and labor-intensive. Even minor changes in the original flow table may result in complete redesign and relayout of the machine. In addition, large machines tend to be slower and not very amenable to fault diagnostics [29]. Decomposing large machines into smaller component machines is not new, much research focuses on heuristic algorithms for decomposing state machines and on logic minimization and interaction optimization for the component submachines [30,31,32]. Decomposition techniques which

are conducive to an implementation of submachines using repetitive structures have not been investigated. This research presents two new decomposition processes, and also a framework for implementing all the submachines using a regular, repetitive structure taking advantage of a computer aided design and layout process using pass transistor logic based Sequence Invariant State Machine (SISM) designs [33]. This method enhances the ease of the design process by not requiring the use of complicated design equations and K-Maps.

On inspection, many state diagrams reveal natural 'bottleneck' states which connect groups of states. A bottleneck state is defined as a state through which a machine *must* pass while progressing from one group of states to another. The state machine can be decomposed around such a state, making each group of states into a submachine. A typical decomposition is to form the group of states which is *first* activated at power-up (i.e., the group of states starting at the top of the state diagram and ending at the bottleneck state) into the *primary* submachine, and the remaining group(s), *after* the bottleneck, into the *secondary* submachine(s). The secondary submachines are activated only if the primary submachine raises a ready signal. Usually, the bottleneck state is made the last (i.e., wait) state of the primary submachine. The primary submachine obviously has separate start-up and wait states. Such a machine is called an *open* state machine. Normally, a secondary machine is formed, having a single state which acts as both a start-up and a wait state. Such a machine is called a *closed* state machine.

The inputs to a state machine can be classified under three general categories: 1) those inputs under which *all* the states make transitions to other states in the machine; 2) those under which states of a *group* transition amongst themselves, and 3) inputs under which a *single* state transitions to other states. An examination of the flow table reveals which of the three classes of inputs discussed above are predominant, and hence, decomposition can be done accordingly. The central idea here is to seek *disjoint* groups of inputs, under which groups of states transition amongst themselves, and in addition, there should be little or no overlap between the groups, i.e., isolated groups of inputs with corresponding isolated groups of states should be identified. These can be formed into submachines.

These methods were designed and simulated for a large statemachine which is currently on an industrial IC. This machine had been implemented as a PLA, using 4 state variables and 139 minterms, as described in [38]. This PLA implementation has a core area with dimensions $270.2\ \mu\text{m}$ by $642.2\ \mu\text{m}$. SPICE simulations under $3\ \sigma$ worst case speed parameters at 100°C and $V_{dd} = 4.5\text{V}$ indicate that this PLA operates at 25 MHz. These results can be compared with those obtained for the same machine, implemented using the decomposition methods outlined above.

After the logic simulations for the circuits generated by the three methods of decomposition were carried out, the layouts were implemented using the program described in [34]. The areas occupied by the SISM portions of the submachines, excluding the input and output forming logic are given to provide a direct comparison with [38]. Method 1 required $(61,110\ \mu\text{m}^2)$. Method 2 required $(67,767\ \mu\text{m}^2)$. Method 3 required $(37,030\ \mu\text{m}^2)$.

For speed comparisons, the slowest machine in each method was first determined. These were; M_1 in method 1 (20 inputs): M_1 in method 2 (17 inputs) and M_J in method 3 (5

inputs). Capacitances were extracted for these submachines and SPICE simulations were carried out under 3σ worst case parameters at 100°C and $V_{dd} = 4.5\text{V}$ and maximum values of estimated capacitances. The slowest of the methods is method 1 (decomposition using state F), which will still work properly at 55 MHz, and the fastest is method 3 (decomposition into one-bit machines), which operates at 140 MHz. These speeds have been calculated excluding the delays through the input forming logic blocks. The remarkable increase in speed in method 3 is obviously due to the smallness of the input matrices in the submachines, where the highest number of inputs is 5.

7.16 General Purpose CCSDS Packetizer

Gary Maki and Qian Chen

Abstract

High speed data communication is a critical element in advanced NASA satellite systems. A NASA standard has been defined and approved that specifies the functionality and format of advanced data systems. The next step is to research hardware architectures that implement the goals of the standard. However, architectural studies have not been undertaken for many of the components in advanced data system networks.

This research proposes to investigate and develop an advanced VLSI architecture to achieve CCSDS packetization. A general purpose packetizer must be able to process high speed data, but provide a great deal of flexibility for general use.

Introduction

High speed data communication is a critical element in advanced NASA satellite systems. A standard has been defined and approved that specifies the functionality and format of advanced data systems by the Consultative Committee on Space Data Systems [6,14]. However, architectural studies have not been undertaken for many of the components in advanced data system networks.

This research is concerned with the investigation of architectural details to implement a general purpose CCSDS packetization VLSI component. A general purpose packetizer must be able to process high speed data, but provide the flexibility to apply to a large range of satellite missions.

CCSDS System

The front end of the CCSDS system is depicted in Figure 6. The sensor data first passes through an Analog-to-Digital converter. The number of output bits can vary from instrument to instrument. To remove sensor irregularities, it may be necessary to perform radiometric correction. Many advanced high rate instruments now will require data compression in order to achieve information transfer in the face of bandwidth limitations.

In current satellite systems, each component is designed to function for specific satellite. It would be more desirable to have general purpose devices to reduce cost and improve reliability where one proven design can be employed on many missions.

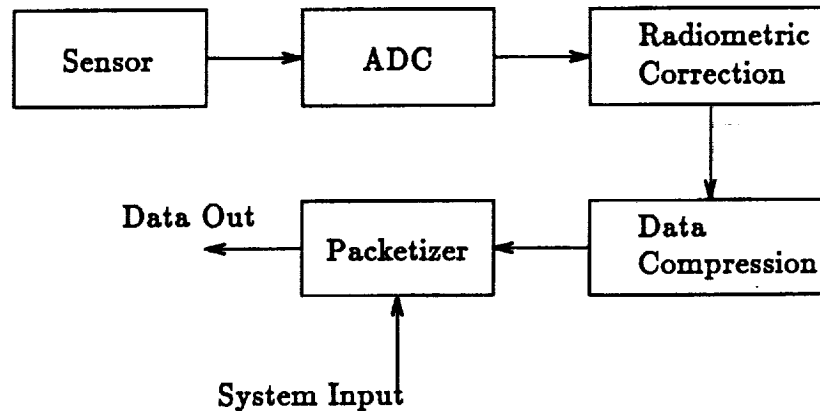


Figure 6: CCSDS Front End System

As shown in Figure 6, the packetizer is driven by the data compression circuit. The compression chip was designed to be general purpose and apply to a large variety of missions.

The data compression chip set was developed under previous NASA grants is the first VLSI implementation that performs high-speed, adaptive, lossless compression and decompression [15,16]. Under nominal conditions the encoder can operate in excess of 50 Msamples/s while the decoder can process data at half of that rate.

The major objective for designing and fabricating the chip set is to provide real time lossless compression for satellite imagery. In order to compress satellite imagery it must adapt rapidly to changing scene statistics and compress image data over a wide entropy range. The bit rate depends on the quantization, which can vary from 8 through 18 bits/sample.

Development work is being pursued on each of the following elements:

- A 18-bit ADC is being designed for potential flight use at the NASA SERC. In addition, an SOS 8-bit ADC is being fabricated at a Navy facility.
- A radiometric general purpose pipelined processor is being specified for potential use in the Landsat program.
- A flight lossless data compression circuit is being specified and is scheduled for implementation prior to January 1993.

The next circuit in the system that ought to be studied is the packetizer.

The CCSDS data unit structure is shown in Figure 7. The CCSDS packet is a variable length packet with all elements except the secondary header specified. The MPDU and VCDU are fixed length data units. The proposed packetizer will be able to generate any of the data units.

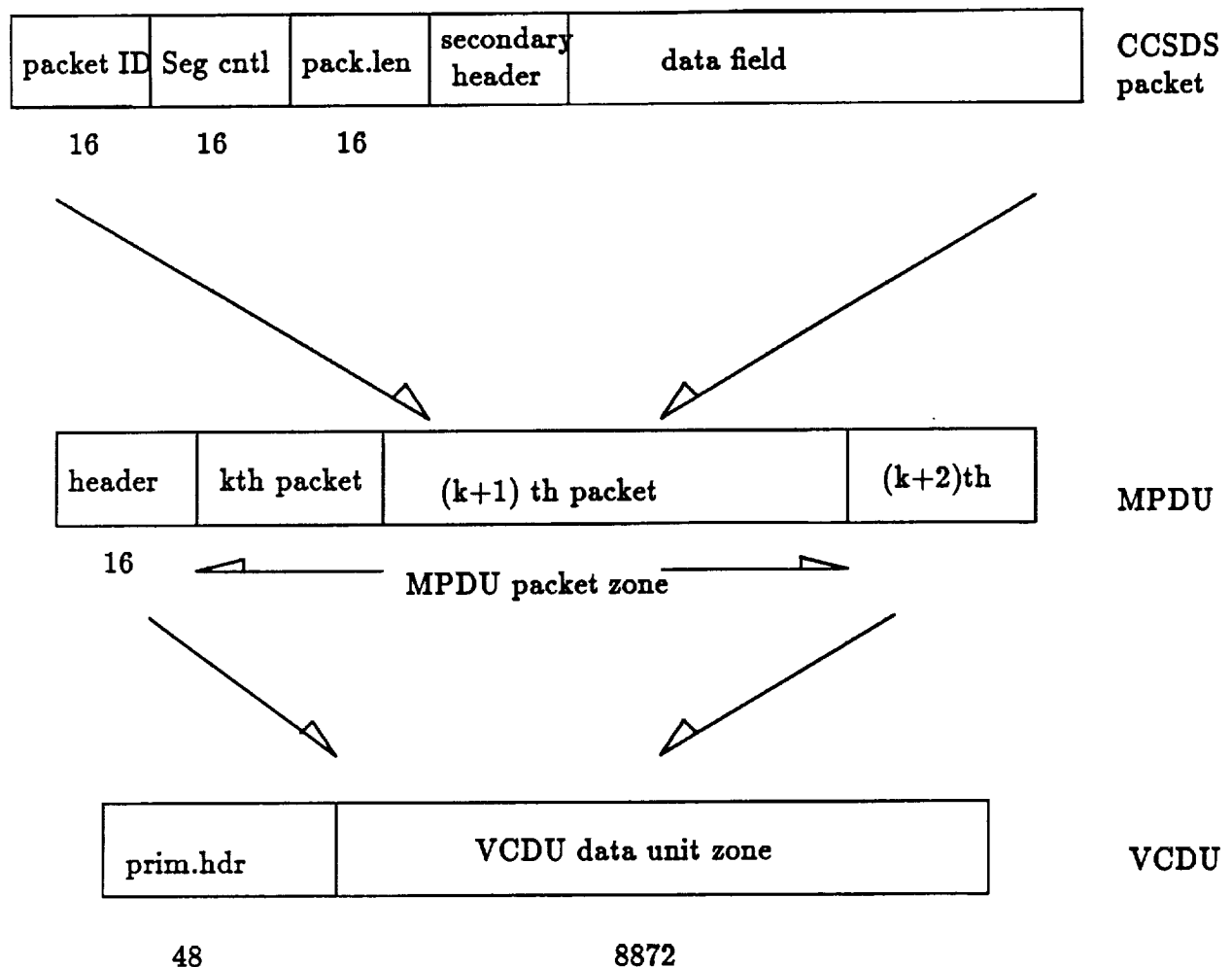


Figure 7: CCSDS Data Structure

CCSDS Packetizer

A general packetizer must address the following issues:

- Variable input data streams. Instruments may output data words with different data widths. Moreover, the data compression output may require a dynamic data width which change with each sample.
- Variable packet size. The CCSDS packet is a variable length packet and the packetizer must be able to produce such a data unit.
- Support several data unit structures. To increase the generality of the packetizer, CCSDS packets, MPDU's and VCDU's must be supported in VCDU data units.

- Variable header structures. The following flexibility is needed to support variable headers.
 - Variable length headers. Each of the CCSDS, MPDU and VCDU headers are different in length and content. Moreover, there is an undefined secondary header field that must be supported.
 - Variable element types. Some elements do not change from data unit to data unit, such as the satellite APID. Some elements are incremented from one data unit to the next. Other elements are inserted in the data stream such as the CCSDS packet length. And finally some elements are fetched from the system and inserted in the data stream, such as time.
- Input/output protocols. Handshaking must be employed on both the input and output along with the ability to support burst mode operation.
- General Purpose system control. Being a general purpose device, it is desirable to allow the system configuration to be driven by a central instrument microprocessor or controller.

Proposed Solution

The solution to a generalized packetizer should incorporate the following features to address the above issues:

- Programmable architecture. A general purpose architecture will be advanced that allows for external programming. External programming is envisioned to be programmed in the similar manner as a programmable chip that is configured in a modern PC. Data words are presented to the chip in an on-line mode, not through loading of computer code in a RAM.
- Configurable architecture. To produce a variety of data units, with variable outputs, the data path must be configurable.
- External memory storage. To store CCSDS packets that are expected in new satellite systems, a medium sized RAM is needed. Such a RAM is unlikely to be realized on a flight chip with today's technology. Therefore, it is necessary to support external memory for data storage. The main problem to be addressed is the means to achieve real time data flow (memory reads and writes) without conflict.
- Variable Header size. The variable header structure will need special attention. The data elements are fixed, can be incremented, or totally replaced by external or internal data.

- CCSDS and VCDU data unit support. Creating CCSDS data units only is relatively straight forward. Since the packetizer needs to support CCSDS packets, this hardware architecture must be employed. Unlike the variable data unit size of the CCSDS packet, the VCDU data unit is fixed length. A VCDU data unit may contain one or more CCSDS packets as shown in Figure 7.

The CCSDS generator will likely be a combination of sequential and parallel state machines driving the data path. The key research element will be to produce a state machine structure that is able to halt and remain in an arbitrary state for an unspecified period of time when a VCDU has been generated, and then, when more data can be output to form another VCDU, restart exactly in the halted state. Sequential machines do not possess this property.

Proposed Research

It is proposed to advance a new general purpose VLSI architecture that will address the needs of high speed CCSDS data systems, specifically the challenges presented by a packetizer. A new general purpose architecture will require new advancements in data architectures that can process variable header data, new advances in sequential circuit theory, and programmable hardware structures.

The CCSDS data system is a flight system, therefore the study will be oriented towards producing a data system component that meets NASA radiation requirements. To fully understand and verify that the proposed architecture is feasible and the technology that is developed under this grant is transferable, a hardware prototype component will be designed, but not fabricated under this grant.

8 University of Idaho Research Report and Proposed Research

8.1 FY93 Progress Report and FY94 Proposals

James F. Frenzel

Summary of Research Results

Research for the past year focused upon two areas: the design of a defect-tolerant cache memory and a defect-sensitivity analysis of an SEU-immune logic family.

Design of a Defect-Tolerant Cache Memory

Previous research demonstrated that a set-associative cache memory can still perform well in the presence of memory defects, due to the inherent redundancy. The design of a defect-tolerant control circuit was completed which implements the LRU replacement algorithm. Once configured, the controller would automatically avoid loading data into faulty memory locations, transparent to the rest of the system. The design has been functionally verified through simulation. These results were presented at the Fourth NASA SERC Symposium and the Eleventh IEEE VLSI Test Symposium.

Defect Analysis of an SEU-Immune Logic Family

This research involves a CMOS logic family developed by the University of Idaho NASA SERC. The logic family has the characteristic that it is immune to transient single event upsets (SEU's), making it particularly attractive for space applications.

The objective of this research was to determine if the properties that provide SEU immunity also reduce the sensitivity to manufacturing defects. It was found through SPICE circuit simulation that the use of weak feedback transistors actually increased the sensitivity of the circuitry to resistive shorts, compared to conventional CMOS logic. However, because the range of resistances actually observed in manufacturing defects is limited, this increased sensitivity is not expected to result in a reduced yield. Additional manufacturing defects, such as open circuits, are currently being modeled and evaluated.

Proposed Research for FY94

Work is proposed to design and fabricate a defect-tolerant cache controller in standard cell technology. Comparisons will be made, based upon size, speed, and power consumption, with conventional memory repair techniques. The results of the defect-sensitivity analysis on the SEU-I logic will be used to develop a test strategy for the logic family. A test chip

will be designed and fabricated, containing intentional design errors chosen to represent manufacturing defects. This chip will be used to assess the validity of the simulations and the effectiveness of the test method.

Highlights of Results

A defect-tolerant cache control circuit was designed which realizes the LRU replacement algorithm. Design of a standard cell implementation of the circuit will begin this summer. Such a device would improve the yield of on-chip cache memories.

A performance analysis of an SEU-immune CMOS logic family in the presence of resistive shorts was completed. It was found that the use of weak feedback transistors, which provide the radiation immunity, increased the sensitivity of the family compared to conventional CMOS.

8.2 Magnetic Bearing Control

Joseph Feeley

Summary of Research Results

Activities this year have been ongoing in three different projects related to the control of magnetic bearings: 1) development of an eddy current model, 2) design of a VLSI fuzzy controller, and 3) activating a magnetic bearing test fixture. The results in each of these areas are summarized below.

Eddy Current Model. A nagging problem in the design of control systems for magnetic bearings has been the lack of an adequate model of the effects of eddy currents on actuator performance. Ignoring, or improperly modeling, these effects can lead to unsatisfactory bearing response and possible instability. A simple, yet accurate, dynamic model of eddy current effects has been developed. It accurately accounts for the additional phase lag introduced by eddy currents. The model extends the traditional magnetic circuit model based on magnetic circuit reluctance by introducing a new dynamic element, the "eddy-inductance." The eddy-inductance is conveniently parameterized in terms of readily available magnetic circuit data. The new model has good intuitive appeal and should prove to be generally useful in analyzing magnetic circuits.

VLSI Fuzzy Controller. Fuzzy control offers an interesting alternative to traditional control approaches, especially when the system to be controlled is nonlinear and difficult to model. The fuzzy control approach may prove useful in dealing with the nonlinear and unstable dynamics of magnetic bearings. A VLSI chip capable of implementing a four-input two-output fuzzy controller has been designed and simulated, and is nearly ready for fabrication. Experience with fuzzy control to date has been dominated by the Japanese; only one commercial fuzzy chip manufacturer has been identified in the United States. Use of this fuzzy chip as a magnetic bearing controller will provide valuable experience in the practical applications of fuzzy control.

Magnetic Bearing Test Fixture. Through the efforts of NASA-Goddard a magnetic bearing test fixture fabricated by Philips Laboratories was obtained for control system testing. The test fixture bearing dynamics and dimensions are similar to those of magnetic bearings used on a cryogenic refrigerator constructed by Philips for NASA. Efforts are underway to make the test fixture operational so that various magnetic bearing control schemes can be evaluated.

Proposed Research for 1993/1994

The objective of research efforts for the coming year will be to compare the effectiveness of the various digital control schemes previously proposed: classical, LQG, and fuzzy. Comparisons will be carried out both by computer simulation and actual implementation using the Philips Laboratories magnetic bearing test fixture. The possibility of integrating a magnetic bearing control system with a power electronics current driver actuator will also be investigated.

Highlights of Results over Last Twelve Months

The main results obtained over the last twelve months are the development of the dynamic eddy current model and the design of the VLSI fuzzy controller chip. The eddy current model will not only improve and simplify the design of magnetic bearing control systems, but will be useful in general for the analysis and design of magnetic actuators containing significant eddy currents. The fuzzy chip will permit actual experimentation with fuzzy controllers on a dynamic system of practical interest: a magnetic bearing. This experience may also have broader implications with respect to closing the gap between Japanese and American expertise in the practical application of fuzzy control theory.

8.3 Neural Network Design and Application

Howard Demuth

Summary

Research on an effective method of training neural networks on data that contains outliers has been completed. A way of avoiding the long training times commonly associated with outliers has been developed and a draft of a paper to be submitted has been prepared.

A unique method for initializing neural networks before training so as to minimize the training times has been investigated with good preliminary results.

Bisection has been applied to inverting the functions stored in neural networks. Research continues on a method of automatically generating values to initialize the bisection method.

Proposed Research During Next Year

Investigate:

1. Calculating the inverse of a network's function. Normally, backpropagation is used to find parameter values for a network so that it will produce a desired output for a fixed input. It occurred to us that if the parameters of the network are fixed, backpropagation can be used to find the inputs to the network that result in a desired output. If the network is viewed as performing the transformation $y = f(x)$, then the backpropagation technique can be used to solve for the inverse relationship $x = f^{-1}(y)$.
2. Initial conditions - Nguyen and Widrow constructed a method for initializing the weights of nonlinear neurons to more useful values than are found with a uniform random distribution. The result of using nguyen-widrow initial conditions is a drop in learning time by a factor of ten or more. We believe their method is good but that there exists room for improvement.
3. New algorithms for training neural networks effectively and quickly.
4. New applications within NASA for neural networks.

8.4 Using Cross-correlation Techniques to Detect Linear System Degradation

Harry W. Li

Summary of research results

The objective of this work is the characterization of a linear system through nonintrusive, background monitoring using crosscorrelation techniques. The work began in November of 1992 and has entered into the design and simulation phase. To date, the accomplishments are as follows:

- Analysis of the problems associated with the implementation of the techniques to a linear system.
- Examination of the statistical properties of the disturbance noise.
- Evaluation of different methods for generating the disturbance noise.
- Analysis of the accuracy limitations using various disturbance signals.
- Preliminary design of a basic system.
- Modeling of the components at the block level.

Proposed research during the next year

It is hoped that some components will not require a full custom design and layout. Rather, we hope to use standard designs which meet the requirements of the system.

- Complete design of the crosscorrelation system, disturbance generators and associated circuits.
- Circuit level simulation of the critical components.
- Simulation and modeling of the entire system.
- Layout, fabrication, and testing of the system.

8.5 Computer Modeling of Thermal Effects in Integrated Circuits

Ken Noren

Proposed research during the next year

Modeling the temperature effects of IC's.

The research will involve computer modeling of IC's. Presently, a weakness in computer models is that they lack variation in their behavior with temperature. There are two problems associated with this. First is understanding how the behavior varies, second is being able to model it. There are two factors which cause variation in temperature. First is the ambient temperature, second is the change in temperature due to self-heating. The research will have as it's main focus modeling the effects of self-heating. Secondary issues are understanding and modeling ambient temperature effects and looking at more applications for the modeling.

8.6 Wavelet Transformations

Jim Peterson

Kraig is exploring features of wavelet transformations so that specific implementations can be achieved that take advantage of unique algorithm structures so as to enhance efficiency and speed. Design methods used in neural networks and quadrature mirror filters, which are used in wavelet implementations, are being investigated for possible applications to the design of wavelet filtering and processing algorithms. Switched capacitor techniques might also offer viable approaches for wavelet implementations and this is being investigated. Kraig is comparing different digital filters that he has identified to use with wavelet analysis by looking at their VLSI implementations. Within the area of switched capacitor filter designs, features being explored include size requirements, regularity of the layout, and simplicity of the design.

The proposed research for 1993-94 is:

1. Explore applications of the wavelet transformation to signal and image processing, with a view toward transportation monitoring and control, and data compression applications.
2. Identify and utilize existing hardware processors to implement wavelet and other signal processing algorithms for applications in control systems, signal processing, and data compression.

8.7 Modeling the VHDL Signal Data Type

Phillip Windley

Few modern VLSI circuits are designed using only classical logic gates [20]. In designs using pass-transistor, tri-state, and pre-charge logic, it is common for circuit nodes to be driven from more than one circuit device. These multiple drivers are designed to have differing drive strengths in order for one to dominate over another in cases of contention. The drive strength is considered to be closely related to current drive or charge sourcing/sinking capability [19,25]. These design techniques dictate that digital logic circuit models and simulations must be capable of including devices down to the transistor level. Transistors, at the logic level, are modeled as simple switches, with electrical properties such as threshold voltage abstracted away. The physical attributes such as transistor size can be represented by the strength of the signal that the transistor drives.

The Lattice Model of Signals

Bryant developed a *lattice theoretic* data type for his original MOS switch-level simulator, MOSSIM, where the members of the signal value data type represent the combination of *logic state*, from the set $\{1, 0, X\}$, and *drive strength* [18,25,27]. The signal values form a partially ordered set (poset), with their order based on strength dominance when circuit signal values are interconnected.

A lattice structure is described through the notion of immediate superiors or *covers*. For two members, a and b , of a poset, a *covers* b if and only if $a > b$ and there exists no member x of the poset such that $a > x > b$ [17]. A lattice can be represented in graph form. The vertices of the graph are the members of the poset and the edges of the graph represent the covers. If the graph is drawn such that whenever x covers y then the vertex x is *higher* than the vertex y it is called a *Hasse diagram* [17]. Figure 8 shows an example of the kind of signal value lattice Bryant defined [25,27]. This example has three strengths; "strong", "weak", and "disconnect". A strong true is depicted as "S1", a strong false is "S0", a weak true is "W1", a weak false is "W0". A strongly driven unknown is "SX", a weakly driven unknown is "WX", and "Z" represents circuit "disconnect". By definition, the logic state of disconnect is unknown. The least-upper-bound (*join*) of two

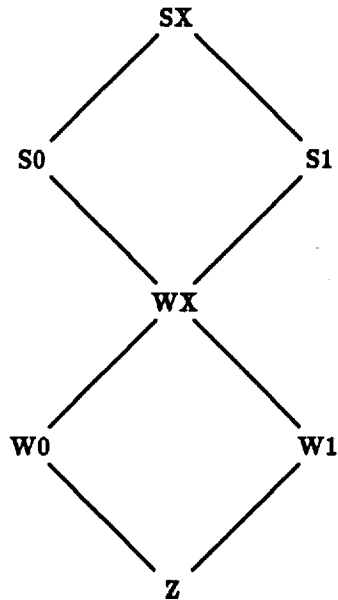


Figure 8: Bryant's Signal Lattice for Two Strengths

or more signal values provides a signal resolution function that determines the result of the interconnection of nodes driven toward those signal values. For example, the result of interconnecting signals S1 and S0 is a signal of value SX. Similarly, the join of the two signals W0 and W1 is Z.

The Unknown State

The unknown state can be the result of a node connected to two outputs, with one driving toward true and the other driving toward false, neither one having sufficient strength to dominate the other, resulting in an invalid logic level. In many logic simulators, the unknown state is also used to model a node whose voltage is not yet known. Combining the cases of *invalid* logic level and *valid but not known* into a single unknown state simplifies the simulation algorithm. A rigorous modeling of the effects of unknown but valid states would require determining Boolean satisfiability, an NP-complete problem [19]. To avoid an exponential algorithm, many simulators do not attempt to distinguish between valid but not known and invalid logic levels. This approach can make the simulator pessimistic since it may propagate the unknown state when resolving other circuit nodes [19].

Extending the Lattice Model

Bryant abandoned the logic state/strength combination approach to signal values for the MOSSIM II simulator, stating "while this approach at first seems very elegant, it cannot

adequately describe the effects of transistors in the X state [19].” Cameron and Shovic demonstrated that the problem with the X state can be overcome by extending the signal strengths to include a possible *range*, giving the signal values some degree of strength indeterminacy [20]. Solving the problem of the unknown state by extending the signal values to include strength indeterminacy may have an advantage over the switch graph approach in that the latter *requires* working at the transistor switch-level. The indeterminate strength approach supports accurate modeling at the switch-level but also allows higher level models, including wired-logic, tri-state buses, as well as combining system blocks implemented with different technologies such as TTL, NMOS, CMOS, and ECL [21].

Related Work

Cameron and Shovic called their signal value data type STATE. A four strength, 21 value, STATE signal model has become the basis for the BOLT HDL and NOVA logic simulator [26]. We have developed an extended lattice representation for STATEs [24,23] and used the lattice and resolution function (join) to demonstrate an automatic translation and verification of circuits described in BOLT using the HOL theorem proving system [22]. The commutative, associative, and idempotent properties of the join operation pass on to the signal value resolution function the desired properties of order invariance and the validity of replacing a subset of interconnected driver values by their resolved value. This last property can serve to prevent the resolution function from over pessimistic propagation of the unknown logic state. In addition to providing a mathematical foundation to the STATE resolution function, the Hasse diagram of the STATE lattice provides a useful, quick, visual understanding of the interconnection of signals and has now been included in the NOVA manual [26].

The t_wlogic Data Type

The VHDL Standard Logic Package t_wlogic data type defines five fully ordered strengths:

- Forced (F)
- Strong resistive (R)
- Weak resistive (W)
- High impedance (Z)
- Disconnect (D)

and represents a further extension of the STATE data type:

1. The indeterminate strengths are allowed to range over *all* possible strengths, including Disconnect.

2. An uninitialized value is included to represent valid but not known signals that is distinct from the invalid logic level.

The true and false **t_wlogic** values that include a degree of strength indeterminacy are represented by the triple **bdK** where:

bd represents a *range* of strengths:

b is the strongest possible strength ($F \geq b \geq D$) which sets a lower bound on the strength of a signal that can overdrive this signal;

d is the weakest possible strength ($b > d \geq D$) which sets an upper bound on the strength of a signal that this signal can overdrive.

K is 1 or 0;

For the cases where $b = d$ (i.e. there is no strength indeterminacy) the value is represented by the double **bK**.

The **t_wlogic** values corresponding to the unknown state are represented as a triple **pqX** where:

p is the strongest possible strength driving toward 0 ($F \geq p \geq D$) which sets a lower bound on the strength of a signal that can overdrive this state to a 1;

q is the strongest possible strength driving toward 1 ($F \geq q \geq D$) which sets a lower bound on the strength of a signal that can overdrive this state to a 0.

For the cases where $p = q$ the value is represented by the double **pX**.

There are two single character values:

1. The value **U** is included to represent the valid but not known (uninitialized) value.
2. The value **D** represents the unknown logic state at the disconnect strength.

A Hasse diagram of the 46 values and 73 covers of the extended **t_wlogic** lattice is shown in Figure 9. Given the lattice represented by the Hasse diagram, the least upper bound of any subset of members of **t_wlogic** represents the resolution of contending circuit elements being driven toward those values. As an indication of the expressive power of this lattice treatment, the information expressed in Figure 9 is presented in a 46 X 46 look-up table, covering nearly five pages in *The VHDL Handbook* [21]. In addition to providing a framework for reasoning about **t_wlogic** signal values and their resolution function, the Hasse diagram also provides a useful, quick, visual understanding of the interconnection of signals during manual analysis of circuits.

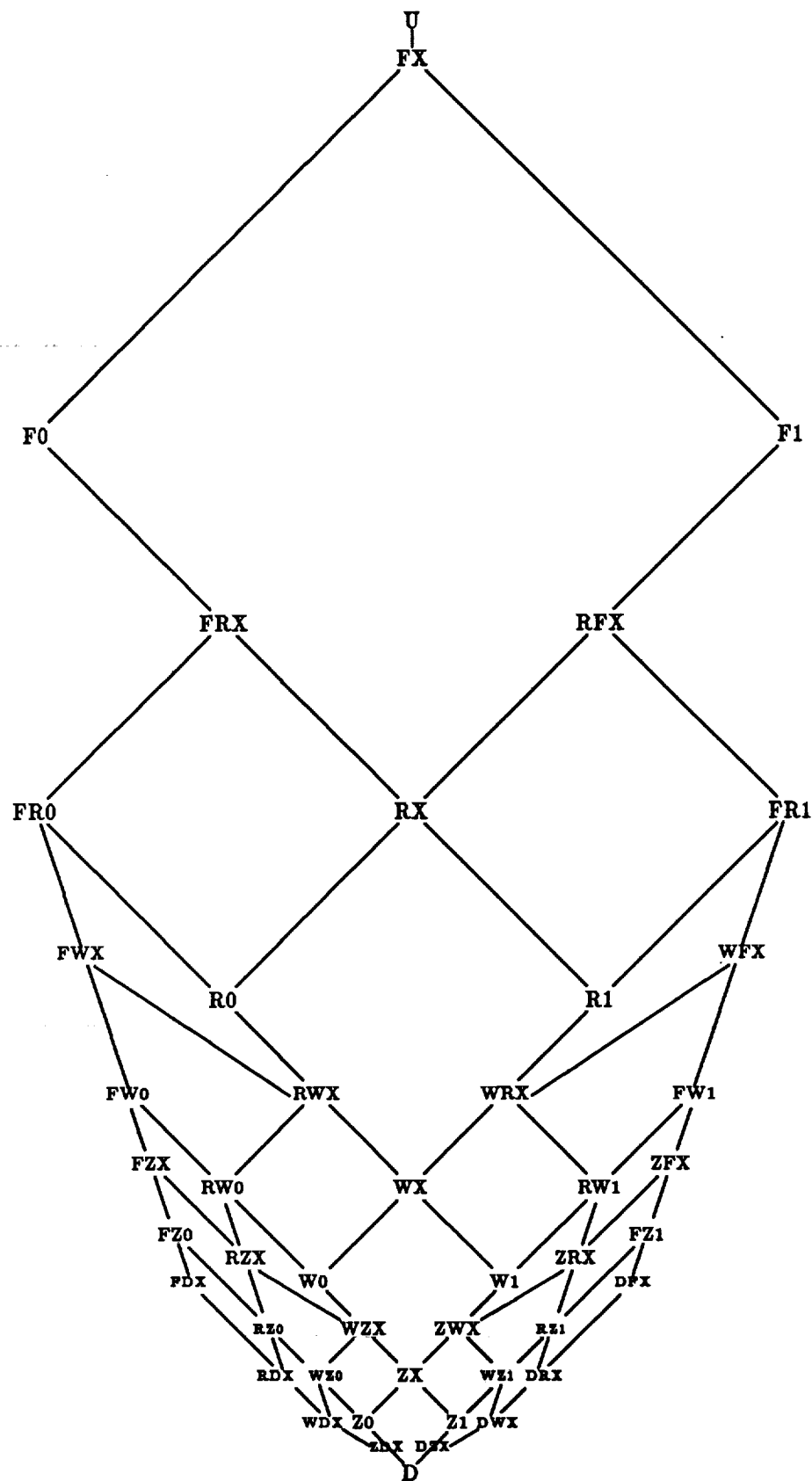


Figure 9: Signal Lattice for VHDL Standard Logic Package

Conclusion

We have provided a foundation for the VHDL Standard Logic Package `t_wlogic` signal data type. This foundation provides the basis for formal reasoning about these values. The lattice development is necessary because neither the previous algorithm or LUTs used for logic simulation programs are suitable for reasoning about such signals. This is important because it provides for the interface between verification through theorem-proving and lower level methods to possibly extend below the point where all signals are represented strictly as booleans. This may include such structures as high level blocks that are interconnected via tri-state busses. The ability to reason about the structures and models used by the CAD tools also enables reasoning about those tools.

8.8 Reasoning about Microprocessor Pipelines

We are designing, verifying, and fabricating a microprocessor for use in safety-critical and security critical missions. The microprocessor, which we call SAWTOOTH, has a modern architecture and features lacking in other verified microprocessors:

- A 5-stage instruction pipeline with feedback.
- A load-store architecture.
- A large register file.
- External and user interrupts.
- Supervisory mode, including privileged instruction and registers.

The work is nearing completion and we will send off a prototype design for fabrication in the next several months. The verification is in progress. We have specifications of all major levels in the hierarchy, proofs of correspondence between 2 of the 4 levels, and are working on the pipeline proof now.

We can conclude, based on our preliminary results, that the use of formal methods has a positive impact of the design process. In one instance, we were able, though the formal specification and analysis, to catch a significant design oversight early in the design process. The problem involved the interaction of supervisory mode and the instruction pipeline feedback path. Assuming that the simulation effectively exercised supervisory mode, the problem would probably have been caught much later in the design process requiring much work to be redone. If the simulation was inadequate, then the problem might not have been caught until after fabrication.

In verifying SAWTOOTH, we have taken a hierarchical approach as shown in Figure 10. The bottom layer of the hierarchy is a model of the microprocessor's structure called the electronic block model. The top-level describes the assembly language programmer's view of the processor. The intervening layers are abstractions which are chosen to reduce the proof effort [28]. These models reduce the amount of data and temporal abstraction

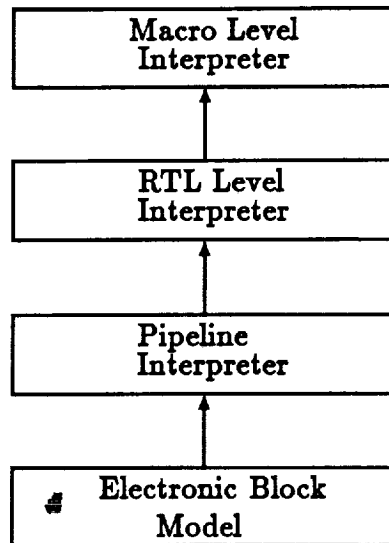


Figure 10: A microprocessor specification can be decomposed as a series of interpreters.

happening at each step to a manageable level. The end result is a proof that the electronic block model implies the top-level model of the processor.

The following is a list of issues that we are investigating as part of this project:

1. Translation of the VHDL model into the specification language of the theorem prover so that we can be confident that the model we verify is the model that was used to construct the device. The work described in Section 8.7 is important to this task.
2. Verifying that the data forwarding circuitry in the pipeline behaves correctly. This has been important work because, as mentioned above, it illuminated several deficiencies in the design related to the subtle problems involved in making the supervisory mode work with the pipeline.
3. Using the pipeline specification to verify that the microprocessors instructions are correctly implemented by the underlying circuitry. This work involves developing new models related to the programmer's level view of a pipelined instruction stream.

Proposed Research for the Coming Year

During the coming year we propose continuing the work on pipelined microprocessors discussed in the last section. Mike Coe is the student performing the work. He has made good progress during the past year, but his research and thesis will not be completed until May 1994.

The following tasks remain to be done:

1. Verification of the SAWTOOTH pipeline data forwarding circuitry.
2. Verification of the pipeline model from the VHDL register transfer description.
3. Verification of the programmer's model of the microprocessor from the pipeline model.
4. Testing the fabricated microprocessor to evaluate the design and verification process.

8.9 Electromagnetics Research

Jeffrey L. Young

Introduction

The following report describes briefly the electromagnetic research activity that is currently being funded by the University of Idaho's Microelectronics Research Center. As reported below, several definitive outcomes were witnessed this past year and the upcoming year holds promise for many exciting studies.

Current Research Activity

Finite difference, time domain (FDTD) techniques have become an important tool for the numerical evaluation of electromagnetic fields in complicated environments. However, when dealing with electromagnetic waves in generalized anisotropic, dispersive media (i.e. the ionosphere), the popular FDTD algorithm manifests a singular short coming: storage of the complete time history of all field constituents. One possible way to circumvent this difficulty is to consider the complete acoustic/electromagnetic equations [See Felsen, *Radiation and Scattering of Waves*, 1973]. By applying standard FDTD techniques to these equations, we believe that a robust algorithm can be developed that will analyze the effects of a dispersive medium on electromagnetic wave propagation. Although this approach is being tested on an one-component model, it should also in theory work for the generalized three-component model.

Future Research Activity

Work is under way to develop an efficient and accurate numerical model that will predict radio wave propagation in an ionized environment (e.g. ionosphere). Several numerical codes have now been developed and preliminary results look favorable. Future work now includes the following:

- Validate the developed two-dimensional, one component numerical model.
- Develop a two-dimensional, three component model.

- Contact NASA in order to ascertain research relevancy. (Contacts with individuals in the Space Station Freedom Office and the Johnson Space Center have been established.) Prepare and submit a proposal to NASA.

8.10 Proposed Research for FY94

John Purviance

Statistical HEMT Circuit Design

The GaAs High Electron Mobility Transistor (HEMT) is being considered for space applications due to its high speed and radiation immunity. However, digital HEMT circuits are strongly dependent upon process parameter variations and device dimensions. The objective of this research is to apply statistical methods to the design of HEMT circuits for the purpose of improving performance and manufacturing yield.

Synthetic Aperture Radar

Synthetic Aperture Radar (SAR) is a two-dimensional imaging system that processes reflected radar signals into an image of the reflecting object. While the image processing may be done using time and/or frequency domain techniques, most methods do not allow real-time processing of the SAR data. This research involves the development of processing algorithms suitable for parallel VLSI implementations.

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9 Special Projects

9.1 Radiation Hard Electronics Solid State Recorder EDAC

Task Objective

- Demonstrate that radiation hard CMOS can be produced in a non-radiation hard commercial foundry.
- Deliver commercially fabricated radiation hard special purpose component proposed to be used in future NASA solid state disc drives which will replace magnetic tape drives.
- Demonstrate full custom VLSI design procedure.

Technology Description

There are three radiation effects to consider:

1. Single event upset (SEU). SEU tolerance is achieved through electronic non-resistor feedback in the proposed designs. This technology was developed at the SERC during the past two years.
2. Single event latchup (SEL). SEL is achieved through specialized layout techniques, as demonstrated in recent tests.
3. Total dose. Total dose tolerance is achieved through IC fabrication. Many commercial foundries produce high total dose levels.

Initial developments have been made that show it is possible to produce radiation hard CMOS in a non-radiation hard foundry. Test cells have demonstrated an LET greater than 120. The proposed development will help bring this technology to maturity.

User Needs and Benefits

The ability to produce radiation hard electronics with commercial foundries would yield:

1. One or two orders of magnitude cost reduction in flight electronics.
2. Design with latest IC technologies to produce faster more dense ICs.
3. Solid state disc drives ought to replace magnetic recorders in future missions. The error correction chip will be a key component in the solid state disc technology.

Current Status

Initial test cells have been fabricated and tested at Brookhaven National Laboratories. The January 1993 and July 1993 tests have shown that the "hard" cells are SEU and SEL immune for LET > 120.

State of Technology

The fundamental electronics is understood and has been demonstrated. The SEU technology was developed over the last two years and published in the NASA Symposium on VLSI Design. The SEL technology is a recent discovery and has been demonstrated at BNL in January 1993.

Technical Approach

- Design custom processor.
- Fabricate in modern MOSIS foundry.
- Test at Brookhaven National Laboratory.

Proposed Budget

Engineering	\$13,000
Fabrication	15,000
Radiation Test	22,000
Total	\$50,000

9.2 Special Project Viterbi Decoder

Viterbi decoders are widely used by NASA and other satellite communication systems. Currently employed constraint length 7 rate one half convolution codes are used. A 0.5 db gain can be achieved if a constraint length 15 rate one half code is used.

The goal of this research is to investigate a VLSI solution to producing a high speed (10 Mbit/sec) Viterbi architecture for a large constraint length (15) convolution code. It is proposed to identify a unique architecture that minimizes the interconnect problem.

The first step will be to identify a unique architecture that can implement the Viterbi decoder with a constraint length of 15. The interconnection problem will be the largest to address. The proposed task would be to create a detailed functional simulation of the decoder system so as to ensure that the performance of the system is what NASA expect.

Here is a list of technical properties of the decoder:

1. Implements a Viterbi Decoder (maximum likelihood) for the rate 1/2 code:

$$G(d) = \frac{1 + d^2 + d^3 + d^4 + d^6 + d^7 + d^8 + d^{10} + d^{14}}{1 + d + d^5 + d^6 + d^7 + d^8 + d^{11} + d^{13} + d^{14}}$$

2. System consists of 128 or fewer identical chips operating in parallel.
3. Each chip will have approximately 276 I/O pins. A tentative signal pin summary is given below. Power pads will be added as available and required.

Pin Name	Count	Description
M	256	Metric and Traceback Signal Paths. Input/Output.
S	10	Winning metric Select. Some Input/Some Output.
Clock	1	System Clock. Input.
Q	2	Data Out. Tri-State.
ResetN	1	System Reset and Initialization Control. Input.
D	3	Data Input. Input.
NoLock	1	Data Sync Not Acquired. Output.
Config	2	Configuration Serial Data path.

4. The maximum data rate for chip to chip communication will be 35-45MHz.
5. The system clock for the decoder will be 35-45MHz.
6. Input data will be supplied at a 20MHz rate, three bits at a time. Incoming data is encoded in normal binary coding to represent eight quantization levels (0-7). It is assumed that 0 corresponds to a noiseless logical ZERO and 7 corresponds to a noiseless logical ONE.
7. Individual branch metrics are calculated as the absolute value of the difference between the expected noiseless values and the actual received values. These are three bit quantities.
8. The effective size of the history buffer for path traceback will be 70 or more bits deep.
9. The smallest metric encountered will be calculated for purposes of metric re-normalization and signal lock determination.
10. The decoder will automatically determine the proper bit lock based upon the metric values.
11. The individual metrics will be represented as 10-12 bit quantities. Attention will be paid to arithmetic circuitry to insure overflow cannot occur.
12. Maximum supported Information rate of: 10 Mbits/Second.

Proposed Budget

Engineering	\$50,000
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9.3 Lossy Data Compression

Lossy data coding research at the MRC has centered on developing waveform based coding techniques. Algorithms under consideration include the discrete cosine transform (DCT), discrete wavelet transform (DWT), and maximally decimated multirate filter banks (MFBs). The wavelet transform and multirate filter banks are known to outperform the discrete cosine transform by reducing coding artifacts in decoded data. However, the DCT is a very well understood algorithm that can be implemented in hardware with a relatively low cost. The DWT and MFBs are still in the research stage and in general have higher hardware implementation costs.

The data compression research will explore the theory and implementation of modern waveform coding techniques. Theoretical tasks ahead include applying these algorithms to lossless data compression and incorporating the Rice algorithm with adaptive versions of these coders for lossy data compression. Adaptive differential pulse code modulation (ADPCM) is being implemented for the flight lossless data compression chip in design for Landsat 7 with the intent of providing a fixed bit rate and is not optimized for best compression ratio. A higher compression ratio can be attained at the expense of a variable bit rate. Research into this use of ADPCM with Rice and minimizing the variable bit rate problem is planned. Finally, research will continue looking at VLSI implementation issues for all of these coders. These ideas are also well suited for video data, if there are needs for this.

Proposed Budget

- **Research Faculty \$50,000**

10 NASA Secondary Teacher VLSI Program

Abstract

An experimental education program was initiated in the summer of 1991 by NASA to expose secondary teachers to modern VLSI technology where the teachers designed VLSI chips. A plan is proposed that provides a transfer of digital technology into the high school system. The approach and preliminary results of this new program are presented in this paper.

10.1 Introduction

The NASA Space Engineering Research Center (SERC) specializes in the design of full custom Very Large Scale Integrated (VLSI) circuits. The SERC has delivered over two dozen different customized high performance VLSI processors to NASA, Lawrence Livermore Laboratories and several private companies such as Hewlett Packard and Ampex Corporation.

The first NASA Institute Workshop for Secondary Science and Math Teachers was conducted during the summer of 1990 to introduce top high school physics and mathematics teachers to basic electronics and digital logic. In 1991 and 1992 sixteen additional teachers were invited to participate in the same one week course. In 1991 and 1992, sixteen teachers who had participated in the first course program were invited to design VLSI test chips. Also in 1992, ten of the original teachers (those who participated in the previous two years) returned to campus to begin to prepare a program that would incorporate digital technology into the high school physics program.

10.2 Digital Design Course

The purpose of the one week program was to expose the teachers to fundamentals of digital logic design. This enables the teacher to use modern technology in teaching physics and provides insight into a rapidly changing scientific area. Teachers from the first course are using their new electronic skills to have their students design electronic measurement devices that are used to verify physics fundamentals.

The topics covered were during this one week course included:

- Digital logic and design with Small Scale Integrated (SSI) chips
- MOS transistor semiconductor physics
- MOS electronics for digital circuit design
- VLSI graphics editor
- Digital logic laboratory

- **Electronics projects laboratory**

The teachers were provided with a kit of all of the parts used in all of the laboratories that they could take home with them. Care was taken in the selection of parts to insure easy availability even in small quantities in their home communities. Both Complementary Metal Oxide Semiconductor (CMOS) SSI circuits and TTL circuits were used. CMOS was chosen, where possible, so teachers could power their circuits with 9 volt batteries for use in high school projects. Other projects presented include devices that are not available in CMOS. The laboratory projects include base gate operation, a timer/counter display circuit, photo gates, a simple logic probe design, a voltage regulation circuit for low cost power supplies and a bi-polar transistor identification (npn vs pnp) and test circuit.

10.3 VLSI Design Program

While the goal of the one week program was to introduce digital logic technology, the four week workshop exposed the teachers to most facets of VLSI design. The teachers identified their own projects and completed the design and layout during the four weeks.

The teachers performed the following engineering tasks:

1. Defined and specified the project.
2. Created the logic design for their chip.
3. Executed a transistor logic simulation and verified that the results were correct according to the chip specification.
4. Performed timing analysis on the chip.
5. Created the transistor level description of the logic design with a graphics editor.
6. Verified that the layout was design rule error free and matched the logic description of the circuit.
7. Prepared test vectors for the chip upon fabrication.

The chips were submitted to MOSIS for fabrication.

10.4 Summary of VLSI Projects

Encoder and Decoder

Craig A. Pedlar	Charles Wagner
Oak Harbor, Washington	Richland, Washington

Our project was to develop a decoder that would take logic inputs (binary code) and convert them into electrical impulses that would appropriately activate a digital device called a "seven segment display". An encoder was used to convert different logic inputs (sent by on-off switches) into a binary code, and then (a) displaying the binary code with LED's and (b) converting the binary code back into the inputs needed to activate the "SSD". Finally, an intermediate circuit was designed to add the outputs of two encoders, one decimal and one hexadecimal. This design was completed and successfully tested, both in NOVA (the logic simulator) and PIGLET. Fabrication and further testing will be accomplished in the future.

Latched Divider/Counter

Dave Aiken	Lynn Taylor
Genesee, Idaho	Ogden, Utah

"LDC" or Latched Divider/Counter (a.k.a. Lynn and Dave's Chip) A Glorified Stopwatch. The divider portion of our chip will take a 3.58 MHZ signal from a commercially available color TV oscillator and reduce it to a 0.001 second signal. The counter portion will tally 0.001 second pulses up to 999.999 seconds and output to six binary to decimal converters connected to six seven-segment displays. The entire chip is set and reset externally with start and stop signals provided by external photogates.

Motion Detector

Charles Martell	Bill Kemp
Portland, OR 97212	Spokane, WA 99003

A battery powered 8 photogate timing system to for outdoor use in analyzing the motion of runners was developed. The study of motion and the concepts of displacement, velocity, and acceleration is a fundamental study in physics and the opportunity to do this outdoors using the students own motion, would add much to a curriculum. The basic idea is that the first photogate turns on the timer and when each photogate is tripped, the time from the beginning to each photogate is stored. By the time all 8 photogates are tripped, 7 times will be available for Motion study. The system is designed to be flexible to be used as an all purpose timer in many different lab activities.

Sequence Analyzer - Academic Quiz Bowl

Mike Gantz	Larry Oval	Fred Burton
McCall, Idaho	Yakima, Washington	Nampa, Idaho

We designed a chip that would function as a sequence analyzer, specifically as a device to perform in an Academic Quiz Bowl competition. Even though there are a few devices on the market that allow one signal (team A) to block signals from other teams (teams

B,C,D) and then display a light, we felt that more flexibility was desired. Our design allows up to 4 teams (with any reasonable number of students per team) to compete. The chip should be able to determine who responded and the order of response. This feature is needed because the current Quiz Bowl format the first team locks out all other teams. If the first team answers incorrectly, the system must be reset in order for the other teams to be able to answer. If all the other teams are holding their buttons down when the system is reset there is no way of determining who is actually 2nd, 3rd, or 4th.

Linear Timer
Larry Volkening
Moscow, Idaho

One educational theme in many science classrooms is teaching students how to detect rates of change as fast as possible and to have students analyze data in as meaningful way as possible. If a student was given the means to detect events beyond the level of the five senses and beyond nominal logic patterns, then abstract thinking skills become a matter of course and not a topic of curriculum. Such is the function of my microprocessor. It is a linear and/or rotational timer engine that is used to clock fine voltage changes resulting from sensor changes in fields such as, light, sound, magnetic, and/or electrical fields. The readout is in binary code in order to reinforce the 'on/off' concept and counting patterns. The student must 'become' part of the chip by acting as a decoder. The standard clock input is 3.58 MHz with several ports for other inputs or readouts to allow for quick changes in clock input and partial clock readings as events were progressing.

10.5 High School Digital Technology

The set of 10 teachers who had been involved in the above courses were invited back to campus during the summer of 1992 to discuss the means to introduce digital logic technology into the high school program. The consensus opinion is that digital technology in the high school physics program can:

- Motivate a large spectrum of students, not only the advanced student but students who may pursue a VO-Tech career.
- Introduce digital technology to students who will face a computerized world thereby enabling an understanding of important aspect of living in a modern society.
- Create excitement and interest in being exposed to new technology thereby increasing an interest in learning more science and technology.
- Expose the student to a valuable tool used in work and recreation.

A course outline and several chapters were created that identified the subject areas to be incorporated in a high school program included:

- Boolean or switching theory
- Basic logic gates
- Elementary circuit synthesis

In addition to the course material, laboratories were proposed to illustrate the theoretical material.

One key feature of the course material is that advanced mathematics is not a prerequisite. Therefore, the course material can be offered to a set of students with a wide range of backgrounds and skills.

In addition to curriculum development, a program was proposed to bring the new technology to the public school system.

- Networks of classes to train teachers in new technology, initially offered at one location
- Regional followup meetings where teachers can share experiences and new ideas
- Electronic mail to help with specific problems and communication
- Equipment for the classroom include:
 - PC CAD systems
 - IC's for logic laboratories
 - Power supplies and bread boards

At this writing, this program is not funded and sources of support are being sought.

10.6 CHIPS (Chips Help Invigorate Students)

Following is a result produced by the teachers involved in addressing the means to introduce digital technology into the high school curriculum.

The Problem

Current educational reform methods do not allow for students to become true partners of applications technology, especially in the context of microelectronics. Students are rarely exposed to the fundamentals of digital logical design.

Discussion of the Problem

One main goal of educational reform is to infuse into curriculums problem solving logic from conceptualization to solution. Yet, many educational reforms are versions of the "updating" concept. Problem solving methods are being taught in the frame of mind that hands-on use of microelectronics will naturally develop higher thinking skills. Students and teachers are taught how to use microelectronics without knowing why microelectronics works or how logic is applied in designing a microcircuit. And as long as there is room for one error in analysis, a problem becomes invalid.

Higher thinking skills should involve the teaching of students to become visionary thinkers, creative problem solvers, logical analyzers of knowledge, creators of new knowledge and individuals able to appreciate applications technology. If students and teachers are to fully realize these goals, they must become part of the process of technology beyond the application of a black box. They must not be held hostage to the directives of a microcircuit black box or a computer interface. This major concern still exists in regards to the argument of teaching math using calculators.

Analyzing the Problem

The problem is the result of years of allowing the education process to lag far behind the technology applications process. Dependence on solving problems has become so far ingrained in the black box mentality, logical reasonable thinking skills have become a lost art in many curriculums and at many age levels (K-12).

The education process needs a quantum jump into the 1990's just to begin teaching students methods used to meet the needs of the next 20+ years. The jump will require three questions to be answered:

1. How does an educator bridge the gap between yesterday's technology applications and today's technology applications, especially in the areas that are seldom referenced in textbooks or typical lab activities?
2. How does an educator acquire current equipment, materials, and training?
3. How does the classroom become a place where the materials, methods, and instructor are constantly revitalized to new concepts at the same pace as technology is being applied to the world outside the classroom?

These questions will never be resolved until the rates of educational change match the rates at which technology is applied to solve problems beyond the classroom. And, if the two rates continue to diverge at an increasing rate, the technology gap may never be closed. If teachers and students are to appreciate the dreams, desires and goals of mankind

in general, changes must be made and they must be made in a manner to ensure continuity.

Developing a Solution to the Problem

The methods and logic used in microelectronics research and design can act as an ideal host vehicle to better understand conventional basics as well as implement new concepts and new technologies into the curriculum. The process needs not to be age level based either. Logical approaches to problem solving can be applied through out the total K-12 curricula.

This is a systems approach to education. Inherent in this approach a concept of revitalization becomes a natural outcome. A 'living system' develops where old concepts are explored and utilized via the logic of microelectronics applications. Example, a new form of student involvement in mechanics is evolving. Through redesigning computer chips applications, it is possible to alter automotive performance. Years ago, similar classroom content evolved based on the operation of carburetors.

The Problem Solution

Teachers and students must be made to feel it is a natural to design a microelectronic device to help solve a problem as it is to pick up a pencil or search out a formula. Specific examples of the basic fundamentals of microelectronics as listed below must fit into the curriculum and be applied as needed towards solving of problems.

- Boolean Logic
- Gates and Transistor Logic Sequence
- Chemistry Technology Considerations
- Quantum Level Considerations
- Clocking and Timed Event Applications
- Computer Simulation Programming
- CAD Technology
- Fabrications Methods
- Data Interpretation
- Scientific Method Applications
- Beginning Basic Bread Boarding

10.7 Summary

Many undergraduate Electrical Engineering students in the USA are not exposed to VLSI design at this same level. Moreover, the teachers were exposed to state-of-the-art CAD tools, the same used by engineers in industry. The teachers left the workshop feeling that they were close to the edge of technology.

The workshop's instructional staff included professors, NASA VLSI engineers, graduate and undergraduate students working in the SERC. The chips are to be submitted to MOSIS for fabrication after which the finished products will be returned to their creators to be put to use performing tasks ranging from acceleration and velocity studies for physics classes to response timers for Quiz Bowl competitions.

The teachers plan to introduce this technology into their classrooms at various levels from the ninth through the twelfth grades. They see VLSI technology as a means to excite a broad spectrum of high school students.

In summary, this VLSI program was viewed as a great success by the SERC staff and the teachers themselves. A great deal of excitement was created with a strong desire to use this technology to make a difference in the secondary science and mathematics programs.