Transputer Based Control System for MTLRS

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Introduction

The Modular Transportable Laser Ranging Systems (MTLRS-1 and MTLRS-2) have been designed in the early eighties and have been in operation very successfully since 1984. The original design of the electronic control system was based on the philosophy of parallel processing, but these ideas could at that time only be implemented to a very limited extent. This present system utilizes two MOTOROLA 6800 8-bit processors slaved to a HP A-600 micro-computer. These processors support the telescope tracking system and the data-acquisition/formatting respectively. Nevertheless the overall design still is largely hardware oriented. Because the system is now some nine years old, aging of components increases the risk of malfunctioning and some components or units are outdated and not available anymore.
The control system for MTLRS is now being re-designed completely, based on the original philosophy of parallel processing, making use of contemporary advanced electronics and processor technology [Beek, 1989]. The new design aims at the requirements for Satellite Laser Ranging (SLR) in the nineties, making use of the extensive operational experience obtained with the two transportable systems.

Design goals

Major considerations followed in the design are to bring down the operational costs, to ensure full capability for all present and future SLR satellites and to facilitate future modifications and alternative applications through a highly structured and modular approach.

I. Optimize cost of operations

Deploying SLR systems is quite expensive, in particular in transportable mode. A modern design aiming at minimizing these costs, must minimize crew size, increase the mean-time-between-failure (MTBF) and facilitate trouble shooting and repair.

a. Minimize crew size

The default mode of operation will be fully automatic. This means that the system will initiate and perform all basic tasks, e.g. maintaining satellite alert information, ephemeris calculation, initiate and perform calibration and tracking procedures, data screening, Normal Point calculation and data mailing. The routine task for the operator (if any) will be to monitor system performance and to respond to problems. Manual mode of operation is always possible through operator intervention.

b. Reliability

Increasing the MTBF will be primarily accomplished through defining a maximum of all functions in software, running in a multiprocessor parallel architecture. The remaining hardware will be built from high quality, highly integrated components, including Programmable Gate Array (PGA) logic. Integrated components also allow a great deal of miniaturization.

c. Self-diagnostics capability

Diagnostic tasks running concurrently with the control tasks will enable rapid detection and localization of problems. Parallel processors are very convenient for hosting these functions.

d. Modular hardware design

The hardware is designed with an optimum number of printed circuit (PC) boards. Same processor-functions at different locations use identical PC-boards. Different application-functions are realized with a minimum number of different PC-boards. Interface-functions are accomplished by separate PC-boards in order to optimize hardware portability. Most spares will be available at PC-board level which enables rapid replacement, reducing system down-time under field conditions.

II. All-satellite capability

a. Satellite altitude

This decade a variety of high and low SLR satellites are or will become available. Typical extreme altitudes are ARISTOTELES (200 km) and METEOSAT (geo-stationary). A design goal is to eliminate any logical restriction to the satellite range in the control system (e.g. by accommodating time interval measurement and event timing).

b. Satellite interleaving

Because the system will be designed for automatic ranging, the implementation of decision schemes in software for interleaving observations to different satellites will be relatively easy.

III. Flexible design

The design of the control system must simplify future modifications in view of new or modified requirements as well as implementation of more advanced technologies. This calls for a highly structured design in software and hardware, which may also enhance the portability of the design to other SLR stations, with different hardware environments.

a. Adaptation to modifications

Hardware. The general electronic design is separated into three major types of functions: 1. interfaces, 2. applications and 3. processors. These different types are physically separated in PC-boards which are individually exchangeable. The hardware uses PGA logic, which can be easily modified (by software).

Software The RT-software system is strictly separated into three independent layers: 1. global (functional), 2. device dependent, 3. interface dependent. In this way, modifications can be implemented locally in the related module at one layer, without affecting other layers.

Because of this high level of structurization it is feasible to implement this design in SLR systems which are quite different from the MTLRS concept, with a minimum of

modifications, primarily in software.

b. Expanding processor capability

If new requirements dictate additional computer power (e.g. RT-filtering, Frame Grabbing) this capability can be easily implemented in the structured design by adding standard processor boards hosting additional software tasks. To enable implementation of different types of (parallel) processors than the transputer which has been selected in the present design, all software is written in ANSI based high-level languages and no RT-program modifications have to be made because the 3L-compiler [3L] supports different processors.

c. Highly manufacturer independent

Custom made hardware usually increases the dependence on particular manufacturers. This is avoided by full restriction to standard bought-out components and self-designed PC boards.

The parallel processor set-up eliminates the necessity of selecting a vendor dependent RT operating system and thus ensures the flexibility of adopting any brand of (future) parallel processor. In the current design the INMOS transputer (see below) has been selected because of its early availability and its capabilities. Any future transition to another parallel processor is possible and will basically only require the exchange of the ***T805*** credit card size processor board.

Lay-out of the design

I. Hardware

In SLR the great progress in (opto-)electronics of the last decades has been applied to aspects such as detection, laser technology and timing, but seems to have largely by-passed the issue of Control System design. Here state-of-the-art electronics is introduced in the MTLRS Control System, resulting in a modular design with a high level of reliability, miniaturization and flexibility.

Probably the most dominant feature in the design is the application of a parallel processor architecture. This choice supports most of the design goals in a unique way, in particular the issues of modularity and of adaptivity to future requirements for extended computing power.

The INMOS transputer

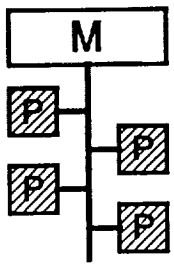

Fig 1

Parallel-processing computers [BYTE nov '88] can be divided into two basic architectures; the shared-memory multiprocessor (fig. 1) and the multicomputer type (fig. 2). All existing microprocessors can be used in the first architecture which will be limited in practice to about 4 processors due to the so called "von Neumann" bottleneck. This bottleneck arises when one processor reads or writes to the shared-memory while the other processors have to wait during this time till the "shared-memory bus" is free! Only few processors like the INMOS T800 transputer family [INMOS 1989] and the Texas Instruments TMS320C40 [TMS User guide] can make an optimal use of the multi-computer architecture because these processors possess high

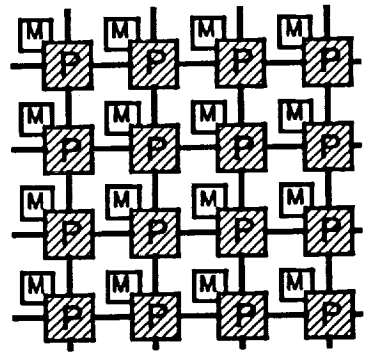

Fig 2

speed communication ports besides their standard address and data busses. Through these ports (links) the processors communicate with each other in a network where each processor possesses its own memory and thus eliminating the von Neumann bottleneck. In a practical multicomputer network the number of processors can be almost unlimited.
The INMOS transputer family consists of T2.., T4.., T8.. and T9... processors supported by link-crossbarswitches and periferal link-adapters. All INMOS processors are equipped with 4 links. Each link consists of one serial transmitting wire and one serial receiving wire both having an unidirectional speed of 20 Mbaud. If a link sends and receives data at the same time, the total data transport will be limited to 23.5 Mbaud/link. The T9000 will be available at the end of 1992 and has a peak performance of 200 MIPS and 25 MFLOPS with link speeds up to 100 Mbaud.

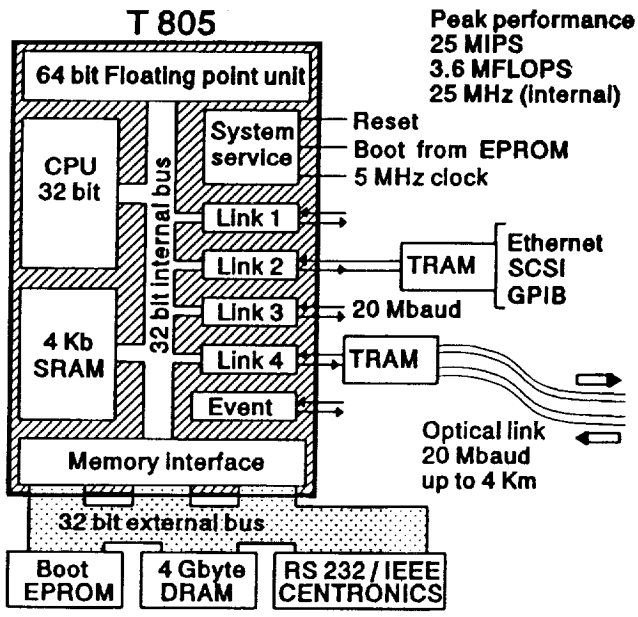

Fig 3

For the MTLRS Control System the T805 has been selected and is running at an internal clock speed of 25 Mhz giving 25 MIPS and 3.6 MFLOPS peak performance. The external 5 Mhz clock is internally multiplied by 5. Fig. 3 illustrates how the processor can be interfaced to the outside world in a flexible way. The present Control System is designed around a minimum of 5 transputers T805 which are interconnected through their links. A link is connected to a server-program running on a host-PC and through this link all the different programs are distributed through the network and loaded to a particular transputer. Each program is started automatically after it is loaded onto the destination processor. The design makes no use of the boot-EPROM facility but this makes the processor also very powerful for embedded designs. The word TRAM is an abbreviation for TRAnsputer Module which is an off-the-shelf interface board delivered by several manufacturers.
For parallel processor networks the software can be programmed in various ways; one task can be cutted into pieces which run in parallel at different processors, different tasks can run in two or more processors so that each processor runs a different task. Also multitasking in one processor can be programmed in a partly parallel way because the T805 can perform processes like cpu- operation, link-communication, timing and memory-IO concurrently. This means that while e.g. one task is busy with link-communication, the cpu is free for other tasks, scheduled in a sequential way following task priority. When a task consists of a number of processes, running concurrently in different processors, process-synchronization can be accomplished by the use of channel I/O (inter process data exchange) and semaphores.
Part of the internal CASH of 4 Kb SRAM is used to hold all registers for up to 99 different tasks and internal processes. If more than 99 modules are running concurrently, external DRAM is also used to hold registers. In contrast to conventional processors where the cpu has to share time to all processes, the T805 is doing this partly parallel which leads to a much higher performance.

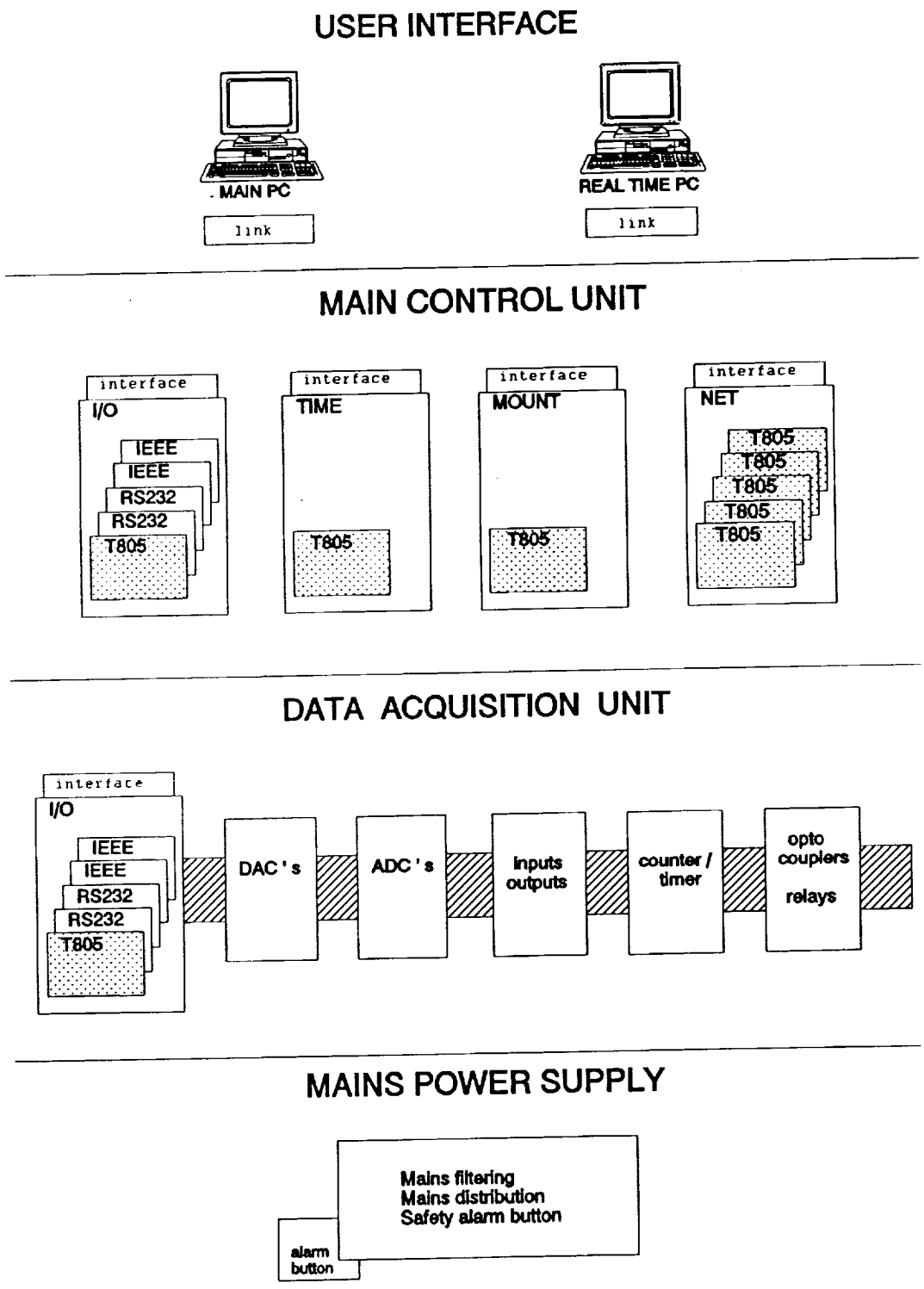
USER INTERFACE
MAIN PC
link
REAL TIME PC
link
MAIN CONTROL UNIT
interface
I/O
IEEE
IEEE
RS232
RS232
T805
interface
TIME
T805
interface
MOUNT
T805
interface
NET
T805
T805
T805
T805
T805
DATA ACQUISITION UNIT
interface
I/O
IEEE
IEEE
RS232
RS232
T805
DAC's
ADC's
Inputs
outputs
counter /
timer
opto
couplers
relays
MAINS POWER SUPPLY
Mains filtering
Mains distribution
Safety alarm button
alarm
button

Fig 4

The hardware lay-out

The hardware system can be separated into four major units, the user interface, the main control unit, the data acquisition unit and the mains power supply (fig. 4). It consists of several printed circuit boards, which largely demonstrate the modularity of the design and make it flexible to future modifications.
The basic board is the processor board ***T805***. On this creditcard size board the T805 transputer is placed, which is dedicated to parallel processing (see above). In addition this processor board contains 4 MByte memory, a special reset system for checking that the processor is still alive (EMI protection) and four 20 MBaud serial link drivers.
Other creditcard size boards in the system are ***IEEE-488*** and ***RS-232*** interfaces for connection to standard devices. These creditcard size boards are daughter boards to the extended eurocard size boards of the Main Control Unit and the Data Acquisition Unit.

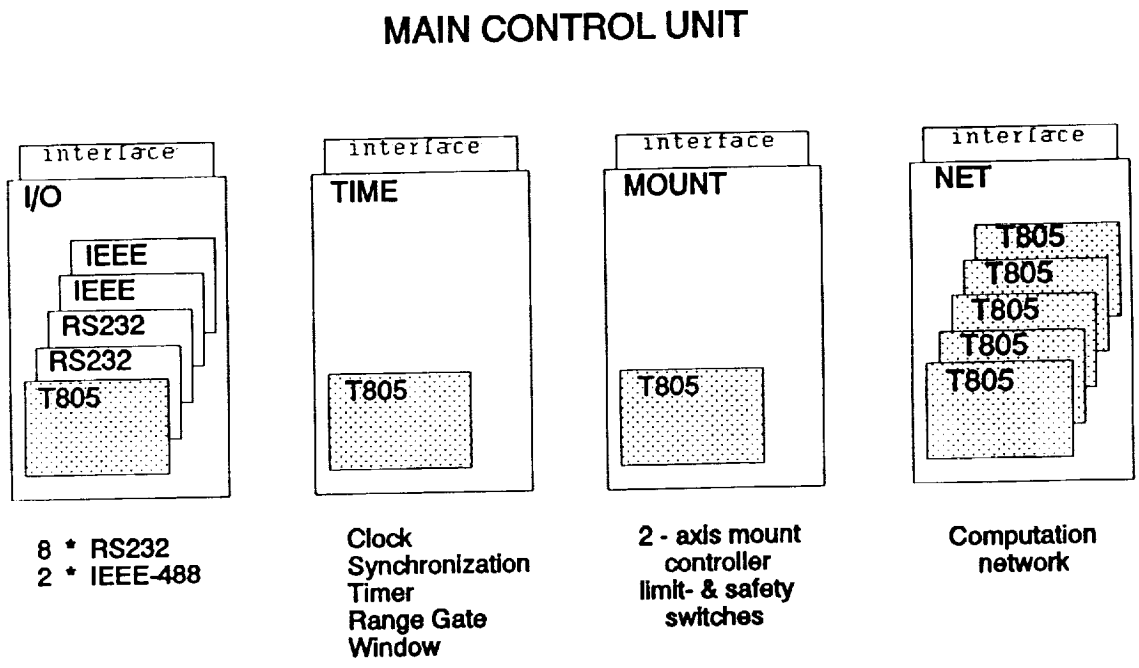

Fig 5

The ***Main Control Unit*** (fig. 5) is made up of four extended eurocard size boards:

1) the ***I/O*** board for connecting the processor to IEEE, RS-232 devices.

2) the ***TIME*** board for all time dependent tasks:
   - 4 channel event counter (low accuracy 20 ns),
   - range gate programmable generator (400 ps one shot accuracy),
   - window programmable generator (20 ns resolution),
   - programmable generator/synchronizer for the shutter, independent from window,
   - RT-clock with battery backup,
   - programmable synchronization for all required signals (e.g. laser firing).

   The ***TIME*** board requires 10 Mhz and 1 pps input signals.

3) the ***MOUNT*** board for driving a 2-axis telescope. The specifications for both axes are:
   - 32 bit position and 16 bit velocity and acceleration controlling,
   - three 16 bit coefficient programming for PID filter,
   - DC and DC-Brushless motors driving,
   - position and velocity mode of operation,
   - interface for quadrature incremental encoder with index pulse,
   - absolute encoder up to 32 bit,
   - limit-, safety switches, etc. ports,
   - joystick connection,
   - nonvolatile RAM for storing position, offset, etc. during power off, without battery backup.

4) the ***NET*** board with a minimum of one processor board with the possibility of extending computer power up to five processor boards. Additional ***NET*** boards can be implemented for expanding the network even further.

Instead of one big backplane interface, four individual backplane ***interface*** boards are designed. The design of each small backplane is dedicated to the typical hardware application, e.g. dependent on the type of encoders etc.
Each backplane can easily be modified to different input signal levels e.g. negative, positive, NIM, TTL, 50 Ω, ...

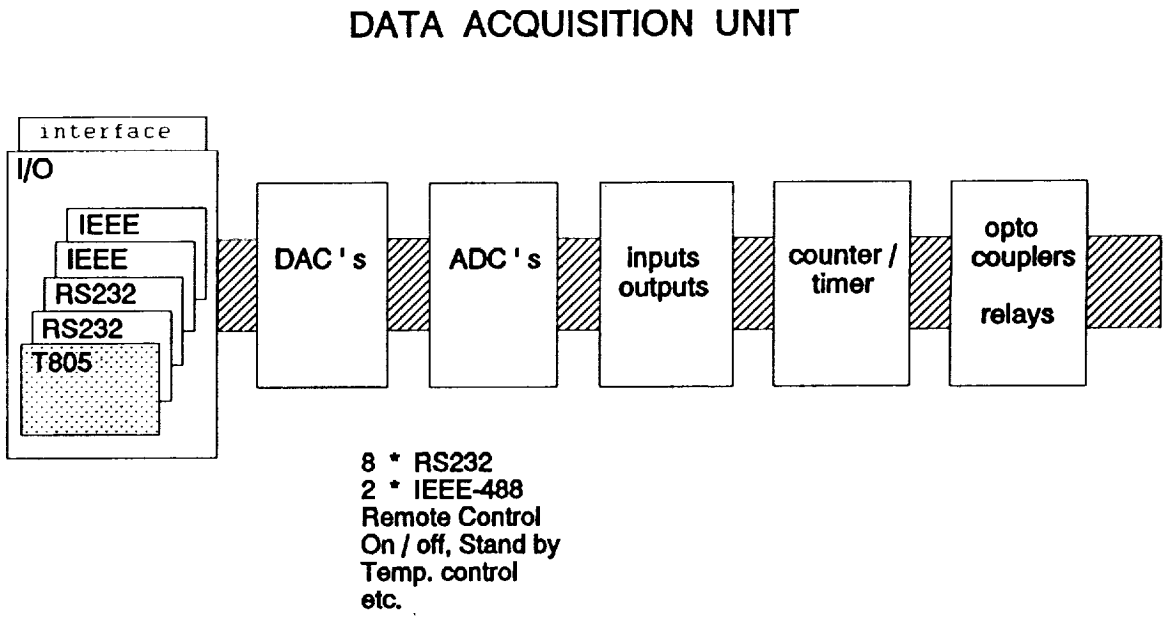

Fig 6

The ***Data Acquisition Unit*** (fig. 6) will be used for controlling additional hardware for the purpose of automation e.g. DC-motors, stepper-motors, temperature control, contacts checking and on/off-switching of equipment. It consists of an ***I/O*** extended eurocard size board which is identical to the one in the main control unit, together with several Data

Acquisition boards like:

- 12 bit D/A-converter (multiplexed for 8 outputs) with programmable range and offset.
- 12 bit A/D-converter (multiplexed for 8 inputs) with programmable range, offset and auto-calibration.
- 24 parallel input/output ports.
- Counter/timer for controlling counting/timing functions.
- Galvanic separation by opto-couplers and solid state relays.

The ***User Interface*** (fig. 4) consists of two identical 486 Personal Computers (PC) which are linked to the transputer network by means of 20 Mbaud ***link*** extension boards located in each PC. At this level the system can also be connected to Local and Wide Area Networks by adding standard interface boards to the PC-ISA bus, utilizing standard protocols.

Finally the ***Mains Power Supply*** (fig. 4) is designed for distribution, switching and filtering mains. It also features an alarm button for safety.

II. Software

General aspects

The computer configuration includes a transputer network and two identical PC-486AT's, the ***Main PC*** and the ***Real-Time PC***, each connected to the transputer network by a so called 'link'(fig. 4). On both PC's the operating system MS-DOS is running together with the highly efficient and friendly Microsoft WINDOWS which is a widely accepted industry standard graphical environment for PC's. In the transputer network the RT-software is running without any operating system. On both PC's the WINDOWS TRANSPUTER FILE SERVER is running. The ***Main PC*** hosts the off-line software and is used for data storage. Tasks like: site installation, preparing predictions, real time processes, data screening, normal point calculations and data mailing are initiated from or performed by the ***Main PC***. The ***Real-Time PC*** interacts with the ranging process as a terminal through the on-line Real-Time (RT) windows transputer file server program, supporting graphics capabilities for the transputer network during all real time processes like: satellite ranging, target calibration, telescope alignment and diagnostics. Through the ***Real-Time PC*** the operator interacts with all ranging related processes. The transputer network is built around several transputers where the actual RT-software is running in order to directly control the hardware. Modification of (default) input parameters for the various modules by the operator is based on WINDOWS dialogue boxes and menus which are on both PC's supported by extensive help information. In case of malfunctioning of one of the PC's, the software is designed to run on one PC only, with minimum inconvenience to the operator. Thus each PC is a back-up unit for the other one.

The off-line software

This software is largely based on the original MTLRS system and will be updated for compatibility with the PC-hardware platform under MS-DOS. The software will be embedded in the WINDOWS graphical environment. Error handling is supported by supplying help information and by allowing operator intervention in run-time whenever feasible. Primarily the new software package has been re-written in C, whereas individual existing modules are kept in FORTRAN-77, callable from C-programmes. Both the C- and the FORTRAN coding are based on to the ANSI-standard to ensure maximum portability of the software. All data files have been

defined in ASCII-format, unless specific requirements dictated the use of a binary format.

The RT-software

The transputer software system consists of a set of communicating processes, logically combined in functions. To make the software usable for other ranging systems and to facilitate future developments, the software has been structured into three layers:

a. the GLOBAL, SLR SYSTEM independent software
b. the DEVICE or data format dependent DRIVER software
c. the INTERFACE type dependent DRIVER software

Diagnostic capabilities are integrated in all three layers of the RT-software and are running concurrently by default or can be activated to run concurrently.

a. Global system

The global system includes all functions of the present MTLRS RT-software. The current MTLRS limitations concerning the observation range, the correction domain and the fixed firing epoch have been eliminated. Interleaving satellite ranging is made possible. To optimize this, the coarse pass prediction integration and the fine prediction interpolation are moved into the RT-software. This also allows firing epoch dependent range residual calculation to speed up data filtering. The meteo data and the UTC-GPS time are made available to the RT-time system.

b. Device driver

A device driver prepares the standard information from the global system to meet the requirements of the device and vice versa. It executes a device function by preparing a device command according to the operational device protocol and by calling interface drivers for data transfer. Device drivers are available for all external devices to be accessed by the global software.

c. Interface driver

An interface driver transfers the data from the transputer network through a hardware interface to each device and vice versa. No modifications are applied to the data. Interface drivers are available for each type of interface and protocol used by the external devices. Event interrupt processing is supported for devices which are capable of asserting the transputer event signal.

International design standard

Because of the structured approach to the design of this control system it is hoped that this activity will contribute to the establishment of an international standard for SLR control systems.

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