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Nomenclature

A	amplifier gain
Af	spectral-power noise density coefficient
a_H	Hooge parameter
AuGeNi	alloy of gold, germanium, and nickel
B	bandwidth
Be	beryllium
BLIP	background limited performance
C_1	input coupling capacitance
C_2	input ground capacitance
C_{GS}	gate-source capacitance
C_i	gate input capacitance
C_{ISS}	input capacitance to ground
CVD	chemical vapor deposition
e_n^2	square of the noise voltage
e^{-2}/nw	monolateral white-series-noise spectral power density of the amplifier
E_d	donor binding density
ENC	equivalent noise charge
f	frequency
FET	field effect transistor
FFT	fast Fourier transform
Ga	gallium
GaAs	gallium arsenide
Ge	germanium
g_m	transconductance
g–r	generation–recombination
H_f	Radeka and Rescia factor
I_D	drain current
I_{DS}	drain-source current
I_G	gate-leakage current
i_n^2	noise current squared
JFET	junction field effect transistor
k	Boltzmann constant
L	gate length
LPE	liquid phase epitaxy
MBE	molecular beam epitaxy
MESFET	metal extrinsic semiconductor field effect transistor
meV	milli-electron volts
MODFET	modulation doped field effect transistor
MOSFET	metal oxide semiconductor field effect transistor
n	current carrier density
N	number of carriers in the channel
n^+	heavily doped N-type region
N_a	acceptor density
N_c	density of states at bottom of conduction band
N_d	donor density
n-JFET	n channel junction field effect transistor
ns	nanoseconds
NS^2	noise slope squared
p^+	heavily doped p-type region
PAR	Princeton Applied Research, Inc.
pF	picofarad
q	electron charge
R_{DS}	static drain to source resistance
R_{ds}	dynamic drain to source resistance
R_s	source resistance
SRS	Stanford Research Systems
S	sulfur
S_f	spectral-power noise density
Si	silicon
S_I	spectral-noise power density
Si_3N_4	silicon nitride
S_{Vf}	voltage noise generator
T	temperature
V_B	bias voltage
V_D	drain voltage
V_{DS}	drain-source bias voltage
Vgs	impressed gate voltage
V_n^2	output noise voltage squared

Zn/As	zinc/arsenic
μ_n	electron mobility
ρ_{GR}	effective resistance of the gate area
ρ_0	1/f noise equivalent gate resistance normalized at f_0
ρ_i	resistance for the rth component of the g–r noise
τ	shaping time
τ_0	characteristic time constant
τ_r	time constant for deep-level trap causing g–r noise
ω	output noise voltage at angular frequency

Summary

The spectral noise characteristics of Aerojet gallium arsenide (GaAs) junction field effect transistors (JFETs) have been investigated down to liquid-helium temperatures. Noise characterization was performed with the field effect transistor (FET) (1) in the floating-gate mode, (2) in the grounded-gate mode to determine the lowest noise readings possible, and (3) with an extrinsic silicon photodetector at various detector bias voltages to determine optimum operating conditions. The measurements indicate that the Aerojet GaAs JFET is a quiet and stable device at liquid helium temperatures. Hence, it can be considered a readout line driver or infrared detector preamplifier as well as a host of other cryogenic applications. Its noise performance is superior to silicon (Si) metal oxide semiconductor field effect transistor (MOSFETs) operating at liquid helium temperatures, and is equal to the best Si n channel junction field effect transistor (n-JFETs) operating at 300 K.

Introduction

GaAs is an emerging semiconductor technology offering the advantages of low noise and high speed coupled with low-temperature operation and radiation hardness. Historically, there have been several investigations of GaAs MESFETs at liquid-helium temperatures because they are commonly used as microwave preamplifiers. There had been relatively little work done with GaAs JFETs until the advent of integrated circuitry on GaAs created a market for the product. The tests reported here were conducted to compare the noise characteristics of a few Aerojet-supplied GaAs JFETs to devices reported in literature: (1) lot 88091411-1A, device A5-7 (old FET); (2) lot 88091411-1A, device D3-8 (third FET); and (3) lot 88091411-1A, device C1-8 (second FET). The major differences among devices are the gate areas, which are $22 \times 50\ \mu m^2$, $52 \times 160\ \mu m^2$, and $88 \times 200\ \mu m^2$, respectively. A fourth FET was from lot 86120811-2, device A1, and may have had a gate area of $88 \times 200\ \mu m^2$. The exact gate area is unknown because the University of Arizona did not return the same FET we loaned them and we cannot be certain of the heredity of the FET.

Two production lots of n-JFETs were tested. Both used essentially the same structure and doping levels. The n-channel JFET was made by growing a 1.0-μm-thick intrinsic GaAs layer using molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate to isolate the channel from the substrate. A 0.3-μm-thick n-channel MBE conduction-channel layer was grown and doped with Si at $\sim 4 \times 10^{16}\ cm^{-3}$. A gate junction was formed by a 0.5-μm-thick p^+ overlayer doped with beryllium (Be) at $\sim 1 \times 10^{18}\ cm^{-3}$. Mesa etching was performed to define geometry and metalizations for gate and drain were applied. No surface passivation was incorporated. The device had an input impedance of $>3 \times 10^{12}\ mm^2$ (fig. 1). A description of the manufacturing process for the Aerojet GaAs n-JFET is in Goebel et al. (1992).

Testing

Testing consisted of measurements of important FET performance characteristics such as noise, gain, and signal-transfer function. The testing was conducted in an evacuated cryogenic test dewar with an infrared detector and appropriate optics and on a probe which could be inserted into a standard 30- or 100-liter liquid helium storage dewar. All testing was conducted in a laboratory environment. A large number of figures and devices were tested and table 1 shows their correlations.

Storage-Dewar Noise Test

A test was conducted on the JFETs prior to installing them in the test dewar. A socket was attached to one end of a 4-ft-long piece of thin-walled stainless steel tubing. Low-thermal-conductivity electrical wiring was run through the tube connecting the socket to a source resistor and power supply at the opposite end. The FET was plugged into the socket and the tube was inserted into the liquid-helium supply dewar. Noise voltage measurements were recorded at several different frequencies and were used as benchmark values for comparison when the FET was installed in the test dewar. We found no significant variations between the storage-dewar and test-dewar measurements. Therefore, this test became a valuable checkout procedure. The test dewar could not approach the cool-down speed and fast turn-around time that this method offered. The accuracy of the storage-dewar test was measured at the 2–4 $nV/\sqrt{Hz}$ level as described in the next section.

Also, in this test mode the signal-transfer function, or gain, was measured as a function of frequency. The results for two of the FETs at 300 K, 77 K, and 4 K are listed in tables 2 and 3. Using these data, the 4 K transconductance (g_m) and gate-source capacitance (C_{GS}) of the FET were calculated at 1220 μS and 8.8 pF, respectively.

Calibration of Noise Spectrum

A system calibration was conducted to determine the system noise versus frequency characteristics. All noise values were measured with an HP 3561A FFT signal

analyzer. A 1 kΩ metal film resistor was immersed in a dewar of liquid helium. Its resistance was measured to verify that there was a small temperature coefficient of resistance. The leads from the resistor were connected to the input of a Stanford Research Systems (SRS) SR552 low-noise preamplifier (fig. 2). The resistor provided the optimum low-noise-source resistance for the preamplifier, but, due to its cooled condition, the level of the Johnson noise it generated was well below the preamplifier threshold. Therefore, the system noise was set by the noise figure of the low-noise preamplifier. The spectral-noise characteristics of the system are shown in figure 3. These values are somewhat larger than those quoted by the preamplifier manufacturer. The SRS values were based upon a model of the amplifier, so our measurements of the actual performance indicate that the model underestimates the performance. To check the accuracy of the measurements, the Johnson noise of the same 1 kΩ metal film resistor at 300 K was measured, the calibration data were quadrature-subtracted from the 300 K data, and the resultant value was compared to the calculated value of Johnson noise. The two curves compared very favorably and are shown in figure 4. Note that in the test dewar the JFETs were operating at 7 K, while in the storage dewar tests they were operating at 4.2 K.

Test-Dewar Noise Test

The test consisted of the circuit (fig. 5) mounted in a small liquid-helium dewar. As before, the output of the FET source was connected to the SRS SR552 low-noise preamplifier, followed by a Princeton Applied Research, Inc. (PAR) 113 preamplifier for additional gain, and then to the HP 3561A FFT signal analyzer. Tests were conducted (1) in the grounded gate mode, (2) in the floating gate mode, (3) with the detector and detector-bias resistor grounded, and (4) in an operational mode with variable detector bias to determine the optimum operating point. Quadrature noise subtraction was not performed in the subsequent tests unless reported otherwise. This is because the lowest noise levels measured for the JFET are 50 percent larger than the SRS552 preamplifier noise at low frequencies. The lowest values are no more than 15 percent larger than if corrected by quadrature subtraction. Since the noise in the JFET is dominated by sources in the channel and not at the gate, no gain corrections have been applied to noise measurements.

Results

The testing is based upon the configuration of the gate mode. The grounded-gate mode is intended to measure the noise generator at the gate and is useful for modeling the equivalent circuit elements of the FET. The floating-gate mode is intended to mimic an idealized high-impedance infrared detector, but unfortunately introduces a large and unpredictable parasitic capacitance to other elements in the circuit. The test dewar was not properly shielded to take full advantage of this test. Testing with an active and relatively low impedance Si:Ga photoconductor demonstrates the signal transfer and operational noise characteristics which the GaAs n-JFET is capable of at cryogenic temperatures in real applications. Unless otherwise stated, the tests were conducted on the D3–8 FET.

Grounded-Gate Mode

The grounded-gate tests were conducted at 77 K at drain voltage (V_D) = 1.4 V, and at 7 K at V_D = 1.4, 3.0, and 5.0 V. During this series of tests, the unit achieved the lowest levels of noise that we achieved with these FETs. Representative data taken during these tests are tabulated in table 4.

The first test was conducted at 77 K at a V_D = 1.4 V. This test was to confirm the operation of the system and to collect some benchmark data. After verifying a correctly operating system, the testing progressed by lowering the temperature to 7 K. The 7 K tests were conducted at all three drain voltages, with the lowest noise levels occurring at the lowest drain supply voltage (table 4).

Figures 6–15 show the spectral noise curves for all of the test conditions. By comparing figure 6 and figure 8, the noise reduction (in overall level and in peak-to-peak variation) achieved by lowering the temperature from 77 K to 7 K is quite apparent at frequencies below 100 Hz (preamplifier gains have been removed).

Noise measurements of the A5–7 and the A1 FETs are summarized in figures 16–20. Note that the lower limit, or noise floor, ~10 nV/√Hz, is due to the PAR 113 input, not due to the FETs. This data predated the introduction of the SRS552 preamplifier. Measurements were made at a typical drain to source voltage V_{DS} = 3.8 V. The old FET shows significantly lower 1/frequency (f) noise operating at 7 K, for a source resistance (R_S) of 1 kΩ, than for higher values of R_S or equivalently lower values of drain-source current (I_{DS}). For all types of FETs operating at room temperature, 1/f noise can be suppressed by increasing the I_{DS}. There also appears to be a bump in the kHz region with the smallest I_{DS}, about which more will be said later, that arises from a "flicker" type mechanism generally attributed to trap filling and emptying. The A1 FET shows a trend of increasing 1/f noise with increasing R_S at 77 K, but shows very little change at 7 K except for the largest value, R_S = 10 MΩ.

Also at 77 K (fig. 18) there appears to be a kHz bump in the noise and none at 7 K. Note the A1 FET is anomalous because its noise at 7 K is larger than its noise at 77 K. The D3-8 FET produced the lowest noise results (fig. 20).

Floating-Gate Mode

It is sometimes reported that the floating-gate (ungrounded) test more accurately mimics a true high-impedance photoconductive detector than the grounded-gate configuration. To conduct these tests, the gate lead was disconnected from the detector and load resistor at the FET packaging gate lead. The tests were conducted at 7 K, at V_D = 1.4, 3.0 and 5.0. Data are tabulated in table 4 and summarized in figure 21.

With the floating gate, the noise level increased wildly in the lower frequencies, 0–100 Hz, and the characteristic 1/f slope was disrupted (figs. 22–24). This is due in part, if not entirely, to low-frequency noise pickup in the laboratory and is attributed to inadequate shielding. Mechanical excitation of the test dewar eliminated microphonics as a cause of this extra noise. The shape of the noise peaks and the levels were not repeatable from day to day, and would change during the day depending on the activity in the lab. However, when the spectrum out to 100 kHz is viewed (figs. 25–27) and compared to figure 9, it can be seen that the overall noise has risen by a much smaller amount. This extra noise or interference was not pursued to conclusion. A more extensive floating-gate testing sequence would be warranted to completely characterize the GaAs n-JFET for this application. Based upon our testing, the experimental configuration may be the limiting factor rather than the JFET.

Gate Grounded through the Detector and Bias Resistor

The test was reconfigured to ground both the Si:Ga detector (Infrared Labs, Inc.) and the detector-bias resistor instead of biased as shown in figure 5. These tests were conducted at 7 K, at V_D = 1.4, 3.0, and 5.0 and with no detector bias. The results are tabulated in table 4 and summarized in figure 28.

Since the gate of the FET was sensitive to the thermal noise generated by the detector and bias-resistor combination in parallel, the noise level was above the grounded gate level, as can be seen by comparing figure 9 to figure 29 or by referring to table 4. Also, the large and erratic fluctuations in the 0–100 Hz range that were prominent when the gate was floating, have disappeared and the 1/f slope has returned (fig. 30).

Operational Mode with Detector Bias

The final test configuration was a fully operational mode with bias applied to the detector. These tests were run at the previously selected values of V_D = 1.4, 3.0, and 5.0. With the drain voltage set at these values, the detector bias voltages (V_B) were 0, 0.5, –0.5, 0.75, and –0.75. Larger detector biases were not necessary to demonstrate functionality. All of the recorded data has been summarized in table 4 and figures 28 and 31–33 and noise versus frequency curves are shown in figures 34–48.

No prominent trend appeared in these data. At all values of V_D and with V_B = 0.5, it makes little difference whether the detector bias polarity is positive or negative, although there is some indication that negative values of V_B produce less noise at 1 Hz. However, at V_B = 0.75, the trend is for negative V_B to provide lower noise at frequencies below 100 Hz.

The increased noise level that occurs when the biased detector is in the circuit is attributed to radiation induced generation–recombination (g–r) noise in the detector. This was confirmed by placing a cold pinhole over the detector to reduce the radiation field by several orders of magnitude and resulted in reduced noise levels.

Some noise data were acquired while the dewar was warming from 7 K to 77 K (figs. 48–54). With the connected detector biased at 0 V and with pinhole illumination, below 25 K the noise level rose by about a factor of 2.5. With the gate grounded or floating no such trend was seen. Radiation induced g–r noise is then the implicated source of this extra noise. Consequently, in this test system the JFET preamplifier is fully capable of BLIP operation with the extrinsic silicon photoconductor.

Discussion

Much of the historical FET testing at cryogenic temperatures has consisted of evaluating available commercial products using a screening process rather than designing a device from the first principles intended specifically for cryogenic operation. Only recently has that technique changed in its focus. Advances in cryogenic infrared focal planes and computers have opened markets sizable enough to warrant the necessary investment in engineering and production time directed at cryogenic operational needs. Largely because of the dominance of silicon processing technology in the semiconductor industry, Si MOSFETs and JFETs predominate the available literature. Smaller volumes of reports have been generated for germanium (Ge), GaAs, and other more exotic materials like silicon on sapphire.

Rogers (1968) explored the use of commercial and experimental Si MOSFETs and GaAs JFETs at 4 K. All the problems that have plagued subsequent investigators of Si devices were noted, explored, and analyzed in his work. Si JFETs freeze well above 4 K, thus preventing channel conduction and useful operation. Cooled MOSFETs with a flat frequency response are suitable for cryogenic preamplifiers. The substrates of Si MOSFETs freeze below 15 K even though the degenerately doped contacts retain high conductivity. At room temperature, the intended bulk conductivity in the channel gives rise to the device's drain current. MOSFETs rely upon this unintentional surface conductivity to maintain a useful channel current at cryogenic temperatures. In 1968, it must have been largely unanticipated that devices operable at 4 K with a MOSFET structure could be found.

The uncontrolled surface states that give rise to a secondary conductivity component do not freeze and were previously viewed as an undesirable defect of the technology. They also give rise to unwanted 1/f noise (Rogers, 1968). The advantage of JFET devices at room temperature is that they have channels buried in the substrate specifically to avoid the problems produced by this surface conduction component. In hind sight, Schrieffer's (1955) investigation showed that the mobility of carriers at the surface of a semiconductor can be as high as one quarter of the value found in the bulk and is highly dependent upon the transverse electric field imposed by the gate. However, the mobility of the surface carriers does not have the same functional dependence with temperature as the dominant bulk dopants. They have significantly lower activation energies and were not well investigated up to that time. Interestingly, Metal oxide semiconductor capacitors became an effective tool to study these states and remain useful to this date, not only for surface states, but for bulk states.

A further complexity arises as these structures exhibit a threshold voltage in the drain-source characteristic curves of any MOSFET device that is dependent upon temperature. It is now known how to moderate, but not eliminate, this effect down to 10 K by using low-threshold implants of boron (Tewksbury, 1981). N-channel and p-channel devices, which operate at room temperature in depletion and enhancement surface modes, respectively, become common enhancement mode devices at 77 K and 4 K (Rogers, 1968). With proper doping of the substrate, n-channel enhancement-mode devices can be designed to retain their threshold voltages down to 10 K (Tewksbury, 1981). The threshold voltage is controlled by the p^+ backside implant and substrate resistivity. Capacitance measurements indicate that ohmic operation of the channel is obtained at 4 K only when the gate overlaps the drain and source contact regions.

Last, but not least, are the hysteresis effects in the characteristic curves and are especially pronounced in n-channel devices. Devices with the least amount of hysteresis were found to be most suitable for operation at 4 K. An explanation of hysteresis is found in terms of filling and emptying of surface traps with time constants of seconds. P-type devices tend to have a smaller 1/f component cryogenically than do n-type devices, although both retain high-quality transconductance characteristics.

Since Roger's (1968) work, the only significant improvements in the cryogenic utility of Si devices have been the introduction of thermally isolated Si JFETs (Low, 1981) and infrared stimulated Si MOSFETs (Arentz, Hadek, and Hoxie, 1983). Qualitative improvements have been noted in the production of both types of Si devices. Si JFETs have been widely produced with audio frequency noise levels of only a few $nV/\sqrt{Hz}$ at 77 K. Si MOSFETs have been produced with noise levels at 4 K, only an order of magnitude larger in the 30 Hz range, while approaching the level of Si JFETs in the kHz range (Goebel, 1977). A full set of n-channel enhancement-mode MOSFET-circuit-model parameters for channel lengths from 2.5–8.5 μm and for temperatures ranging from 10–300 K derived from measurements of production-line devices has been published by Tewksbury (1981), but without a viewpoint oriented to the noise problem. The pursuit of lower noise levels at 4 K operational temperatures still requires the development of devices in alternative semiconductor materials.

As early as 1967, germanium JFETs were applied to cryogenic amplification of charged particle detector signals by Kelm (1968), Elad and Nakamura (1967), and Green (1968). While they never evolved into a commercial product line, they showed great potential as cryogenic amplifiers, thus renewing interest as recently as the 1980s (Arentz, Strecker, Goebel, and McCreight, 1983). The early investigations reported high values of transconductance, g_m = 7000 μS, at low temperatures and low noise levels in the MHz range, 0.7 $nV/\sqrt{Hz}$, and low equivalent noise charge (ENC), ~40 rms e^-. The latter investigation demonstrated the utility of Ge JFETs in the now classic electrometer amplifier, which incorporated the FETs as a cold front end operating down to 1.8 K. Unfortunately, in recent years in spite of its great potential and simplicity of manufacture, Ge FET technology has not advanced as much as GaAs. Potentially, if pursued along the lines required to use the lower activation energy material GaAs, modern epitaxial equipment could improve the room temperature behavior of Ge FETs, thereby reducing their relatively large gate leakage current when compared with Si FETs. This situation can only be attributed to market forces, as GaAs

is being investigated intensively for the electro-optics industry and for quantum-well structures. However, for infrared-detector applications, Ge potentially combines the large dynamic-voltage range of Si with the low-temperature capability of GaAs. While GaAs provides low-temperature capability, its dynamic range is currently limited to a few volts before breakdown voltage is achieved.

In figure 55, the 4 K grounded gate noise performance of the Aerojet GaAs JFET is compared with a J-230 Si JFET at 55 K, a TIXM12 Ge JFET at 4 K, and a ZK-111 at 4 K, each operating at 100 μW power dissipation. The noise levels of the other three devices are from Arentz, Strecker, Goebel, and McCreight (1983). The GaAs FET shows superior noise performance, even to the Si JFET above 10 Hz, and is only a factor of two noisier at 1 Hz. This is a remarkable accomplishment.

As long ago as 1961, GaAs JFETs were investigated with an eye to cryogenic operation (Jonschner, 1961, 1964). GaAs was chosen because bulk conduction carriers do not freeze completely until well below 2 K. However, GaAs technology was not pursued vigorously due to the meteoric rise of Si technology, largely because of the relatively simple implementation of Si technology at room temperature and its economical scalability. The large device structures necessary for low-noise operation at audio frequencies were not incorporated into GaAs MESFET design. This is largely the result of the well-developed ambient-temperature Si MOSFET and JFET product lines that are available. GaAs has been aimed at applications that can take advantage of the higher mobility available in this material. For microwave preamplifiers, higher mobility translates into increased frequency bandwidth. Furthermore, improvements in sensitivity can be realized by cooling the FET to 4 K, thereby reducing the Johnson noise associated with the transconductance term, $1/g_m$.

The Aerojet GaAs JFET is one of the first modern devices intended for the audio frequency region with the low temperature capability that is desirable for use with infrared photoconductors. It is free of the troublesome drain-voltage threshold and hysteresis effects that plague Si MOSFETs. We discuss some of the available literature on cryogenic operation of GaAs FETs.

In a very recent work, Alessandrello et al. (1990) demonstrated the operation of a GaAs MESFET model 3SK 164 and analyzed its performance as a charge-sensitive preamplifier. Operating at 4 K, the 3SK 164 displayed a reduction of two orders of magnitude in its 1/f spectral-power noise density (S_f) coefficient (A_f), where $S_f = A_f f^{-\alpha}$ and $\alpha = 1$. At the optimum bias point, transconductance was 6 mA/V, with an input capacitance of 5 pF and a relatively low power dissipation of 360 μW. The 3SK 164-M has a double-gate structure in which two separate gates are interconnected. They obtained an A_f value of 1.7×10^{-13} V^2/Hz at 77 K and 3.8×10^{-14} V^2/Hz at 4 K. The ENCs measured at 77 K and 4 K were 58 and 20 rms e^-, respectively. Using selected devices as components in a double-cascode circuit loaded with a bootstrapped current source, a low-noise high-gain bandwidth amplifier was built with a power dissipation of 10 mW. The amplifier could respond to a 1 m length of 50 Ω coaxial cable terminated at the sending end with a 20 nanosecond rise time when the detector capacitance was 35 pF.

The functional behavior with temperature (T) of the current carrier density (n), which gives rise to the drain current (I_D), is exponential and dependent on the bulk donor density (N_d) and acceptor density (N_a):

$$n = \left[\frac{N_c(N_d - N_a)}{2}\right]^{1/2} \exp\left[-\frac{E_d}{2kT}\right] \qquad (1)$$

Here, E_d is the donor binding energy, which for GaAs with Si and sulfur impurities is typically 6 meV, N_c is the density of states at the bottom of the conduction band, and k is the Boltzmann constant. Equation (1) gives rise to sufficient n at 4 K to maintain the I_D of the MESFET at a value of 0.6 mA, with $g_m = 6$ mA/V and $R_{ds} = 3000$ Ω.

The bulk conductivity (σ) of any semiconductor is related to the carrier mobility (μ) simply by the relation $\sigma = e\mu n$. Lee (1989) quotes values of E_d for Si, Ge, and GaAs of 50, 10, and 3 meV, respectively. So there is some variation in quoted values among devices in the literature depending upon which dopants are introduced into the bulk material during wafer processing. The temperatures at which σ attains its maximum value for Si, Ge, and GaAs are approximately 100 K, <100 K, and 60 K, respectively (Lee, 1989).

Alessandrello et al. (1990) analyzed the low-temperature noise in MESFETs as a combination of g–r noise in the bulk depletion region and 1/f noise from the drain current. The g–r arises from the impurities and defects which are more abundant in GaAs than Si. The 1/f component is modeled to arise from an addition of Lorentzians due to single traps as discussed by van der Ziel (1986). In addition there is another low-frequency-noise source originating at the interface between the conducting channel and the semi-insulating substrate. The known decrease in trapping time constant (τ_i) with decreasing temperature gives rise to a shift in the 1/f noise spectrum (the tail of the distribution of trapping time constants) to higher frequencies. Hence, the apparent reduction in noise-power spectral density in GaAs MESFETs with

decreasing temperature is consistent with the expression of the g–r noise arising from the effective resistance of the gate area (ρ_{GR}) in the form

$$S_{V_{gr}} = 4kT \sum_i \frac{\rho_{gr}(\tau_i/\tau_0)}{1+(2\pi f)^2\tau_i^2} \qquad (2)$$

As the temperature decreases, the tail of the distribution in τ_i moves to higher frequencies. At low temperatures in Si MOSFETs, the noise is dominated by surface trapping sites which display an increasing τ_i with decreasing temperature, thereby causing their noise performance to degrade. It was discovered very early (Williams and Thatcher, 1932) that equation (2) behaved as a 1/f spectrum in the high frequency limit. There has been considerable discussion in the literature concerning the appropriate expression for this type of noise. Discussions become confused because there are usually two separate 1/f noise generators to consider, the one in equation (2) and the one discussed below.

The 1/f noise generator has a spectral-noise power density (S_I) described by the experimentally deduced Hooge's law (Hooge, 1969):

$$S_I = \frac{a_H I_D^2}{fN} \qquad (3)$$

Here, a_H is the Hooge parameter, I_D is the drain current, f is the frequency, and N is the number of carriers in the channel. The 1/N factor has stirred considerable controversy since its introduction by Hooge, but for FETs it seems to be on solid observational ground (Hooge, 1990; van Vliet, 1991). When the FET is operated below saturation, Alessandrello's expression for the voltage noise generator (S_{Vf}) in series with the gate, referred to the input terminals, is

$$S_{Vf} = \frac{q\mu_n\alpha_H I_D V_{DS}}{g_m^2 L^2}\frac{1}{f} \qquad (4)$$

where q is the electron charge, μ_n is the electron mobility, V_{DS} is the drain-source bias voltage, g_m is the FET transconductance, and L is the gate length. Here, the scalable parameter is L. More L gives less 1/f noise. L is the important scalable dimension, rather than amplifier gain (A). That is why low-noise FETs have serpentine gate patterns. This is true not just for GaAs but also for Si devices.

Analysis of their measurements indicate that the total low-frequency noise is dominated by a 1/f noise generator, although it is conceded that several different mechanisms other than the one in the drain to source channel may give rise to the 1/f spectrum. So they measure the spectral power density (S_f) of the 1/f noise source in series with the gate, $S_f = A_f f^{-\alpha}$, with $\alpha = 1$, and quote A_f under various conditions. At audio frequencies, the g–r noise generator is overwhelmed by the 1/f noise generator in MESFETs and appears to be a Hooge type. The reduction of 1/f noise with decreasing temperature is attributed to the dominant temperature dependence of the electron mobility (μ_n). Furthermore, the 1/f noise is covariant with V_{DS}, which is consistent with the g–r theory of Lauritzen and Sah (1963) expressed in equation (4). Thus, Alessandrello et al. (1990) have biased the preamplifier at low V_{DS} near the linear region. Because they were unable to design the FETs, Alessandrello et al. (1990) could not identify the origin of the 1/f component. Later we will review other reports that were able to identify the origin of the 1/f component.

For a MESFET, where the g–r noise is dominated by equation (4), the gate length (L) controls the 1/f noise level as a $1/L^2$ factor. As mentioned earlier, the design of high-frequency-response preamplifiers requires little L for slight gate input capacitance (C_i). The factor of merit, $H_f = A_f C_i$, introduced by Radeka and Rescia (1988) to measure 1/f noise, can be used to intercompare FETs by normalizing out the gate capacitance. By using selected devices from several batches and several processing runs, Alessandrello et al. (1990) claim to have demonstrated the lowest value to date of $H_f = 5.7 \times 10^{-26}$ J for a GaAs MESFET model NE41137 at 4 K. That is only one order of magnitude larger than the best quality Si JFETs operating at 300 K. For the 3SK 164-M, they obtained $H_f = 1.9 \times 10^{-25}$ J at 4 K and $H_f = 8.5 \times 10^{-25}$ J at 77 K.

When the spectral noise density is dominated by the 1/f component, the equivalent noise-charge ENC referred to the input for semi-Gaussian shaping is given by

$$ENC = \left[0.75\bar{e}_{nw}^2\left(\frac{1}{\tau}\right) + 3.2A_f\right]^{1/2} C_i \qquad (5)$$

$\bar{e}_{nw}^2$ is the monolateral white-series-noise spectral power density of the amplifier, τ is the shaping time, and C_i is the total input capacitance of the amplifier including detector, feedback, input, and test capacitances. For the GaAs MESFET, A_f was deduced independent of the spectral noise measurements by employing the noise slope squared (NS^2) technique:

$$NS^2 = \frac{\partial ENC}{\partial C_i} = 0.75\bar{e}_{nw}^2\left(\frac{1}{\tau}\right) + 3.2A_f \qquad (6)$$

The values of A_f obtained with this technique agreed with the spectral noise measurements at 77 K and 4 K. However, the thermal-noise component did not change appreciably with temperature, having a value of about

3.2×10^{-19} V^2/Hz. By implication, the channel thermal-noise resistance rose at 4 K from its value at 77 K, which is consistent with the reduction in carrier density (n) imposed by the Boltzmann factor in equation (1) at 4 K of $\sim 10^{-1}$. The very low values for ENC obtained at 4 K and 77 K of 20 and 58 rms e^-, respectively, demonstrate the superior performance possible with GaAs FETs at cryogenic temperature.

As might be expected, Alessandrello et al. (1990) acknowledge that the selection of devices is still an important step in obtaining the lowest available noise performance. Semiconductor manufacturing and processing still play the dominant roles in noise performance, so the user is at the mercy of whoever specified the device manufacturing run and luck.

For comparison, we measured the noise spectrum of the Aerojet GaAs JFET at 77 K and 7 K, and, through a simple model, deduced the values of A_f and g_m. We fit a two-component curve to the total noise-power spectrum (S_t) between 1 and 100 kHz:

$$S_t = S_w + S_{V_f} \tag{7}$$

An $\bar{f}^{-1/2}$ noise curve is attached to the noise-voltage spectral-density curve at 1 Hz, while a constant-noise (white-noise) curve is fit at 100 kHz. At other frequencies, the quadrature sum is computed. The transconductance can be calculated from the white-noise component:

$$g_m = \sqrt{\frac{1}{4kTS_w}} \tag{8}$$

The sums are compared to the 7 and 77 K data in figures 21 and 56–59. The agreement is satisfactory and yields values for A_f and g_m of 8.0×10^{-15} V^2/Hz and 250 μS at 77 K and 1.3×10^{-15} V^2/Hz and 24.5 μS at 7 K. Intercomparisons for the different Aerojet FETs are made in figures 60–62. The noise measured for FETs C1–8 and D3–8 are essentially the same at 7 K, while FET A5–7 has a larger 1/f component. As was the case for Alessandrello et al. (1990), the A_f at 7 K is lower, in this case by a factor of 2, than at 77 K. Assuming a C_i = 10 pF gives a Radeka and Rescia (1988) factor (H_f) of 1.3×10^{-26} J. This is a factor of 4 lower than the value reported by Alessandrello et al. (1990). C_i = 5.6 pF of a similar Aerojet device has been measured at 4 K (Alwardi, 1987). Our value is the lowest reported to date for GaAs technology at temperatures ≤7 K and closely approaches (within a factor of 2.5) the best quality Si JFETS at 300 K. The measurements of tables 2 and 3 demonstrate a source-follower bandwidth of about 1 MHz when biased with R_S = 1 kΩ. We could anticipate a possible ENC ~ 10 rms e^-. Using an early version of the Aerojet GaAs JFET, Alwardi (1987) found ENC ~ 40 rms e^- at 4 K. This is somewhat noisier than anticipated here, but consistent with the higher spectral noise density he reported for the device. As a benchmark, Alwardi also measured Si JFET read noise at 55 K and achieved ENC ~ 10 rms e^-.

At 100 K, the 3SK 164 achieved the lower limit achieved by Alessandrello et al. (1990) to measure gate leakage current, I_G = 10 fA. In a MESFET, the gate structure is a single-sided Shottky diode with the source-drain structure formed in the bulk by a depletion region that arises from the impressed gate voltage (V_{gs}). The barrier forces an approximately exponential dependence of I_G on T. Extrapolation of I_G measurements made above 100 K indicate a totally negligible I_G at 4 K.

For Si JFETs the standard noise model is discussed by Small and Leslie (1989) in their analysis of a low-noise JFET preamplifier for capacitance bridges. With C_{GS}, the voltage noise ($\bar{e}_n^2$) arising in the channel, the current noise ($\bar{i}_n^2$) resulting from the shot noise of the gate-leakage current (I_G), and the coupling of the channel voltage noise by C_{GS} above the 1/f corner are given by

$$\bar{e}_n^2 = a\left(\frac{4kT}{g_m}\right) \tag{9}$$

$$\bar{i}_n^2 = 2aI_G + \left(ae\omega C_{GS}\right)^2 \tag{10}$$

where a is a constant equal to 0.7 and is determined by the geometry of the gate-to-channel coupling. Depending on the FET model employed, a lies somewhere between $\sqrt{0.35}$ and 2/3. Empirically, we have used a = 1. Small and Leslie have investigated the dependence of a on FET operational parameters and found there were variations dependent upon unmodeled parameters such as the effect of high electric fields on carrier mobility and noise temperature. An adequate choice seems to be a = 1. In terms of the equivalent voltage and current noise generators of the FET, the measured output noise voltage at angular frequency (ω) is given by

$$\bar{v}_n^2 = \left[\bar{e}_n^2 + \left(\frac{\bar{i}_n}{|Y|}\right)^2\right] A^2 B \tag{11}$$

where

$$|Y| = \omega\left(C_{ISS} + C_1\right) \tag{12a}$$

is for the input shorted circuit and

$$|Y| = \omega\left(C_{ISS} + \frac{C_1 C_2}{C_1 + C_2}\right) \tag{12b}$$

is for the input open circuit.

C_1 is the input coupling capacitance, C_2 is the input ground capacitance, A is the amplifier gain, C_{ISS} is the input capacitance to ground, and B is the effective bandwidth. Like Alessandrello et al. (1990) Small and Leslie use the FET in an amplifier circuit that implements positive feedback for amplification purposes. Hence, they need to remove the gain to arrive at an input-referred noise generator. In contrast, we use a simple biased FET without positive feedback in the source follower and quote the fractional gain in tables 2 and 3. Equations (12a) and (12b) show that the input-shorted and input-open noise measurements can give very different noise levels if the value of C_2 is much smaller than C_1. In that case the measured output noise can be somewhat less than for the input-shorted circuit. When C_2 is much greater than C_1, both configurations give similar results. It is not simply true that the floating-gate noise measurements of a FET give a more accurate indication of true noise performance when coupled with an "ideal" infrared photoconductor.

When the FET gate is shorted, the second term in equation (10) disappears. However, when floating or activated by a source such as a detector, then the second term can become significant, especially at high frequencies. This term, or something like it, is probably the source of extra noise in the ungrounded-gate tests. Usually the term is important only at MHz frequencies. It should not be large at audio frequencies. An unmodeled inductance term could conceivably produce audio-frequency pickup detected in an improperly shielded test configuration.

We have used the work of Alessandrello et al. (1990) to introduce the concepts and as a benchmark to compare the performance of the Aerojet JFET, but there are many other reported investigations of GaAs MESFETS. While we cannot report on all of them, it is worthwhile to look at a few.

Sato, Sokolich, Doudoumopoulos, and Duffy (1988) investigated audio-frequency noise performance at 4 K in GaAs enhancement and depletion MESFETs operated with ultralow drain current. Upon cooling, the 1/f noise declined an order of magnitude from its 300 K value to 300 $\mu V/\sqrt{Hz}$ at 10 kHz. This was sufficient to reveal the white-noise source at a level of 30 $\mu V/\sqrt{Hz}$. They achieved $\bar{f}^{-\alpha}$ noise performance at low frequencies with $0.8 < \alpha < 1.2$. Low-power dissipation suitable for infrared-detector focal-plane-array transistor operation was achieved, and $I_D \sim 1.0$ μA. A_f at 10 K for enhancement and depletion mode FETs was reported at values of 1.3 and 8.0×10^{-12} V^2/Hz—three orders of magnitude larger than measured for the Aerojet FET.

Their device construction used a buried p-layer beryllium (Be) implantation for low-noise optimization to isolate the active layer from the semi-insulating substrate. This reduced the drain to source substrate leakage, usually observed near pinchoff, and shielded the active conducting layer of the MESFET from the back-gating effect. In order to ensure full depletion of the buried layer and to minimize the effective g–r volume associated with the space charge in the conducting channel, heavy shallow Si and deeper Be implantations were necessary. A W–Ti–nitride gate and drain-source (n^+) implantation maintained drain-gate and source-gate spacing at 0.1 μm. Ohmic contacting to the drain-source diffusions was with gold, germanium, and nickel (AuGeNi) alloying. Surface passivation was a plasma-enhanced CVD Si_3N_4 deposition.

This MESFET construction is in marked contrast to the epitaxial structures grown on GaAs substrates in the Aerojet JFETs. In the latter, conduction takes place in the epitaxial layers, whereas, in the former, the crystal or substrate itself is the conduction medium. The superior noise performance of the epitaxial materials is correlated with the superior lattice quality of that material. The low number of dislocations and impurities in epitaxially grown layers and the large number of interstitial damage sites concomitant with high-temperature crystal growth and doping procedures can be associated with the origin of the 1/f noise component.

Some further insight into the materials and processing status of GaAs FETs is found in the work of Su, Rohdin, and Stolte (1983). They experimentally investigated the origin of low-frequency noise in GaAs JFETs and MESFETs. They found that traps in the depletion region of the MESFET are primarily responsible for the low-frequency noise. JFET structures eliminate the contribution of the metal–semiconductor interface to the low-frequency noise. Both JFETs were fabricated with Si-implanted channels and a Zn/As implanted p^+ layer as well as JFETs with a Zn diffused p^+ layer to block the surface-layer contribution to the channel carriers. Both JFET varieties had higher low-frequency input-noise levels than typical MESFETs. The conclusion was that the metal–semiconductor interface was not the dominant noise source in MESFETs. By comparing the MESFETs of differing gate-source spacing (1–5 μm) operated in the saturation region, they found no appreciable difference in the low-frequency noise behavior. Thus, they concluded that the free surface, as a whole, was not the dominant contributor to the low-frequency noise. The immediate vicinity of the gate edge could not be ruled out as the noise source.

Traps in the gate/substrate-channel depletion regions were investigated by Su, Rohdin, and Stolte in light of the proposal by Sah (1964) that fluctuations in deep traps in a depletion region are associated with long time constants and thereby contribute to low-frequency noise. They constructed MESFETS with and without LPE buffer layers on undoped and Cr-doped substrates in thicknesses from 3–30 μm. Buffered devices showed a reduction in noise of >90 percent. Thermal correlation of noise in these devices indicates that the noise source is associated with g–r traps in the bulk-depletion region, not surface states. They could not determine whether the g–r traps in the gate-depletion region or in the substrate-channel region are dominant. Mobility fluctuations in the neutral channel do not produce the required temperature behavior of the low-frequency noise.

Confirmation of the g–r trapping origin of the 1/f noise (eq. (4)) comes from the noise level dependence on gate length measured by other investigators on different device families. The observed approximate 1/wL dependence of noise voltage is predicted in the gate-depletion region if velocity saturation is neglected, which is not guaranteed for MESFETs. In theory, this situation is obtained when the gate lengths are greater than five times the channel thickness, which was the case for some of the other devices, but is not necessarily the case for these Aerojet JFETs. The measurements of Goebel et al. (1992) show that the area dependence of noise voltage is realized for the Aerojet n-JFETs within a family of devices that differs in gate area only. Hence, reduction in the deep trapping density in the bulk material responsible for the g–r component should lead to further improvement, not only in GaAs MESFETs, but GaAs JFETS as well. In the foreseeable future then, it is entirely possible that GaAs JFETs operating at 4 K will be able to attain low-frequency noise levels superior to the best room-temperature Si JFETs.

Su, Rohdin, and Stolte (1983) provide an excellent set of measurements of low-frequency-noise spectra that display the Lorentzian time constants associated with equation (2). The origin of these time constants appears to be in the undoped substrate of GaAs, rather than the surface-interface region. Chromium doped substrates do not show any pronounced time-constant effects. Thus, three terms in equation (6) are required for a more complete description of the MESFET, as has been noted by others:

$$S_t = S_w + S_{V_f} + S_{V_{gr}} \qquad (13)$$

The noise spectra in figures 16 and 18 show the appearance of Lorentzian-like behavior when large values of R_S limit the magnitude of I_D, which is the situation that might occur in an infrared focal-plane array. Note that the Lorentzian behaviors appeared in an earlier version of the Aerojet JFET. We did not investigate the behavior in the later versions. The particularly pronounced Lorentzian behaviors in one of the FETs at 7 K are in the same range of frequencies, or time constants, as the undoped substrate of Su, Rohdin, and Stolte (1983). This could indicate that the epitaxial layers of the earlier versions of the JFET were of inferior quality compared to the later versions. The later versions should have much lower trap densities.

A final comparison is with the MODFETs in GaAs with 1 μm gate length studied by Liu, Das, Kopp, and Morkoç (1985). They examined the noise spectrum in the frequency range 10^{-2}–10^{8} Hz. They analyzed the noise with two components:

$$\overline{v}_{ng}^2 = 4kT\Delta f\left[\frac{\rho_0 f_0}{f} + \sum_{i=1}^{n}\frac{\rho_i(\tau_i/\tau_0)}{1+(2\pi f)^2\tau_i^2}\right] \qquad (14)$$

ρ_0 is the 1/f-noise-equivalent gate resistance normalized at f_0, ρ_i is a similar resistance for the ith component of the g–r noise, τ_0 is the characteristic time constant, and τ_i is the time constant for deep-level trap causing the g–r noise. ρ_0 and ρ_i are inversely proportional to gate area. The kHz time constant is similar to that noted above and exhibits a temperature dependence that translated to a trap activation energy 0.40 eV below the conduction band.

Device construction consisted of single-period AlGaAs/GaAs modulation-doped heterostructures, a transistor structure of a 1 μm undoped GaAs buffer layer, a thin layer of undoped $(Al_xGa_{1-x})As$ (20–60 Å), and 600 Å of Si doped $(Al_xGa_{1-x})As$ grown on a Cr-doped GaAs substrate. The device had relatively large 1/f noise without any white noise below 10 MHz. The results indicate that a mixture of 1/f noise generators is unmistakably present in the MODFET structure, which is not likely to be a valuable structure for low-noise devices.

The origin of the 1/f noise is vigorously debated in the literature (van Vliet, 1991; Hooge, 1990). For FETs, the debate is over what factor in the conductivity equation

$$\sigma = en\mu_n \qquad (15)$$

gives rise to the fluctuations associated with the noise for bulk and surface carriers. One choice is mobility (Hooge, 1976), as represented by equation (3). The other choice is carrier density (see Hafez, Ghibaudo, and Balestra (1990) for Si MOS devices and Bhatti and Jones (1984) for Si JFET devices) as represented by equation (2). For large bulk samples the interpretation of noise measurements for 1/f generator mechanisms is relatively straightforward, but for small active devices the interpretation becomes

very difficult. When observed (historically this has not always been the case) an L^2-dependent component should be attributed to interface states (van Vliet, 1991). This is not to be confused with quantum 1/f noise, which is a fundamentally limiting phenomenon arising from the infrared catastrophe of quantum electrodynamics (Handel, 1975) and is orders of magnitude smaller. Apparently all carrier collection processes in solids are susceptible to a 1/f-like noise mechanism, which leads to the widespread confusion and debate over their origin. Finally Pellegrini (1981) has produced a unified theory of noise that covers flicker, island burst and g–r mechanisms, and volumes of influence within the material. Although the origin of 1/f noise is of fundamental importance, and greater understanding will improve our ability to design FETs, we cannot contribute significantly to the debate.

Conclusions

The Aerojet GaAs JFET is useful as a cryogenically cooled 4 K infrared detector preamplifier in the source-follower configuration. The noise performance is superior to Si MOSFETs operating at 4 K and approaches that of Si JFETs at room temperature. Thus, it is applicable with discrete photoconductive and photovoltaic infrared detectors. Development of a dual JFET package would give balanced transimpedance amplifiers in GaAs wider applicability to photovoltaics. The GaAs JFET's noise is somewhat inferior to Si JFETs at frequencies below 10 Hz. Presently, that limits its consideration for bolometric detectors to frequencies higher than 10 Hz where the GaAs JFET is superior. The manufacturing technology employed is well controlled and reproducible, yielding high-quality devices by design. The GaAs JFET shows tremendous potential as a cryogenic infrared detector preamplifier.

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Table 1. Summary of noise versus frequency for the D3–8 JFET

Operating condition/ frequency	nV/√Hz						Figures	Summary figures
	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz		
Grounded gate 77 K								
Drain 1.4 volts	89.64	22.22	5.685	4.428	3.277	4.15	6, 7	59
Grounded gate 7 K								
Drain 1.4 volts	36.56	10.16	5.492	4.377	3.177	3.006	8, 9, 10	20
3.0 volts	63.42	14.21	5.209	3.357	3.681	3.053	11, 12	20
5.0 volts	918.3	161.3	17.19	4.34	2.992	3.181	13, 14, 15	20
Floating gate 7 K								
Drain 1.4 volts	65.35	20.77	12.33	6.565	4.729	4.328	22, 23	21
3.0 volts	132.8	37.91	15.78	7.307	4.767	4.469	24, 25, 26	21
5.0 volts	937.6	142.1	48.92	9.966	5.135	4.912	27, 63–65	21
Detector and bias resistor grounded 7 K								
Drain 1.4 volts	260.2	88.77	36.22	7.392	3.931	4.025	29, 30	28
3.0 volts	280.9	90.68	38.06	8.815	4.097	4.188		28
5.0 volts	1406	157.2	42.08	8.655	5.669	3.911	66–70	28
Detector bias applied 7 K								
Drain 1.4 volts								
Bias volts 0	691	105.1	24.29	5.454	4.067	4.909	34	31
0.5	788.9	92.42	20.01	5.875	3.604	4.338	35	31
–0.5	1181	116.9	26.85	5.339	4.2	4.029	36	31
0.75	1783	375.2	49.9	6.05	3.817	3.593	37	31
–0.75	851.1	83.51	18.42	7.495	4.159	5.05	38	31
Drain 3.0 volts								
Bias volts 0	808.2	104.6	18.46	8.63	7.027	6.596	39	31
0.5	984.6	138.1	25.57	14.69	13.36	9.761	40	32
–0.5	781.2	92.72	20.89	8.531	7.647	6.471	41	32
0.75	821.8	82.94	21.38	10.2	7.269	7.207	42	32
–0.75	784.3	125.7	26.33	8.785	6.898	6.761	43	32
Drain 5.0 volts								
Bias volts 0	6653	640.5	117.7	16.94	8.604	6.687	44	33
0.5	5392	629.9	113.2	17.79	8.294	6.843	45	33
–0.5	8091	746	138.1	17.63	8.715	6.596	46	33
0.75	4434	510.8	91.94	14.34	7.464	6.816	47	33
–0.75	8142	763.8	142.1	16.54	8.303	6.668	48	33

Table 2. Cross reference for FETs figures

Figure number	FET number/temperature	Figure number	FET number/temperature
6	D3–8/77 K	39	D3–8/7 K
7	D3–8/77 K	40	D3–8/7 K
8	D3–8/7 K	41	D3–8/7 K
9	D3–8/7 K	42	D3–8/7 K
10	D3–8/7 K	43	D3–8/7 K
11	D3–8/7 K	44	D3–8/7 K
12	D3–8/7 K	45	D3–8/7 K
13	D3–8/7 K	46	D3–8/7 K
14	D3–8/7 K	47	D3–8/7 K
15	D3–8/7 K	48	D3–8/7 K
16	A5–7/7 K	49	D3–8/NA
17	A5–7/7 K	50	D3–8/NA
18	A1/77 K	51	D3–8/NA
19	A1/7 K	52	D3–8/NA
20	D3–8/7 K	53	D3–8/NA
21	D3–8/7 K	54	D3–8/NA
22	D3–8/7 K	55	D3–8 and others/NA
23	D3–8/7 K	56	D3–8/7 K, 77 K
24	D3–8/7 K	57	D3–8/7 K
25	D3–8/7 K	58	D3–8/77 K
26	D3–8/7 K	59	D3–8/77 K
27	D3–8/7 K	60	A5–7, C1–8, D3–8/7 K
28	D3–8/7 K	61	A5–7, C1–8, D3–8/7 K
29	D3–8/7 K	62	A5–7, C1–8, D3–8/7 K
30	D3–8/7 K	63	D3–8/7 K
31	D3–8/7 K	64	D3–8/7 K
32	D3–8/7 K	65	D3–8/7 K
33	D3–8/7 K	66	D3–8/7 K
34	D3–8/7 K	67	D3–8/7 K
35	D3–8/7 K	68	D3–8/7 K
36	D3–8/7 K	69	D3–8/7 K
37	D3–8/7 K	70	D3–8/7 K
38	D3–8/7 K		

Table 3. Gain of A5–7 FET as a function of source resistance

Temperature	Drain volts	Source resistance	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
77 K	3.7	1 kΩ	0.44	0.44	0.44	0.44	0.44	0.46	0.22
77 K	3.7	10 kΩ	0.75	0.77	0.77	0.77	0.77	0.7	0.12
77 K	3.7	100 kΩ	0.9	0.89	0.89	0.89	0.87	0.43	0.08
77 K	3.7	1 MΩ	0.92	0.92	0.92	0.92	0.71	0.12	0.08
77 K	3.7	10 MΩ	0.9	0.87	0.87	0.78	0.21	0.08	0.08
4 K	3.7	1 kΩ	0.44	0.45	0.45	0.45	0.45	0.44	–
4 K	3.7	10 kΩ	0.76	0.77	0.77	0.77	0.77	0.64	–
4 K	3.7	100 kΩ	0.88	0.9	0.9	0.9	0.86	0.32	–
4 K	3.7	1 MΩ	0.9	0.93	0.93	0.93	0.69	0.1	–
4 K	3.7	10 MΩ	0.88	0.88	0.88	0.76	0.15	0.05	–

Table 4. Gain of A1 FET as a function of source resistance

Temperature	Drain volts	Source resistance	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
300 K	3.7	1 kΩ	0.52	0.52	0.52	0.52	0.52	0.48	0.24
300 K	3.7	10 kΩ	0.8	0.82	0.81	0.81	0.81	0.74	0.14
300 K	3.7	100 kΩ	0.92	0.93	0.93	0.92	0.91	0.49	0.08
300 K	3.7	1 MΩ	0.95	0.96	0.96	0.95	0.81	0.17	0.08
300 K	3.7	10 MΩ	0.95	0.93	0.93	0.89	0.33	0.09	0.08
77 K	3.7	1 kΩ	0.44	0.48	0.46	0.46	0.46	0.45	0.24
77 K	3.7	10 kΩ	0.8	0.78	0.78	0.78	0.78	0.71	0.14
77 K	3.7	100 kΩ	0.95	0.9	0.9	0.9	0.89	0.46	0.1
77 K	3.7	1 MΩ	0.95	0.93	0.93	0.93	0.75	0.14	0.08
77 K	3.7	10 MΩ	0.92	0.89	0.88	0.83	0.24	0.14	0.08
4 K	3.7	1 kΩ	0.46	0.46	0.46	0.46	0.46	0.47	0.28
4 K	3.7	10 kΩ	0.76	0.77	0.77	0.77	0.77	0.68	0.16
4 K	3.7	100 kΩ	0.88	0.9	0.89	0.9	0.87	0.39	0.08
4 K	3.7	1 MΩ	0.92	0.94	0.93	0.93	0.77	0.15	0.08
4 K	3.7	10 MΩ	0.88	0.87	0.86	0.76	0.2	0.06	0.08

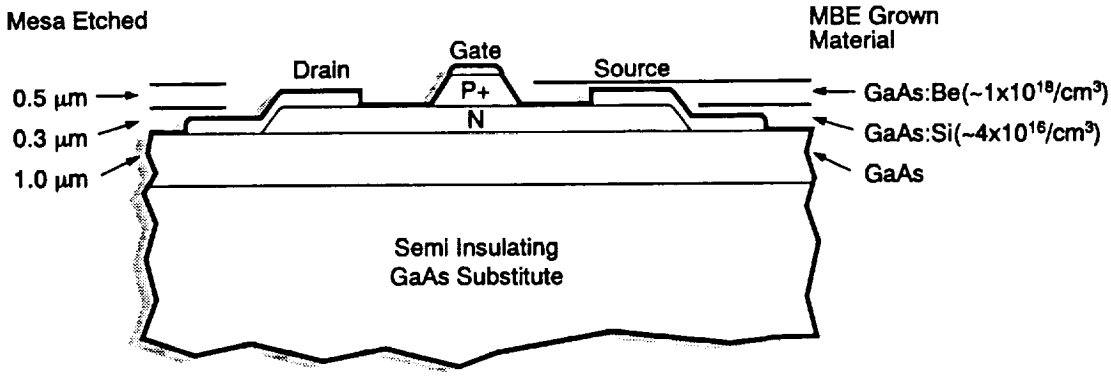

Figure 1. n-channel GaAs JFET design for cryogenic operation.

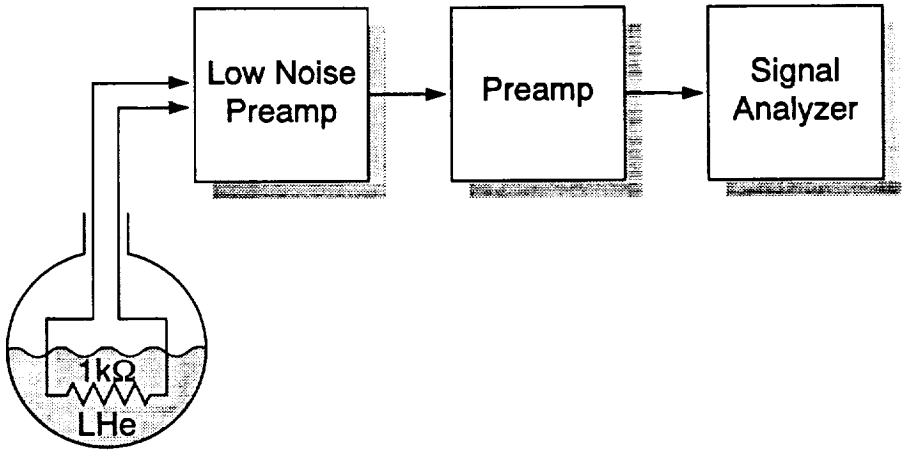

Figure 2. Noise measurement system calibration configuration.

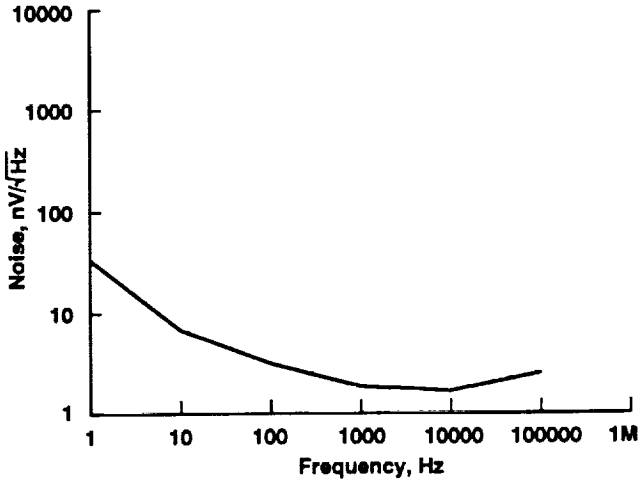

Figure 3. Noise versus frequency of SR552 amplifier with a 1kΩ input resistor cooled to 4K.

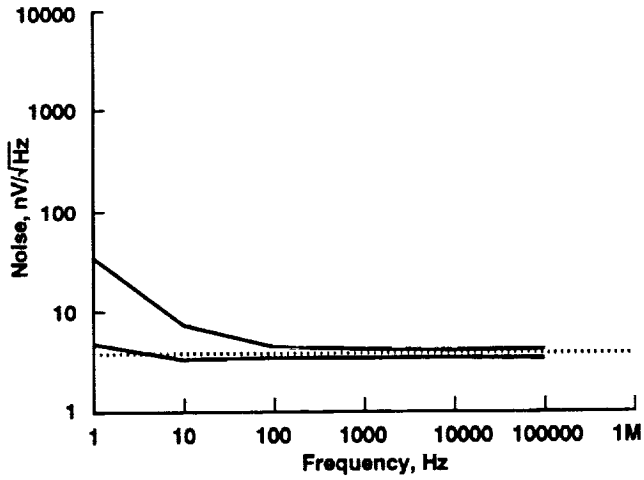

Figure 4. Measured Johnson noise of a 1kΩ input resistor at 300K.

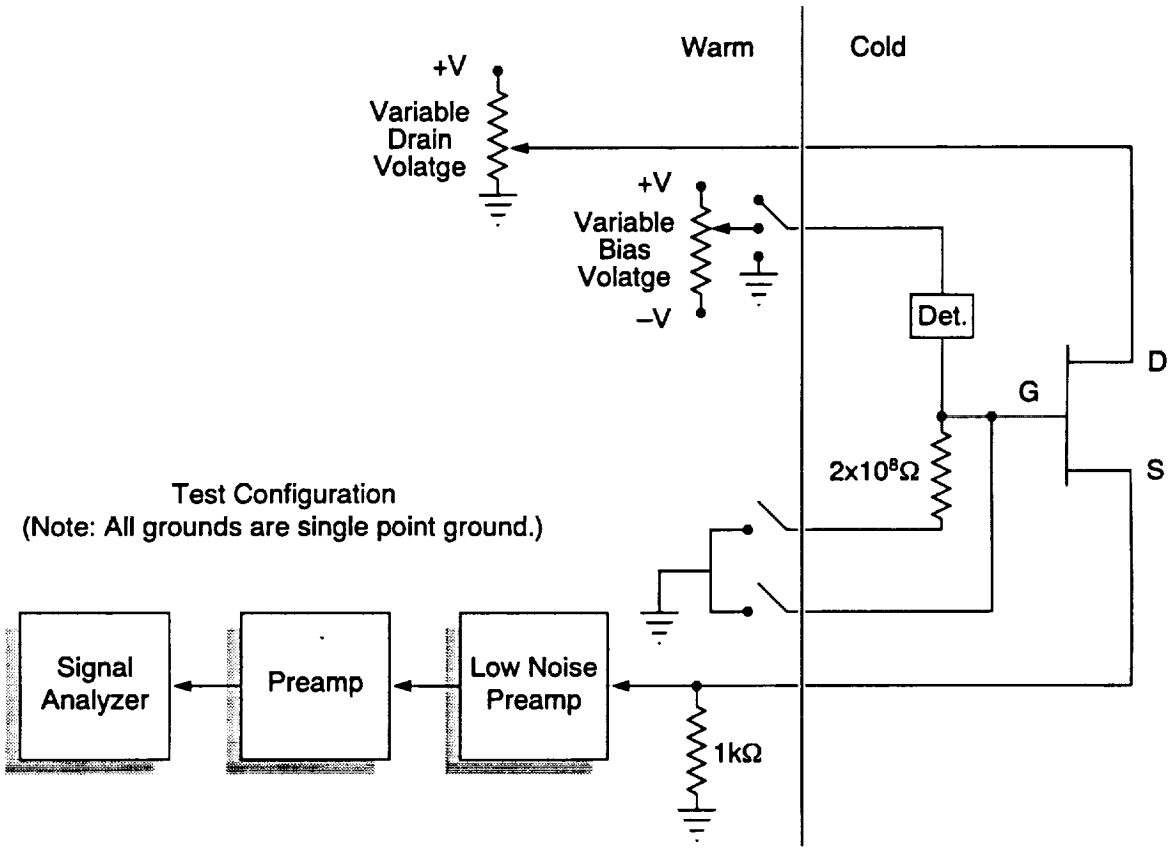

Figure 5. GaAs JFET noise test configuration.

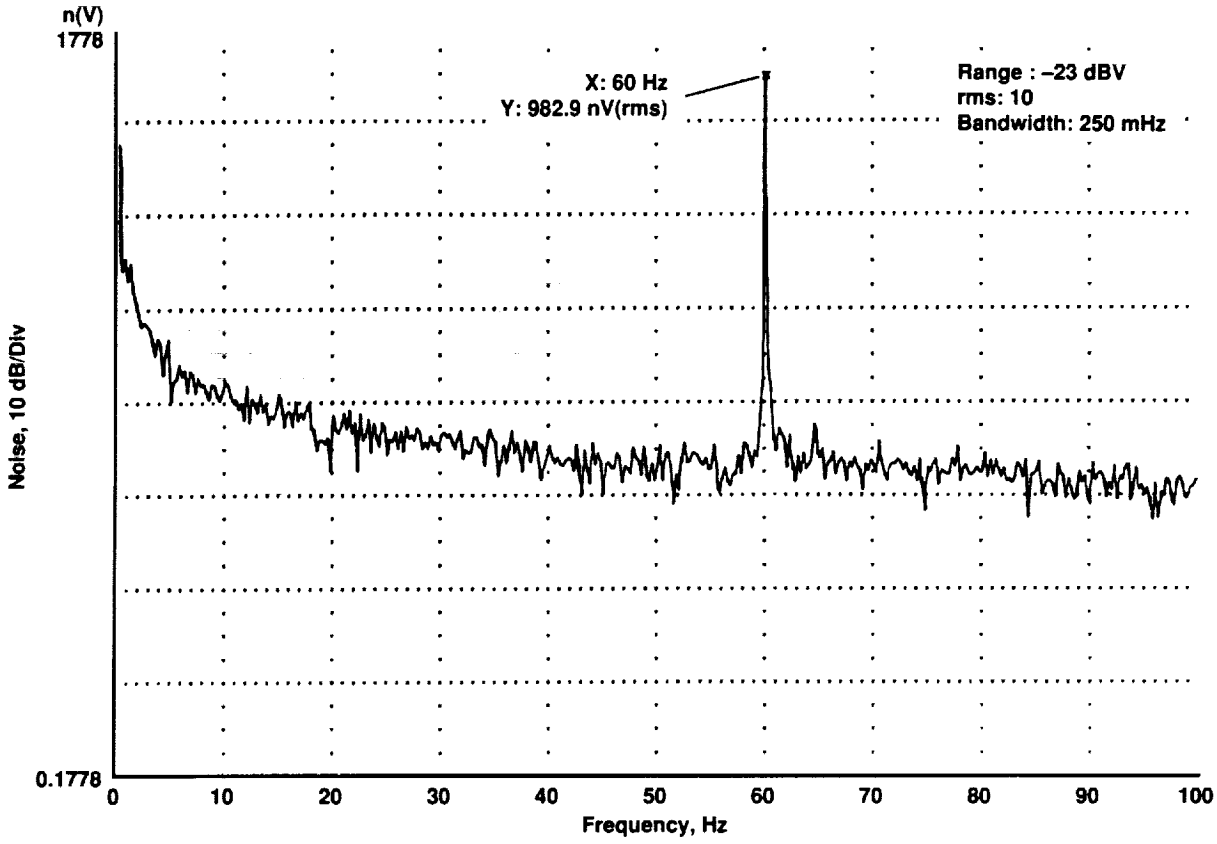

Figure 6. FET D3–8 at 77K: V_D = 1.4 V, R_S = 1kΩ, gate grounded, raw data.

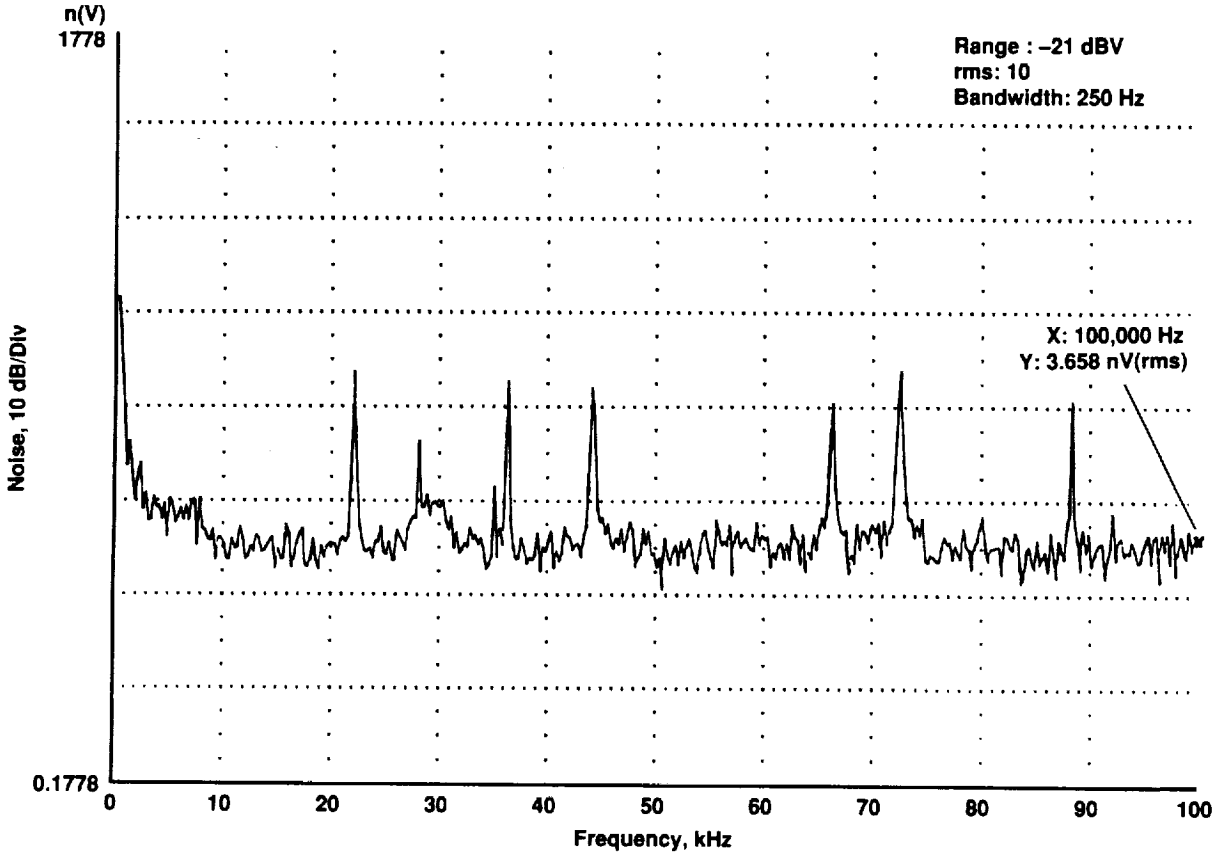

Figure 7. FET D3–8 at 77K: system input noise, gate grounded, raw data.

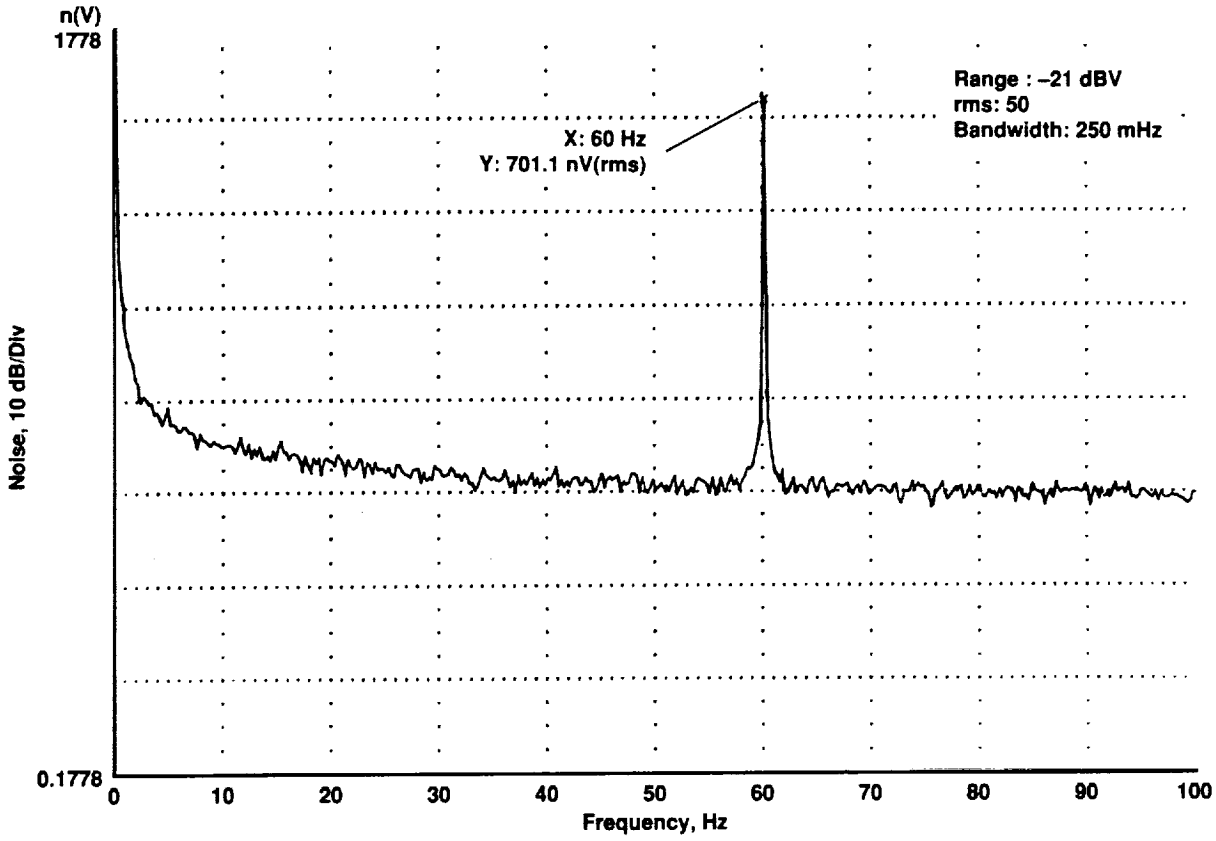

Figure 8. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, gate grounded, raw data.

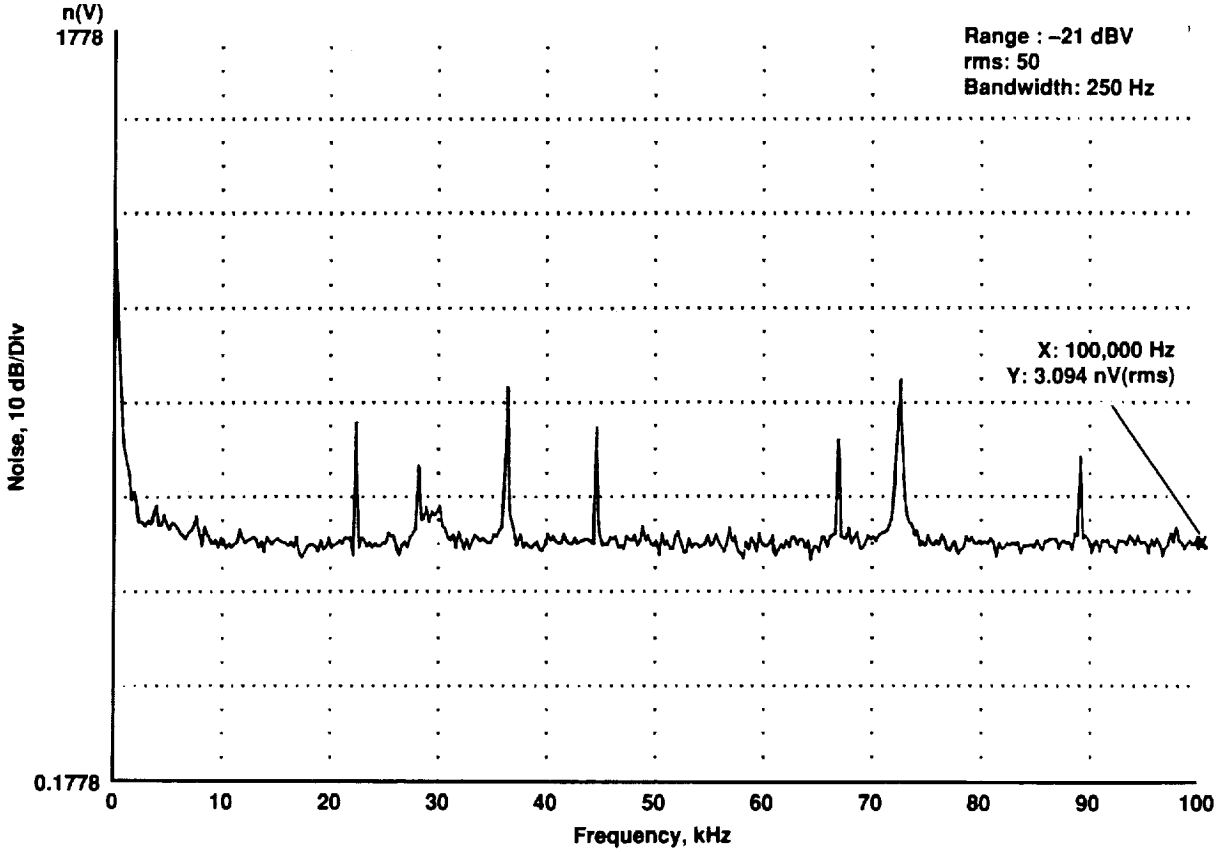

Figure 9. FET D3–8 at 7K: system input noise, raw data.

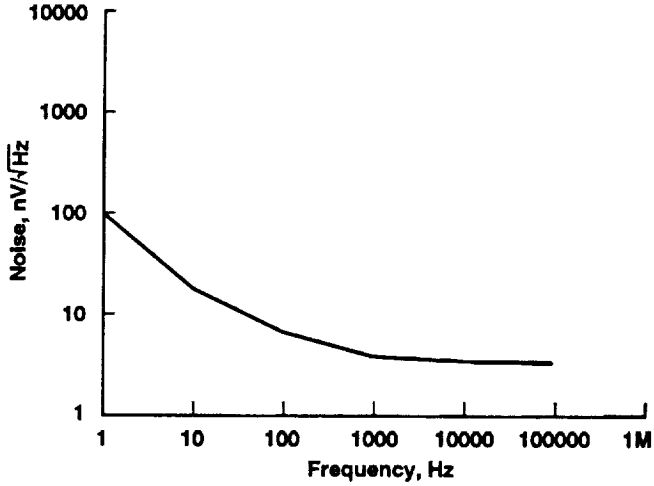

Figure 10. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, gate grounded, summary data.

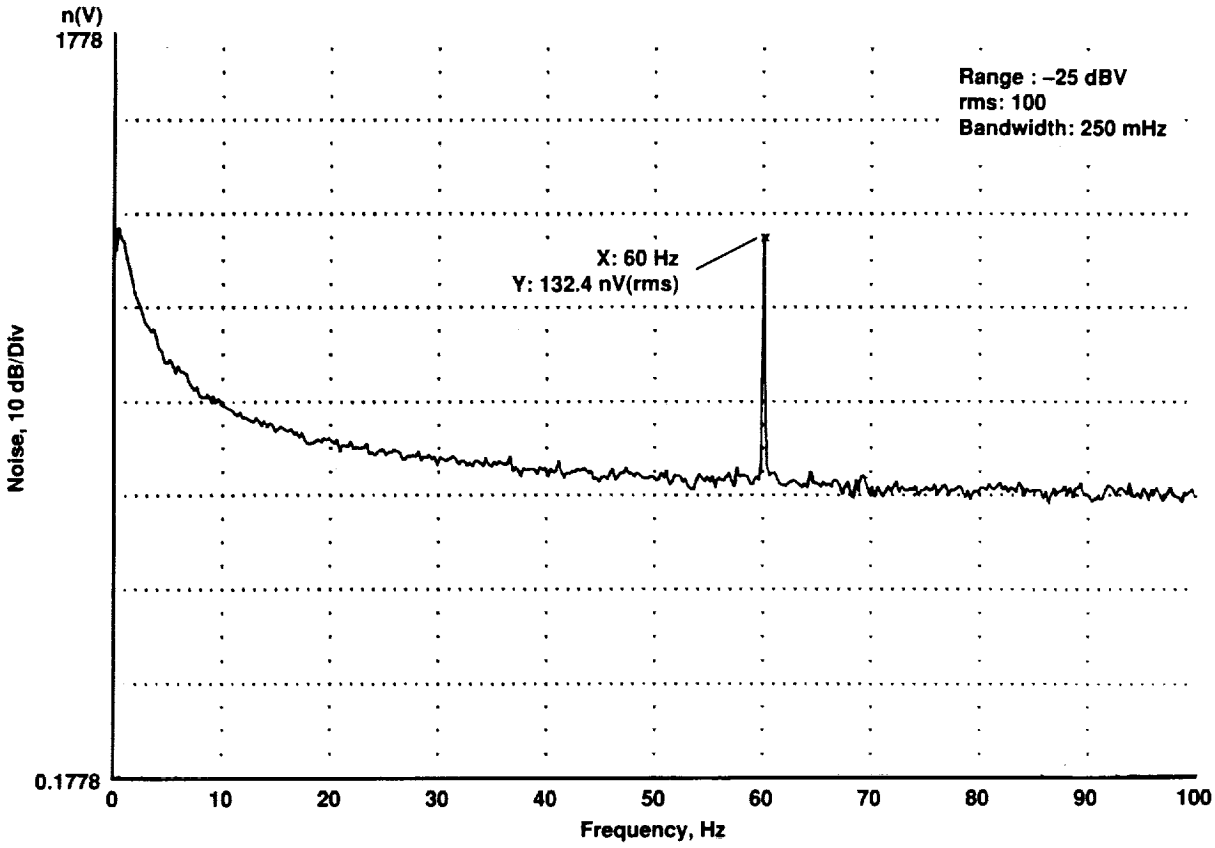

Figure 11. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, gate grounded, raw data.

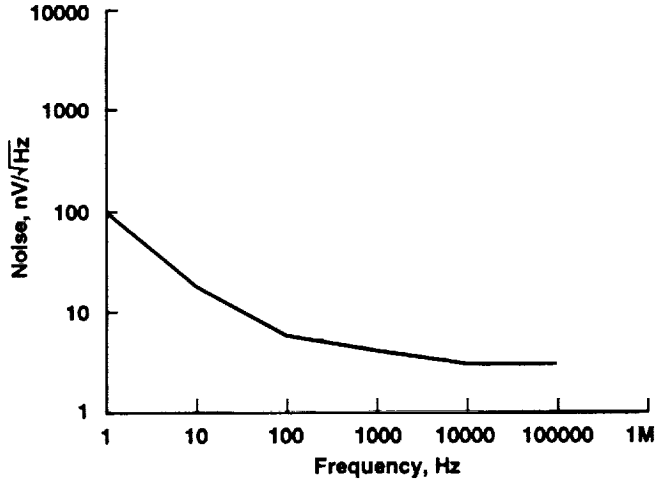

Figure 12. FET D3–8 at 7K: V_D = 3.0V, R_S = 1kΩ, gate grounded, summary data.

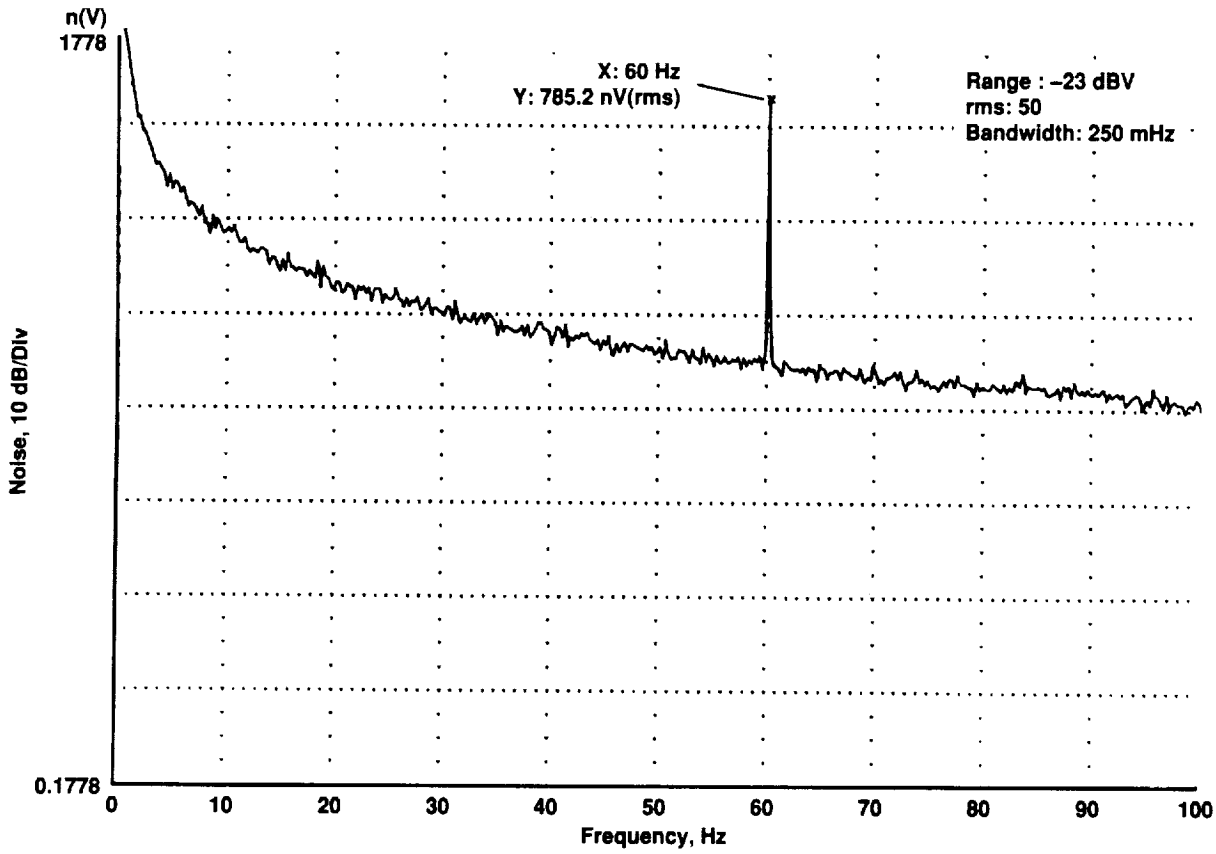

Figure 13. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate grounded, raw data.

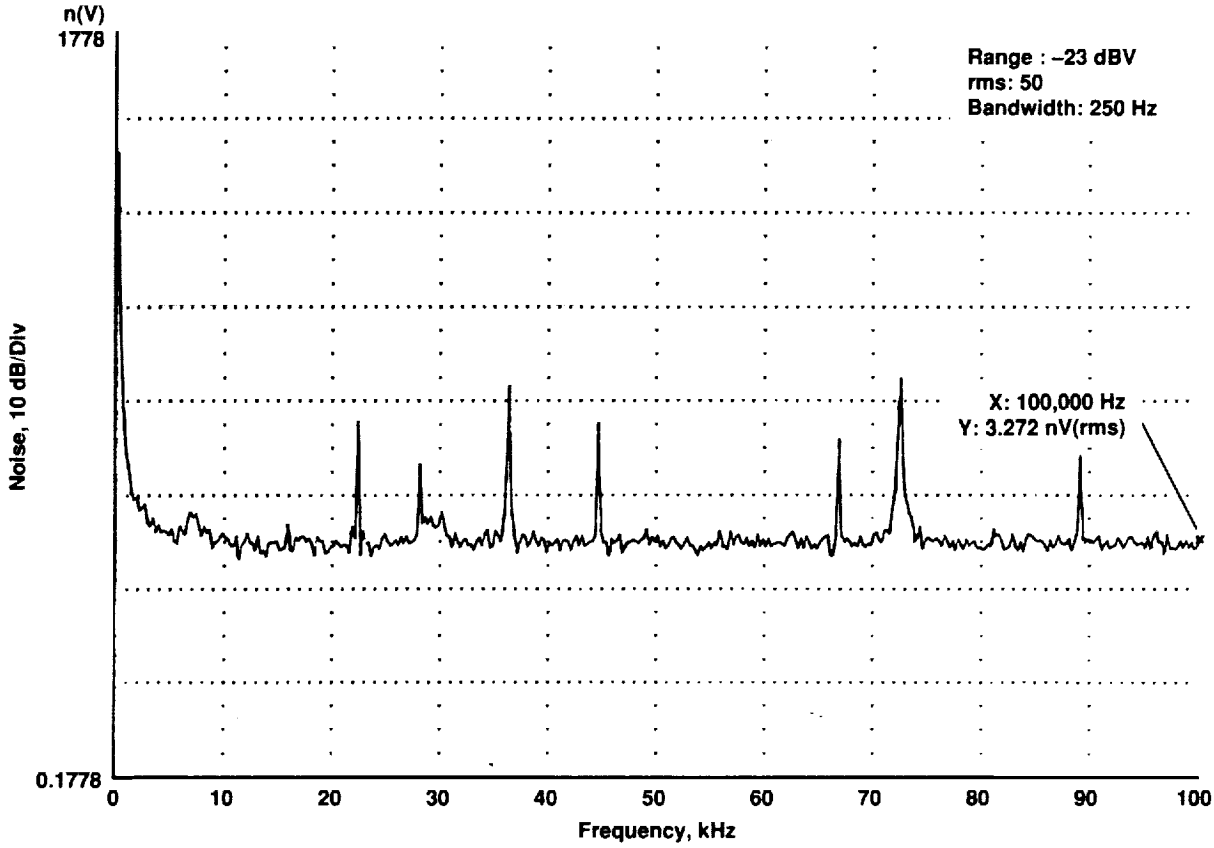

Figure 14. FET D3–8 at 7K: system input noise, raw data.

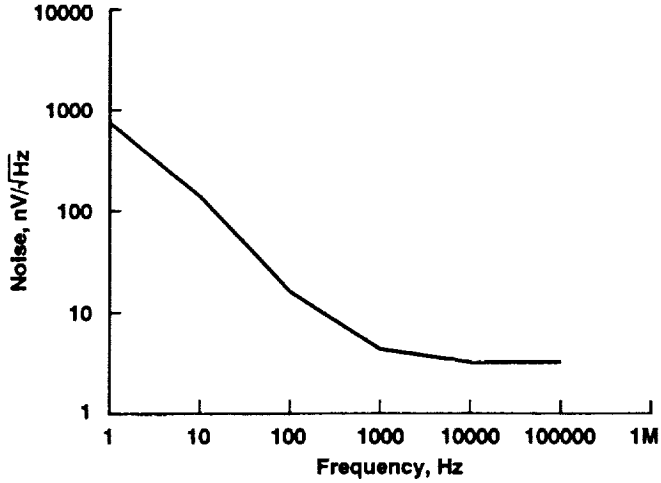

Figure 15. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate grounded, summary data.

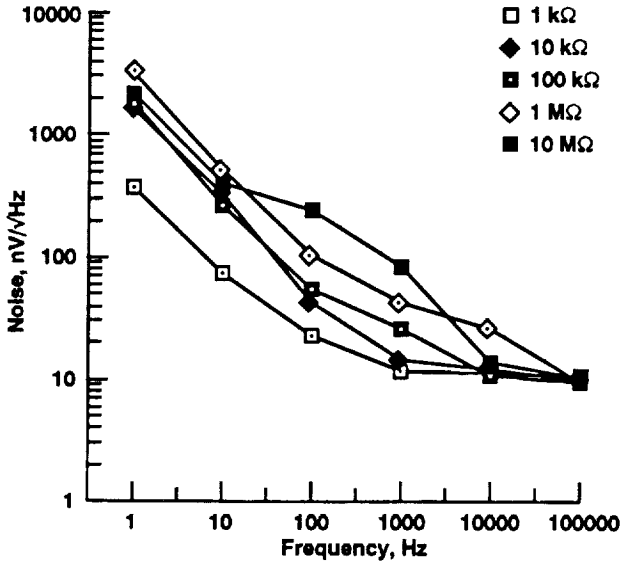

Figure 16. A5–7 FET noise spectrum as a function of source resistance at 7K.

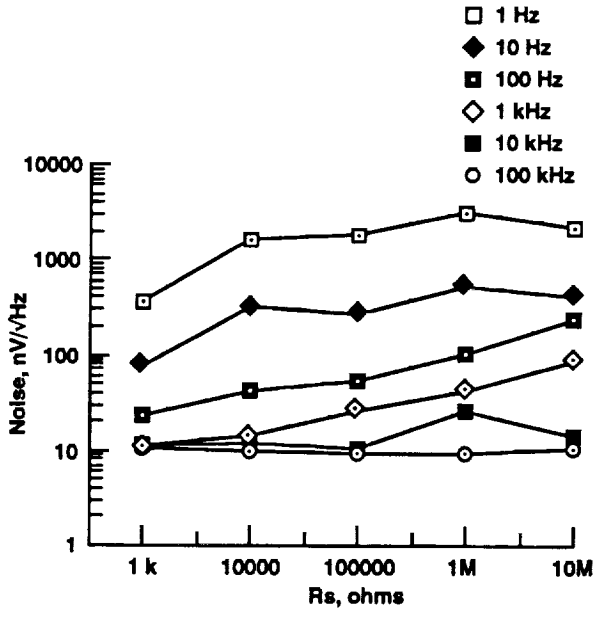

Figure 17. A5–7 FET noise spectrum as a function of source resistance at 7K.

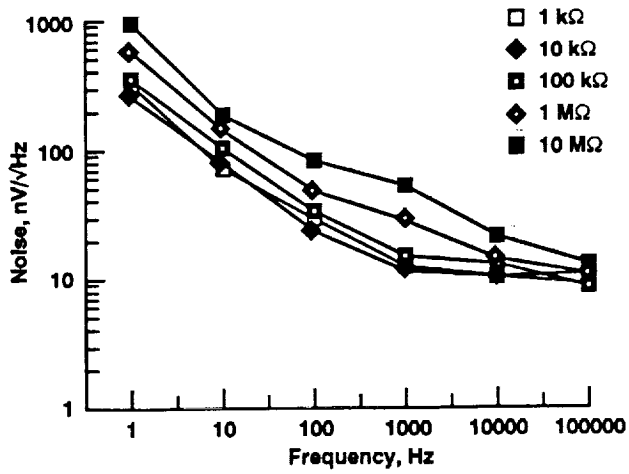

Figure 18. A1 FET noise spectrum as a function of source resistance at 77K.

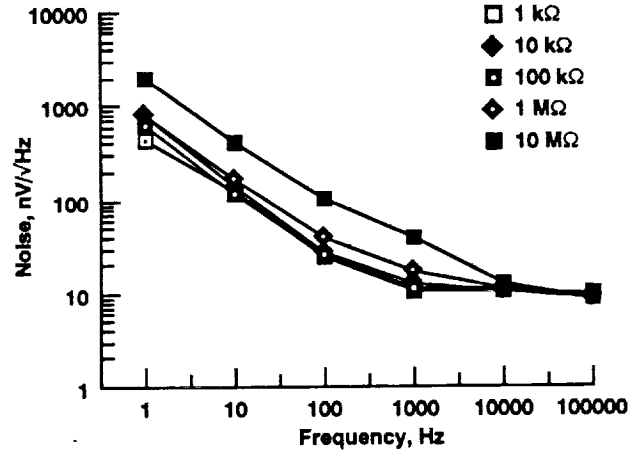

Figure 19. A1 FET noise spectrum as a function of source resistance at 7K.

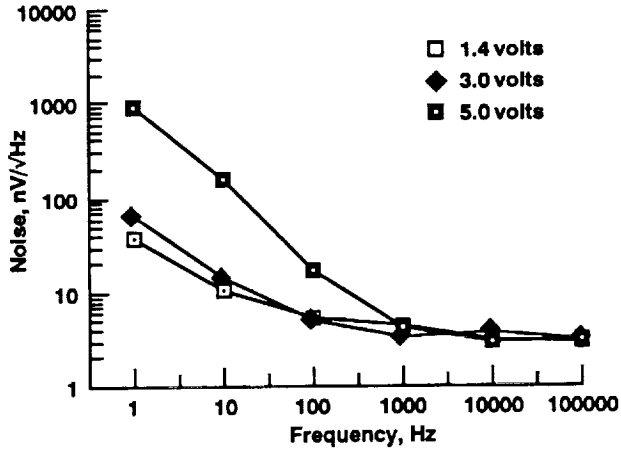

Figure 20. D3–8 FET noise spectrum in the grounded-gate mode at 7K.

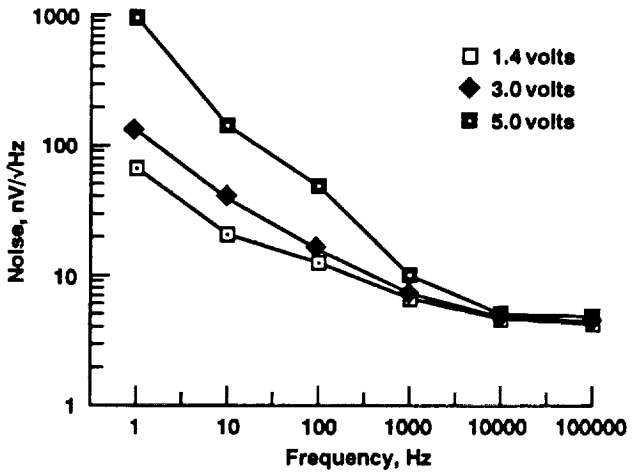

Figure 21. Noise spectrum of D3–8 at 7K with gate floating.

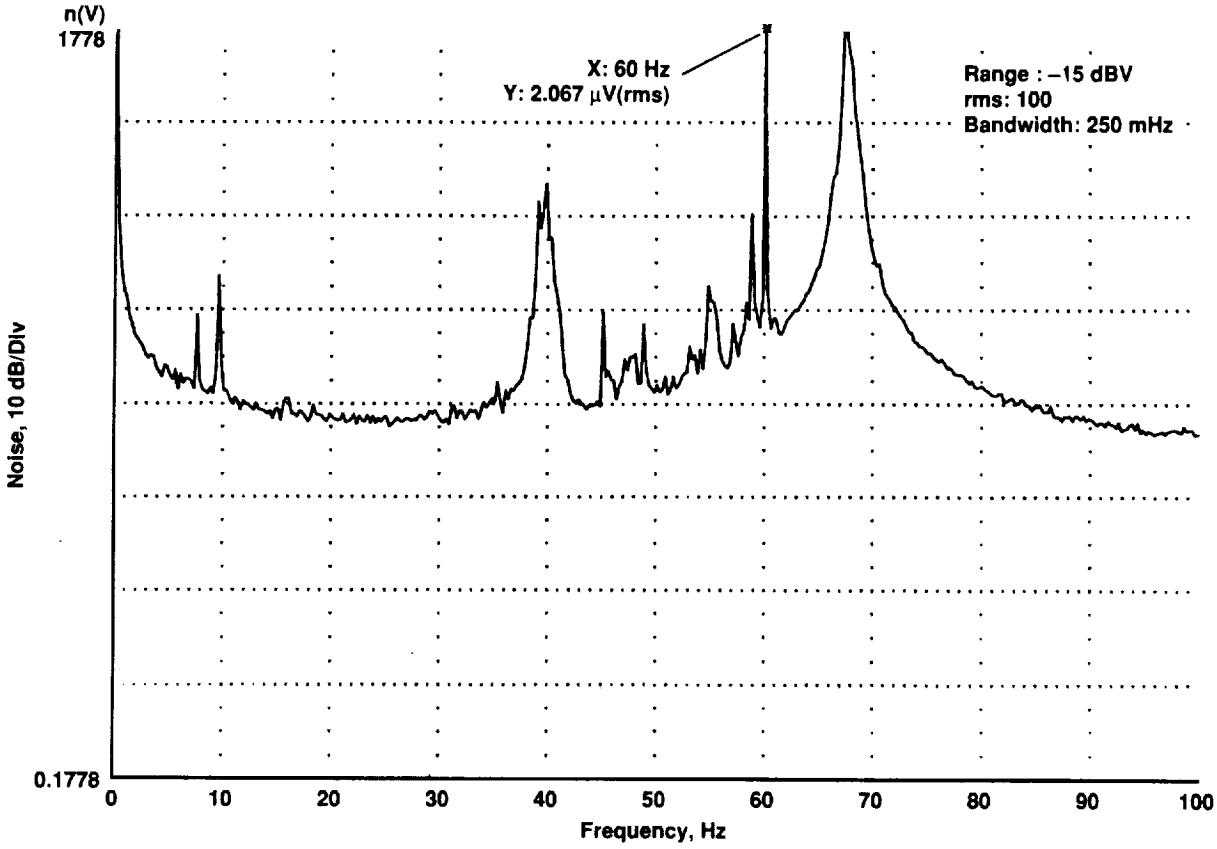

Figure 22. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, gate open, raw data.

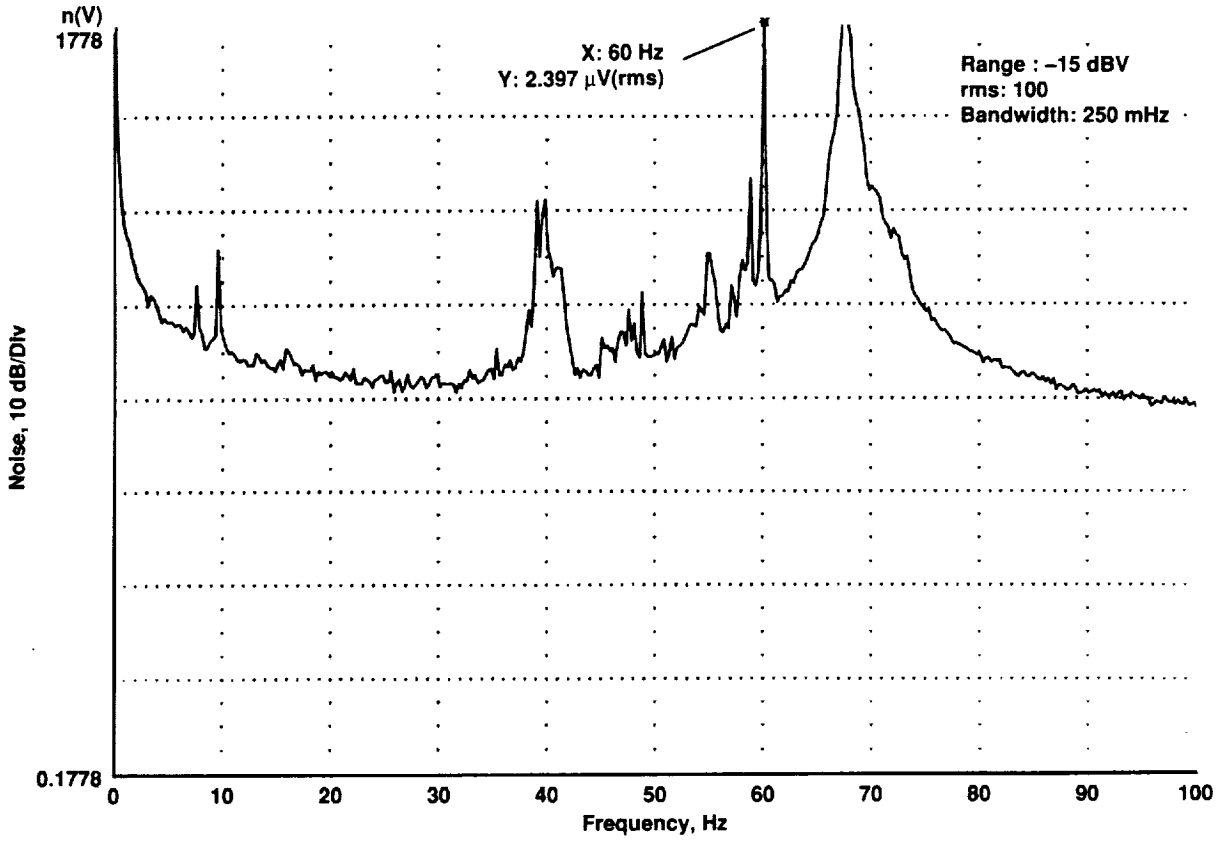

Figure 23. FET D3–8 at 7K: V_D 3.0 V, R_S = 1kΩ, gate open, raw data.

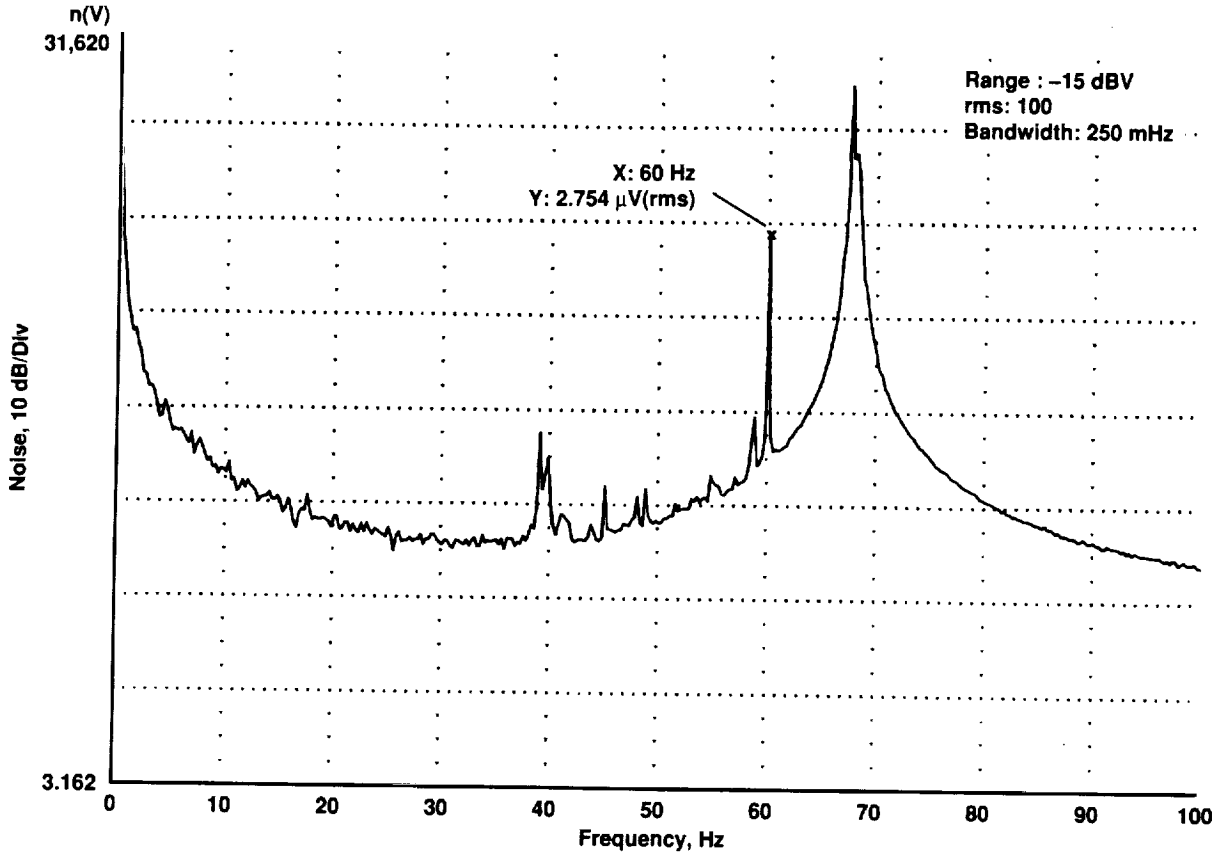

Figure 24. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate open, raw data.

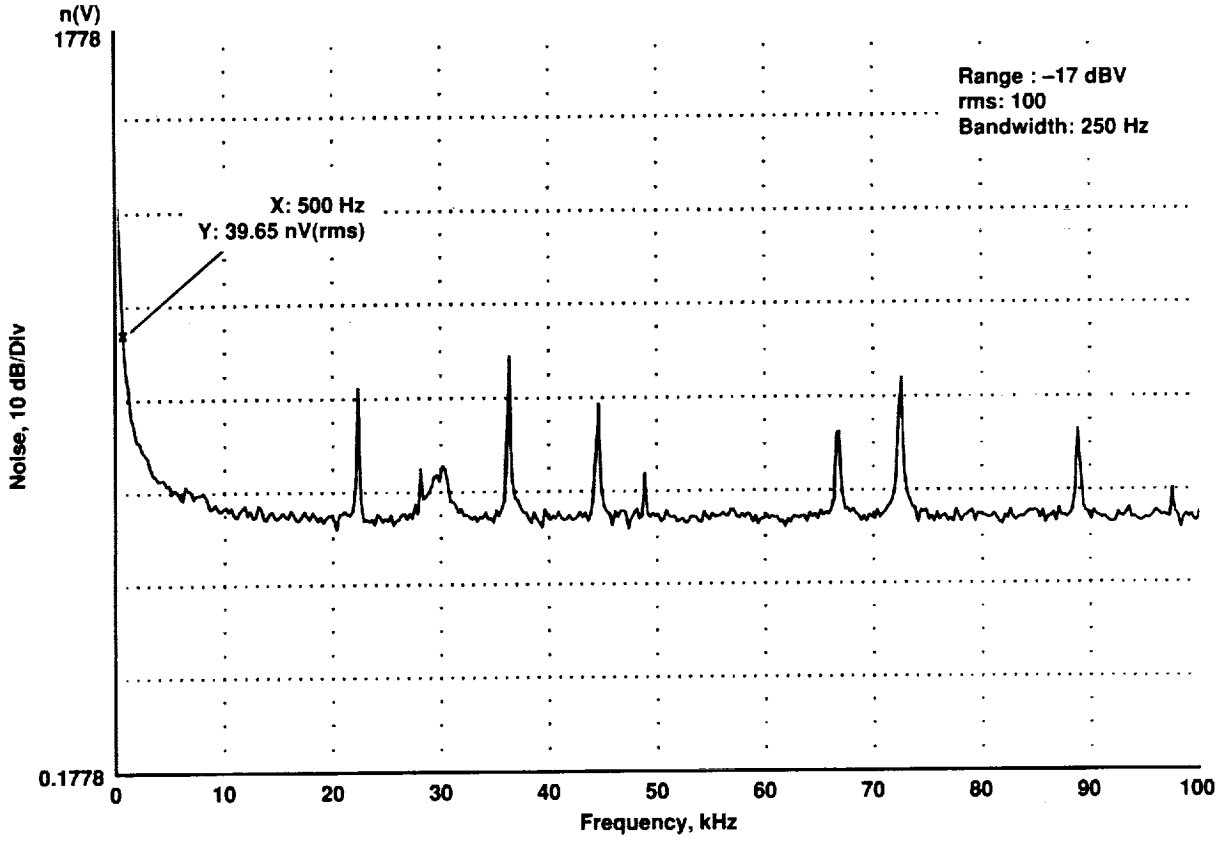

Figure 25. FET D3–8 at 7K: V_D = 1.4 V, system input noise, raw data.

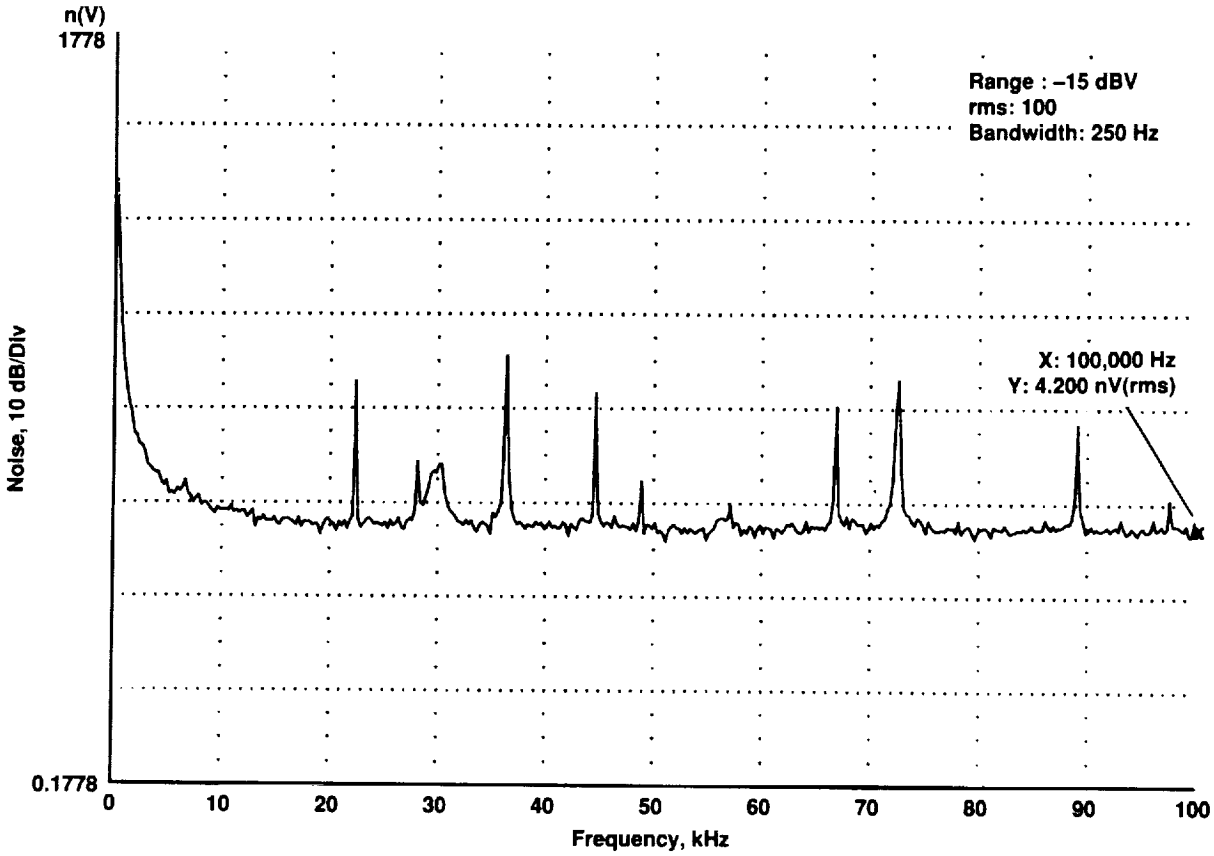

Figure 26. FET D3–8 at 7K: V_D = 3.0 V, system input noise, raw data.

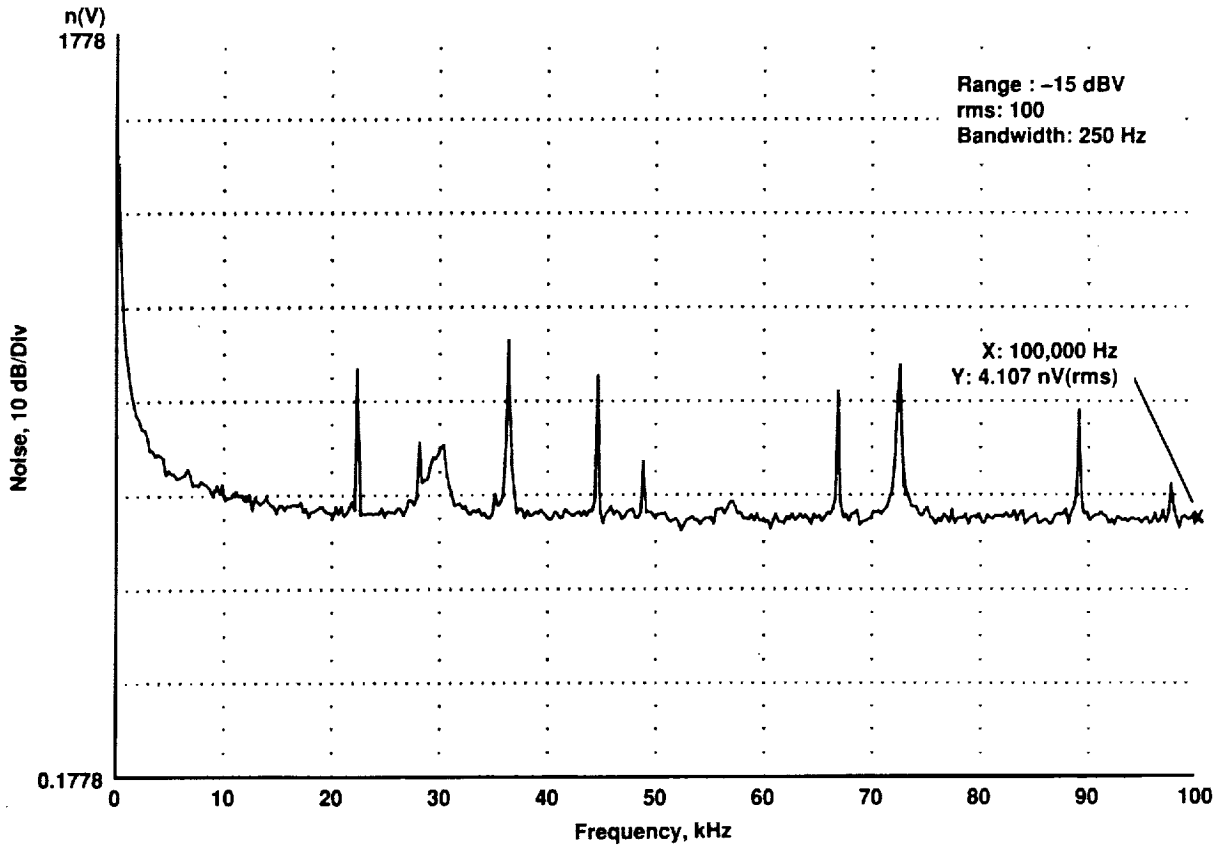

Figure 27. FET D3–8 at 7K: V_D = 5.0 V, system input noise, raw data.

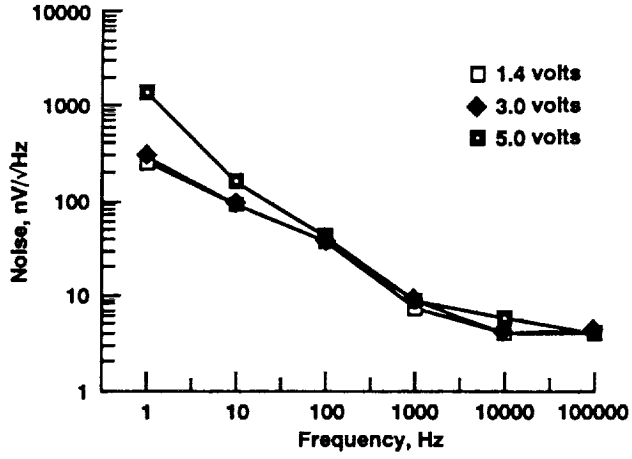

Figure 28. Noise spectrum of D3–8 at 7K with detector and bias resistor grounded.

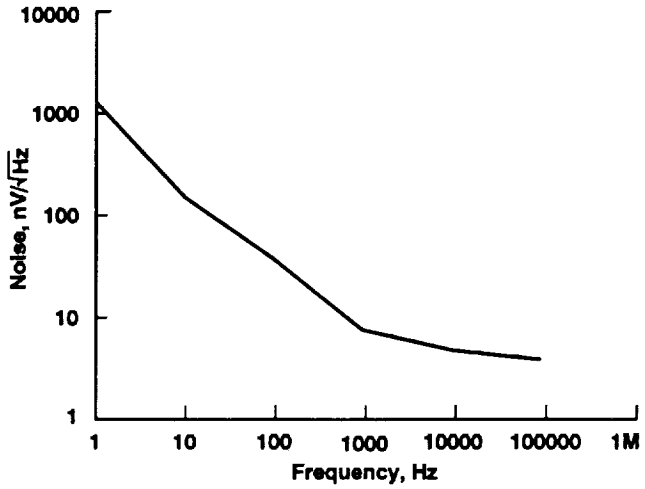

Figure 29. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate grounded through 2 x 10^8 Ω, summary data.

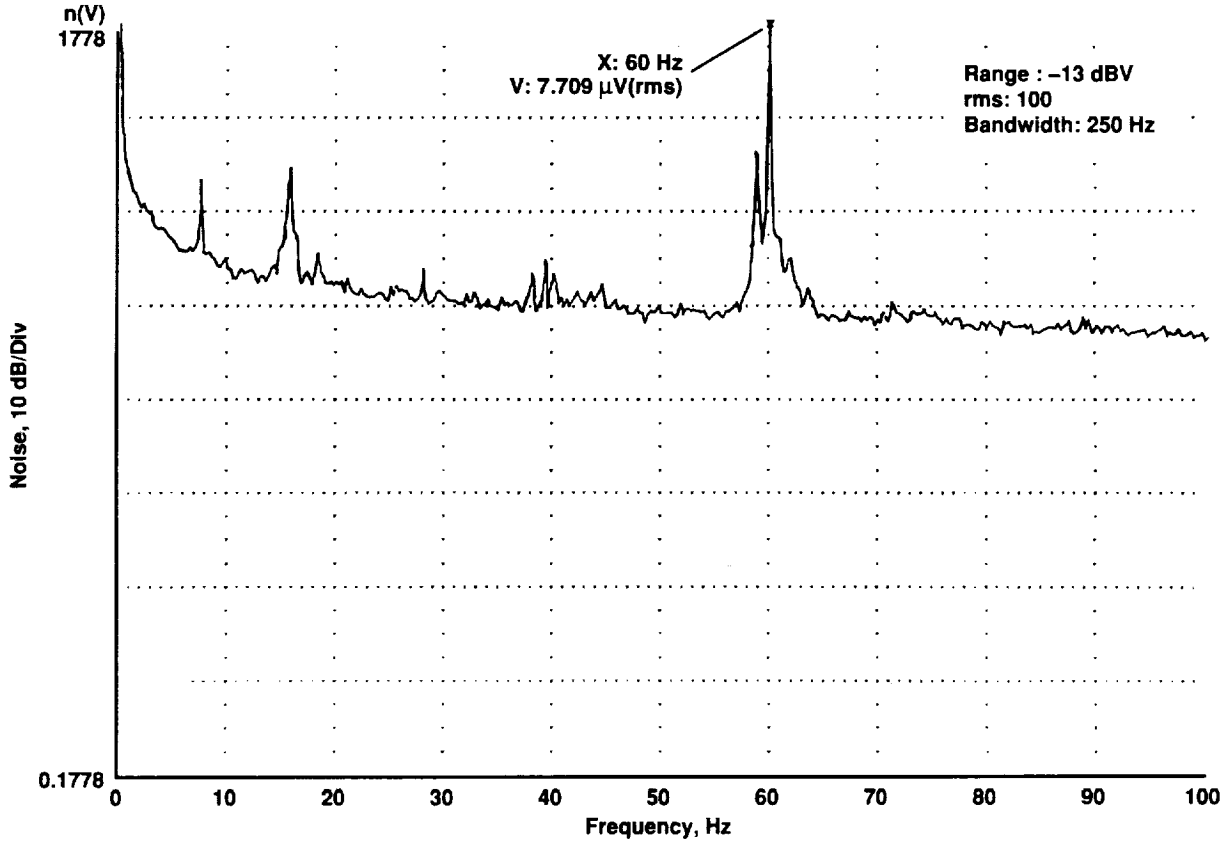

Figure 30. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, gate grounded through 2 x 10^8 Ω, raw data.

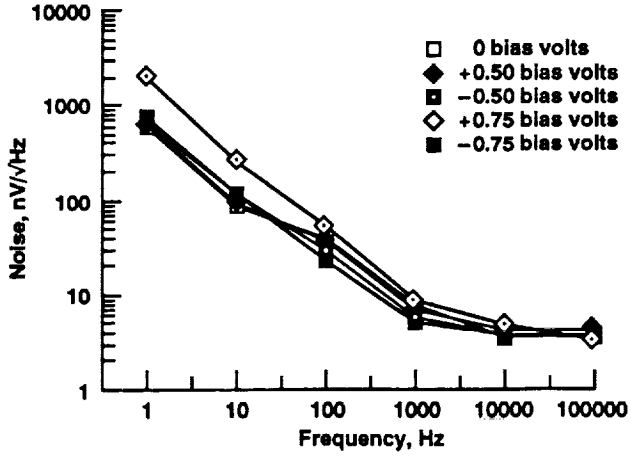

Figure 31. Noise spectrum of D3–8 at 7K with detector biases and V_D = 1.4 V.

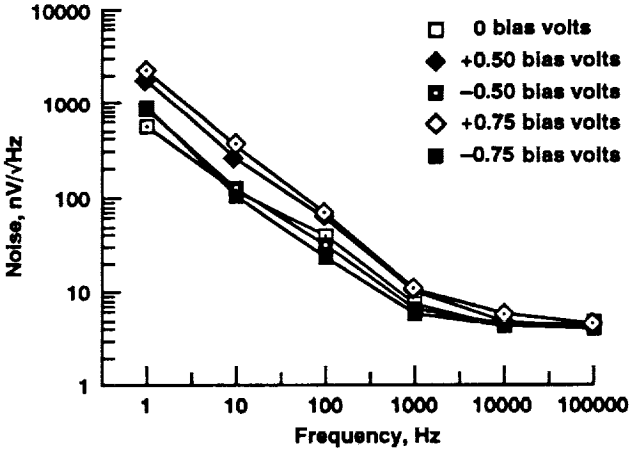

Figure 32. Noise spectrum of D3–8 at 7K with detector biases and V_D = 3.0 V.

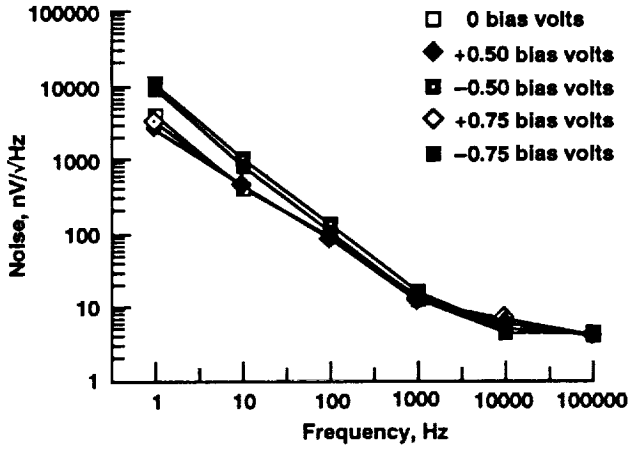

Figure 33. Noise spectrum of D3–8 at 7K with detector biases and V_D = 5.0 V.

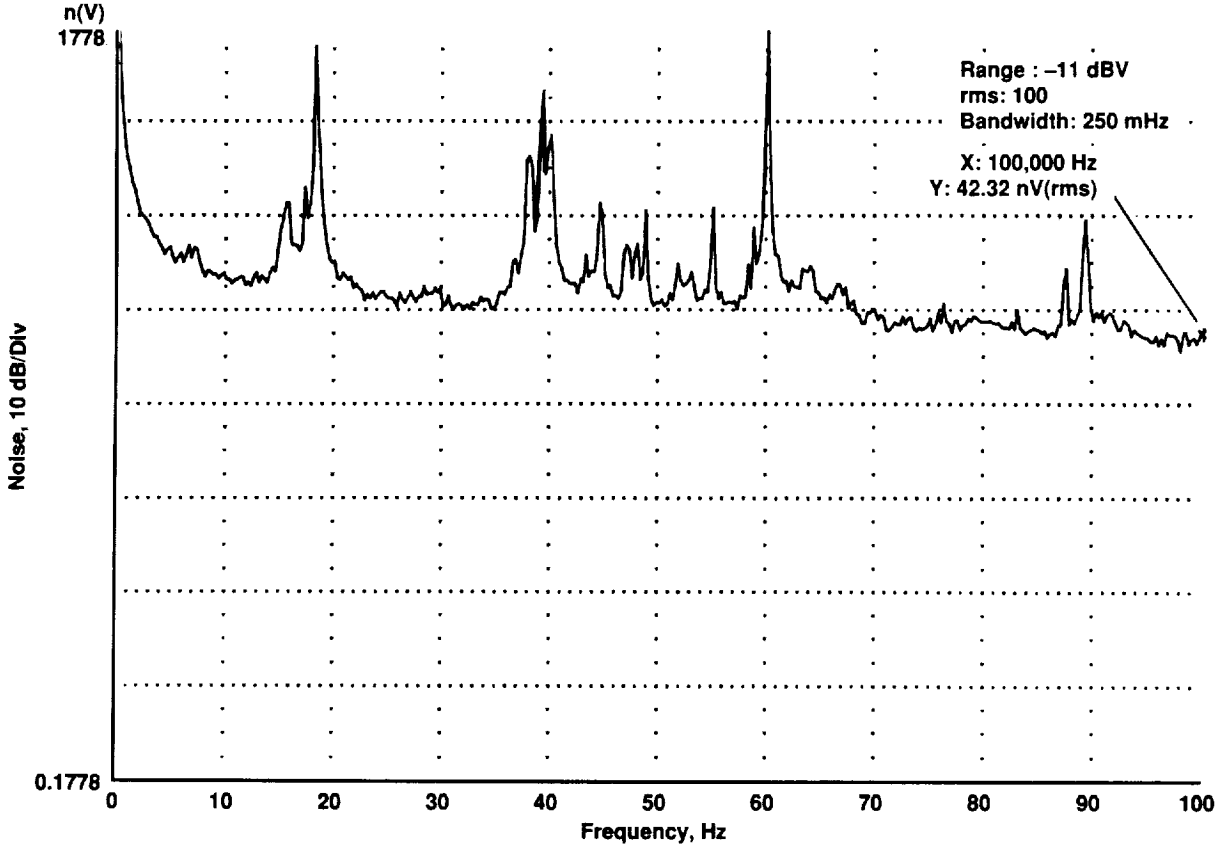

Figure 34. FET D3–8 at 7K: V_D 1.4 V, R_S = 1kΩ, V_{Det} = 0.0V, R_B = 2 x 10^8 Ω, raw data.

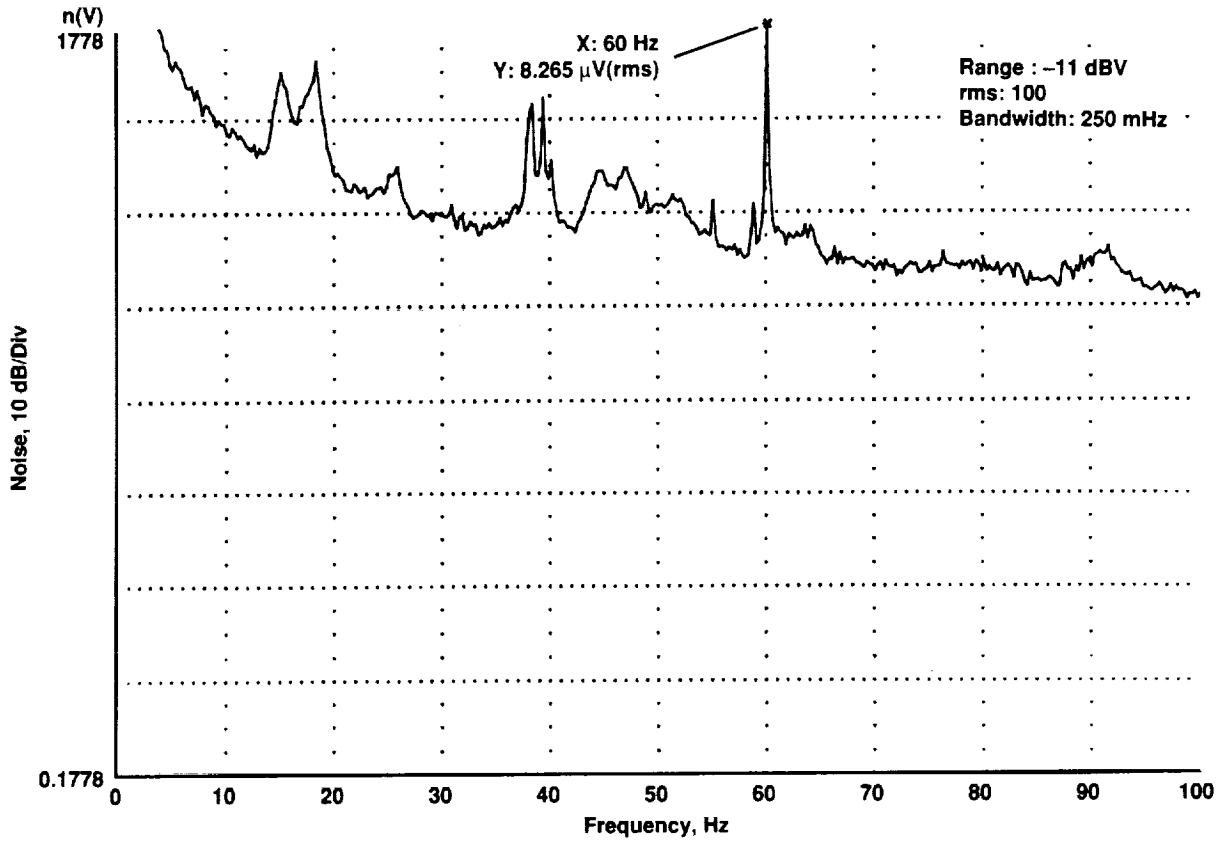

Figure 35. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, V_{Det} = 0.5 V, R_B = 2 x 10^8 Ω, raw data.

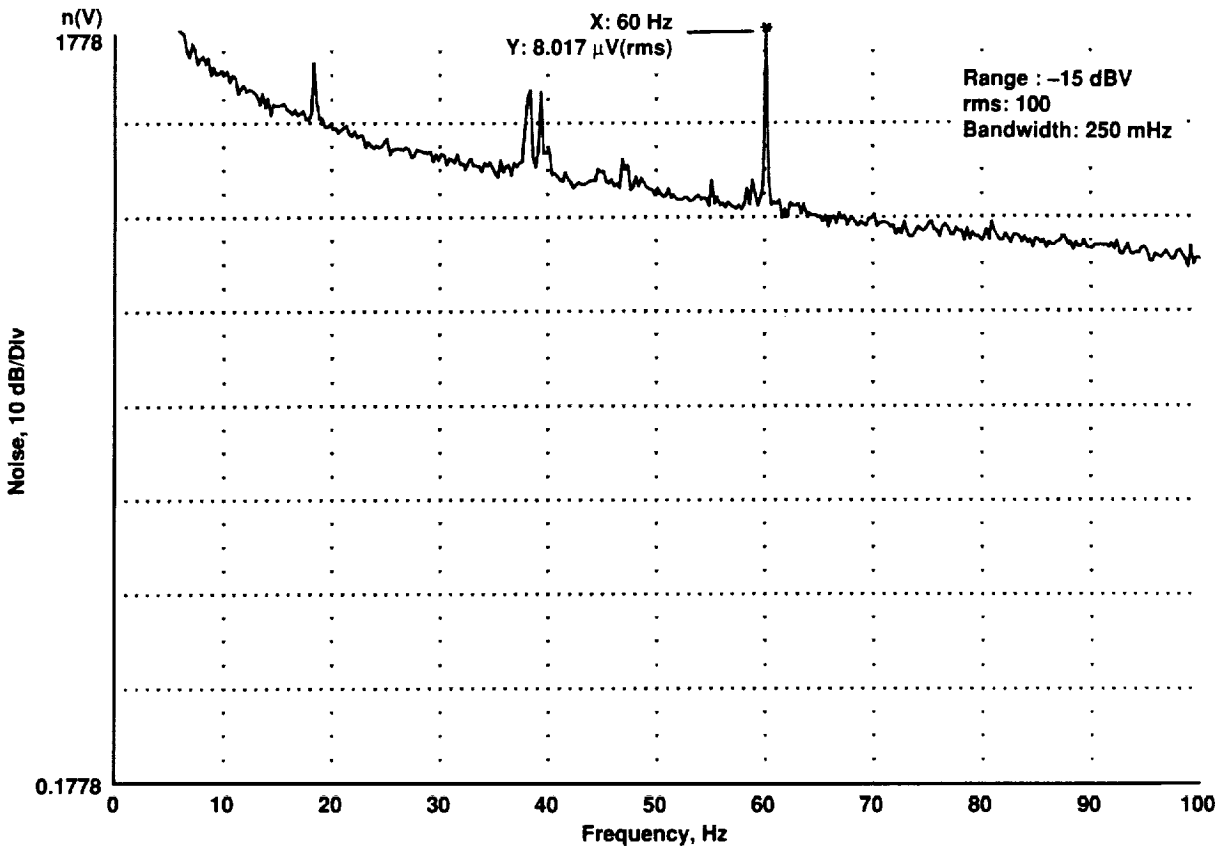

Figure 36. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, V_{Det} = –0.5 V, R_B = 2 x 10^8 Ω, raw data.

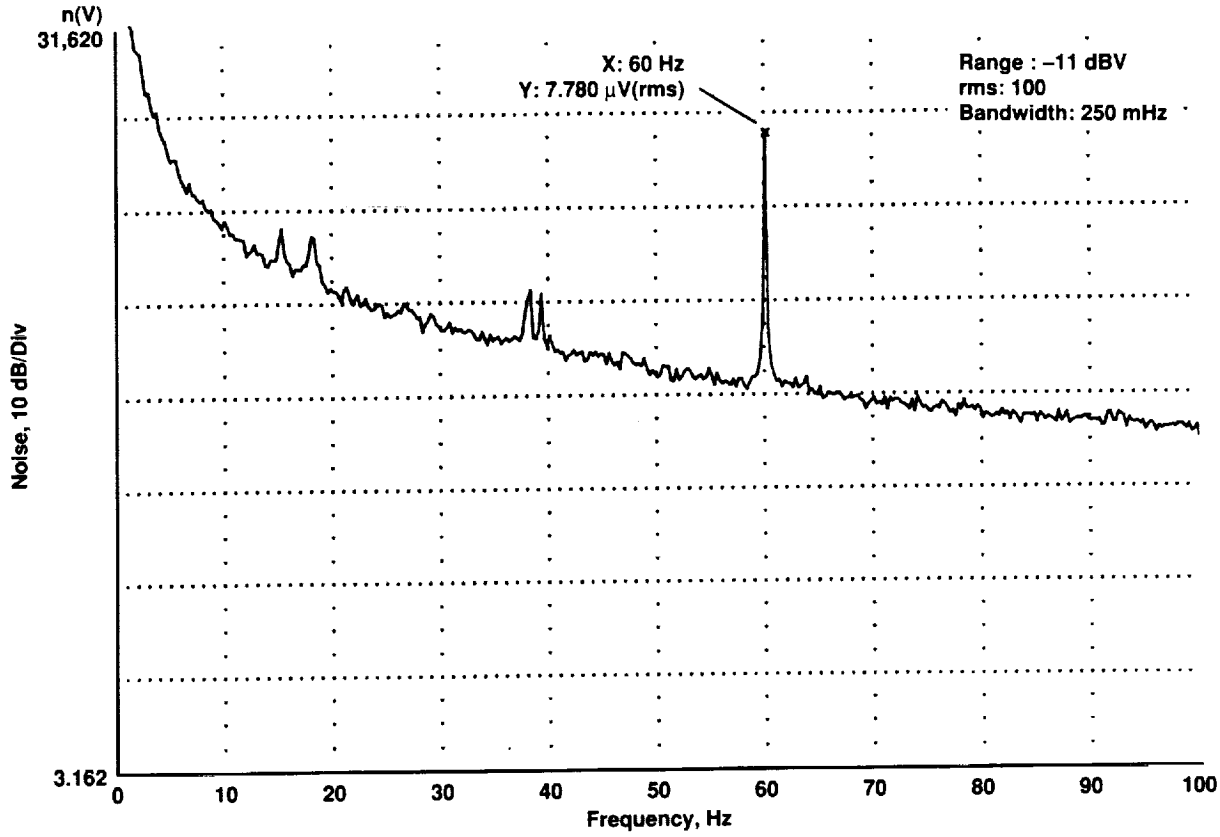

Figure 37. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, V_{Det} = 0.75 V, R_B = 2 x 10^8 Ω, raw data.

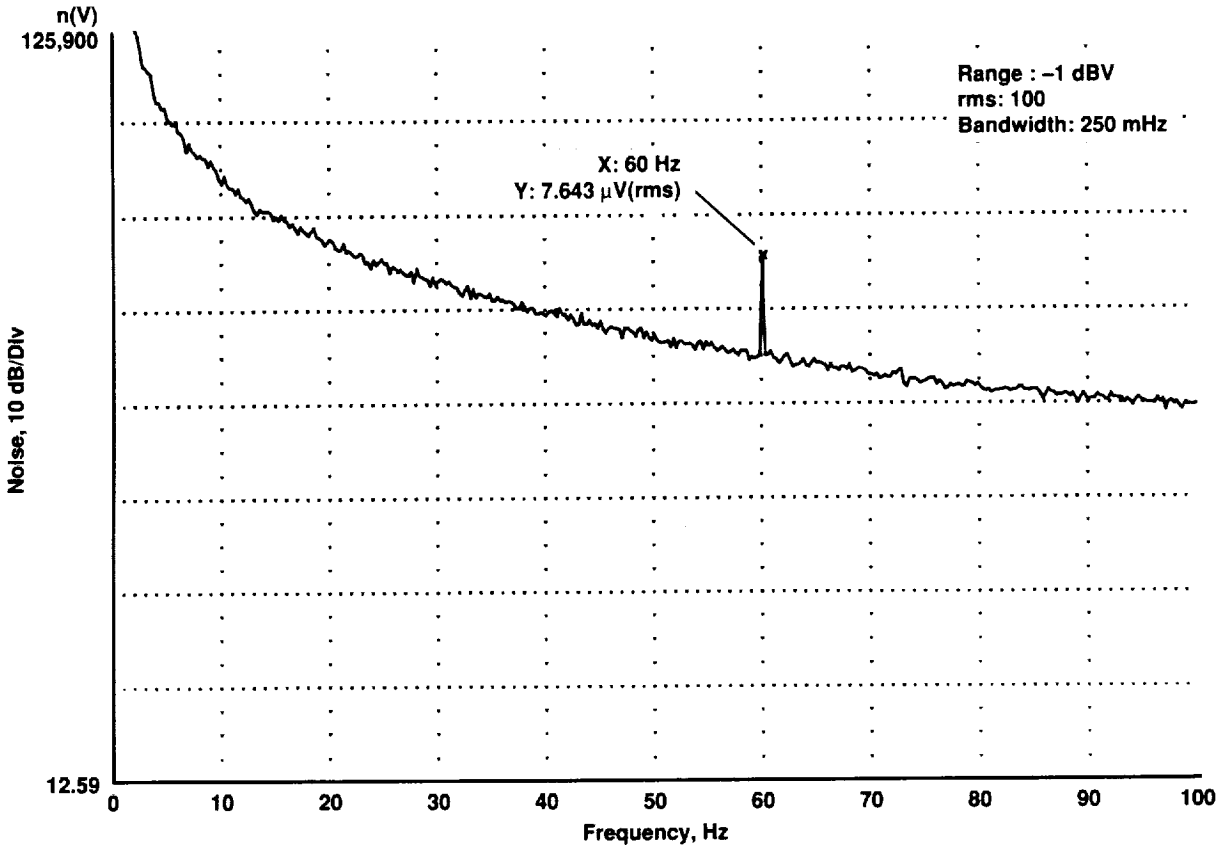

Figure 38. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, V_{Det} = –0.75 V, R_B = 2 x 10^8 Ω, raw data.

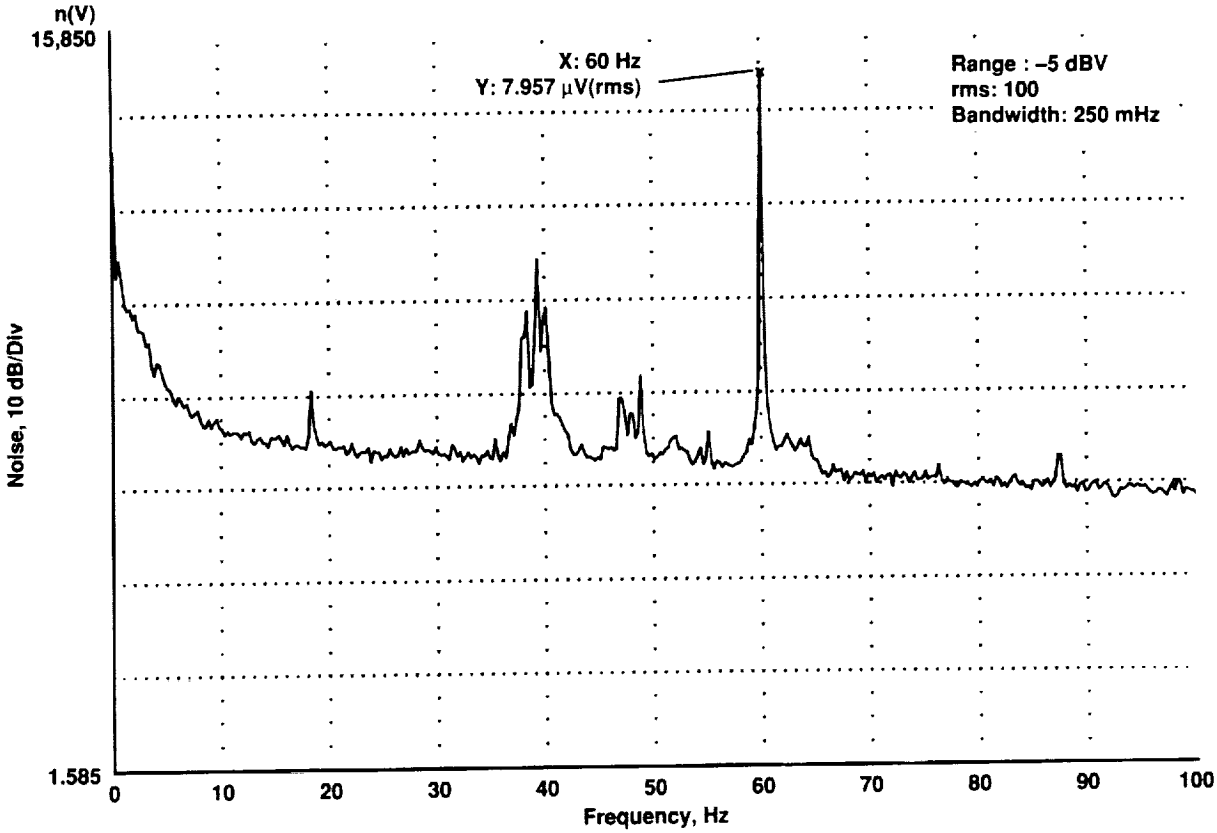

Figure 39. FET D3–8 at 7k: V_D = 3.0 V, R_S = 1kΩ, V_{Det} = 0.0 V, R_B = 2 x 10^8 Ω, raw data.

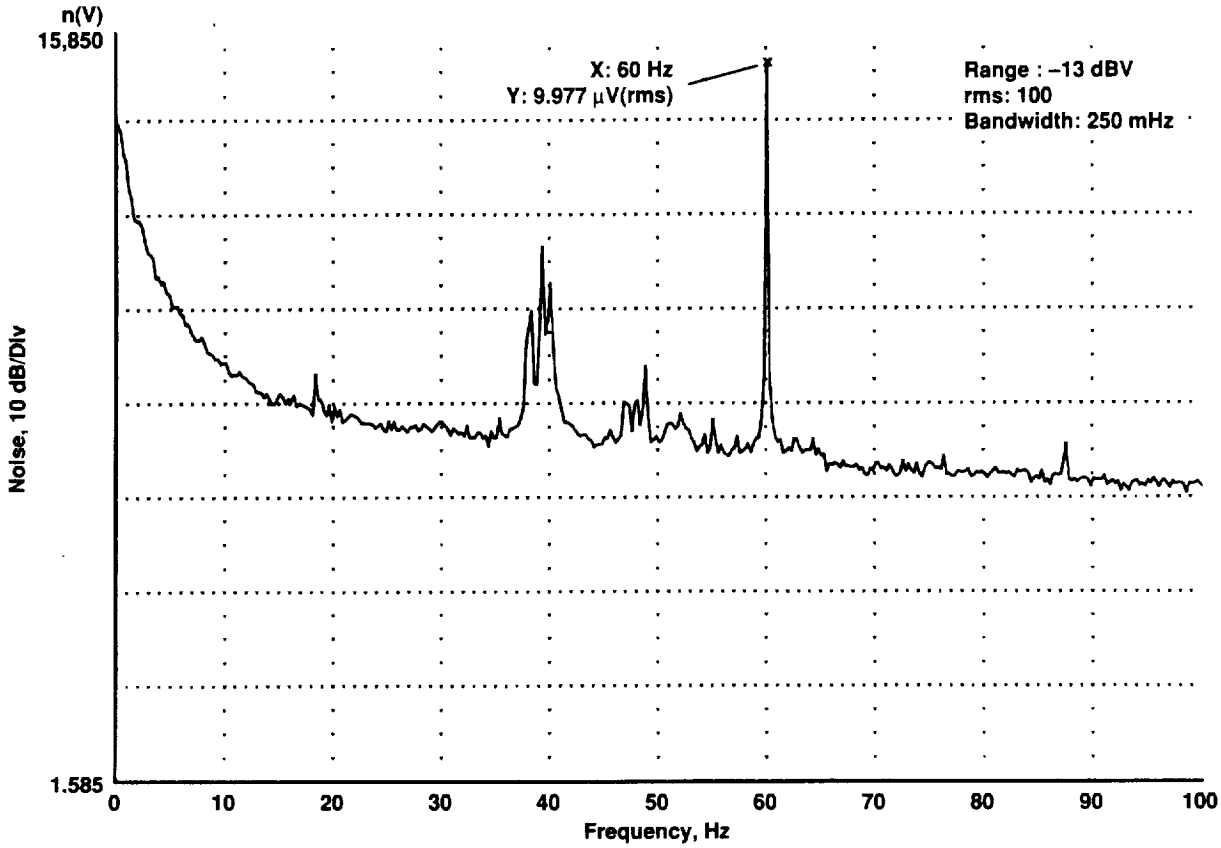

Figure 40. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, V_{Det} = 0.5, R_B = 2 x 10^8 Ω, raw data.

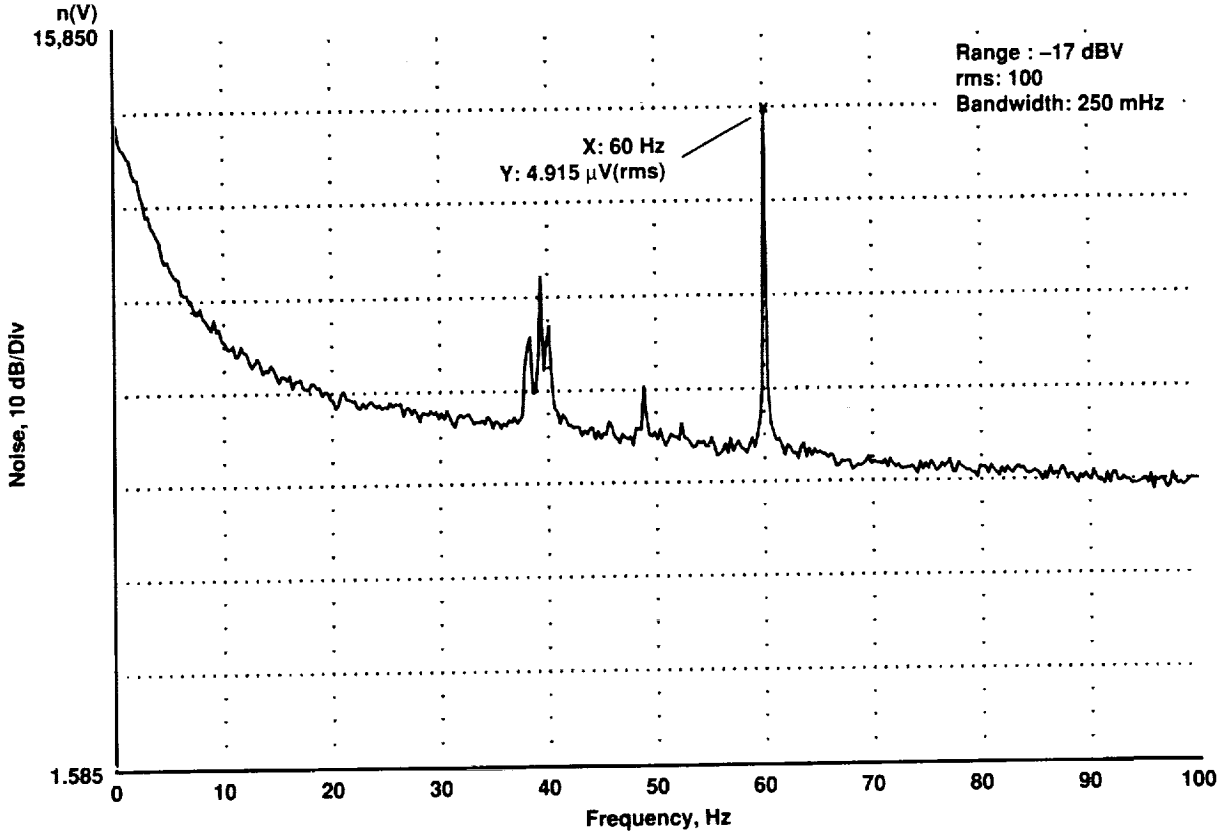

Figure 41. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, V_{Det} = –0.5 V. R_B = 2 x 10^8 Ω, raw data.

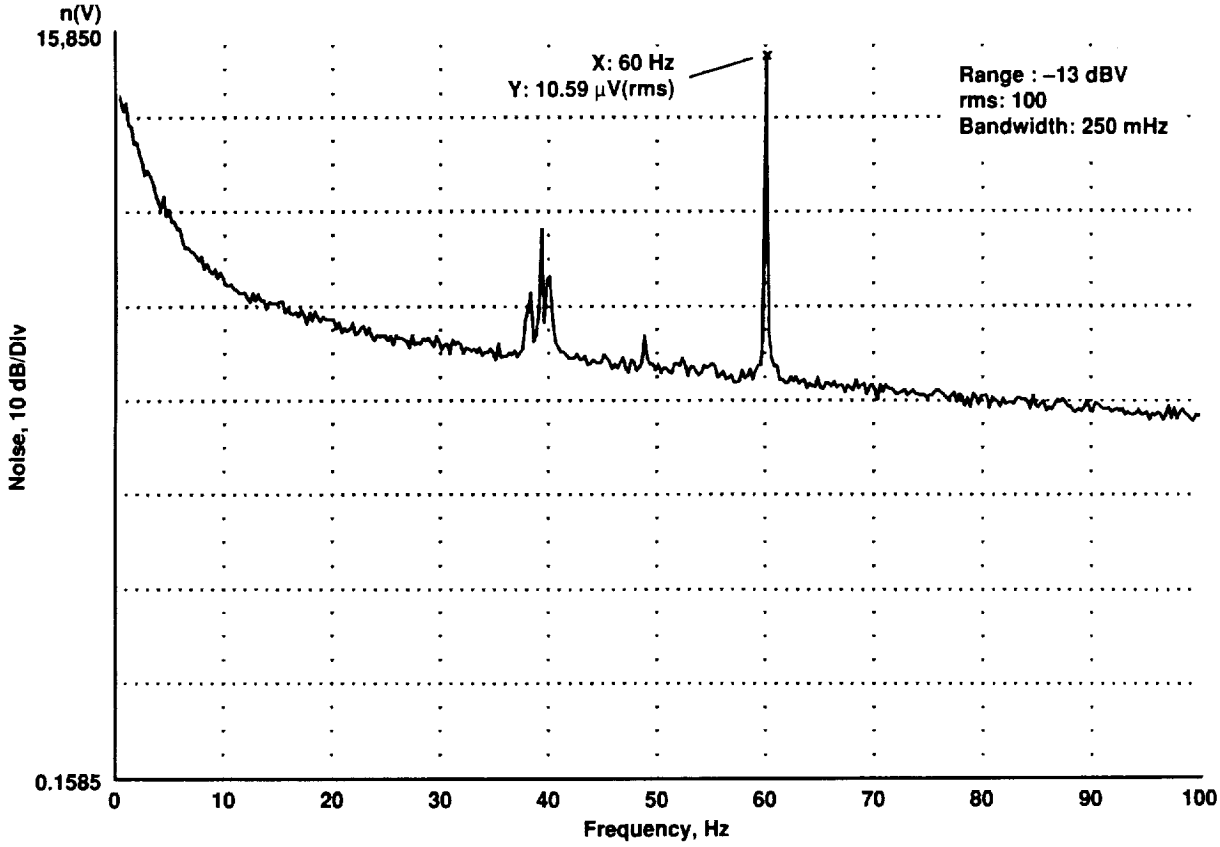

Figure 42. FET D3–8 at 7K: V_D = 3.0, R_S = 1kΩ, V_{Det} = 0.75 V, R_B = 2 x 10^8 Ω, raw data.

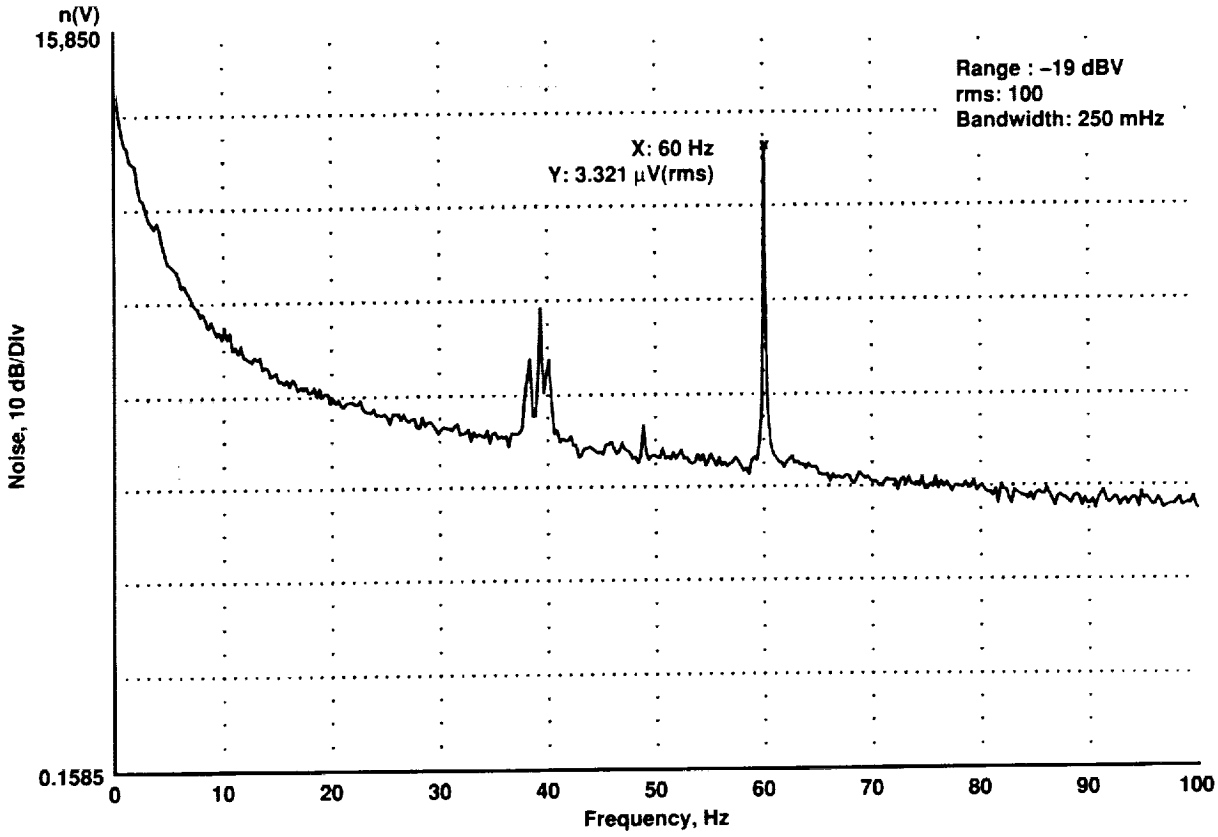

Figure 43. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ , V_{Det} = –0.75 V, R_B = 2 x 10^8 Ω, raw data.

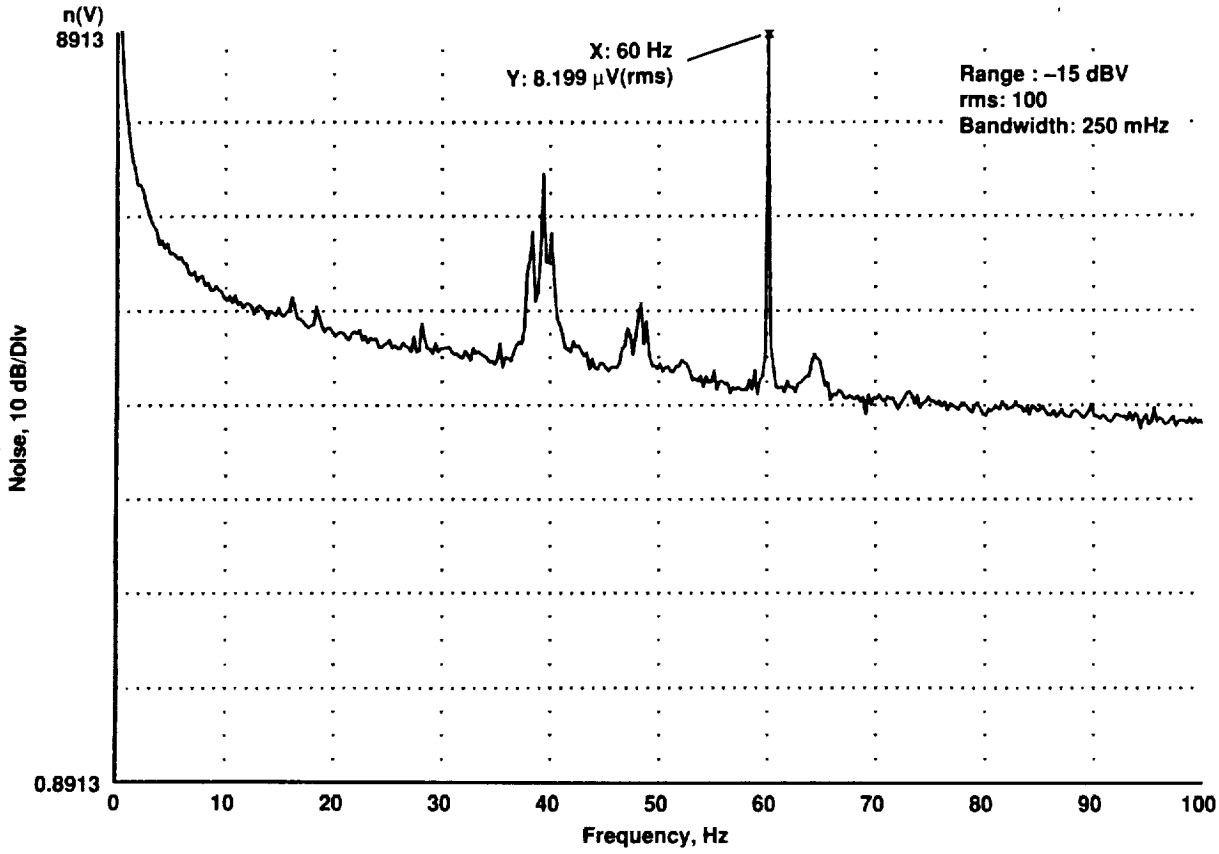

Figure 44. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, V_{Det} = 0.0 V, R_B = 2 x 10^8 Ω, raw data.

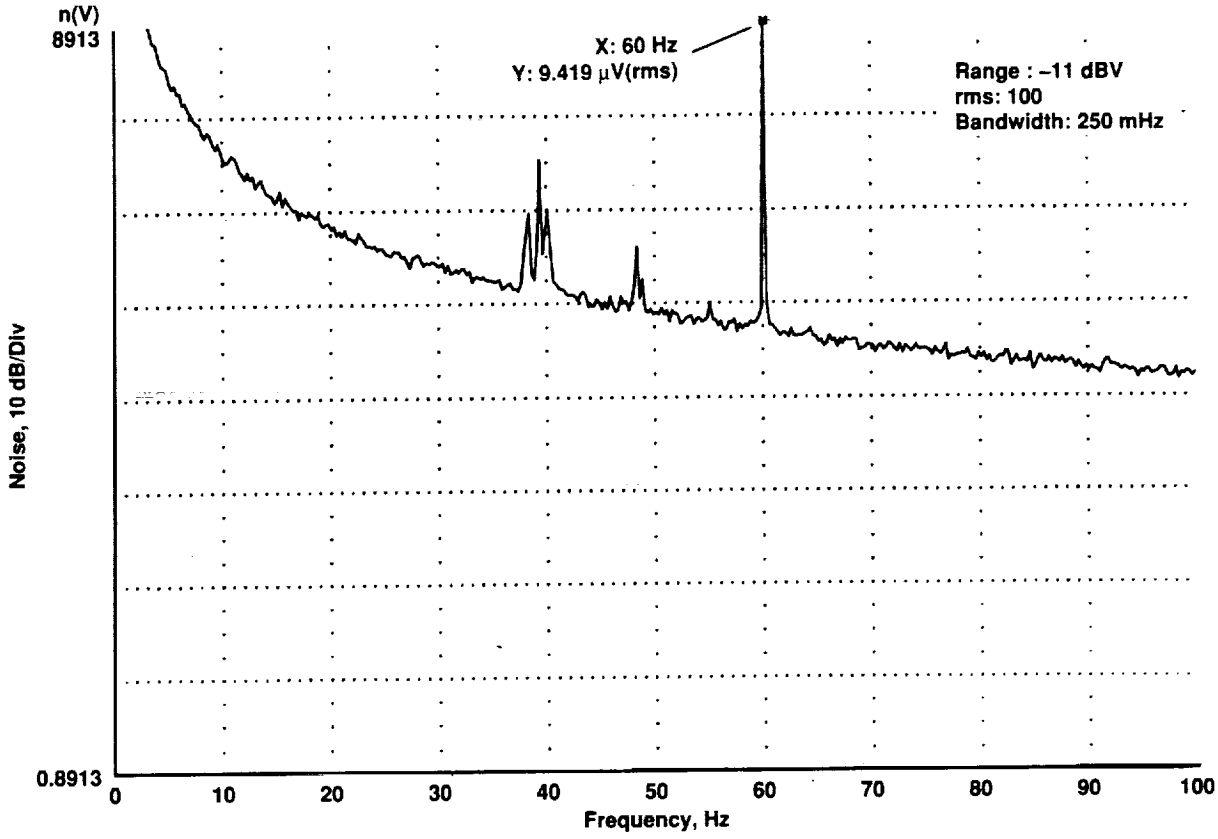

Figure 45. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, V_{Det} = 0.5, R_B = 2 x 10^8 Ω, raw data.

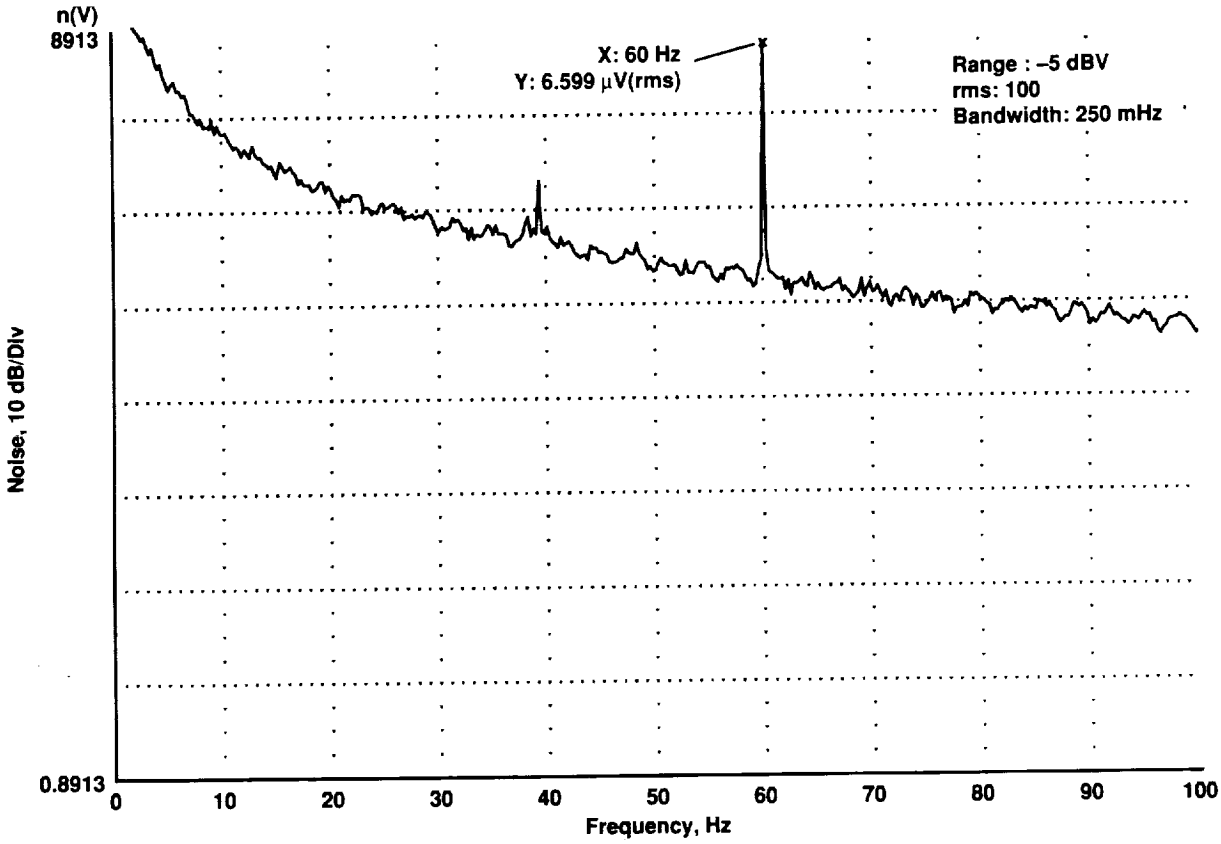

Figure 46. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, V_{Det} = –0.5, R_B = 2 x 10^8 Ω, raw data.

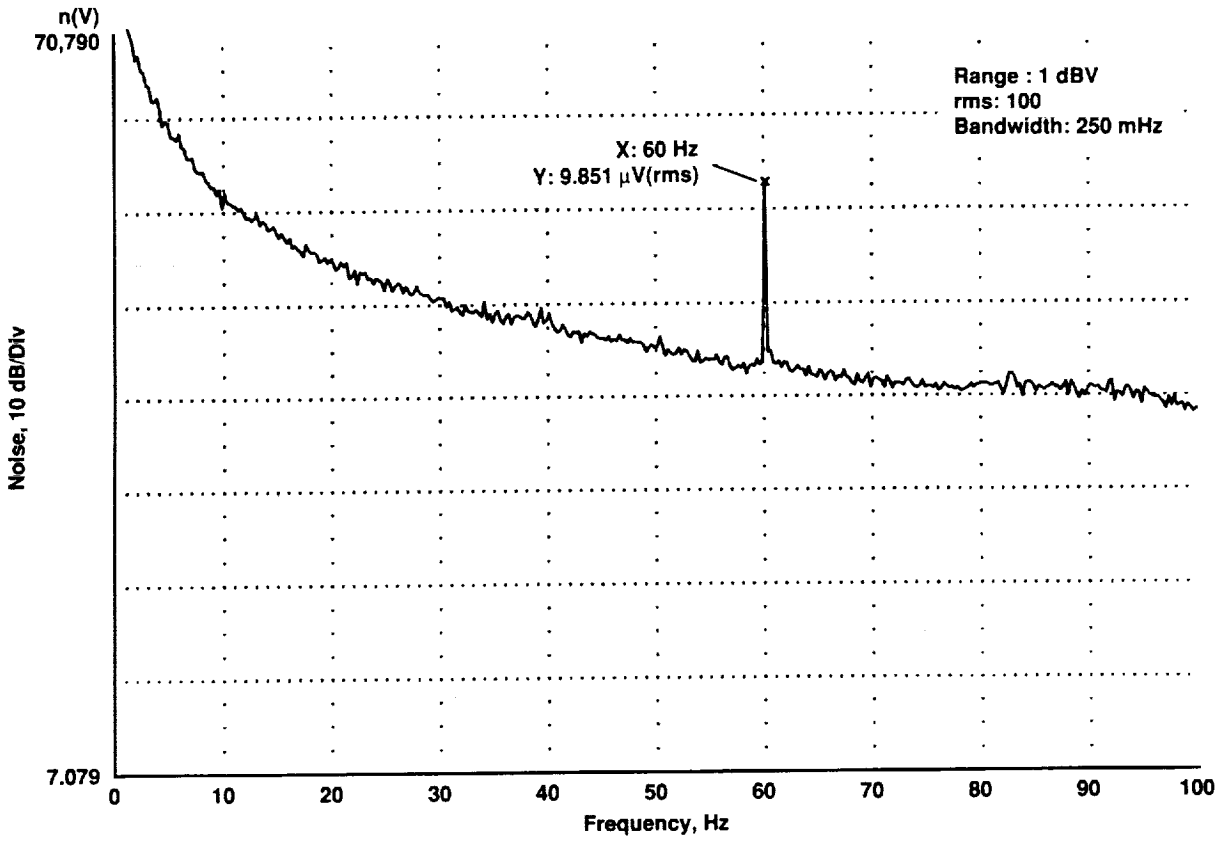

Figure 47. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, V_{Det} = 0.75 R_B = 2 x 10^8 Ω, raw data.

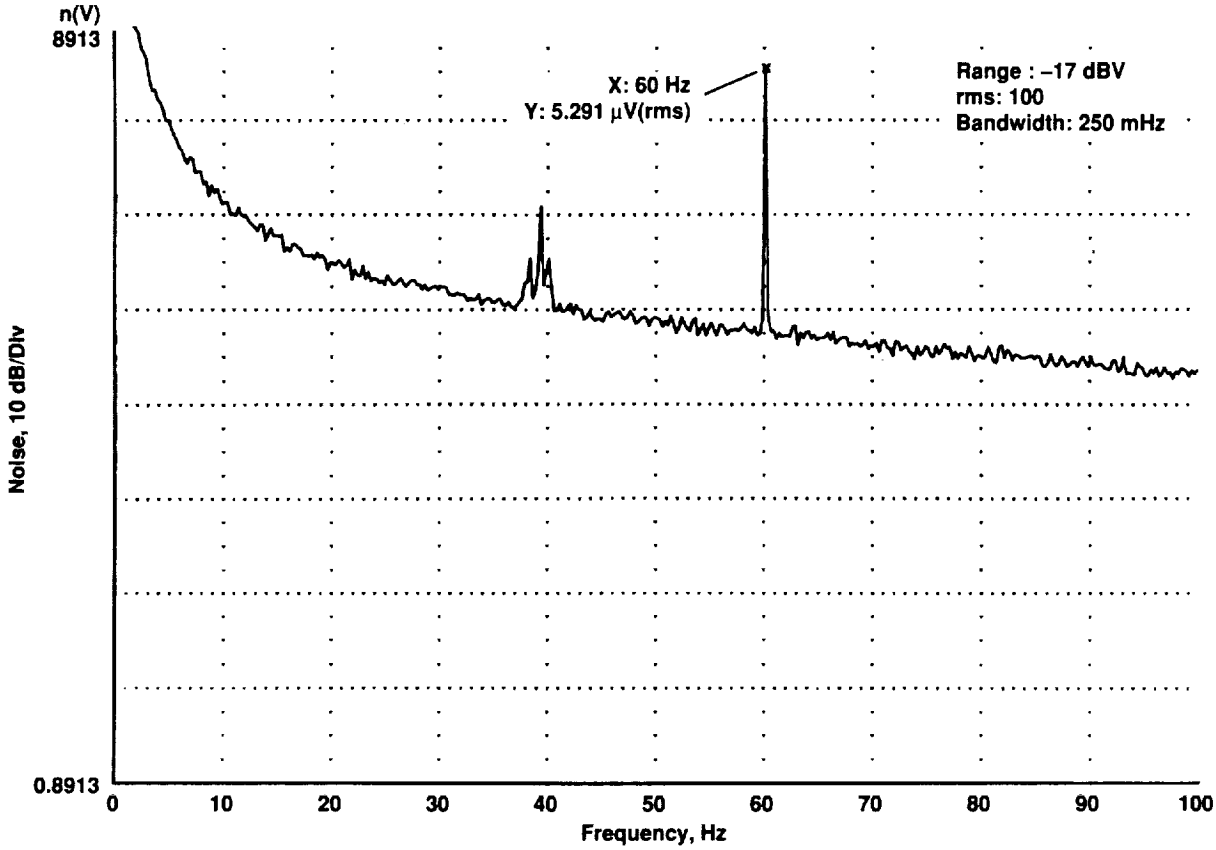

Figure 48. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, V_{Det} = –0.75 V, R_B = 2 x 10^8 Ω, raw data.

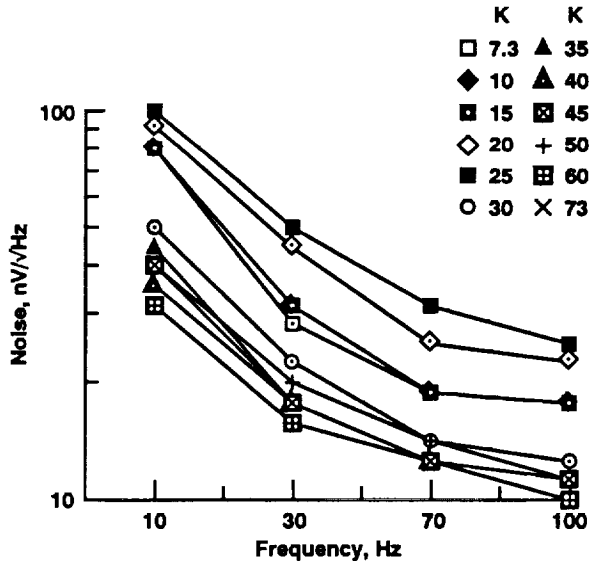

Figure 49. FET D3–8 warm-up curves.

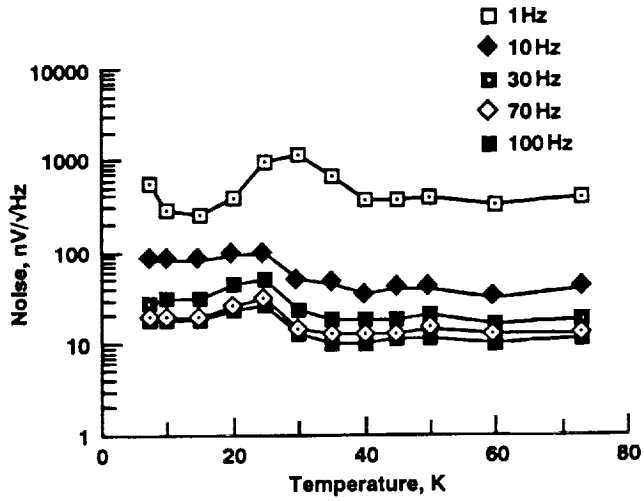

Figure 50. FET D3–8 warm-up data with gate floating.

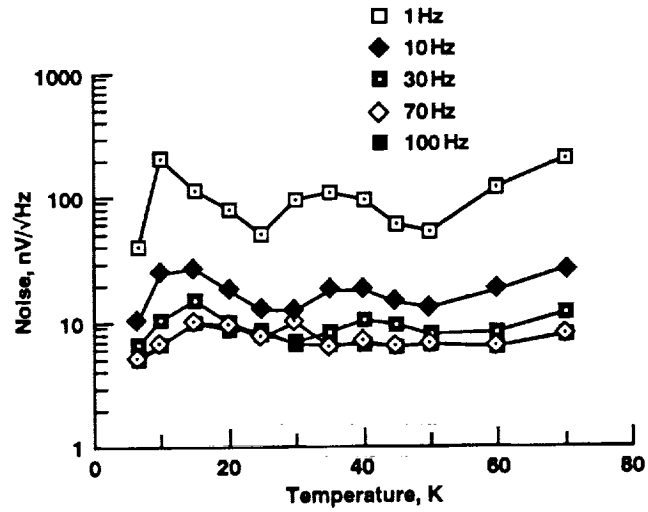

Figure 51. FET D3–8 warm-up data with gate grounded.

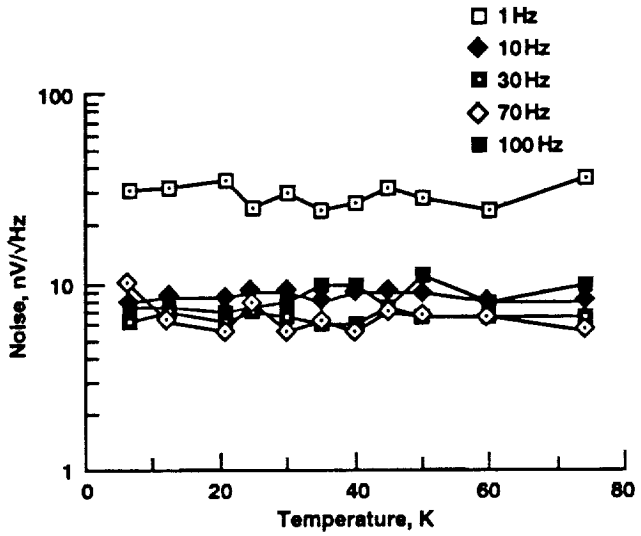

Figure 52. FET D3–8 warm-up data with detector and pinhole.

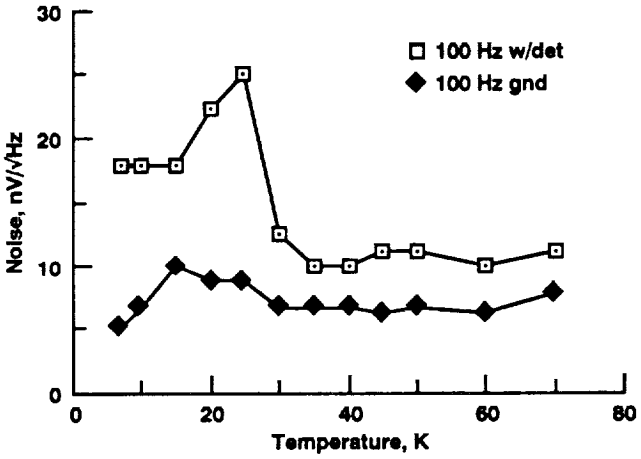

Figure 53. FET D3–8 100 Hz noise with detector or with gate grounded.

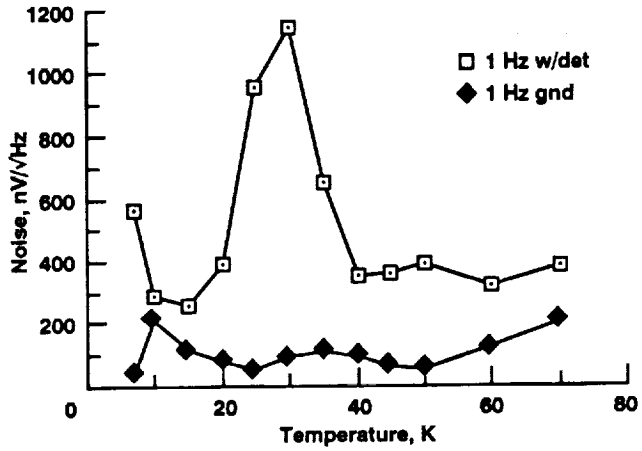

Figure 54. FET D3–8 1 Hz noise with detector or with gate grounded.

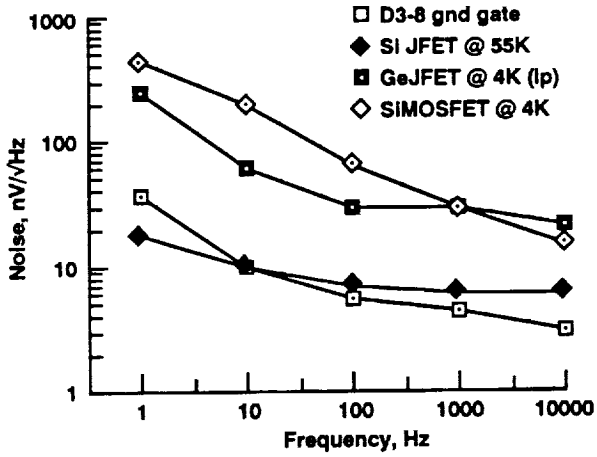

Figure 55. Noise spectrum comparison of various FETs.

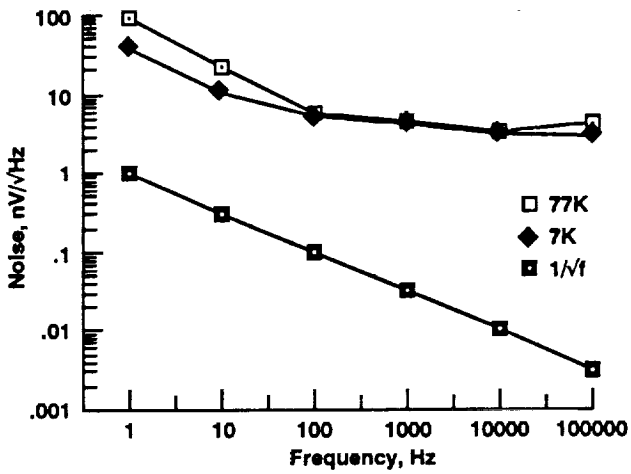

Figure 56. D3–8 noise spectrum compared to 1/√f curve.

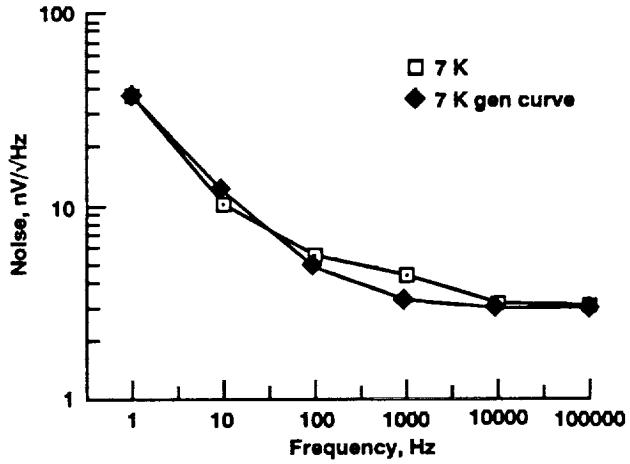

Figure 57. D3–8 noise spectrum and generated curve at 7K.

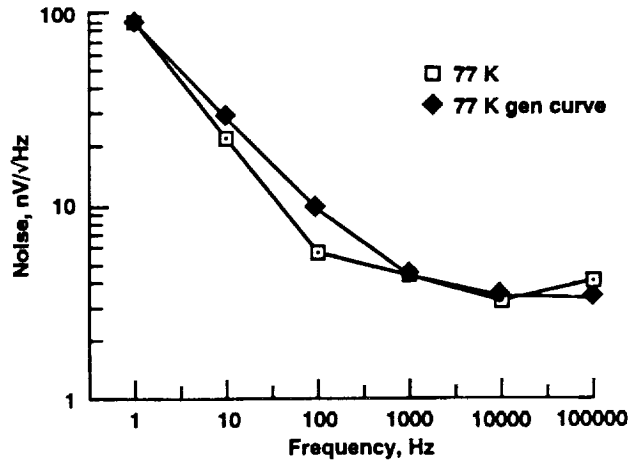

Figure 58. D3–8 noise spectrum and generated curve at 77K.

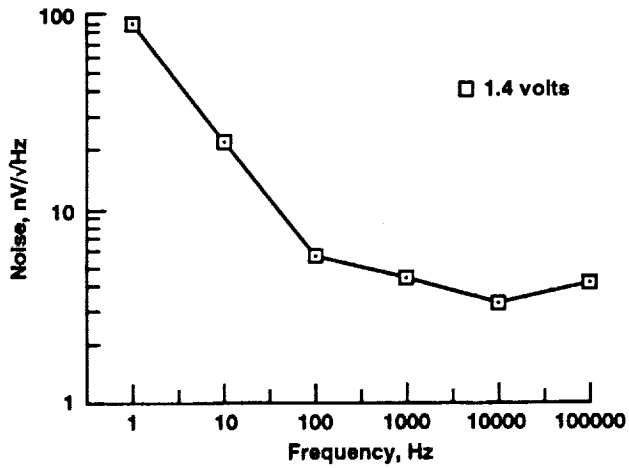

Figure 59. Noise spectrum of D3–8 at 77K in the grounded gate mode.

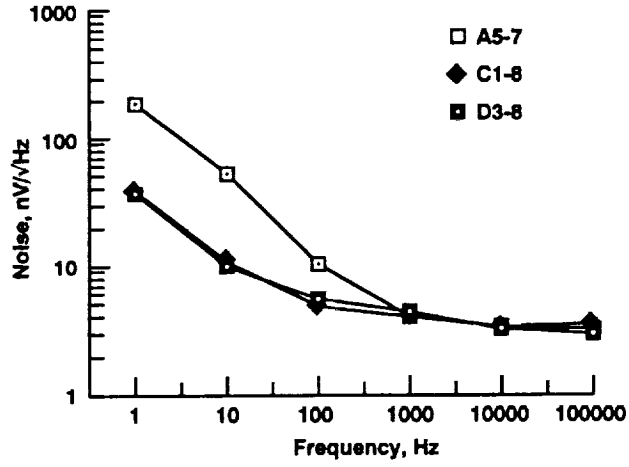

Figure 60. Noise spectrum comparison of FETs at 7K with 1kΩ source resistor.

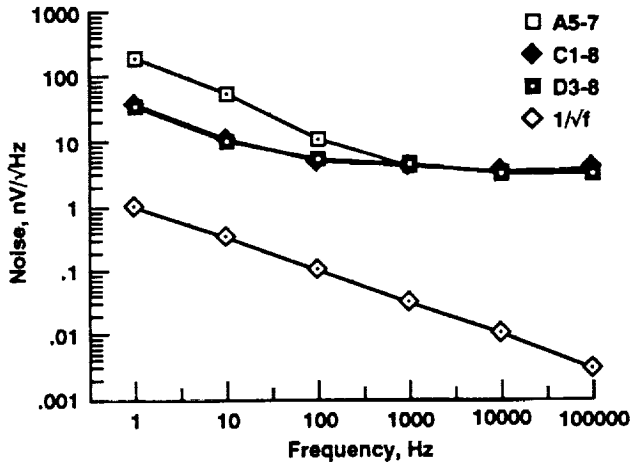

Figure 61. Noise spectra of three FETs plus 1/√f at 7K.

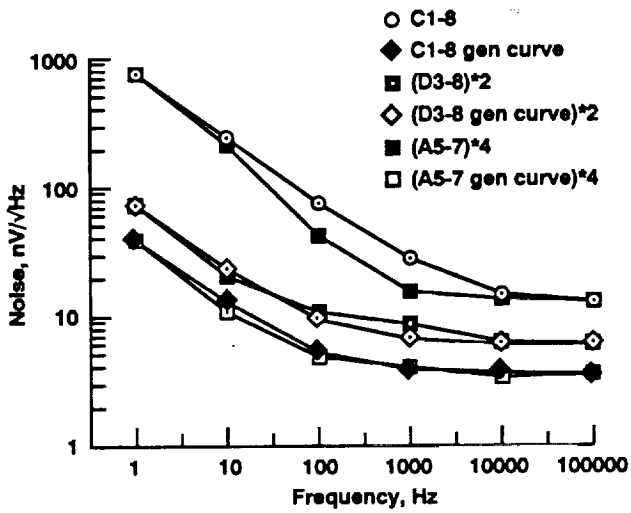

Figure 62. Noise spectra with generated curves at 7K.

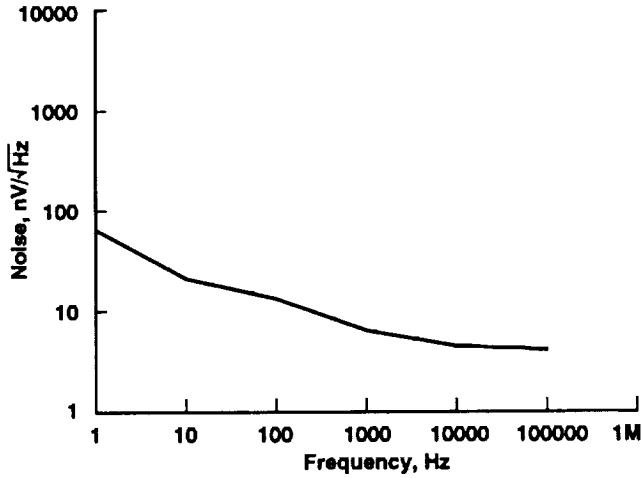

Figure 63. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1kΩ, gate open, summary data.

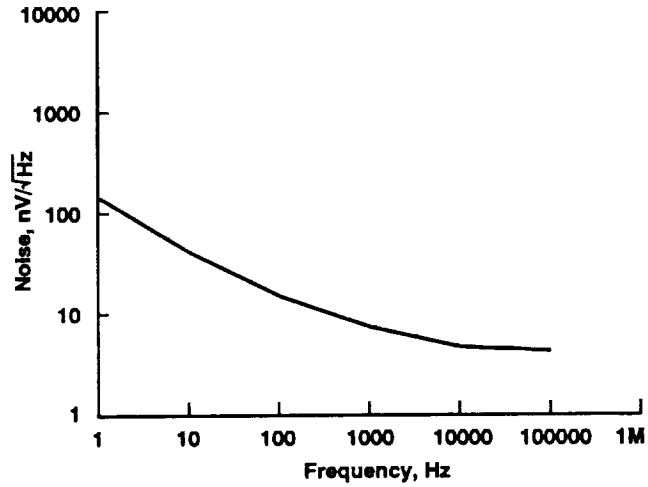

Figure 64. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, gate open, summary data.

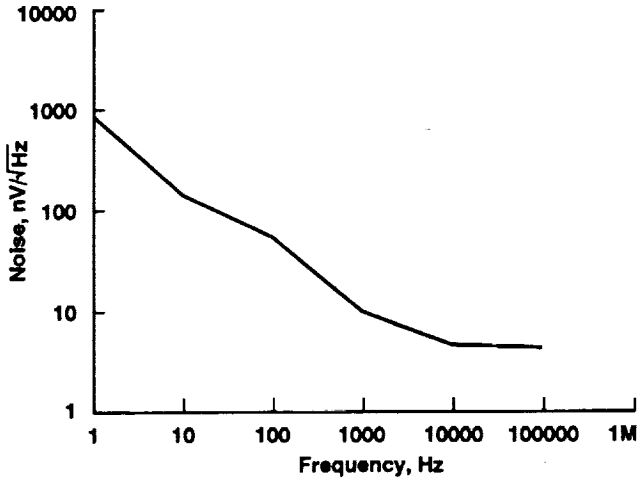

Figure 65. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate open, summary data.

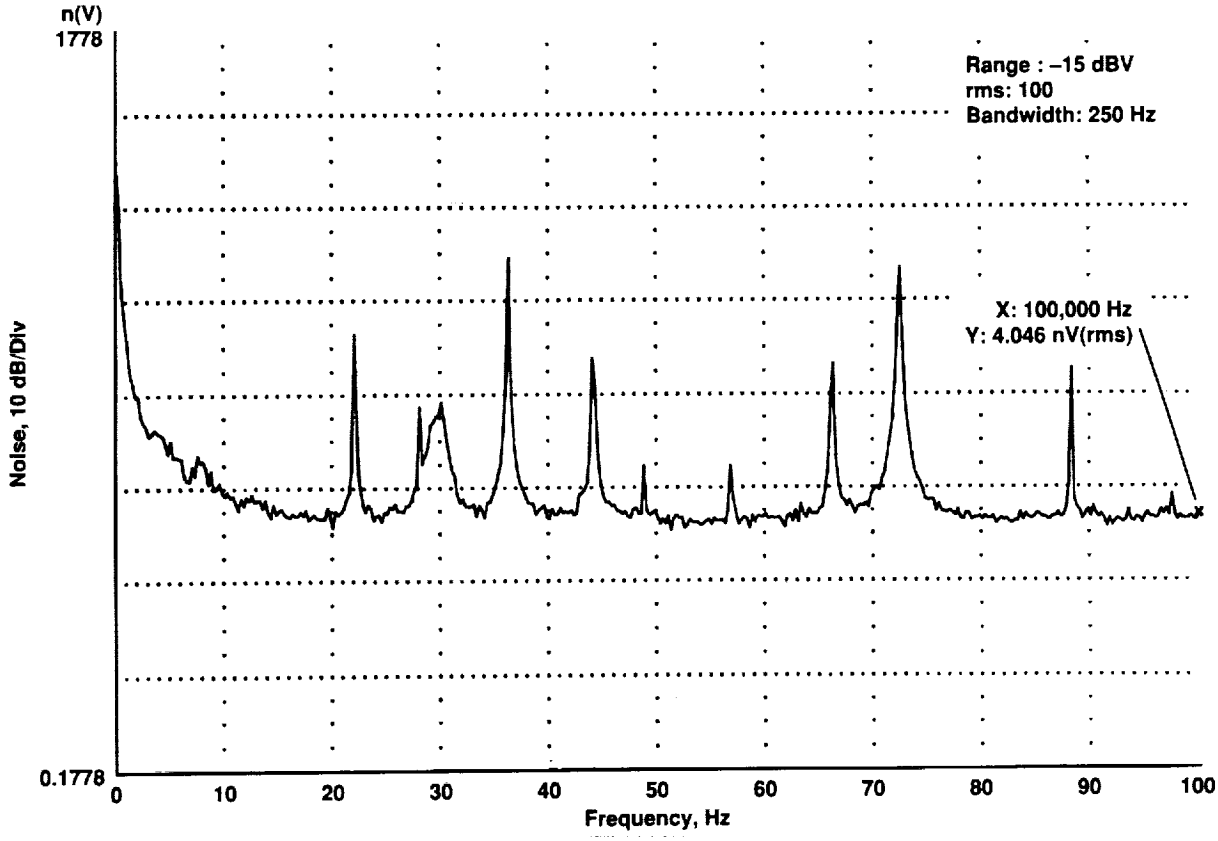

Figure 66. FET D3–8 at 7K: V_D = 1.4 V, system input noise, raw data.

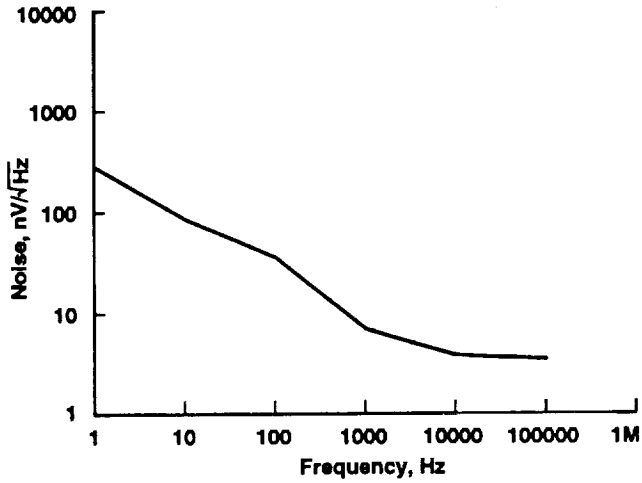

Figure 67. FET D3–8 at 7K: V_D = 1.4 V, R_S = 1KΩ, gate grounded through 2 x 10^8 Ω, summary data.

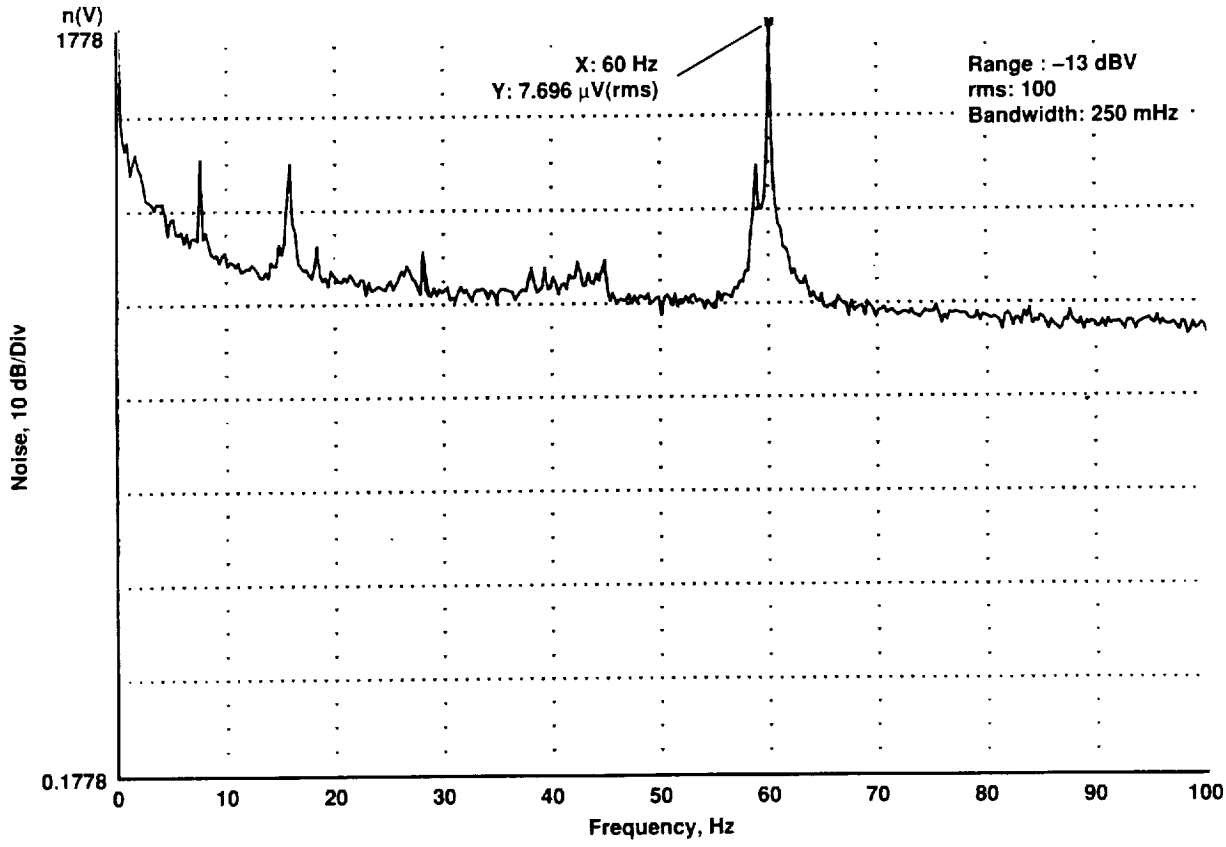

Figure 68. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, gate grounded through 2 x 10^8 Ω, raw data.

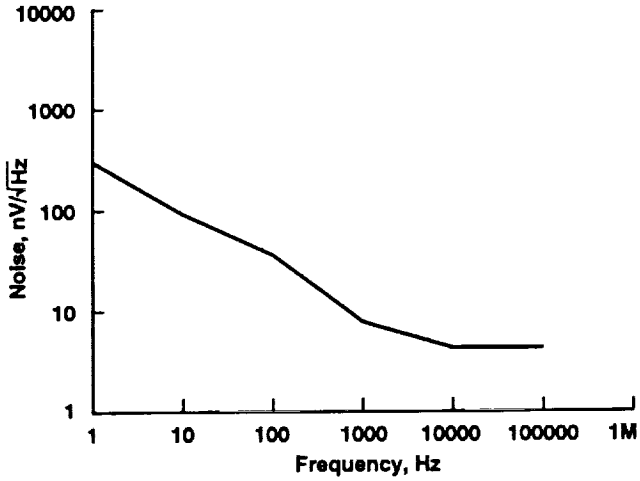

Figure 69. FET D3–8 at 7K: V_D = 3.0 V, R_S = 1kΩ, gate grounded through 2 x 10^8 Ω, summary data.

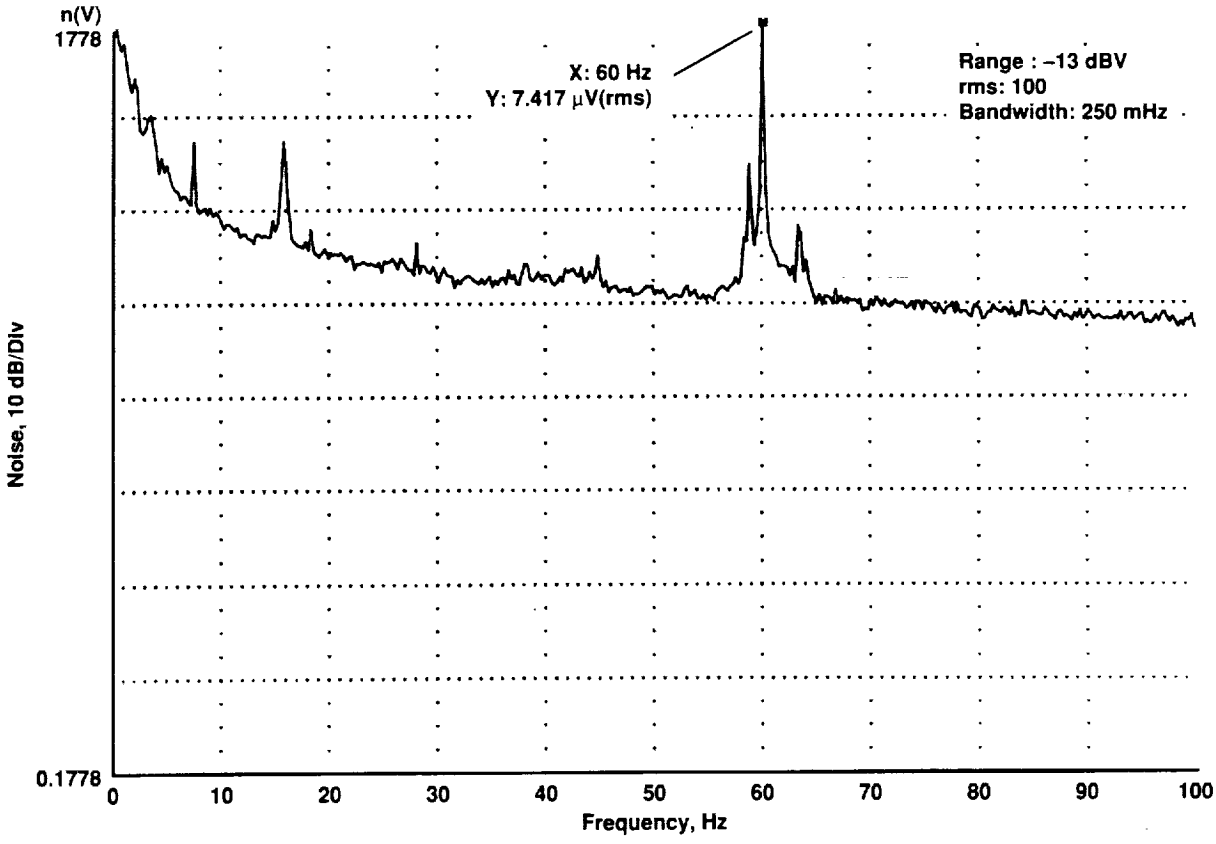

Figure 70. FET D3–8 at 7K: V_D = 5.0 V, R_S = 1kΩ, gate grounded through 2 x 10^8 Ω, raw data.

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13. ABSTRACT *(Maximum 200 words)*

The spectral noise characteristics of Aerojet gallium arsenide (GaAs) junction field effect transistors (JFETs) have been investigated down to liquid-helium temperatures. Noise characterization was performed with the field effect transistor (FET) (1) in the floating-gate mode, (2) in the grounded-gate mode to determine the lowest noise readings possible, and (3) with an extrinsic silicon photodetector at various detector bias voltages to determine optimum operating conditions. The measurements indicate that the Aerojet GaAs JFET is a quiet and stable device at liquid helium temperatures. Hence, it can be considered a readout line driver or infrared detector preamplifier as well as a host of other cryogenic applications. Its noise performance is superior to silicon (Si) metal oxide semiconductor field effect transistor (MOSFETs) operating at liquid helium temperatures, and is equal to the best Si n channel junction field effect transistor (n-JFETs) operating at 300 K.

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