Technology, Design, Simulation, and Evaluation for SEP-Hardened Circuits

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Abstract- **This paper describes the technology, design, simulation, and evaluation for improvement of the SEP hardness of gate-array and SRAM cells. Through the use of design and processing techniques, it is possible to achieve an SEP error rate less than 1.0E-10 errors/bit-day for a 90worst-case geosynchronous orbit environment.**

1 Single Event Upset

Single Event Phenomenon (SEP) occurs when a particle or heavy ion interacts with the silicon, depositing charge on critical circuit nodes, causing data loss. Devices that retain data (RAMs and flip-flops, for example) are subject to SEP, and a particle interaction in one part of the chip can cause data loss in a circuit located far away. Non-storage nodes can propagate the pulse to other circuit nodes, but no permanent data will be lost. Storage devices like RAMs, latches, and flip-flops may detect false clock pulses, or reset signals caused by a pulse on a circuit node somewhere in the clock, or reset generation and buffering circuitry, and lose data.

The storage node critical charge, Q_c, is the amount of charge that must be deposited on the storage node in order to upset the stored data. Increasing the critical charge for the sensitive nodes in a cell will decrease the SEP error rate by lowering the probability of encountering an ion with sufficient LET value to upset the cell. This critical charge can be increased by changing the transistor sizes to make the cell more stable, adding parallel paths in the cell, and increasing the feedback switching time. A more stable storage cell will require a greater voltage change on the storage node, or a longer voltage pulse to disturb the data.

2 Charge Deposition Model

In the past, the literature has implied that the charge generated by a single event may be modeled by using an ideal current source with an exponential time decay. Using this method, the current source is connected directly to the sensitive node, and the charge applied is the time integral of the current pulse. This method can over-predict the value of the critical charge for the memory cell because the current source causes the junction to which the current source is applied to become forward biased and sink a significant

amount of charge to the power supply. Physically, the charge collection process is self-limiting, and the junction will never conduct current in the forward direction. This is a very common error which has led to substantially over-predicting the SEP hardness of a particular design. This can lead to substantially higher SEP error rates in the circuit than can be tolerated by the system design. In this paper, we describe process, simulation, and design techniques that may be used to improve the SEP hardness of CMOS circuits.

3 SEP Simulation

We have used both HSPICE and DAVINCI (tm) [1] to model SEP phenomenon. In the SPICE simulation, the cell sub-circuit is accurately modeled using device parameters which have been demonstrated to correlate with measured silicon values. Figure 1 shows the sub-circuits that model the charge deposition. They use idealized MOS devices as switches, and standard SPICE components for everything else. This modeling technique prevents forward-biasing of the junction and provides a more accurate simulation of the charge required for circuit upset [2]. An internal node, Ndep, is initialized to a voltage, Vdep, by switch N3 where $Vdep \times Cdep = Qdep$ (Qdep is the simulated deposited charge). A switch, P2 or N2, is turned on in approximately 0.1 ns, shorting the node under test to a power supply through a resistor that represents the resistance of the bulk silicon.
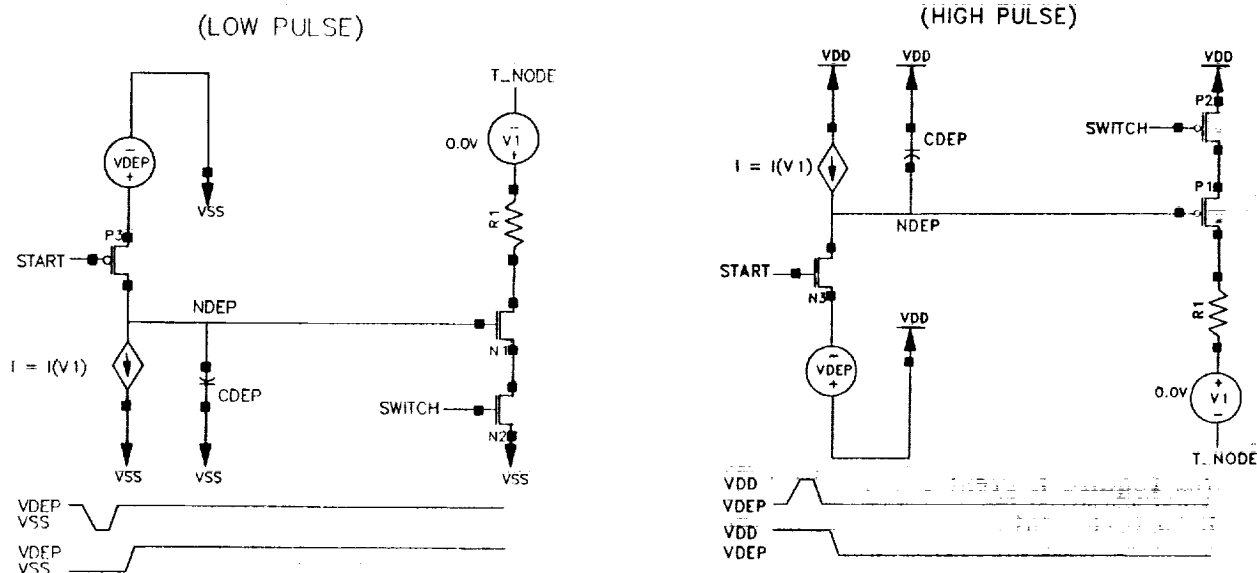

Figure 1: SPICE Charge Deposition Circuit

As charges are added to the node under test, the same amount of charge is removed from the internal node Ndep. When the internal node Ndep is depleted of charge, a switch, P1 or N1, turns off so the circuit can recover its node voltages. A similar but slightly different version of this charge deposition model is used for p+/n- and n-/p+ junction interactions. This technique has proven extremely valuable to optimize the design and layout of logic and memory circuits for SEP hardness.

Numerical simulation of the charge deposition from a heavy ion hit has been attempted by others. [3,4] We have performed three-dimensional numerical simulation of single event upset using the three-dimensional simulator, DAVINCI tm. The simulations were performed on an n-channel junction of a twin-tub CMOS device with approximately 4 um of an epitaxial layer. In figure 2, the potential contours of the device junction are shown 48 ps after a single event hit with a gold ion. Note that the n+ junction is no longer at five volts and that the distribution of the funnel favors the epi/p-well junction. As the voltage at the n+ junction is reduced, there is less potential difference to the funnel as opposed to the potential difference of the funnel to the epi, which is held at five volts.

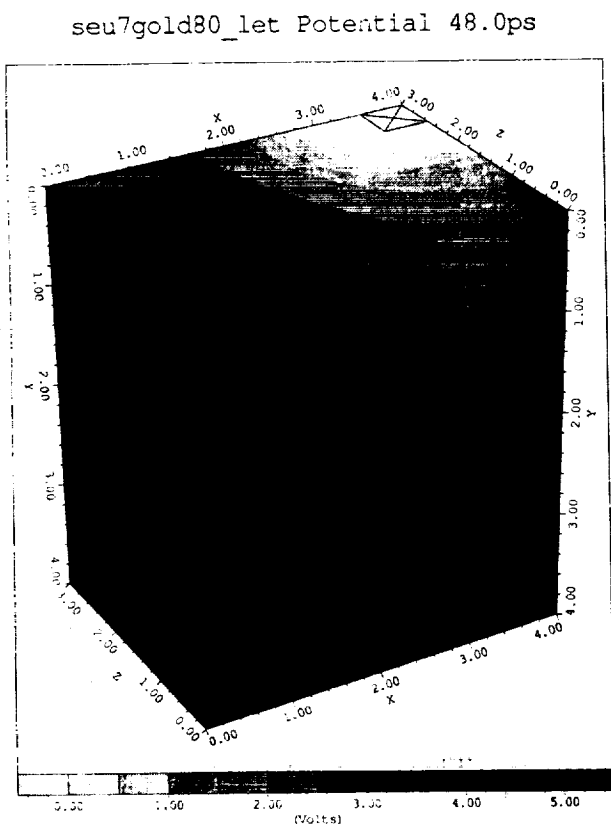seu7gold80_let Potential 48.0ps   seu7- Node Voltages

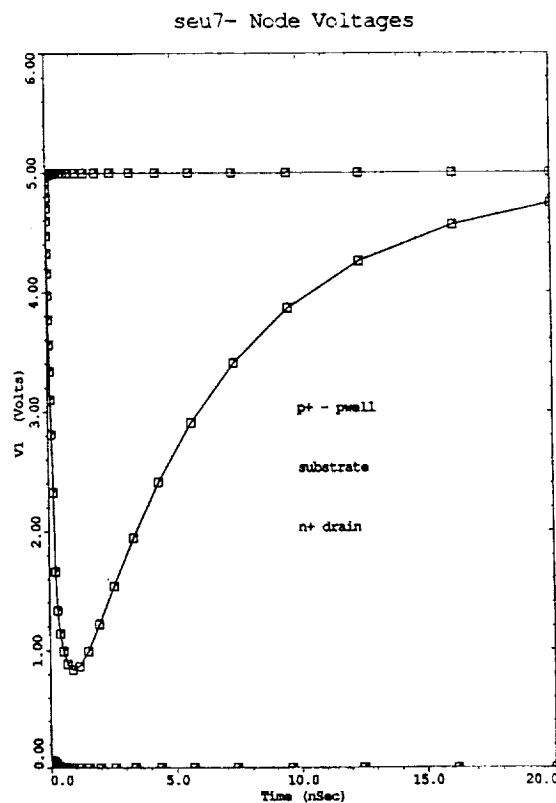Figure 2: Junction Potential After Ion Strike

Figure 3: n+ junction vs. p-well and substrate

Figure 3 shows the potential of the n+ junction relative to the p-well contact and epi substrate contact. Note that the time constant is ~5-10 ps. Whether a flip-flop will change state as a result of this SEP event will depend upon how long the n+ junction potential is below the switch point of the cell. The n+ junction can go to zero volts and not cause an upset if it recovers before the zero can propagate back through the cross-coupled logic. We have found DAVINCI tm useful for looking at wafer fabrication process methods for SEP hardening of CMOS devices, as it enables the evaluation of effects of doping concentration, epi thickness, etc.

4 Heavy Ion Testing And SEP Numerical Calculation

Heavy ion testing for this work was performed at Brookhaven National Laboratories, using their Tandem Van de Graaff system. Three ion conditions were chosen for this testing. They included Gold at 350 MeV, Iodine at 320 MeV and Bromine at 285 MeV. The LET values were further varied by adjusting the angle of incidence from 0 to 60 degrees.

To determine the SEP error rate from measured data, the effective cross- section is selected at an LET of 100 $MeV \times cm2/mg$ (surface value). The upset rate calculation can be performed using either CREME [5] or SpaceRad [6] programs. The simulation conditions for determining the error rates quoted in this paper are as follows:

1. Geosynchronous circular orbit, 35900 km;

2. Orbital inclination, 0 degrees;

3. Adams 90% worst-case environment, including the earth's shadow and geomagnetic storms;

4. All ions from Hydrogen through Uranium $1 < Z < 92$.

5 Process Techniques For SEP Hardening Of CMOS Devices

Wafer fabrication processing can have a strong effect on the SEP sensitivity of CMOS circuits. As shown in the DAVINCI tm simulations above, over half of the charge deposited by a heavy ion can be collected at the epitaxial junction, away from sensitive circuit nodes, if the epitaxial layer is sufficiently thin. Also, because the drive current of p-channel devices is typically less than that of n-channel devices, the most SEP-sensitive nodes tend to be n-channel nodes supported by p-channel transistors. Therefore, to minimize the charge collection on these nodes, a p-well type process is desirable since the p-well-to-substrate junction will help to collect a substantial portion of the deposited charge.

Also, because n-type dopants (n-type substrates are used for a p-well process) diffuse much slower than p-type dopants, it is possible to fabricate much thinner epitaxial layers for a p-well process, further improving the SEP sensitivity of the technology. The lower sheet resistances and (typically) higher doping of a p-well process also help to eliminate SEP-induced latch-up. High doping concentrations also help to increase the junction capacitance, further improving SEP susceptibility. Thin gate oxide also increases node capacitance, thereby increasing the critical charge on a node and improving SEP hardness. Poly-resistors or natural p-channel transistors can also be added to the process to allow the design of high-density SEP-hardened memory cells.

SOS and SOI (Silicon-On-Sapphire and Silicon-On-Insulator) processes reduce the amount of charge collected on the junction and the effective critical charge on each node. Thin-film SOI devices are also sensitive to bipolar snap-back. This has the effect of making

the channel region of the n-channel transistors sensitive to SEP upset. Therefore it is not sufficient to process a design on SOS/SOI substrates to obtain good SEP performance. Design and special processing techniques must be used also to assure SEP hardness of the circuits.

Commercial CMOS wafer fabrication processes usually do not consider SEP upset and latchup in their design. They are optimized for speed and density, both of which can compromise good SEP performance. UTMC has designed its twin-tub epitaxial p-well CMOS process (including poly-resistors) and layout rules to provide an optimum balance between good SEP performance, latchup immunity, speed, and density.

6   SEP Hardening Techniques For Memory Circuits

In the design of memory systems, several techniques may be used to provide SEP-insensitive memory systems. These include the use of redundant memory with voting logic and/or error detection and correction. Both of these techniques require additional system overhead and result in a degradation of system performance, as well as increased cost and weight. Some systems cannot afford this additional overhead, and therefore require the use of SEP-hard SRAMs.

Several SEP hardening techniques for SRAM memory cells have been reported in the literature. These include the use of cross-coupled resistors, cross-coupled capacitors, and cross-coupled p-channel transistors. [7,8] A schematic diagram of a memory cell with cross-coupled resistors (as used in UTMC's rad-hard 64K SRAM) is shown in figure 4. All of these techniques serve to increase the write time constant of the cell, thereby increasing the effective critical charge on the internal nodes of the cell. All of the techniques increase the wafer fabrication processing complexity and the area of the SRAM cell. The advantages and disadvantages of each are shown in Table 1.
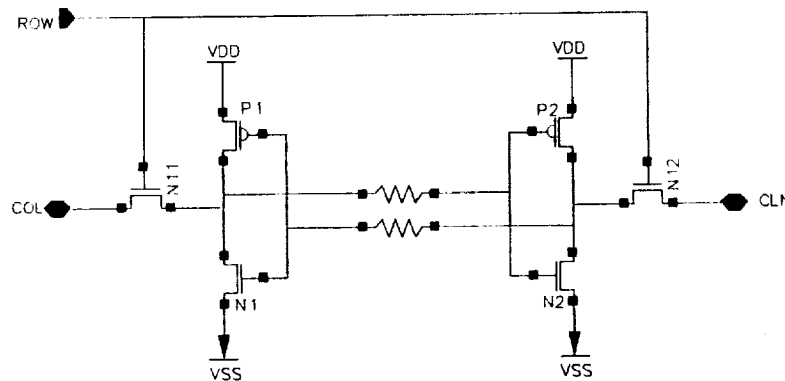

Figure 4: Memory Cell Schematic

Today, cross-coupled resistors are used in many SEP-hard designs primarily because the processing required to add and control the resistors is a relatively straight forward extension of standard CMOS SRAM processing techniques. However, if proper care is not taken to optimize the cell layout for performance, SEP sensitivity, and resistor tolerance,

SRAM Cell Hardening Technique	Advantages	Disadvantages
Cross-coupled resistors	Known processing. First published technique.	TCR of resistor causes SEP sensitivity to change over temperature. Cell area. Effects of resistor geometry.
Cross-coupled capacitors	Minimum variation of SEU with temperature.	Cap oxide defect sensitivity. Cell area.
Cross-coupled transistors	Minimum cell area.*	Process control on transistor Vt.

* Technology and layout dependent

Table 1: Advantages and Disadvantages of SRAM SEP-Hardening Techniques

SEP performance may be greatly degraded at high temperature (above 85 C), and write cycle time may be degraded at low temperature (-55 C).

6.1   SEP-Hardened Memory Design

We have taken great care to optimize the performance of the rad-hard 64K SRAM over the entire military temperature range (-55 C to 125 C). The size of the transistors in the cell were optimized in concert with the cross-coupled resistor values using the SPICE simulation techniques described earlier to assure that the product would be manufacturable and meet data sheet specifications, including a 1E-10 error/bit/day requirement, over the entire military temperature range. UTMC's 64K SRAM memory cell is more stable than most SRAM memory cells because the p-channel transistor in the 64K SRAM memory cell is larger than the n-channel transistor and will supply almost as much current. The increased p-channel size increases the switch point of the cross-coupled inverters from approximately Vtn (0.8 V) to approximately Vdd/2 (2.5 V). The increased switch point requires that a particle-induced voltage pulse on one of the storage nodes exceeds Vdd/2 instead of Vtn before the other storage node can be affected. A more stable memory cell is harder to write and requires additional area. The increased p-channel transistor size increases the die size by approximately 7%.

In UTMC's 64K SRAM, the write time specification can be met even with the more stable memory cell because the write circuitry forces the memory cell columns to Vdd and Gnd during a write operation. Although the write circuitry that provides Vdd and Gnd is larger than a standard write circuit that only provides Gnd, it increases the die size by less than 0.5%.

The 64K SRAM uses high-valued polysilicon resistors in series with the gates of both cross-coupled inverters and increased capacitance on the storage nodes to increase the

feedback switching time. Increased stability and increased feedback switching time provide improved SEP protection. The 64K SRAM can use a lower valued resistor because the memory cell is more stable than a typical SRAM. The lower valued resistor is more manufacturable and is less affected by temperature. The polysilicon resistor process provides a tighter than typical control over the resistor value. This tight resistance control provides greater SEP protection over a wider temperature range and also allows shorter write times. Including a resistor in the memory cell increases the die size by less than 9%. The cross-coupled resistors are incorporated in the single layer of polysilicon which also forms the gates of the transistors. Metal contacts for power and ground are incorporated in every cell to help collect some of the charge deposited by a particle passing through a nearby junction.

The effect of the cross-coupled resistors is to increase the threshold LET for SEP upset and reduce the effective saturated cross-section of the device. [9] These effects for UTMC's 64K SRAM are shown in figure 5 and 6. Using the LET threshold and effective cross-section from these graphs, the error rate in errors/bit/day as a function of resistor value may be calculated for any space environment using CREME or SpaceRad as described above. The error rate at 125 C (worst case) for UTMC's 64K SRAM is shown in figure 7 as a function of resistor value. By screening devices at the wafer level for resistor value and p-channel drive current, we can guarantee an error rate of less than 1.0E-10 errors per bit per day at 125 C.
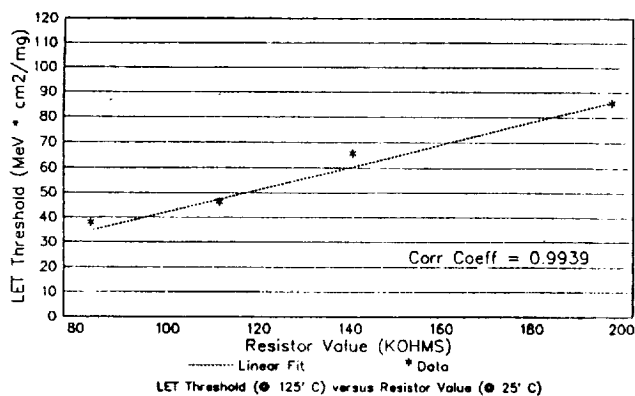
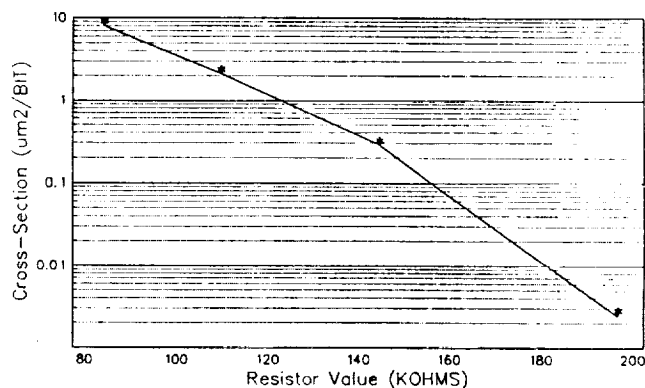Figure 5: LET Threshold vs. Resistor Value

Figure 6: Error Rate vs. Resistor Value

6.2 SEP-Hardened Flip-Flop Design

In logic systems, storage nodes such as flip-flops must retain data reliably, or the integrity of the logic system can be severely compromised. A SEP-induced upset of a single bit in a microprocessor register can send the system into an irrecoverable state. Detection of these types of errors can require substantial overhead in software and hardware complexity and
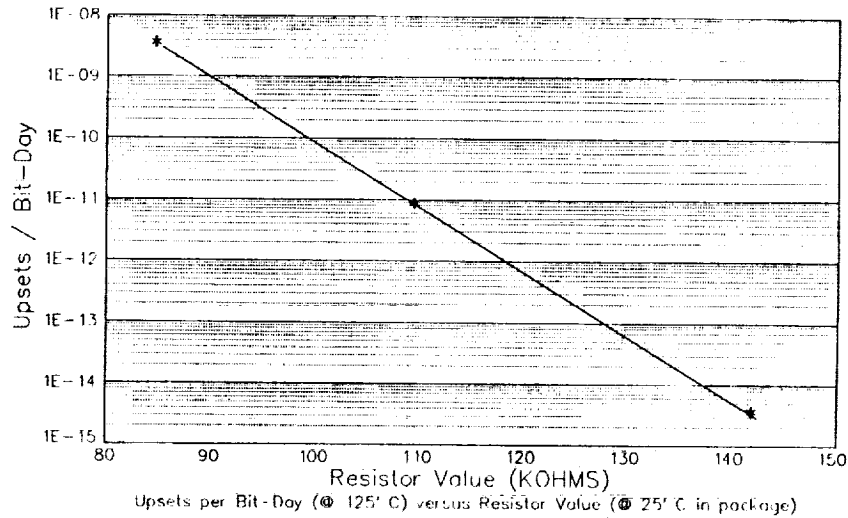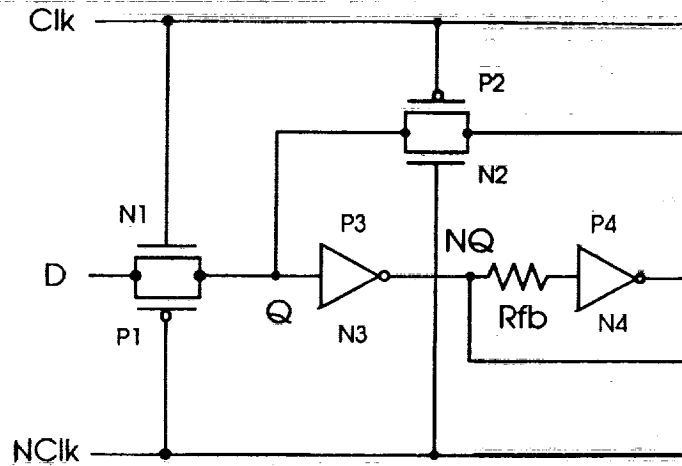
Figure 7: Error Rate vs. Resistor Value

Figure 8: Resistor Application in Flip-flop

is possible to substantially improve the SEP performance without introducing additional processing complexity. However, there is usually a penalty in increased die area.

If the wafer fabrication process technology has poly-resistors available (used for SEP-hardening SRAM cells described above), these resistors may be used to increase flip-flop hardness as shown in figure 8. This technique can result in some performance degradation of the flip-flop over temperature as reported by Sexton et al. [10] If resistors are not available, circuit techniques, coupled with the simulation techniques similar to those described above, can be used to develop flip-flop register cells which have improved SEP performance over conventional flip-flop circuits. [11,12]

To determine the effectiveness of the simulation techniques described above, we simulated the SEP upset for a number of the flip-flop cells in UTMC's gate-array library. The simulations for one of these cells, DFAPCB - a D-type flip-flop whose logic diagram is shown in figure 9, was compared with experimental data from heavy ion tests performed at Brookhaven National Laboratory. To accurately determine the upset rate of the flip-flop,

LOGIC SYMBOL

TRUTH TABLE

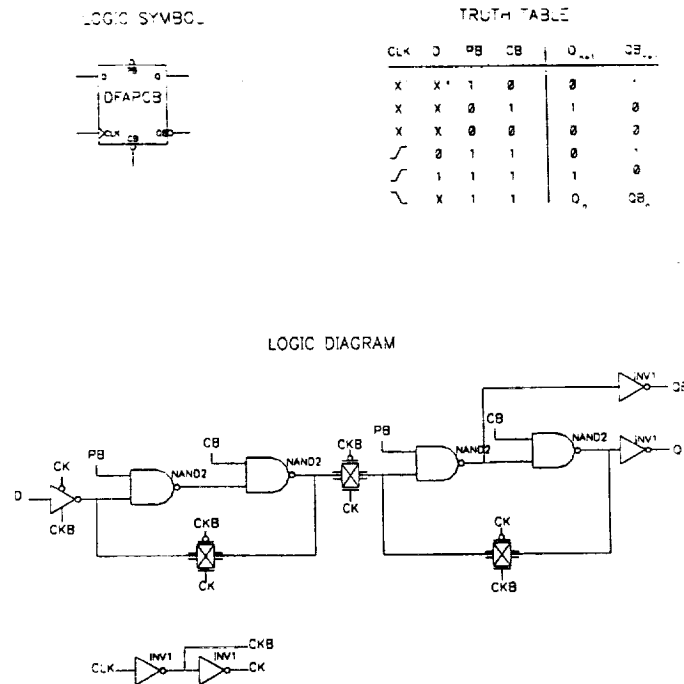| CLK	D	PB	CB	Q	QB
X	X	1	0	0	·
X	X	0	1	1	0
X	X	0	0	0	0
∫	0	1	1	0	·
∫	1	1	1	1	0
∿	X	1	1	Q	QB

LOGIC DIAGRAM

Figure 9: D-type Flip-flop Logic Diagram

it was necessary to determine the effective critical charge (the charge required to upset the state of the flip-flop) for every node within the circuit for both a high-node state and a low-node state. The effective critical charge, along with the junction area for each node, was then used to determine the upset rate for the node using the SpaceRad program. The sum of the upset rates for all nodes was then taken as the upset rate for the flip-flop. The simulated error rate for the DFAPCB flip-flop was 4.24E-8 errors per cell per day. This compares to an experimentally determined error rate of 3.38E-8 errors per cell per day for this flip-flop cell.

We have also developed SEP-upset improved cells which support our radiation-hard gate array cell library. Some of the cells are capable of providing an error rate of 1.0E-10 errors per cell per day. Fully redundant cells have also been designed which require twice as many transistors as a non-redundant design, but are SEP-immune. The results of this work have provided a number of guidelines for selecting and designing an SEP-hard flip-flop. These guidelines are discussed in Table 2.

7 Conclusions

Use of the simulation techniques described in this paper substantially increases the confidence that a design will meet its objectives for SEP hardness, and the cell layout can be optimized without compromising circuit performance. We have demonstrated an SEP error rate less than 1.0E-10 errors/bit-day for a 90% worst-case geosynchronous orbit environment over the entire -55 C to +125 C temperature range for a rad-hard 64K SRAM

Problem	Flip-Flop Design Approach
Minimize stacked p-channel devices	Remove NOR gates and replace with NAND gates.
Eliminate transmission gates	Remove transmission gates and replace with clocked inverters.
Minimize sensitive node area	Simplify design as much as possible consistent with functional requirements. Add redundant (parallel) transistors on sensitive nodes internal to the cell.

Table 2: Design Considerations for Improving SEP Hardness of Flip-Flops

while maintaining a less than 55 ns cycle time. We have also demonstrated the capability to model the SEP error rate of gate array cells and have applied the simulation and design techniques described in this paper to develop SEP-tolerant and SEP-hard flip-flop designs.

SEP hardness of integrated circuits cannot be assured by screening commercial devices, or by normal system-level or logic-level design techniques. Good SEP hardness can only be obtained by using a wafer fabrication process which provides the proper characteristics and proper attention to good design practices at the transistor level. Since commercial semiconductor manufacturers do not consider SEP effects when designing their circuits, it will be necessary to develop custom circuits which are designed for SEP hardness for mission-critical applications.

8 Acknowledgments

References

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