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**QUARTZ/FUSED SILICA CHIP CARRIERS**

*SBIR 1988 Phase II*

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## TABLE OF CONTENTS

I.	<b>Executive Summary</b> .....	1
II.	<b>Introduction</b> .....	2
III.	<b>Package Design</b> .....	4
	1. Task 1: Single Chip Package	
	2. Task 2: Multichip Module	
	3. Breadboarding	
	4. Task 3: Phased Array Module	
IV.	<b>Observations</b> .....	10
	1. Package Assembly	
V.	<b>Test Results</b> .....	24
	1. Mechanical	
	2. Electrical	
VI.	<b>Summary</b> .....	37
	1. Recommendations	
VII.	<b>Appendices</b> .....	40

## EXECUTIVE SUMMARY:

Under the Small Business Innovative Research (SBIR) Program, a contract was awarded by NASA's Lewis Research Center to develop high-frequency, high-performance packaging for microwave and millimeter-wave monolithic integrated circuits (MMICs). The primary technology thrust was the use of fused silica as the package substrate material to improve the radiofrequency (RF) performance at operating frequencies through the Ka-band. The research effort proceeded from a Phase I study (contract NAS3-25565) through Phase II fabrication demonstrations (contract NAS3-25870). This report documents the findings of the Phase II research effort.

Packaging is an important technology area that is essential for utilizing MMIC devices in systems. Unfortunately, packaging is generally available only at frequencies below approximately 12 GHz and is electrically and mechanically inappropriate for high frequency operation. Much work needs to be done to develop high frequency packages that provide minimum degradation to an electrical signal and are physically suited to integration into systems. This SBIR program aggressively attempts to develop packaging for high frequency operation using new packaging materials, processes, and concepts.

In its simplest form, a MMIC package consists of several parts. The primary part is the RF substrate which carries the electrical signals to and from the MMIC device. The MMIC device must then be enclosed to protect it from environmental hazards, which requires that "walls" and a lid be added to the RF substrate. Finally, a "base" is added to the assembly to provide mechanical and thermal support to the package and MMIC device. The SBIR contract effort described in the following report utilizes this structure as a baseline, then adds many advanced features such as multilayers, multicavities, power dividers, and integral radiating elements.

For this effort, the operating frequency and overall antenna configuration require MMIC spacing (package size) of a fraction of an inch. The designs described in this report address several problems and challenges associated with high frequency operation and results in a phased array module of dimensions 1" by 2", including radiating elements: representing a substantial increase in circuit density.

The SBIR Phase II research utilized the StratEdge Process, a co-lamination of fully fired ceramics, to fabricate the components. Three separate package designs were fabricated: 1) a broadband single chip carrier, 2) a multilayer, multicavity module, and 3) a phased array module. A top-level discussion of the process and the detailed component results will be presented in this report.

## INTRODUCTION:

The primary objective of this research and development effort was to develop monolithic microwave integrated circuit (MMIC) packaging which will operate efficiently at millimeter-wave frequencies. The packages incorporated fused silica as the substrate material which was selected due to its favorable electrical properties and potential performance improvement over more conventional materials for Ka-band operation. The first step towards meeting this objective is to develop a package that meets standard mechanical and thermal requirements using fused silica and to be compatible with semiconductor devices operating up to at least 44 GHz. The second step is to modify the package design to add multilayer and multicavity capacity to allow for application specific integrated circuits (ASICs) to control multiple phase shifters. The final step is to adapt the package design to a phased array module with integral radiating elements.

To reiterate, the goals of this program are:

- 1) Develop and build a standard package with fused silica substrates,
- 2) Modify the design into a multichip module, and
- 3) Develop the design into a phased array module.

For this program the three goals correspond to Tasks 1, 2, and 3. Task 1 was a continuation of the SBIR Phase I work. Phase I identified fused silica as a viable substrate material by demonstrating various plating, machining, and adhesion properties. In Phase II Task 1, a package was designed and fabricated to validate these findings. Task 2 was to take the next step in packaging and fabricate a multilayer, multichip module (MCM). This package is the predecessor to the phased array module and demonstrates the ability to via fill, circuit print, laminate, and to form vertical interconnects. The final task was to build a phased array module. The radiating elements were to be incorporated into the package instead of connecting to it with wire or ribbon bonds. The dimensions for the proposed fused silica module for this contract are 1" x 2" and that includes the radiating elements and operates at 30 GHz. On an industry wide basis, there has been little or no progress in the design and manufacture of T/R modules that can exploit the use of MMIC devices without negating their size and system cost advantages. Most packaging has been cumbersome, frequency limiting, and fails to address power and hermeticity concerns.

In order to achieve the proposed higher performance, several issues had to be addressed such as material and electrical characteristics. Gallium arsenide (GaAs) MMIC phase shifters which operate at about 30 GHz are to be used. This requires that the cavity size be kept small, both for facilitation of interconnecting ribbon or wire bonds as well as to ensure resonances outside the frequency band. The substrate materials considered were silica and alumina. However, silica had the more desirable electrical characteristics of lower dielectric constant and lower loss tangent.

The dielectric constant,  $\epsilon_r$ , for silica is 3.83 and 9.9 for 99.6% alumina. With a lower  $\epsilon_r$ , the

microstrip trace widths can be wider for a given substrate thickness, or the substrate can be thinner for a given trace width. A wider trace will provide lower DC losses through the trace since the cross-sectional area will be greater. In addition, larger line widths are easier to fabricate. If the substrate thickness is reduced, then the package will be smaller. The loss tangent is 0.000002 for silica and 0.0002 for 99.6% alumina at 1 MHz. The lower the value the less energy is lost to the material as heat. Also, the less material there is, the loss value will decrease. The choice was to design the single-chip carriers and the phased array module with fused silica.

Several characteristics that make fused silica undesirable are its poor thermal conductivity, low coefficient of thermal expansion (CTE), and low strength. Therefore, design issues and processing modifications needed to be addressed prior to completing any packages. Since there was no readily available processing data on building a silica MCM, the entire material set and processes had to be developed for this program.

## PACKAGE DESIGN:

### Task 1 Design: Single Chip Package

This design followed from the Phase I effort so that fused silica could be validated as a packaging material. The package consisted of a 10 mil kovar base, two RF feedthroughs and ten DC I/Os printed on a 5 mil fused silica substrate, a 10 mil silica seal ring, and a 10 mil kovar lid. It was designed to operate at 30 GHz. The dimensions were 0.430"x0.300"x0.025" excluding the lid.

Figure 1 shows the construction of the package. The top of the RF layer employed a thick-film etchback process to ensure fine line definition for good electrical performance. The 5 mil RF substrate was selected to permit flush mounting of the MMIC, and also to keep the microstrip line width nearer the width on the GaAs chip. A seal glass was printed on the top of the RF traces and the bottom of the seal ring for assembly. The subassembly had the vias drilled and cavity cut with a CO<sub>2</sub> laser.

The vias were filled with gold and the top and bottom ground planes printed to complete the electrical grounding. The base were attached with a Au/Ge preform. The base supports the fragile fused silica subassembly and also acts as electrical ground and heat sink for the MMIC. The lid were attached with a Au/Sn preform for sealing after die attach and bonding.

### Task 2 Designs: Multichip Module

The prototype multichip module design from NASA includes one 50 ohm RF input and four outputs through multibit, solid-state phase shifters. See Figure 2. In order to accommodate this requirement, a Wilkinson power divider was necessary to distribute the energy evenly to the four MMIC phase shifters. A Wilkinson power divider was an obvious choice for balanced distribution of power from a single source to the set of 4 phase shifters. The Wilkinson, by theory, would evenly split the source power into 2 equal half power source units. This can be accomplished if the source transmission line and two split transmission lines maintain the characteristic impedance of the source, namely 50 ohms. The power of each branch would be ideally 50% of that of the input source. A simple resistive network determines that a 100 ohm delta resistance across the branches would result in maximum transfer of power with zero reflective loss. In addition, there are two ASICs that will control the phase shifters through buried DC bias traces. To avoid crosstalk, the traces were be routed with multilayer capability. The actual design was refined through breadboarding as required.

The StratEdge process was used to laminate four silica layers together with a combination of high, 850°C, and low, 475°C, temperature processes. The StratEdge

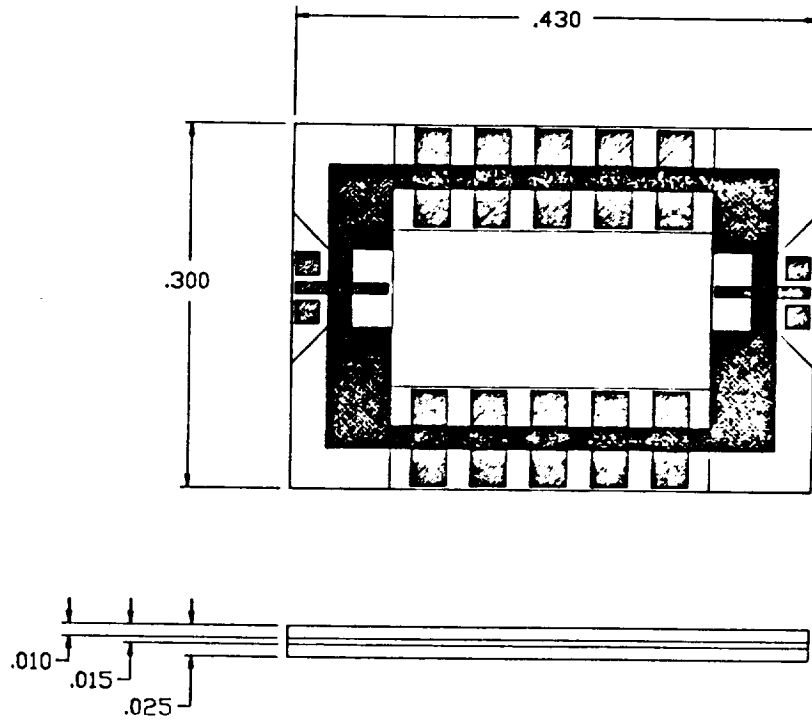


Figure 1. Initial DC to 30 GHz package design with two RF feedthroughs and 10 DC I/Os.

- △ 1 FUSED SILICA, .010 THK
- △ 2 INVARI BASE, .015 THK

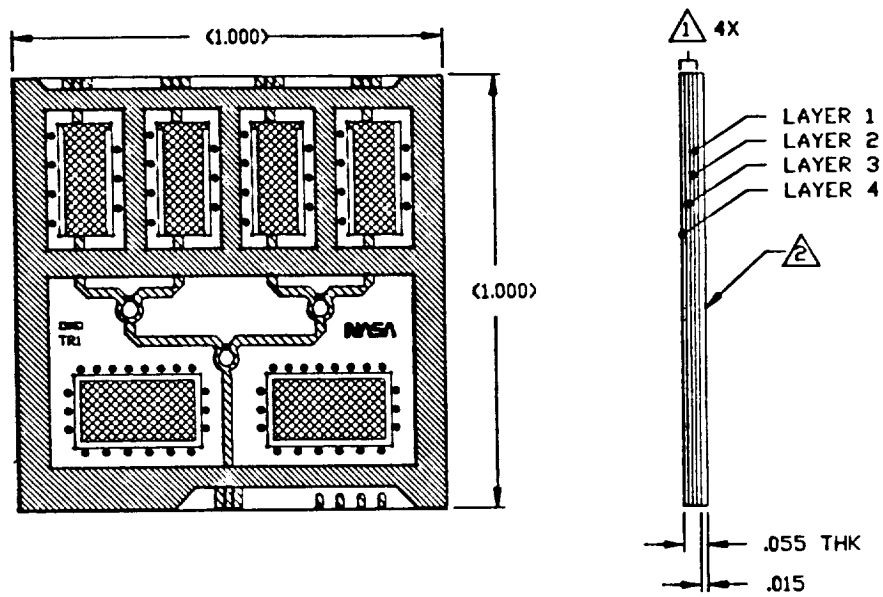


Figure 2. Initial 30 GHz multichip module design showing cavities for the two ASICs and four MMIC phase shifters.



process was employed to address two problem areas:

- A) The modular testing of the individual thin and thick film substrates before final assembly, and
- B) The ability to combine thin and thick film layers with a low temperature process that would not degrade the thin film metallization.

All silica layers were laser machined as necessary to form vias, recesses, cavities, and walls. The two DC layers and the seal ring were fabricated with high temperature processing. The standard thick film process were as follows: 1) Via filling and 2) Print conductors. The RF layer was fabricated with thin film processing to ensure electrical performance.

The assembly consisted of printing high temperature seal glass and interconnects on the DC layers and assembling. The RF layer and the seal ring were printed with the low temperature sealing glass and interconnects. Then the DC subassembly, RF layer, and the seal ring were aligned for final substrate assembly. The invar base was attached with a Au/Ge preform providing structural support, electrical ground, and a heat sink. Finally, the lid was sealed with a Au/Sn preform to complete the package.

## **Breadboarding**

Several design aspects for the antenna needed to be identified prior to locking in the final design. This was accomplished by 'breadboarding' or testing an individual circuit without building an entire package.

### **Aperture Coupled Patch:**

The first design was an Aperture Coupled Patch. These were designed to verify the microwave coupling action from the top of a substrate to the bottom. In addition, this test was to determine if the radiating elements were to be 'broadside fire' or 'end fire'.

### **Task 2:**

The second breadboarding experiment was the comparison between the one-quarter and one-third wavelength Wilkinson power divider. Touchstone and Microwave Design System software packages were used to model the power divider design. Theory dictates that a one-quarter wavelength design should give the best performance. However, the design model of the components indicated that performance was optimal with a one-third wavelength design.

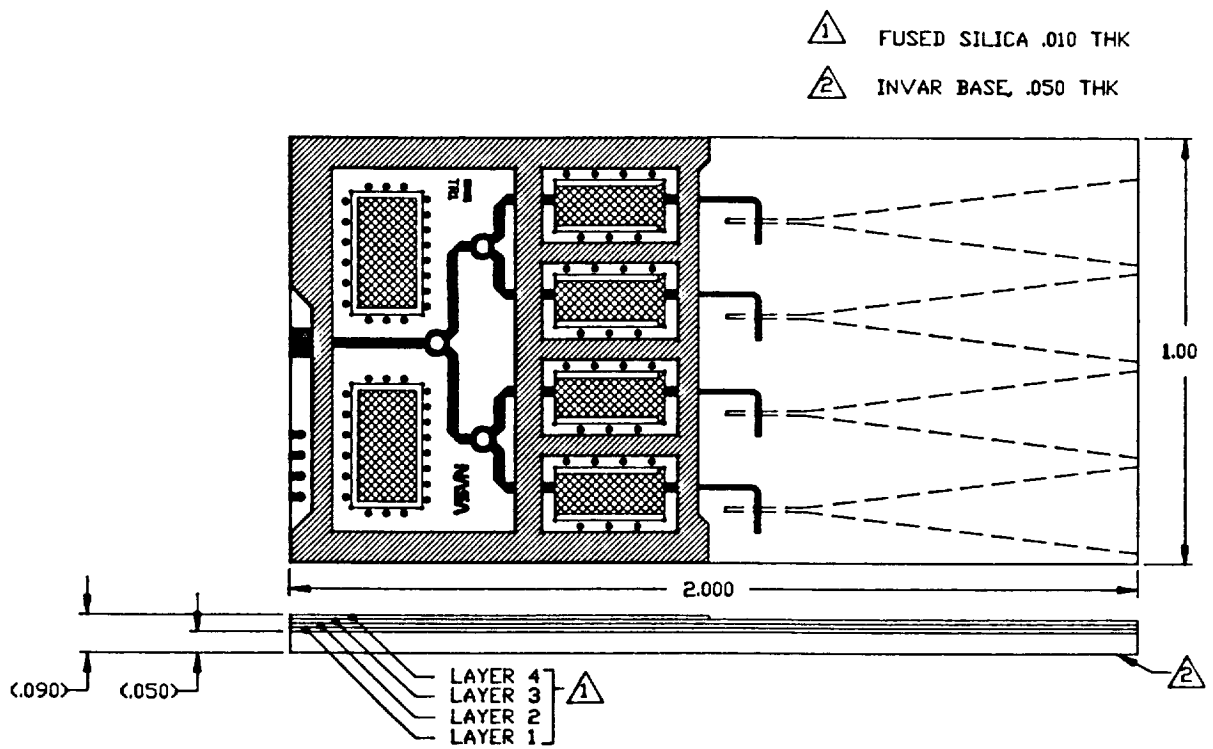


Figure 3. Initial 30 GHz phased array module design showing cavities and the integral radiating elements.

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## OBSERVATIONS:

During fabrication and assembly of the package components, various parameters, processes, and fabrication details were monitored. These details were monitored due to the novelty of the design and the lack of previous assembly information. The following paragraphs list and discuss some of the physical characteristics observed during fabrication.

### TASK 1: Single Chip Package

#### LAPPING/POLISHING

The substrates were received with a 0.1 microinch peak-to-valley finish. This polish produces an optically clear finish on both sides of the substrate. Also, a smooth surface is believed to enhance electrical performance by reducing resistive losses.

#### LASER MACHINING

The vias and cavities were drilled through the silica substrates using a CO<sub>2</sub> laser. There was minimal slag after processing. Slag is the spill over from the molten material adhering to the via or cavity walls. When the substrates were received in-house, they were ultrasonically rinsed in acetone for two minutes and isopropanol for two minutes to remove most of the slag.

#### VIA FILL

Via filling is accomplished through our proprietary multiple step via fill process to ensure adhesion and complete filling.

#### SCREEN PRINTING

A thick film screen printing process was used to define the electrical conductor patterns and adhesive seal glass patterns on the silica substrates.

##### Conductor:

A high temperature, 850°C, thick film gold conductor was printed onto the substrates. After the gold was fired, the adhesion was very good. However, due to the assembly process, the gold conductors go through another 8 to 10 firings. When the gold adhesion is tested after assembly, the gold usually peeled off the substrate. The repeated thermal cycling weakened the gold conductor bond to the substrate.

## Seal Glass:

There were two candidates for the seal glass, one devitrifying and one vitreous. A devitrifying glass will crystallize after heating and a vitreous glass will remain amorphous. After many experiments, the vitreous glass, labelled 40-00070, was found to be hermetic when fused silica substrates were assembled without any printed gold traces. However, when the gold traces were printed on the substrates and then assembled, hermeticity was not repeatably achieved. The project was continued in order to build packages to verify electrical characteristics.

## ASSEMBLY

The parts were aligned in a simple, edge-align ceramic fixture, of StratEdge design, weighted with ceramic blocks, and run through the furnace together. A ceramic fixture was required since the parts will be run at 900°C.

## BASE ATTACH

The base, Au/Sn preform, and 2-layer silica subassembly were hand aligned under a microscope and clipped together. The assembly was sent through a 15% hydrogen - 85% nitrogen atmosphere furnace at 400°C. There was a little excess solder near the four corners of the package (Figure 4).

## LID ATTACH

A similar process was applied for the lid, Au/Sn preform, and package assembly.

## ENDVIEW DESCRIPTION:

Lid: 0.370" x 0.235" x 0.010" lid - kovar  
Preform - Au/Sn

Layer 2: Gold ground plane - 40-00051 gold conductor  
Via fill - 40-00006 gold via fill  
0.430" x 0.300" x 0.005" fused silica  
High temp seal glass - 40-00070 seal glass

Layer 1: High temp seal glass - 40-00070 seal glass  
RF feedthroughs - 40-00051 gold conductor  
0.430" x 0.300" x 0.005" fused silica  
Gold ground plane - 40-00051 gold conductor

Base: Preform - Au/Ge  
0.430" x 0.300" x 0.010" base - kovar

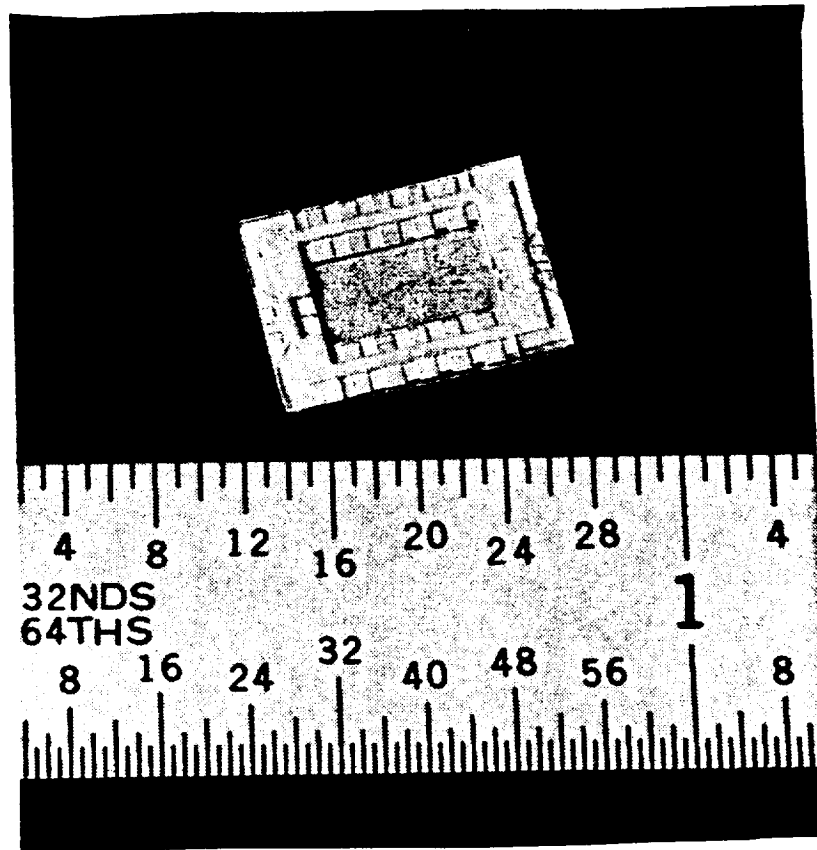


Figure 4. Photo of the assembled DC to 30 GHz package.

## BREADBOARDING (Part 1)

### APERTURE COUPLED PATCH -

The aperture coupled patch was built with two silica substrates laminated together to simulate a broadside-fire radiating element. The substrates assembled were printed, assembled, and electrically tested at NASA LeRC.

### LAPPING/POLISHING

The 1.000" x 1.000" x 0.005" antenna substrate was received with a 0.1 microinch finish and the 1.000" x 1.000" x 0.030" patch substrate was received with a 10 microinch finish. Since the microstrip trace was on the 5 mil substrate, that layer was polished to minimize resistive losses. However, the patch substrate had the microwave energy passing normal to it and it was believed that the rougher surface would not adversely affect the RF signal. Subsequently, a rougher finish was applied to that substrate to increase thick film gold and glass adhesion on the patch substrate.

### CIRCUIT PRINT

The high temperature gold conductor was used for this application. Since there was not any thin film circuitry, low temperature processing was not required. After printing, drying, and firing, the conductors were etched to provide the required high resolution patterns.

### SEAL GLASS PRINT

The high temperature seal glass, 40-00070, was only printed on the 30 mil substrate. This provided enough adhesion for this test.

### ASSEMBLY

The two substrates were aligned on a simple, edge-align, ceramic fixture, weighted with ceramic blocks, and run through the furnace for assembly. This was required to ensure the glass would flow and adhere to the opposing face of the antenna substrate.

### ENDVIEW DESCRIPTION:

Layer 2: Gold Antenna - 40-00051 H gold conductor  
1.000" x 1.000" x 0.005" fused silica  
Gold ground plane - 40-00051 gold conductor

Layer 1: High temp seal glass - 40-00070 seal glass  
1.000" x 1.000" x 0.030" fused silica  
Gold Patch - 40-00051 gold conductor

#### WILKINSON POWER DIVIDER -

The modeling of the power divider was performed using the Touchstone simulator from EEsof (Appendix A). Once the concept was proven from the ideal case, the models were transferred from electrical to physical parameters. This meant including line length, and both conductor and dielectric losses. Another analysis with Microwave Design Software (MDS) was performed across the frequency band of interest, and the design of the power divider was optimized. The analysis resulted in differences from fundamental theory. With respect to the design, the physical length of the divider branches should have been 1/4 wavelength (the theoretical optimum) and the branch resistor 100 ohms. The MDS showed that the branches should have been 1/3 wavelength and the resistors at 86.9 ohm (Appendix B). Experiments were set up to measure both the theoretical and the analytical designs.

#### LAPPING/POLISHING

The substrate dimensions required for this experiment were 2.25"x2.25"x0.010". The plates were all polished to a 0.1 microinch finish. The smooth surface increases thin film materials adhesion.

#### THIN FILM

There were two types of Wilkinson power dividers fabricated and tested. The first design consisted of a one-quarter wavelength power divider with a 100 ohm nichrome (NiCr) resistor. The second type was a one-third wavelength power divider with a 86.9 ohm tantalum nitride (Ta<sub>2</sub>N) resistor. Both designs used a thin film gold conductor and thin film resistors.

The thin film vendor experienced difficulties processing the fused silica. For example, metallization did not extend to within 3 mils of the substrate end, the test resistors were shorted to ground, and the resistor values were not at specification. However, after several plates, he was able to identify a process that ensured good mechanical and electrical properties. The thin film vendor was also responsible for dicing the 2.25" square plate into 1" square test circuits.

#### ENDVIEW DESCRIPTION:

Ta<sub>2</sub>N Layer 1: Gold conductor  
Nickel barrier layer  
Titanium/Tungsten adhesion layer

Tantalum nitride resistor layer  
1.000" x 1.000" x 0.010" fused silica  
Titanium/Tungsten adhesion layer  
Nickel barrier layer  
Gold ground conductor

NiCr Layer 1: Gold conductor  
Nickel barrier layer  
Titanium/Tungsten adhesion layer  
Nichrome resistor layer  
1.000" x 1.000" x 0.010" fused silica  
Titanium/Tungsten adhesion layer  
Nickel barrier layer  
Gold ground conductor

## TASK 2: Multichip Module

Several processing techniques were evaluated during assembly of this multilayer package to improve manufacturability. They are discussed below and in the RESULTS section.

### LAPPING/POLISHING -

It was believed that a rougher surface finish would increase gold trace adhesion. This would allow for an increased mechanical bond between the gold and the substrate. Therefore, the initial substrates were lapped to a 10 microinch finish. This also lowered the substrate cost. During via fill firing though, about half of the substrates cracked through the thermal via areas. Processing stopped while the cause was investigated. After running several experiments, it was found that the optically polished substrates withstood more handling than the lapped substrates. All substrates were then sent to be optically polished to increase surface strength. Although the rougher surface may have helped in gold adhesion, the smoother surface appeared to remove any sharp radii that would initiate cracks due to the CTE mismatch. Also, a smooth surface enhances electrical performance by reducing resistive losses.

The gold that was used with the 10 microinch substrates was fired at 850°C. The initial design included a high temperature DC subassembly and a low temperature RF subassembly. When the decision was made to use the polished substrates, a 475°C gold was used for via fill and conductor printing. This would decrease the thermal stresses during firing.



## LASER MACHINING -

Refer to the procedure mentioned in Task 1.

## THIN FILM PROCESSING -

After learning how to process the fused silica from the power divider test circuits, the next circuit pattern processed was the RF layer. This pattern included transitions, three power dividers, and one test resistor. The substrate was polished, laser drilled, and then thin film processed. The vendor had difficulty keeping the cavity walls free from gold. Eventually, the gold was removed by selective placement of etching solution and then rinsing the substrate. This was very tedious but worked at the time. The vendor eventually developed an alternate method to remove any excess gold.

In addition, the resistors needed to be processed so that they would have the required value after final assembly. Several experiments were run to determine what the starting resistor value should be.

## VIA FILLING -

### Thin Film Layers:

A low temperature gold conductor was used to fill the vias. This was done to minimize the thin film resistor variation during heating cycles and to protect the thin film metallization from oxidizing.

### Thick Film Layers:

Via filling is accomplished through our proprietary multiple step via fill process to ensure adhesion and complete filling.

As previously mentioned, the substrates began to crack severely during via fill firing. The yield was only 50% at best. A low temperature, 475°C, conductor was then used as a via fill material. Since there would be less stress induced by a lower temperature, the substrate was able to withstand the via filling.

## SCREEN PRINTING -

### Conductor:

A low temperature, 475°C, gold conductor was used on the seal ring, DC bias, and ground layers. The process used was that of 'print/dry/fire' which produced a trace thickness of about 0.4 mils.

### Seal Glass:

The seal glass that was initially chosen for sealing the two DC layers together had a high temperature, 900°C, sealing profile, i.e. 40-00070. However, this glass could not be used to seal the RF layer and the seal ring. A low temperature, 475°C, glass was identified for this process. However, when the via fill and conductor inks were changed to low temperature processes, all the seal glass needed to be changed to the low temperature glass. This glass was identified as 40-00079.

### Interconnect:

Low temperature interconnect was printed to connect vias from one layer to another.

### CERAMIC ASSEMBLY -

The initial plan for assembly was to print the seal glass and interconnects on the tops and bottoms of each layer separately and then assemble all the layers simultaneously. However, it was determined that when one side of the substrate is printed and glazed, there is not enough strength in the substrate to withstand the squeegee pressure during the second print.

The assembly process was changed to print the top of layer 1 and the bottom of layer 2 and then assemble. Print the top of that composite subassembly and the bottom of layer 3 and then assemble. Then print the top of that subassembly and the bottom of layer 4 and then assemble.

### BASE ATTACH -

Soldering the base on the package was the next step. A Au/Ge preform was designed for base attach. Several experiments were run to determine the expansion mismatch effect. All substrates cracked when assembled with Au/Ge performs.

Experiments were run with Au/Sn solder paste. This process worked with several of the test samples and with two packages. However, on the next three packages, the substrates cracked during cool down. The cool down was even extended to twice the time and subsequent parts still fractured after assembly. The CTE mismatch is believed to be the cause of the cracking.

In order to electrically test the packages, a process had to be defined which would allow base attachment without fracturing the package. A silver-filled epoxy was identified which had a cure temperature of 150°C. An experiment was run to assemble a package and no cracking was observed. In order to prove the concept of this program, it was decided to use the conductive epoxy as the sealing material for the remaining packages.

## 50 OHM THROUGH LINES -

The 50 ohm microstrip transmission lines were epoxied in place with the same silver-filled material used for base and lid attach.

## LID ATTACH -

The lid/preform was supplied separately from the package. However, several electrical tests required that the lid be attached to the package. Initially, the lid was to be attached with a Au/Sn solder preform. However, when the base was attached with the silver epoxy, the lid would also have to be attached with the silver epoxy.

## ENDVIEW DESCRIPTION:

Lid: 1.000" x 0.925" x 0.010" Lid - Kovar  
Preform - 80% Au 20% Sn OR (Conductive epoxy - 400102)

Layer 4: Top conductor - 40-00040 low temp gold conductor  
Via fill - 40-00040 low temp gold conductor  
Glass pull - 40-00070 high temp seal glass  
1.000" x 1.000" x 0.010" fused silica - seal ring  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Layer 3: Top interconnect - 40-00080 low temp interconnect  
Top seal glass - 40-00079 low temp seal glass  
Via fill - 40-00040 low temp gold conductor  
1.000" x 1.000" x 0.010" fused silica - RF Subassembly  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Layer 2: Top interconnect - 40-00080 low temp interconnect  
Top seal glass - 40-00079 low temp seal glass  
Top conductor - 40-00040 low temp gold conductor  
Via fill - 40-00040 low temp gold conductor  
Glass pull - 40-00070 high temp seal glass  
1.000" x 1.000" x 0.010" fused silica - DC Bias layer  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Layer 1: Top interconnect - 40-00080 low temp interconnect  
Top seal glass - 40-00079 low temp seal glass  
Top conductor - 40-00040 low temp gold conductor  
Via fill - 40-00040 low temp gold conductor

Glass pull - 40-00070 high temp seal glass  
1.000" x 1.000" x 0.010" fused silica - DC Bias layer  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Base: Conductive epoxy - 400102  
1.000" x 1.000" x 0.015" base - invar

## BREADBOARDING (Part 2)

## RADIATING ELEMENT TEST CIRCUITS -

## LAPPING/POLISHING

The substrate dimensions required for this experiment were 2.25"x2.25"x0.010". The substrates were all 0.1 microinch polished. The smooth surface increases thin film materials adhesion.

## THIN FILM

The next test circuit pattern was the radiating elements. These were processed separately so that NASA could test the two designs and identify the design with the best performance. This processing went relatively well except that there was a requirement of a one mil gap in one of the element designs and the thin film vendor only provided a 1.2 to 1.5 mil gap. Since the vendor could not produce the circuit with required dimensions, this design was not integrated into the radiating element portion.

The thin film vendor had identified a process by this time and was able to produce the test circuits with a relatively good yield. The thin film vendor was also responsible for dicing the 2.25" square plate into 1.0"x1.1" test circuits.

## ENDVIEW DESCRIPTION:

Layer 1: Gold conductor pattern (Two possible patterns)  
Nickel barrier layer  
Titanium/Tungsten adhesion layer  
1.000" x 1.000" x 0.010" fused silica  
Titanium/Tungsten adhesion layer  
Nickel barrier layer  
Gold radiating element conductor pattern (Two possible patterns)

### TASK 3: Phased Array Module

#### LAPPING/POLISHING -

Same procedure as stated in Task 2.

#### LASER MACHINING -

Same procedure as stated in Task 2.

#### THIN FILM PROCESSING -

The final pattern was the combined power dividers and radiating elements. When the vendor began processing the lasered fused silica, the substrates warped. The cause for the warpage was never identified. Stresses built up during laser machining was thought to be the primary cause. The vendor was able to develop a flattening procedure which made the parts usable for further processing. In addition, the process for removing excess gold was defined by using an extra mask developed by the vendor at his expense. However, 25 two-up substrates only yielded 26 completed parts. The CTE mismatch over the 1"x2" area is believed to cause the decreased yield.

#### VIA FILLING -

Same procedure as stated in Task 2.

#### SCREEN PRINTING -

Conductor:

Same procedure as stated in Task 2.

Seal Glass:

All the DC layers and packages containing the 50 ohm through lines used the same procedure as stated in Task 2.

However, the RF and Seal Rings required conductive and non-conductive epoxies to complete package assembly.

Interconnect:

Same procedure as stated in Task 2.

CERAMIC ASSEMBLY -

The same assembly procedure was used as on Task 2. Twelve packages were assembled using the low temperature process. When a 100% DC continuity check was performed, none of the packages passed. These parts were used for the packages requiring the 50 ohm through lines. The process was changed to create an increased continuity between interconnect bumps between layers. The RF substrates would be printed twice with seal glass and interconnect bumps. After glazing, there was about 40 mils camber across the substrate length. This caused a new assembly technique to be developed.

The top of the DC subassembly was printed with a non-conductive epoxy and a conductive silver-filled epoxy. The bottom of the RF layer had to have the epoxies hand painted since the substrates were too warped to be screen printed. The DC subassembly and RF layer were assembled and placed in a dryer to cure the epoxies. Next, the top of the RF layer and the bottom of the seal ring had the epoxies applied to them. They were then assembled and placed in a dryer to cure.

BASE ATTACH -

The silver-filled epoxy was used for base attach as on Task 2. After NASA tested the packages with the 50 ohm through lines and the 1"x2"x0.050" bases, they requested that StratEdge build the functional packages with a 1"x1"x0.050". NASA would cut the bases in half and StratEdge would assemble the base with the silver epoxy (Figure 5).

50 OHM THROUGH LINES -

Same procedure as stated in Task 2.

LID ATTACH -

Same procedure as stated in Task 2.

ENDVIEW DESCRIPTION:

- Lid: 1.000" x 0.925" x 0.010" Lid - Kovar  
Preform - 80% Au 20% Sn OR Conductive epoxy - 400102
- Layer 4: Top conductor - 40-00080 low temp gold conductor  
Via fill - 40-00079 low temp gold conductor  
Glass pull - 40-00070 high temp seal glass  
1.000" x 1.000" x 0.010" fused silica - seal ring  
Bottom seal glass - Low temp seal glass - 40-00079 OR

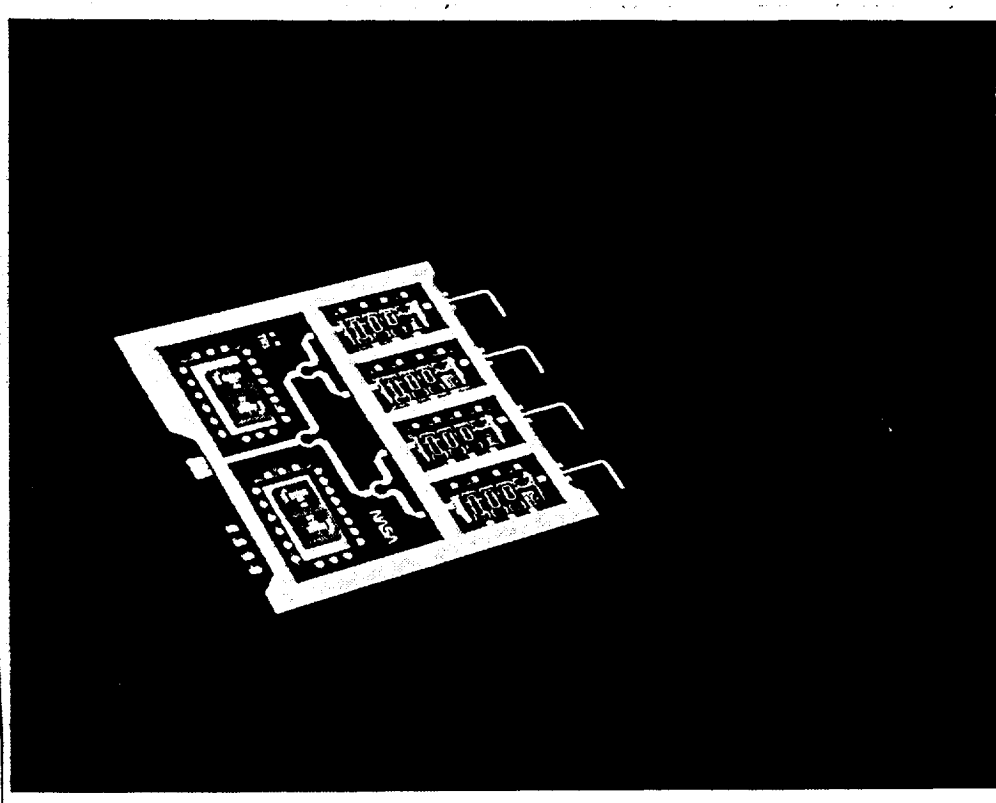


Figure 5. Photo showing assembled Phased Array Module with ASICs and MMICs in their respective cavities.

Non-conductive epoxy - 400103

Bottom interconnect - Low temp interconnect - 40-00080 OR  
Conductive epoxy - 400102

Layer 3: Top interconnect - Low temp interconnect - 40-00080 OR  
Conductive epoxy - 400102  
Top seal glass - Low temp seal glass - 40-00079 OR  
Non-conductive epoxy - 400103  
Via fill - 40-00040 low temp gold conductor  
1.000" x 2.000" x 0.010" fused silica - RF Subassembly  
Bottom seal glass - Low temp seal glass - 40-00079 OR  
Non-conductive epoxy - 400103  
Bottom interconnect - Low temp interconnect - 40-00080 OR  
Conductive epoxy - 400102

Layer 2: Top interconnect - Low temp interconnect - 40-00080 OR  
Conductive epoxy - 400102  
Top seal glass - Low temp seal glass - 40-00079 OR  
Non-conductive epoxy - 400103  
Top conductor - 40-00040 low temp gold conductor  
Via fill - 40-00040 low temp gold conductor  
Glass pull - 40-00070 high temp seal glass  
1.000" x 2.000" x 0.010" fused silica - DC Bias layer  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Layer 1: Top interconnect - 40-00080 low temp interconnect  
Top seal glass - 40-00079 low temp seal glass  
Top conductor - 40-00040 low temp gold conductor  
Via fill - 40-00040 low temp gold conductor  
Glass pull - 40-00070 high temp seal glass  
1.000" x 2.000" x 0.010" fused silica - DC Bias layer  
Bottom seal glass - 40-00079 low temp seal glass  
Bottom interconnect - 40-00080 low temp interconnect

Base: Conductive epoxy - 400102  
1.000" x 2.000" x 0.050" base - Invar OR  
1.000" x 1.000" x 0.050" base - Invar



## TEST RESULTS:

### TASK 1: Single Chip Package

#### MECHANICAL

While Phase I addressed the feasibility of incorporating fused silica as a substrate material, Phase II Task 1 must demonstrate that all processes in the physical construction techniques applied can be combined on a single unit without degrading any of its critical components or connections.

The Task 1 results showed that the concept of making a package with fused silica as the substrate material is feasible but that several areas still need to be addressed, such as gold adhesion, hermeticity, electrical performance, and manufacturability. In addition to the Task 1 packages there was a concurrent contract with Hughes Aircraft Company to fabricate three types of single-chip, fused silica hermetic packages. The operating frequencies were 32 GHz, 35 GHz, and 44 GHz. Figure 6 shows the 44 GHz package.

The manufacturability of the NASA packages and the Hughes packages was very low. The 5 mil and 10 mil fused silica substrates were very difficult to handle without breaking or cracking. Also, the Coefficient of Thermal Expansion (CTE) mismatch was the main cause of cracking during processing. The CTE of silica is  $0.5 \times 10^{-6}$  in/in/°C and the CTE of gold is  $15 \times 10^{-6}$  in/in/°C. The rule of thumb for processing various materials is that roughly a 10% difference in CTEs is acceptable. The difference in CTE between the silica and gold is 3000%. Needless to say this caused many processing difficulties.

Eventually, a process was defined so that packages could be built consistently. All assembled parts were tested for hermeticity on a Varian Porta-Test II portable helium leak detector. If the parts held to greater than  $1 \times 10^{-8}$  atm-cc/sec during helium spray then they were considered hermetic.

Most of the packages built were able to pull vacuum down to  $10^{-9}$  atm-cc/sec. However, when the parts were sprayed with helium, the leak rate was greater than  $1 \times 10^{-8}$  atm-cc/sec. The parts were airtight but did not pass MIL-STD-883C, Notice 9, Method 1014.9. This was the final iteration for the single-chip carriers. The hermeticity and electrical performance could not be met and the manufacturability yield was at best 10%.

#### ELECTRICAL

Electrical data from Task 1 showed encouraging results. Although none of the parts met all target values, excellent performance was achieved to well above 30 GHz.

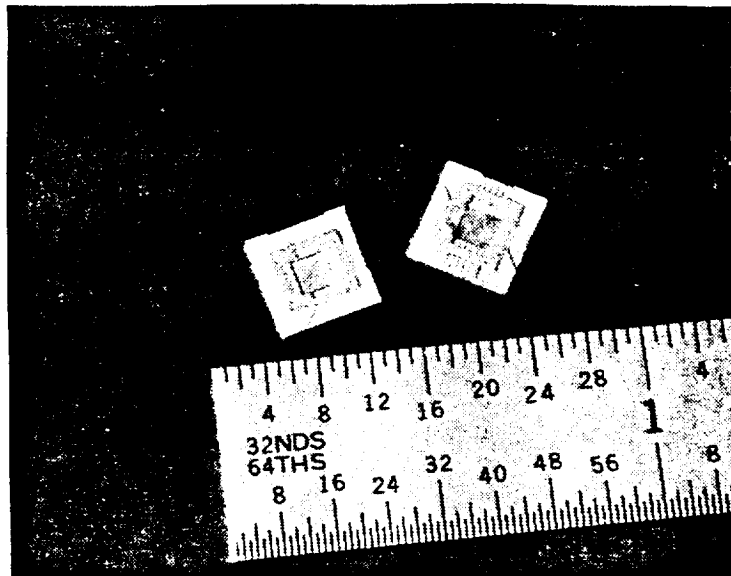


Figure 6. Photo showing the DC to 44 GHz package.

There were two notable examples 1) a Hughes designed 44 GHz hermetic package was built and tested favorably up to 35 GHz (Figure 7), and 2) a modified Hughes designed 44 GHz non-hermetic package was tested to 50 GHz with excellent results (Figure 8). Unfortunately, the performance could not be duplicated between parts. It was thought that when the processing parameters were sufficiently defined, the electrical design could be refined allowing higher performance and greater consistency among parts. Eventually, the project was descoped due to the inability to duplicate the previous success within the fixed cost of the program.

## WILKINSON POWER DIVIDER DESIGN:

### MECHANICAL

There were several test patterns and circuit patterns required for this program. The first pattern was to evaluate whether the Wilkinson power divider should have nichrome or tantalum nitride resistors. There were errors in the initial layout and the vendor had difficulties with the placement of the test resistor. After this was corrected, the processing proceeded acceptably with the tantalum nitride.

### ELECTRICAL

There was a discrepancy between the theoretical design and a modeled design. The two designs were fabricated on thin film and tested on an HP 8510C Network Analyzer. The results showed that the modeled design had slightly improved performance over the theoretical design. The decision was made to build the Task 2 and Task 3 power dividers with the one-third wavelength design.

## TASK 2: Multichip Module

### MECHANICAL

Task 2 showed that a multichip, multilayer package can be assembled in fused silica. Although the yield was relatively low, the concept was proven. The Multichip Module required innovative processing techniques in order to minimize damage to the thin film circuitry and to optimize the CTE mismatches. The first requirement being polished substrates to provide increased substrate strength and increased gold adhesion. The second being a low temperature assembly process to protect the thin film circuitry and to minimize CTE stresses. The base had to be attached with a silver-filled epoxy since Au/Sn soldering caused the package substrates to crack. This would suffice for electrical evaluations.

### ELECTRICAL

DC continuity testing was measured with a Hewlett-Packard E2378A Multimeter.

```

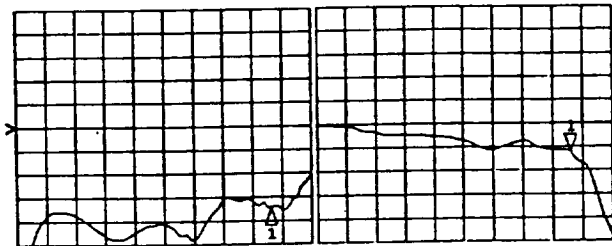
S11          log MAG      S21          log MAG
REF 0.0 dB   REF 0.0 dB
Δ  5.0 dB/   1  1.0 dB/
1  -17.204 dB 1  -1.2307 dB
Ap

```

```

MARKER 1
34.75 GHz

```



```

START 0.25000000 GHz
STOP  40.25000000 GHz

```

Figure 7. Plot of the insertion and return loss for the Hughes DC - 44 GHz package.<sup>1</sup>

<sup>1</sup>Y.C. Shih, et al., "A High Performance Quartz Package For Millimeter-Wave Applications", *1991 IEEE MTT-S Digest*, pp 1063-1066.

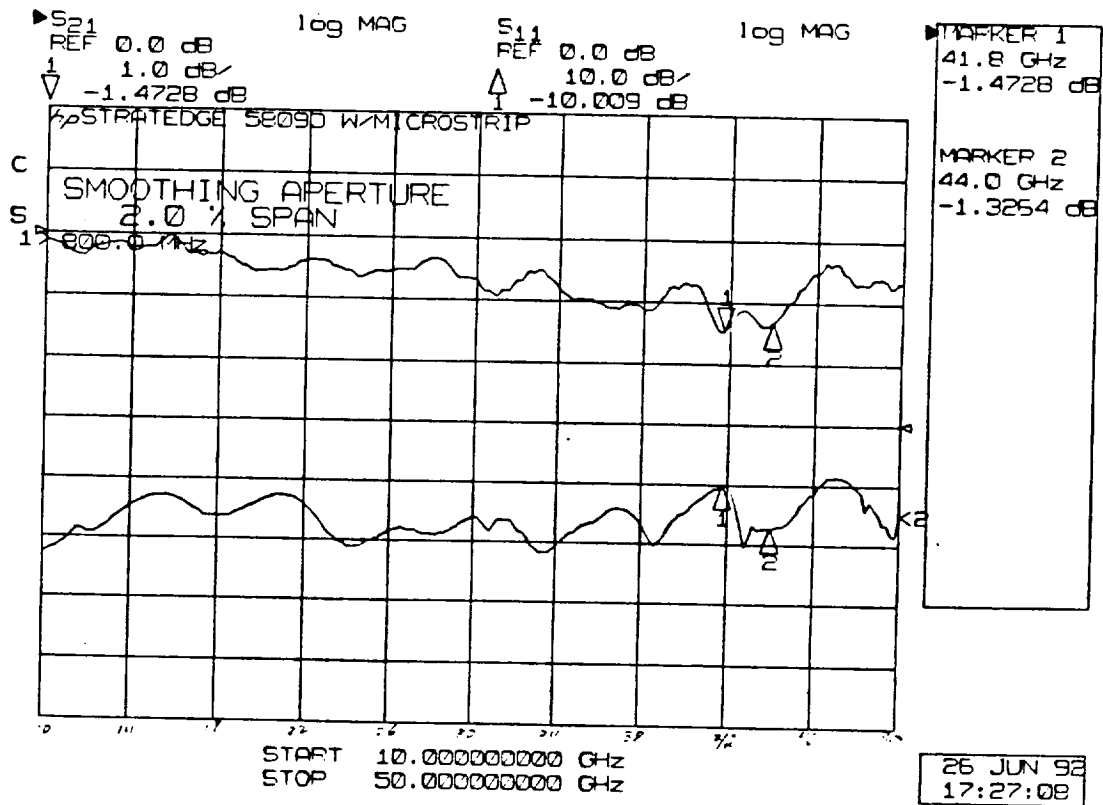


Figure 8. Plot of insertion and return loss for the modified Hughes DC - 44 GHz package.

After assembly of each section, the parts were tested for DC connection between various points on the subassemblies. The parts were not 100% electrically tested but only random points were checked. Of the points checked, all were connected. This proved to be inadequate since when NASA received the packages and performed DC testing, about half of the finished Task 2 packages were not completely connected.

The assembled Task 2 packages were sent to NASA LeRC for mounting on a test fixture. The parts were sent back to StratEdge to be tested on the Hewlett-Packard 8510C Network Analyzer for electrical performance. The package parameters were measured from 28 to 33 GHz for a 5 GHz bandwidth window. The insertion loss (S21) was measured on the module (Figure 9) with and without a lid to determine the amount of resonance effects the lid produced. The insertion loss measured from port 2 to port 1 included the losses of the microstrip lines, the transitions through three walls, the power division through 2 Wilkinson power dividers, two ribbon bonds, and a microstrip insert through the phase shifter cavity of 0.250". Theoretically, assuming no loss in any part of the path, the magnitude of S21 would be the 3 dB times 2 power dividers, or 6 dB. NASA requested markers be placed at the center frequency, and at both 500 MHz and 1 GHz bandwidths to determine the windows of operation for the module. The magnitude of S21 measured on the module varied from approximately 10 to 13 dB within a 1 GHz bandwidth at the center frequency of 31.5 GHz (Figure 10). Subtracting the 6 dB loss from the 2 power dividers, between 4 and 7 dB of loss was induced across the band due to the other transmission line effects. The center frequency of 31.5 GHz was chosen because the 1/4 wave node was at that frequency. The S21 response ranged from 10.3 to 11.8 dB across the 1 GHz bandwidth with the lid placed on the module (Figure 11), reducing the variance of the power loss from 3 dB to 1.5 dB across the band. The return loss was better than 12.9 dB over the bandwidth with no lid (Figure 12) and better than 10 dB with the lid (Figure 13). The presence of the lid not only reduced the variance of the insertion loss, but also reduced the magnitude of the return loss by coupling to the RF line. It should be noted that there are secondary effects with respect to the RF performance due to the lid (Appendix C). Although the module will perform differently when MMICs are inserted, at least some of the transmission parameters can be determined from the measured behavior of the module using the current methodology.

## BREADBOARDING -

### APERTURE COUPLED PATCHES:

#### MECHANICAL

Assembly requirements for the Patches were much less demanding. Since there were no thin film circuits, a high temperature assembly process could be employed. After the thick film gold was printed and etched, the 40-00070 glass was used to assemble the two layers together to form the Aperture Coupled Patch.

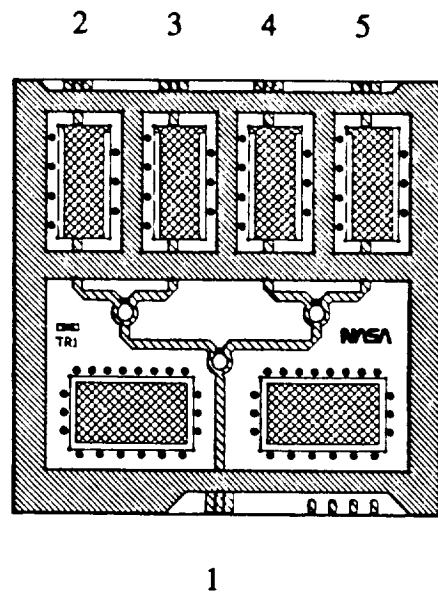


Figure 9. Port configuration on the Multichip Module as tested on the HP 8510C Network Analyzer.

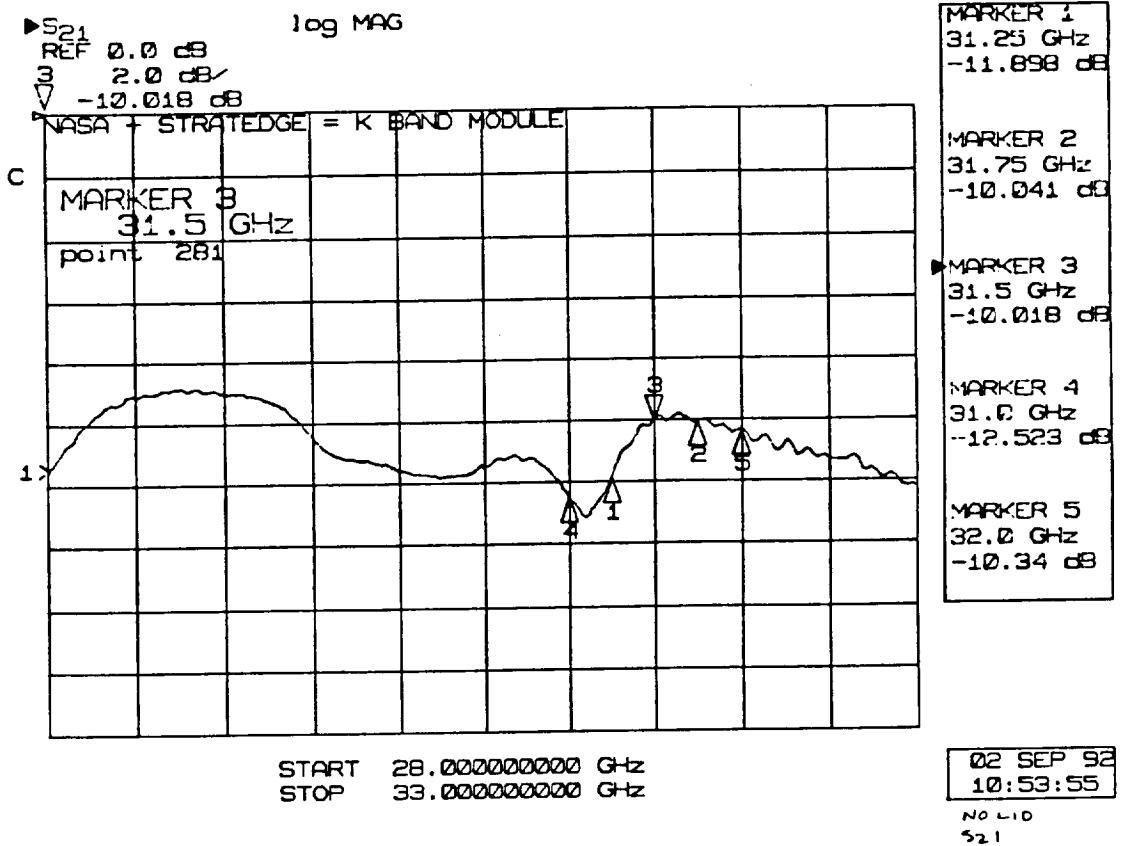


Figure 10. Plot of Wilkinson Power Divider insertion loss from port 1 to port 2 without the lid.



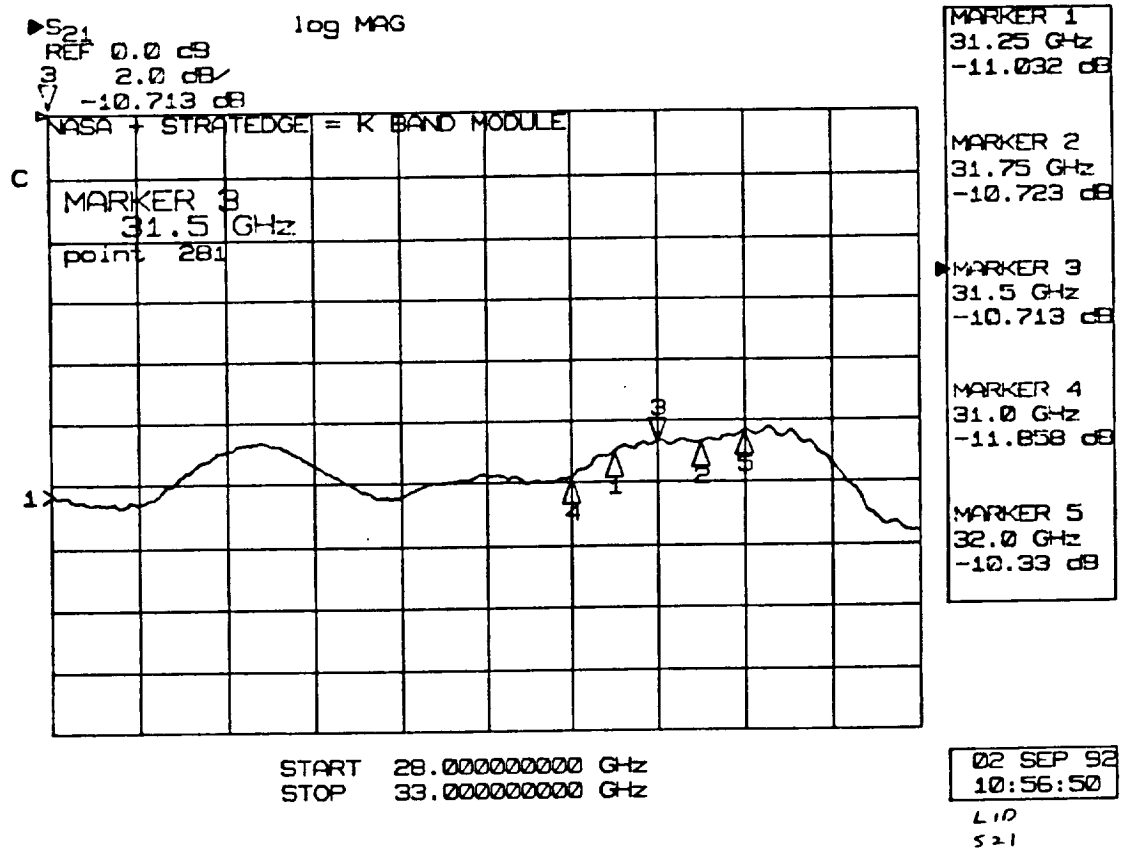


Figure 11. Plot of Wilkinson Power Divider insertion loss from port 1 to port 2 with the lid.

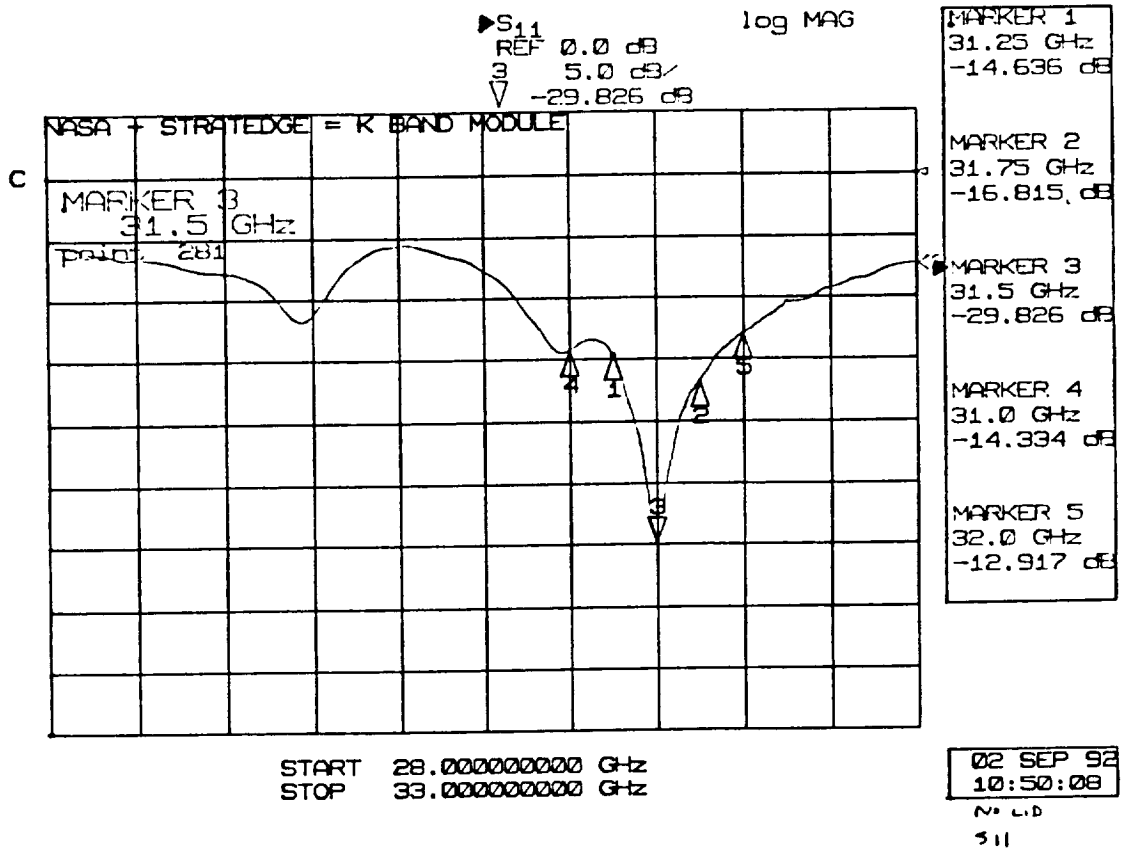


Figure 12. Plot of Wilkinson Power Divider return loss at port 1 without the lid.

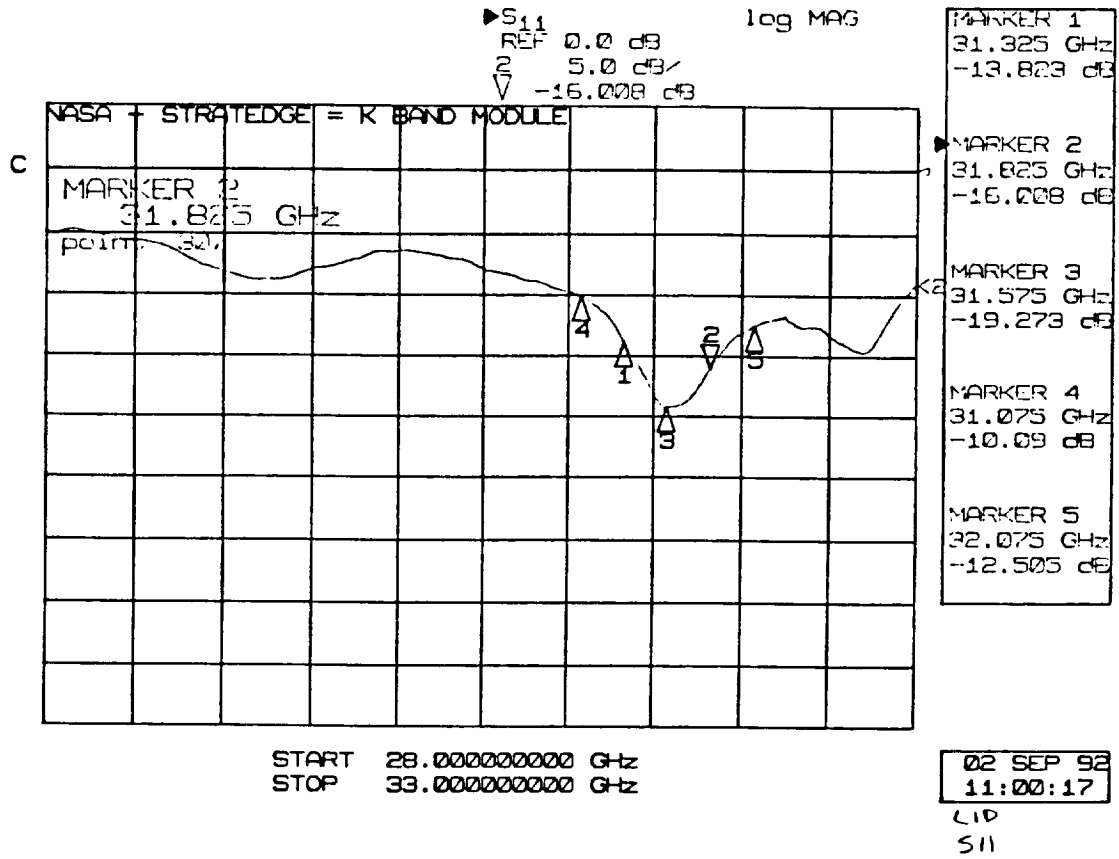


Figure 13. Plot of Wilkinson Power Divider return loss at port 1 with the lid.

## ELECTRICAL

NASA performed the testing on the broadside-fire packages in order to determine if this configuration would be acceptable for the Task 3 design. The results were acceptable but were slightly under the performance of end-fire elements. In addition, there were concerns with the fused silica not having enough strength and would require a metal base for support. With this in mind, NASA LeRC decided to use the 'end-fire' radiating element due to required structural support.

### RADIATING ELEMENT DESIGN:

This processing went relatively well except that there was a one mil gap requirement in the horn of the Microstrip/Slotline Taper element. The vendor only provided a 1.2 to 1.5 mil gap. Since the vendor could not consistently provide the one mil gap, NASA LeRC decided to use the alternate design, i.e. the Microstrip Taper/Slotline design. The two designs are shown in Figure 14.

### TASK 3: Phased Array Module

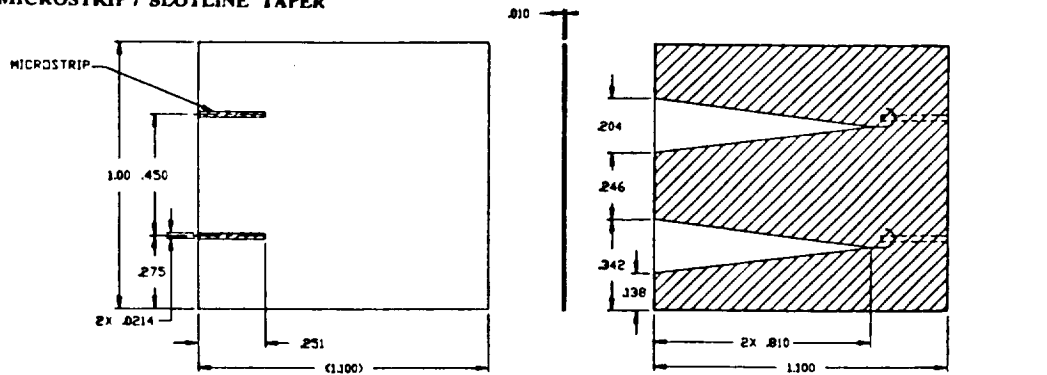
## MECHANICAL

On the Task 3 parts, it was determined that to get the 1"x2" RF substrates to adhere to the two DC layers without cracking, it was necessary to use conductive and non-conductive epoxies. The two DC layers were assembled with the low temperature glass and interconnect, but the RF layer and seal ring were attached with the conductive and non-conductive epoxies. The two epoxies were used instead of the seal glass and interconnect materials. Due to the cracking in the RF layers, only one fully functional module was able to be fabricated. However, all five 50 ohm through modules were able to be fabricated since electrical connection was not requirement. All packages were visually inspected for workmanship. Where possible, the packages were reworked for minor cosmetic flaws.

## ELECTRICAL

A 100% continuity testing of subassemblies was not incorporated until after all the Task 3 DC subassemblies were complete. When the DC subassemblies were tested, there was about a 50% electrical yield. Several of the subassemblies could be repaired. The ones that could not be repaired were used for the packages requiring the 50 ohm microstrip through lines. NASA was able to get the radiation patterns with these packages. The remaining electrically good subassemblies were used to fabricate functional packages. Functional testing will be conducted by NASA LeRC at their facility.

**MICROSTRIP / SLOTLINE TAPER**



**MICROSTRIP TAPER / SLOTLINE**

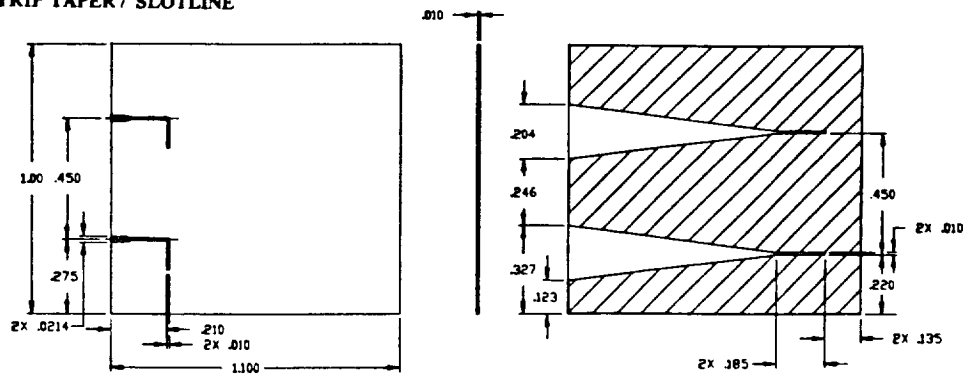


Figure 14. Two possible designs for the Task 3 radiating elements.

## SUMMARY

Much was learned about processing fused silica on this program. There were positive and negative aspects for using fused silica in microwave packages. On the positive side, StratEdge learned how to get the package to perform electrically at the specified frequency. The complex thin film designs worked for the modules.

On the negative side, StratEdge learned that fused silica is very difficult to handle and process into packages. The CTE mismatch is the major cause of low adhesion strength and that there are no compatible processing materials like there are with alumina. The thin film vendor ran into many processing difficulties partly due to the stresses caused by lasering the substrate.

The primary question that needs to be asked is whether the program met the specified goals. The goals of this program were:

- 1) Develop and build a standard package with fused silica substrates (Task 1),
- 2) Modify the design into a multichip module (Task 2), and
- 3) Develop the design into a phased array module (Task 3).

### TASK 1:

The Task 1 package was fabricated with a high temperature process. The Task 1 packages met many of the mechanical and electrical goals as stated in the Task 1 Summary report. Similar packages, developed under an alternate program, were electrically tested through 44 GHz but only a few yielded hermetic results. Several package configurations were designed and fabricated which increased StratEdge's fused silica processing knowledge. Unfortunately, resources did not permit us to obtain consistent results. Packages developed in this configuration at similar dimensions appear viable with only moderate additional resources.

### TASK 2:

The Task 2 process pushed the processing limit of packaging. First, the processing temperature needed to be kept below 500°C in order to minimize resistor degradation. Second, conductors and glasses needed to be developed to have minimal stress during firing due to the CTE mismatch between the silica and the inks and glasses. Third, since the soldering materials were not able to be matched to the low CTE silica, a conductive epoxy had to be used for base and 50 ohm through attach. Mechanically, the process goal was met with respect to substrate lamination. However, the bases could only be attached with a conductive epoxy.

Electrically, only a few of the modules were 100% DC electrically connected. One module was tested on the Network Analyzer and found to have approximately 11 dB insertion loss

across a 5 GHz bandwidth centered at 31.5 GHz. After analysis this value appears to be reasonable. This was the first time that a multilayer, multichip module that combined thick and thin film processing was assembled. The overall electrical performance was acceptable within the frequency band of interest, but further optimization should offer enhanced performance.

### TASK 3:

Only one of the Task 3 products was able to be completely assembled that met the DC electrical requirements. However, not all of the mechanical requirements were met. The two DC layers were assembled with the low temperature glass but the RF and seal ring had to be attached with conductive and non-conductive epoxies. There were five 50 ohm through modules that were assembled. The substrates were assembled with the low temperature seal glass and interconnect. They will be tested radiation patterns. The functional package will have the MMIC chips attached, wire bonded, and electrically tested. NASA will perform these tests at a later date.

### Recommendations:

In order to address a low cost package produced in large quantities (greater than 100,000), a number of process steps must be modified. The following recommendations should yield a more reliable and affordable approach.

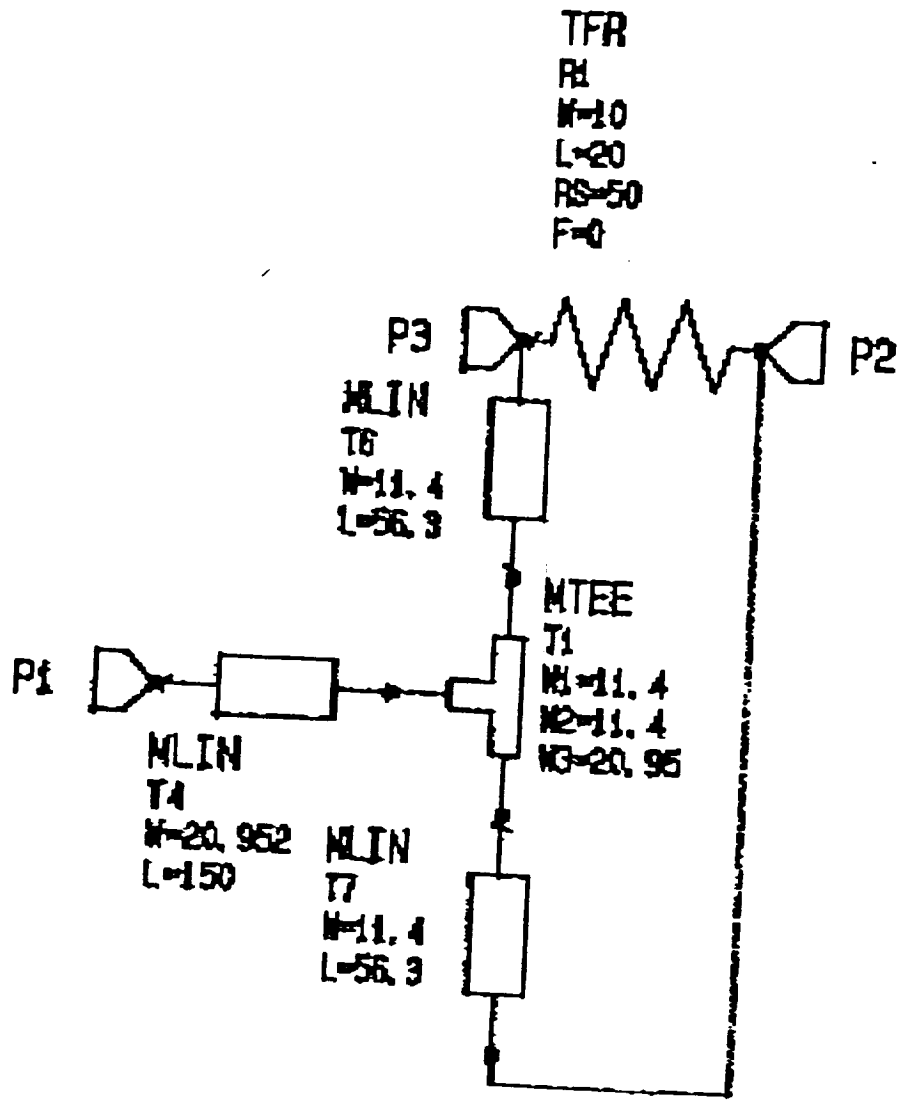
1. To address the stress cracking of the substrate:
  - A) Use a material system that has a CTE greater than that of fused silica. For example: alumina, cordierite, a silica based low temperature cofire system, or combinations of more compatible materials to increase strength and electrical performance.
  - B) Consider the use of ultrasonic machining instead of laser machining.
  - C) Redesign the corner radii in the cavities.
  - D) Use thicker silica on the DC layers
2. To address the costly thin film layer which includes RF circuitry and a resistive network:
  - A) Examine the electrical performance of this layer in thick film. For example, StratEdge Corp's etchable thick film gold provides 3 mil lines and spaces and holds 0.25 mil tolerance.
  - B) The thin film resistor needs to be addressed. From a processing perspective, the thin film profile needed to accommodate the resistive network is not compatible with many seal glasses employed to bond the silica layers together.

3. To address the issue of substrate fracture due to Au/Sn soldering:
  - A) Consider using alumina for the DC layers so that there is no CTE mismatch between the base/solder and the substrate.
4. Other possibilities include:
  - A) Redesign in 99.6% alumina
  - B) Redesign DC circuitry and interconnect distances
  - C) Use one substrate for DC layers
  - D) Use dielectric build up for DC bias and grounding.



**APPENDIX A**

**Power Divider Model**



CONTRACT NO.
DESIGN
CHECK
DESIGN
DESIGN ACTIVITY

Wilkinson Analysis : Thin Film Analysis/Model

FREQ GHz  
 TIME nS  
 CAP pF  
 IND nH  
 LNG in

VAR

F0=30  
 L0=.067  
 L1=.02  
 W0=.0114  
 W1=.01  
 A0=.05 ; LINE ATTEN DB/INCH  
 A1=250  
 RHO1=5E5  
 K0=3.8

CKT

MSUB ER4KO H=.01 T=.0002 RHO=1 RGH=2E-6  
 1 MLIN 1 2 W4W0 L4L0  
 1 MLIN 1 3 W4W0 L4L0 1 K4KO A4A0 F4FO  
 1 RES 2 3 R=100  
 MSUB ER4KO H=.01 T=.0002 RHO1RHO1 RGH=2E-6  
 MLIN 2 3 W4W1 L4L1 1 K4KO A4A1 F4FO  
 DEF2P 2 3 WILK  
 1 DEF3P 1 2 3 WILK

OUT

WILK DB[S11] GR1  
 WILK DB[S21] GR1A  
 WILK DB[S22] GR2

FREQ

SWEEP 26 40 1

GRID

RANGE 26 40 1

GR1 -30 0 10

GR1A -6 0

GR2 -30 0 10

OPT

FREQ-GHZ	DB[S11] WILK	DB[S21] WILK	DB[S22] WILK
26.0000	-7.106	-5.153	-7.106
27.0000	-7.058	-5.225	-7.058
28.0000	-7.013	-5.296	-7.013
29.0000	-6.969	-5.365	-6.969
30.0000	-6.928	-5.432	-6.928
31.0000	-6.889	-5.498	-6.889
32.0000	-6.852	-5.563	-6.852
33.0000	-6.817	-5.627	-6.817
34.0000	-6.784	-5.689	-6.784
35.0000	-6.753	-5.751	-6.753
36.0000	-6.724	-5.812	-6.724
37.0000	-6.696	-5.871	-6.696
38.0000	-6.671	-5.930	-6.671
39.0000	-6.648	-5.988	-6.648
40.0000	-6.626	-6.045	-6.626

Wilkinson Analysis : Ideal Resistor Model

FREQ GHz  
 TIME nS  
 CAP pF  
 IND nH  
 LNG in

VAR

F0=30  
 L0=.058 ; exactly quarter wavelength  
 L1=.012 at 30 GHz  
 W0=.0114  
 W1=.0114  
 A0=.05 | LINE ATTEN DB/INCH  
 A1=420 | ATTEN EQUIV TO 100 OHMS/SQU.  
 K0=3.8

CKT

MSUB ER4KO H=.01 T=.0002 RHO=1 RGH=2E-6  
 MLIN 1 2 W4W0 L4L0  
 MLIN 1 3 W4W0 L4L0 | K4KO A4A0 F4FO  
 RES 2 3 R=100  
 | TLINP 2 3 Z=70 L4L1 K4KO A4A1 F4FO  
 | STEE 2 3 4 W1=.1 W2=.14 W3=.0097  
 | SLSC 4 W=.0097 L4L1  
 | SLIN 3 5 W=.14 L=.3  
 DEF3P 1 2 3 WILK

OUT

WILK DB[S11] GR1  
 WILK DB[S21] GR1A  
 WILK DB[S22] GR2

FREQ

SWEEP 26 34 1

GRID

RANGE 26 34 1  
 GR1 -30 0 10  
 GR1A -60 0  
 GR2 -30 0 10

OPT

FREQ-GHZ	DB[S11] WILK	DB[S21] WILK	DB[S22] WILK
26.0000	-22.378	-3.055	-52.613
27.0000	-24.635	-3.045	-45.913
28.0000	-27.605	-3.038	-42.948
29.0000	-31.538	-3.033	-41.451
30.0000	-34.491	-3.032	-40.846
31.0000	-31.517	-3.034	-40.963
32.0000	-27.575	-3.038	-41.825
33.0000	-24.597	-3.046	-43.658
34.0000	-22.330	-3.056	-47.028

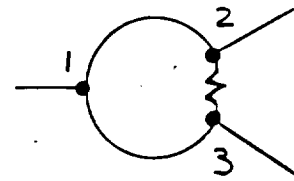
WILK - POWER DIVIDER

DIM:

FREQ GHz

VAR:

F0=30  
 L0=.067  
 L1=.02  
 W0=.0114  
 W1=.01  
 A0=.05 | LINE ATTN DB/INCH  
 A1=250 | ~~ATTEN EQUIV TO 300 OHMS/INCH~~  
 RHO1=5E5  
 K0=3.8



PORT IDENTIFICATION

CKT:

\* Please see attached models which depict resistor at {6.9 Ohms  
 MSUB ER4KO H=.01 T=.0002 RHO=1 RGH=2E-6  
 MLIN 1 2 W4W0 I4L0  
 MLIN 1 3 W4W0 I4L0 I4KO A4A0 F4F0  
 RES 2 3 R=300  
 MSUB ER4KO H=.01 T=.0002 RHO=RHO1 RGH=2E-6  
 MLIN 2 3 W4W1 I4L1  
 TLINP 2 3 Z=70 I4L1 K=2.83 A4A1 F4F0  
 DEF3P 1 2 3 WILK

OUT:

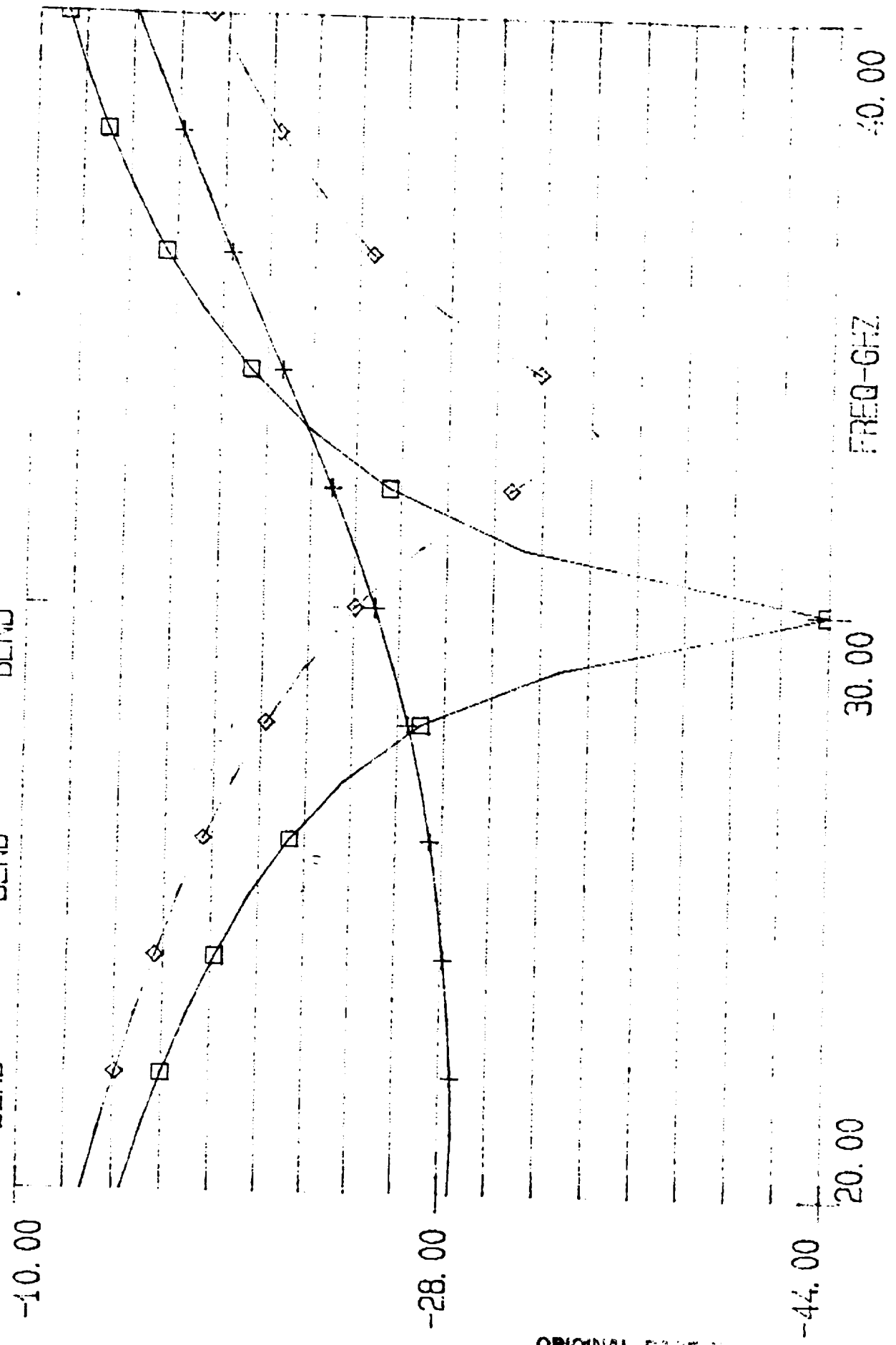
WILK DB[S11] GR1  
 WILK DB[S21] GR1A  
 WILK DB[S22] GR2  
 WILK DB[S32] GR2A  
 FREQ  
 SWEEP 26 40 1  
 GRID  
 RANGE 26 40 1  
 GR1 -30 0 10  
 GR1A -6 0  
 GR2 -30 0 10  
 GR2A -30 0  
 OPT

FREQ-GHZ	DB[S11] WILK	DB[S21] WILK	DB[S22] WILK	DB[S32] WILK
26.0000	-22.166	-3.087	-39.274	-24.822
27.0000	-24.680	-3.078	-39.866	-25.049
28.0000	-28.248	-3.073	-20.544	-24.524
29.0000	-33.712	-3.072	-21.296	-23.470
30.0000	-36.017	-3.074	-22.083	-22.194
31.0000	-29.912	-3.081	-22.822	-20.900
32.0000	-25.574	-3.093	-21.360	-19.674
33.0000	-22.581	-3.109	-21.494	-18.543
34.0000	-20.330	-3.129	-21.085	-17.506
35.0000	-18.538	-3.155	-22.173	-16.551
36.0000	-17.059	-3.184	-20.940	-15.665
37.0000	-15.808	-3.218	-19.572	-14.830
38.0000	-14.730	-3.257	-18.189	-14.033
39.0000	-13.790	-3.299	-16.850	-13.258
40.0000	-12.962	-3.344	-15.580	-12.491

EESof - Touchstone --

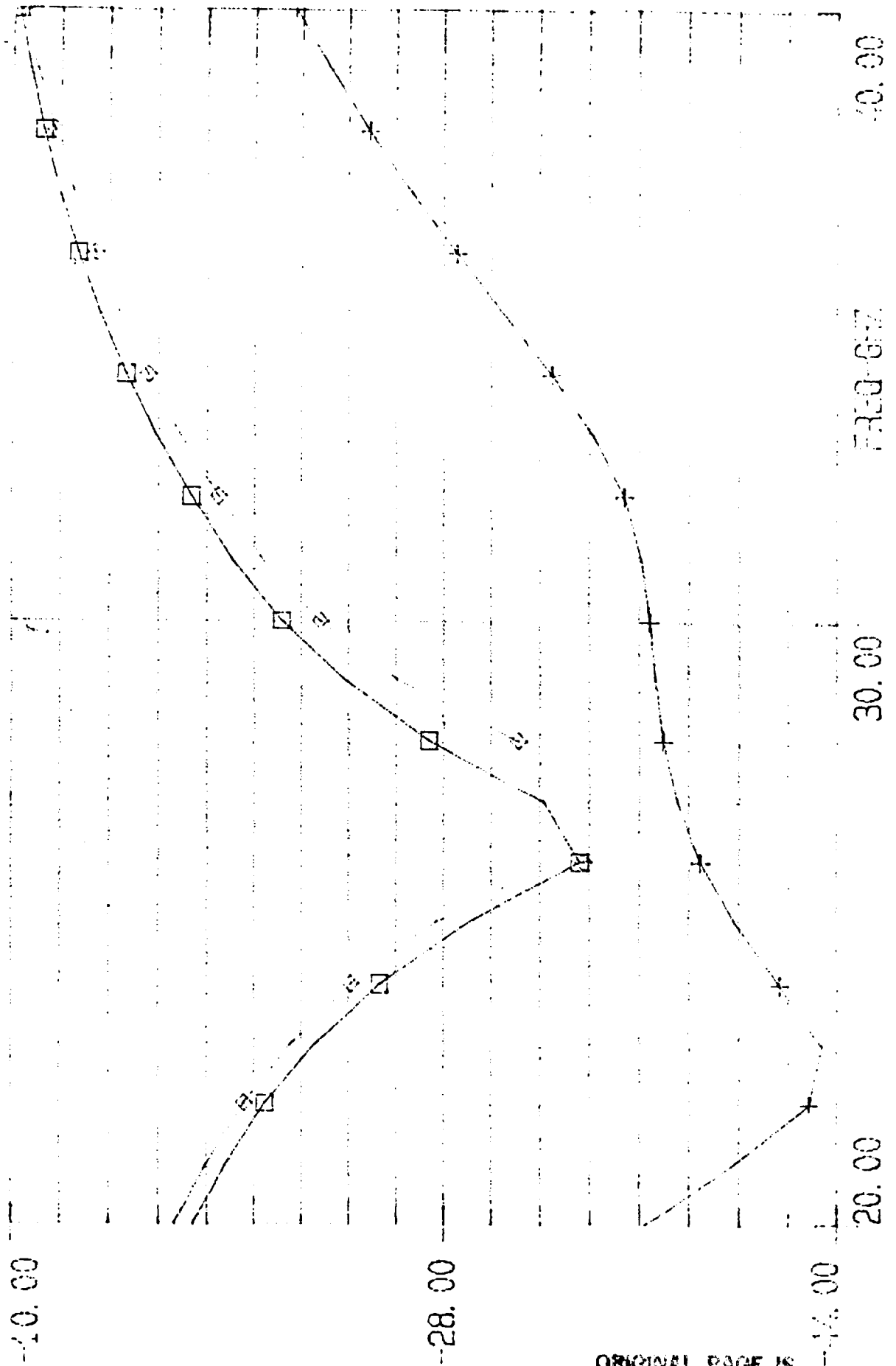
THIN FILM RESISTOR ANALYSIS

□ DB[S11] + DB[S22]    ◇ DB[S32]  
BEND                    BEND



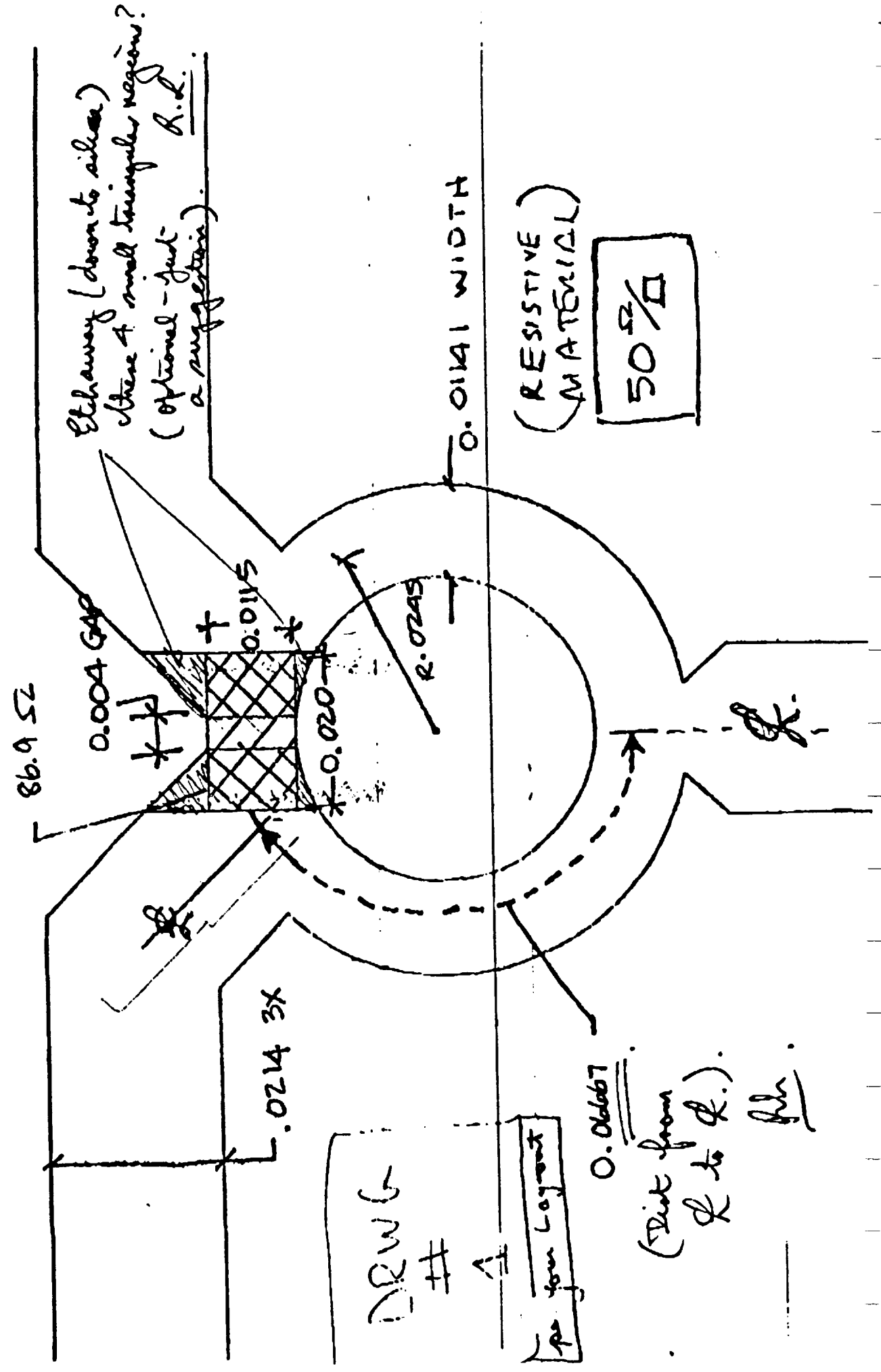
EPSON TOUCHSTONE - LUMPED RESISTOR ANALYSIS (Thin Film Resistor Removed)

□ 03[S21] + 03[S22]    ◆ 03[S32]  
 BEND                    BEND



ORIGINAL PAGE IS  
 OF POOR QUALITY

SINGLE CROSS-HATCH = RESISTIVE MATERIAL ITSELF  
 DOUBLE CROSS-HATCH = CONDUCTOR OVER RESISTIVE MATERIAL



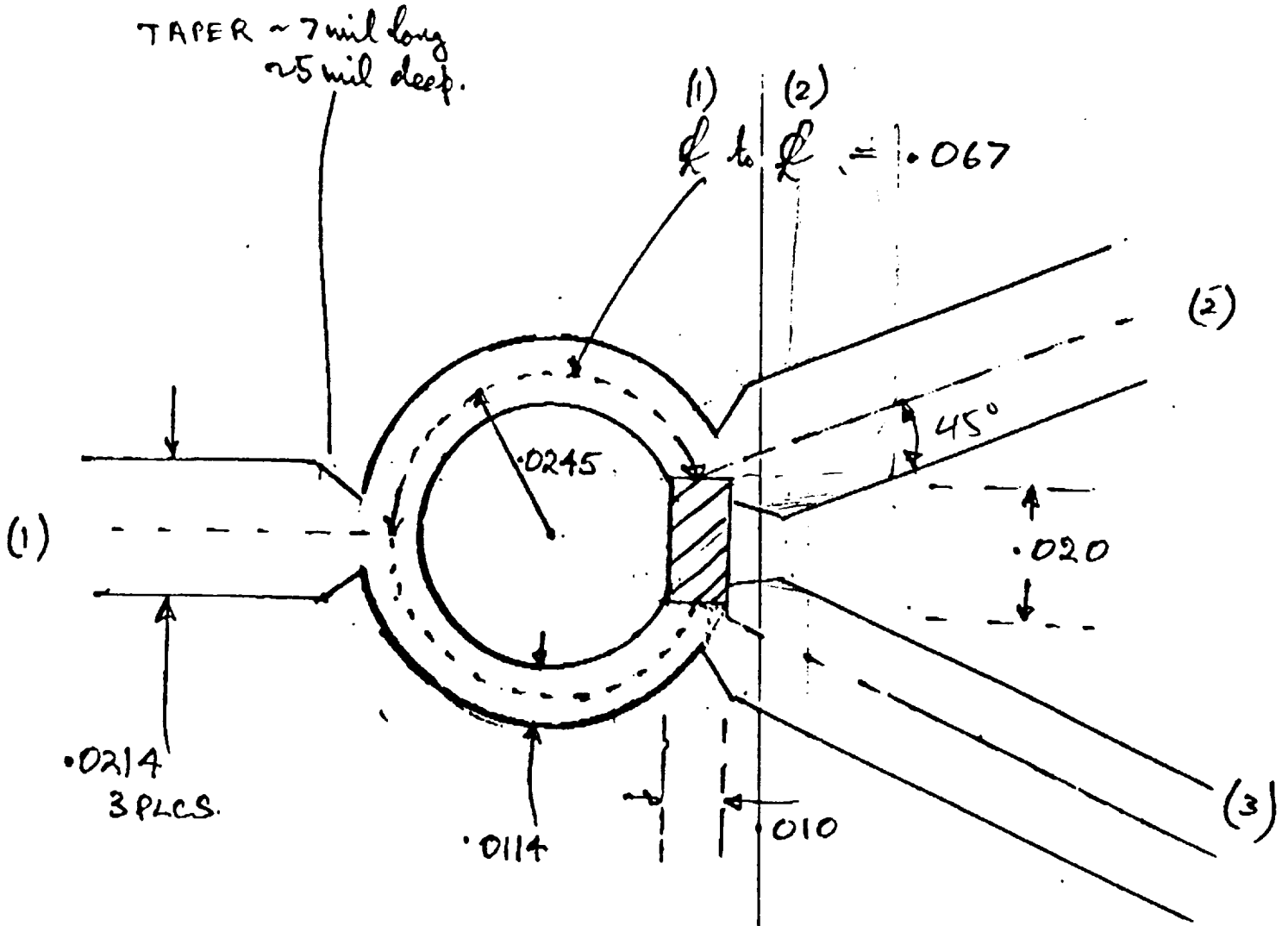
Etchaway (down to silica)  
 where 4 small triangular regions?  
 (Optional - just a suggestion) R.D.

(RESISTIVE MATERIAL)  
 50%

DRAW # A  
 per your layout

0.00667  
 (Dist from R to R.)  
 R.D.





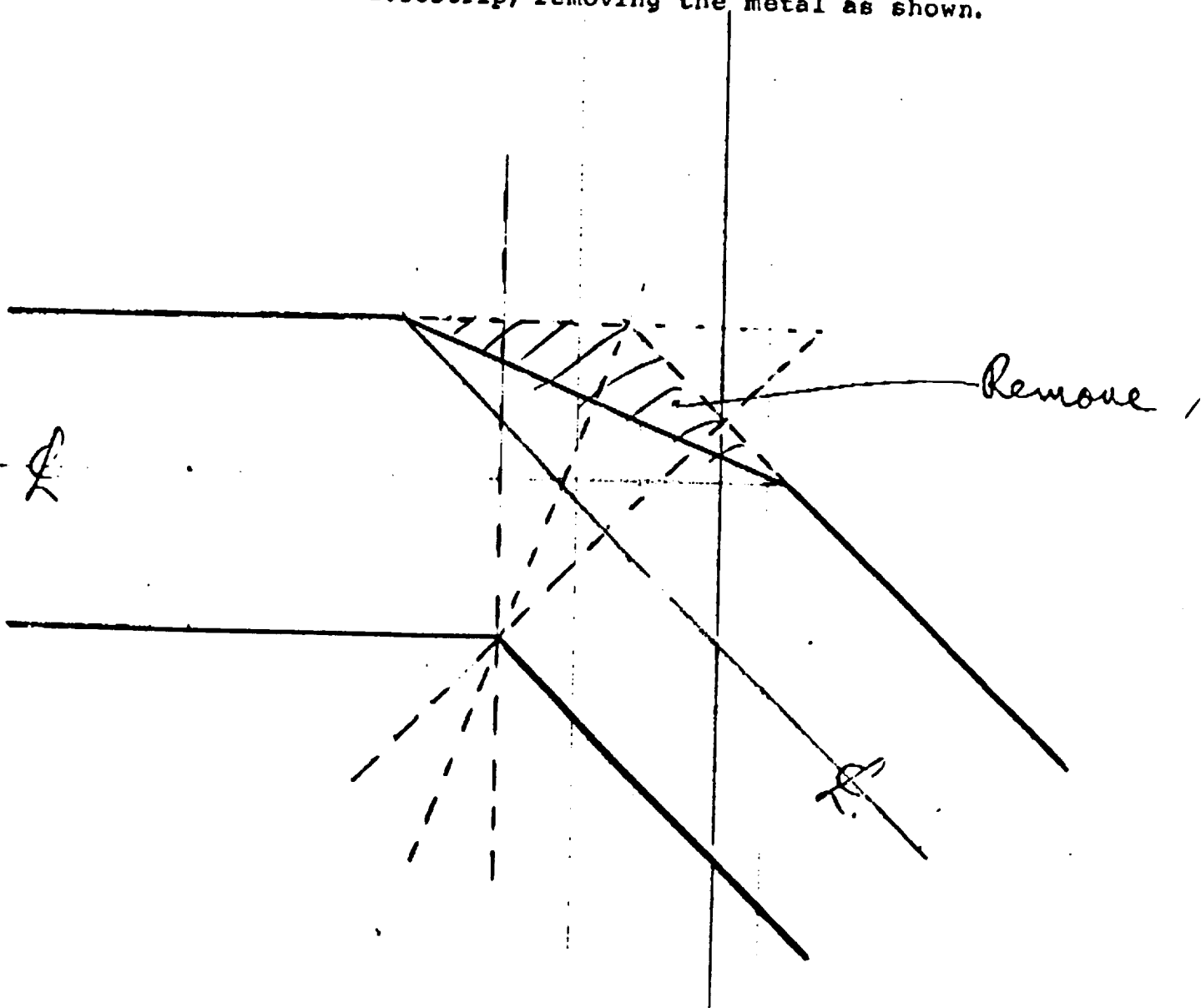
30 GHz WILKINSON POWER DIVIDER.

SCALE 40:1

R.L. 8/13/91

"LIMONIX"  
"QUANTUMIX"  
laser trimming  
ckt

Simply cut across the outer corner where the center lines intersect the microstrip, removing the metal as shown.



**APPENDIX B**

**Actual Package Power Divider Results and Discussion**

To: G. Holz, R. Bub  
Fr: M. Goetz  
Dt: 1/27/92  
Re: Summary Report - Wilkinson Power Divider Measurements

### INTRODUCTION

The following is a summary of the measurement procedure, technique, and results from the thin film, 1/4 and 1/3 wavelength, Wilkinson power dividers. The measurement plots are referred to by the thin film resistor value incorporated in the divider, and the time of the measurement, i.e. 100-20:26:06. No conclusions are made to specific results, as they are determined by the customer's results and expectations. Since there were no electrical specifications supplied by the customer, only general performance observations can be made.

### MEASUREMENT PROCEDURE AND TECHNIQUE

Measurements were made on the power dividers using the HP8510C Network Analyzer, interfaced with the Wiltron 3680K Universal Test Fixture. Cable adapters were used to transition from 2.4mm to 2.92mm connectors. A 3.5mm right angle launch was also used to connect port 1 of the VNA to the PD1 (source). Port 2 of the VNA was connected to PD2, and PD3 was terminated with 50 ohms. This configuration afforded measuring the following scattering parameters: S11, S21, S12, S22. Port 1 was then connected to PD3 while PD1 was terminated with 50 ohms. From that connection, S32 was measured.

A Thru-Reflect-Line (TRL) calibration was developed within the network analyzer with the following configuration: 401 pts., step mode, fstart=1GHz, fstop=50GHz. The bandwidth of interest was then set between 26-34GHz. The marker(s) were set initially for a center frequency of 30GHz, which was the designed frequency of operation.

2.5mm(100 mils) of line was calibrated out on the power divider using the Wiltron TRL cal kit. This was for the purpose of de-embedding the connectors.

One effect on the measurements was the assembly of the right angle launch. The TRL cal was made on the two standard ports of the UTF, using the 2.4mm cables. The right angle launch had a 3.5mm connector, so the port 1 cable was replaced with a 3.5mm cable. The magnitude of the effect of this replacement is unknown. 3.5mm connectors and cables are designed to be mode-free to 26.5GHz, but the frequency range of measurement was 26-34GHz.

### DISCUSSION

There were two types of Wilkinson power dividers designed, manufactured, and tested. The first is a 100 ohm, 1/4 wavelength, NiCr substrate, the second is an 86.9 ohm, 1/3 wavelength, TaN substrate. Both designs used a thinfilm gold conductor and thinfilm resistors.

### 100 ohm NiCr

\*The insertion loss (S21) mag/phase matched well for the five devices measured, (100-19:09:09). The phase was aligned using electrical delay for each device. The magnitude of the insertion loss ranged from 4-5 dB across the band. On graph 100-17:07:48, the magnitude had a range of 5-6 dB.

\*The return loss (S11) mag was between 13-23 dB at the center frequency 30.2775GHz, (100-18:44:37, 100-17:09:13).

\*The S12 and S22 mag were measured on graph 100-20:15:52. The result again show a good match, with the range of S12 between 4-5 dB, and S22 >10 dB across the band. A desirable return loss for S22 would be >15 dB in the operating band.

\*The S32 mag/phase was measured on two devices. On graph 100-16:01:44, the magnitude had a range of >12 dB. Graph 100-15:58:57 had an S32 response of 5-10 dB. No conclusions were made as to the desired value, but it should be noted that there was a significant difference between the two parts. The effect is possibly attributed to inconsistencies in the thinfilm resistor.

\*Graphs 100-19:11:00, -19:03:26, and -19:20:19 were individual measurements on a single 100 ohm device. The insertion loss was greater than expected, with a range of 6-8 dB. The return loss was >28 dB at the designed center frequency of 30GHz, and the phase was linear across the band.

### 86.9 ohm TaN

\*The insertion loss (S21) mag/phase matched well for the five devices measured, (86.9-19:22:52). The phase was aligned using electrical delay for each device. The magnitude of the insertion loss ranged from 3-6 dB across the band. On graphs 86.9-16:34:51, and -16:55:14, the magnitude ranged from 3.5-5.0 dB.

\*The return loss (S11) mag ranged from 17-30 dB at the center frequency 30.2775GHz, (86.9-19:43:05). Individual S11 measurements were made, with >22 dB return loss at the center frequency (86.9-16:41:35, -16:49:49).

\*The S12 and S22 mag were measured on graph 86.9-20:23:54. The insertion loss ranged from 3-4 dB, with the return loss >10 dB across the band. Again, the S22 mag should be >15 dB.

\*The S32 mag/phase was measured on graph 86.9-16:10:56. The insertion loss was >11 dB across the band.

\*Graphs 86.9-19:43:27, -19:38:31, and -19:48:03 were individual measurements on a single 86.9 ohm device. The insertion loss ranged from 7-10 dB. The return loss was >32 dB at the center frequency of 30GHz, and the phase was linear across the band.

Graphs 86.9-20:22:06, -20:19:11, and -20:23:26 were also individual measurements on a single 86.9 ohm device. The insertion loss ranged from 3-4 dB. The return loss >28 dB at a frequency of 30.4GHz, and the phase was linear across the band.

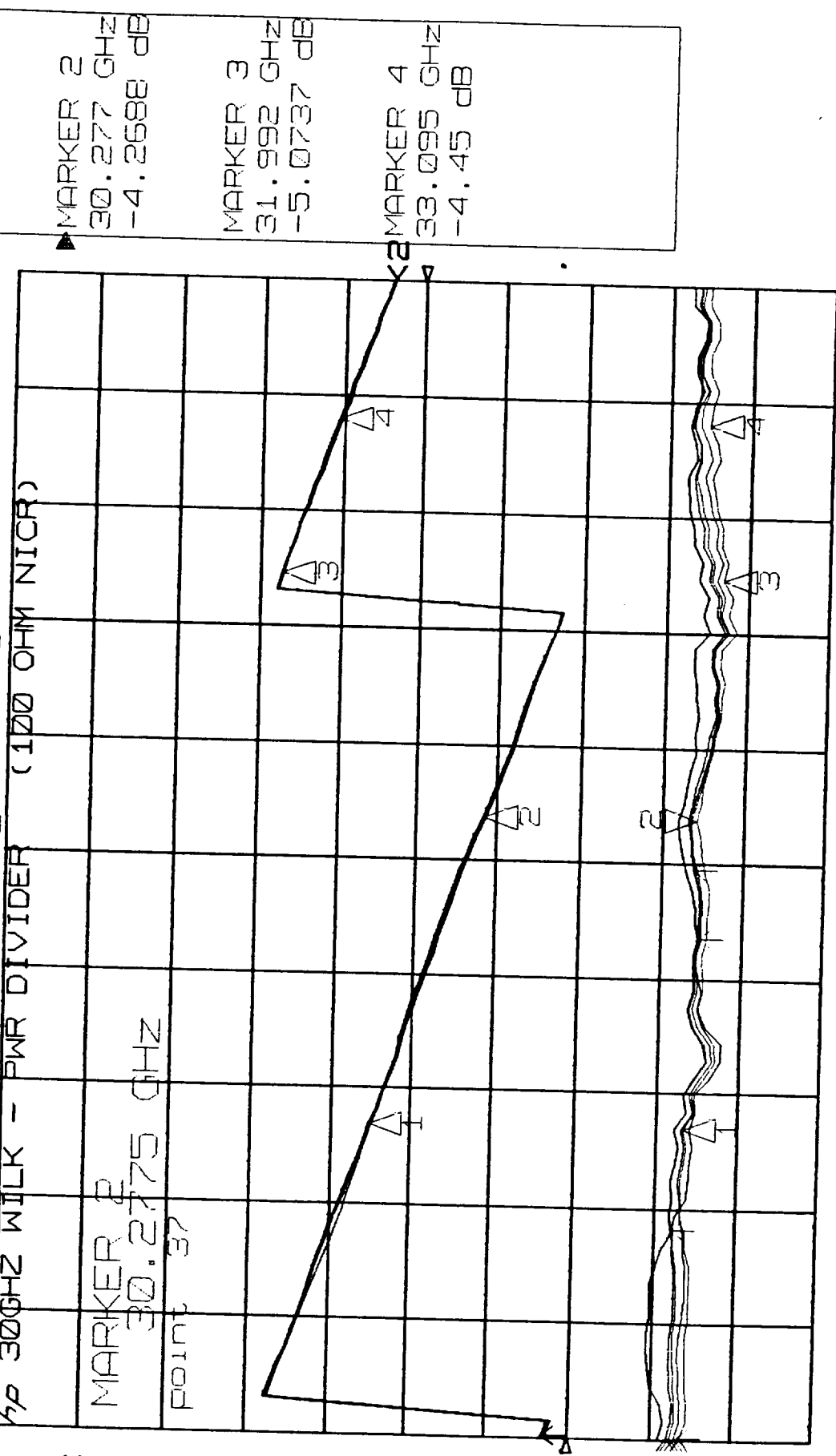
### CONCLUSIONS

Although there were no electrical specifications for performance requirements, either to previous measured data, or to existing design, a Touchstone model was developed for the purpose of determining some ideal or reasonable results. An ideal bandpass power divider would have a narrow operating range, where the

divider elements would be matched and balanced to the input port of the device. The return loss (S11) of the input port should be great at the designed center frequency (>20 dB). The impedance of the divider elements should be matched to the resistor element and the input port, and would have a minimal insertion loss (3-4 dB) across the band. The elements should be balanced, such that the same loss is attained on each.

An MDS circuit is presently being designed from the physical properties of the devices. Measurement data will be imported from the network analyzer, and an optimization will be performed to determine the modifications made to the physical model to match the electrical model. The model can therefore be used for future designs.

▲ S21 & M2 REF 0.0 dB  
 ▼ 3.0 dB / -4.2688 dB  
 ▲ S21 & M6 REF 0.0 °  
 ▼ 100.0 % / -84.875 °  
 4P 30GHZ WILK - PWR DIVIDER (100 OHM NICK)

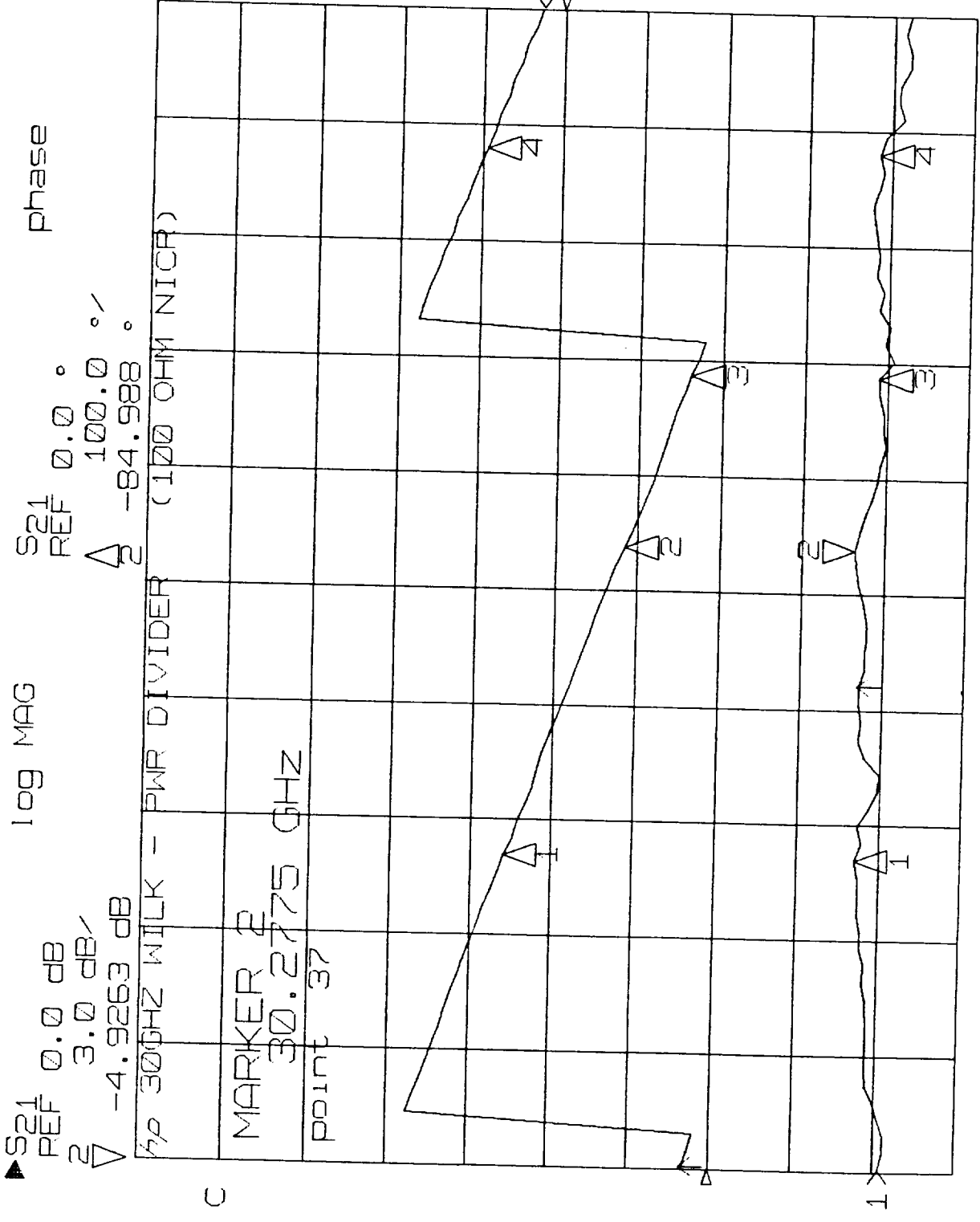


START 25.867500000 GHz  
 STOP 34.075000000 GHz

20 JAN 92  
 19:08:08

▲ S21 REF 0.0 dB  
 2 ▽ 3.0 dB  
 ▽ -4.9263 dB  
 S21 REF 0.0°  
 2 ▲ 100.0°  
 ▽ -84.988°

30GHz WILK - PWR DIVIDER (100 OHM NICR)  
 MARKER 2  
 30.2775 GHz  
 point 37  
 MARKER 1  
 28.072 GHz  
 -5.1067 dB  
 MARKER 2  
 30.277 GHz  
 -4.9263 dB  
 MARKER 3  
 31.502 GHz  
 -5.6902 dB  
 MARKER 4  
 33.095 GHz  
 -5.5544 dB



START 25.867500000 GHz  
 STOP 34.075000000 GHz

15 JAN 92  
 17:07:48



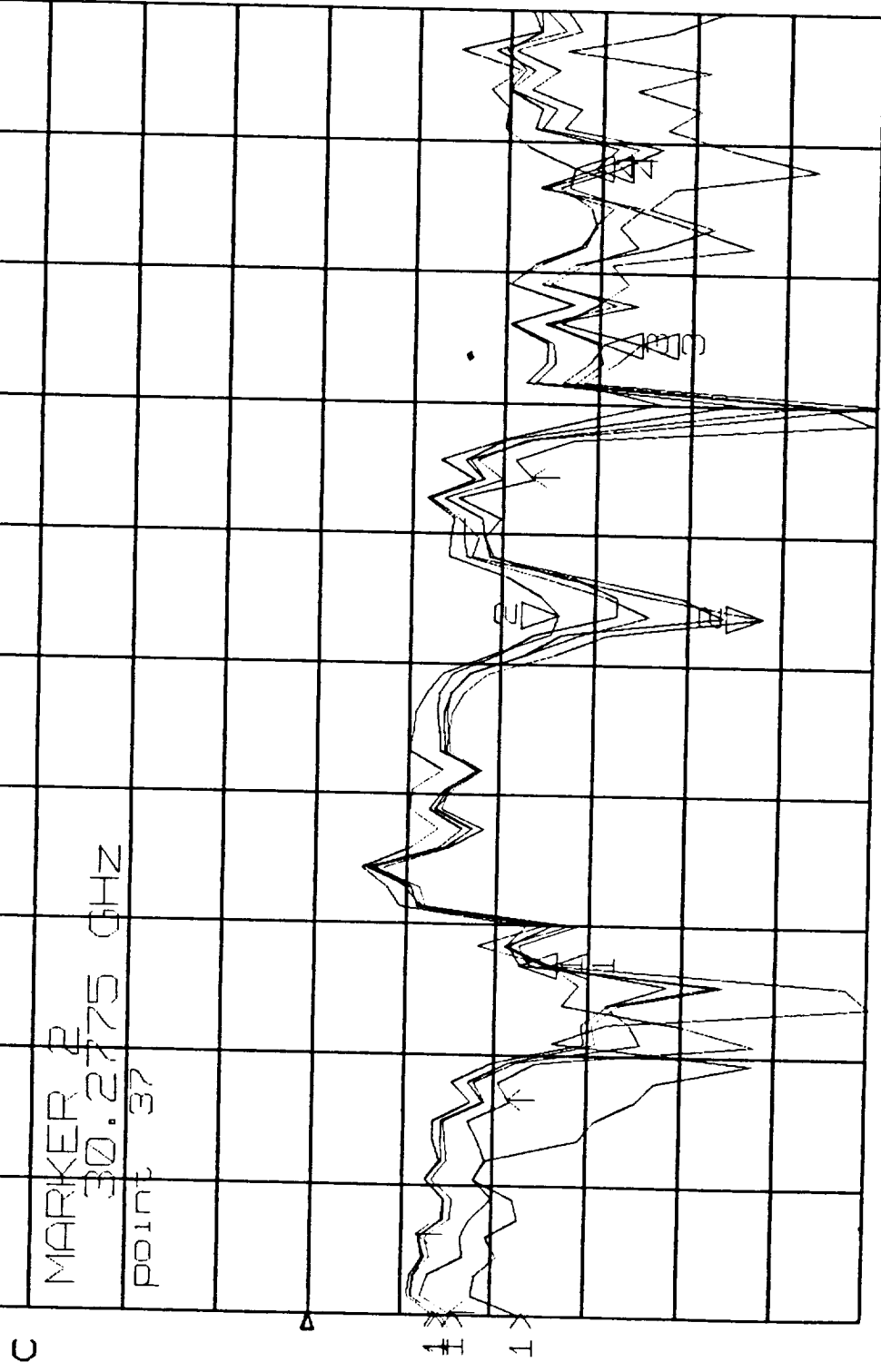
▶ S11 & M1 109 MAG

REF 0.0 dB

2 5.0 dB

▽ -23.078 dB

HP 300HZ WILK - PWR DIVIDER (100 OHM NICR)



MARKER 2  
30.2775 GHZ

point 37

MARKER 1  
28.072 GHZ  
-13.008 dB

MARKER 2  
30.277 GHZ  
-23.078 dB

MARKER 3  
31.992 GHZ  
-13.258 dB

MARKER 4  
33.095 GHZ  
-13.548 dB

START 25.867500000 GHZ  
STOP 34.075000000 GHZ

20 JAN 92  
18:20:00

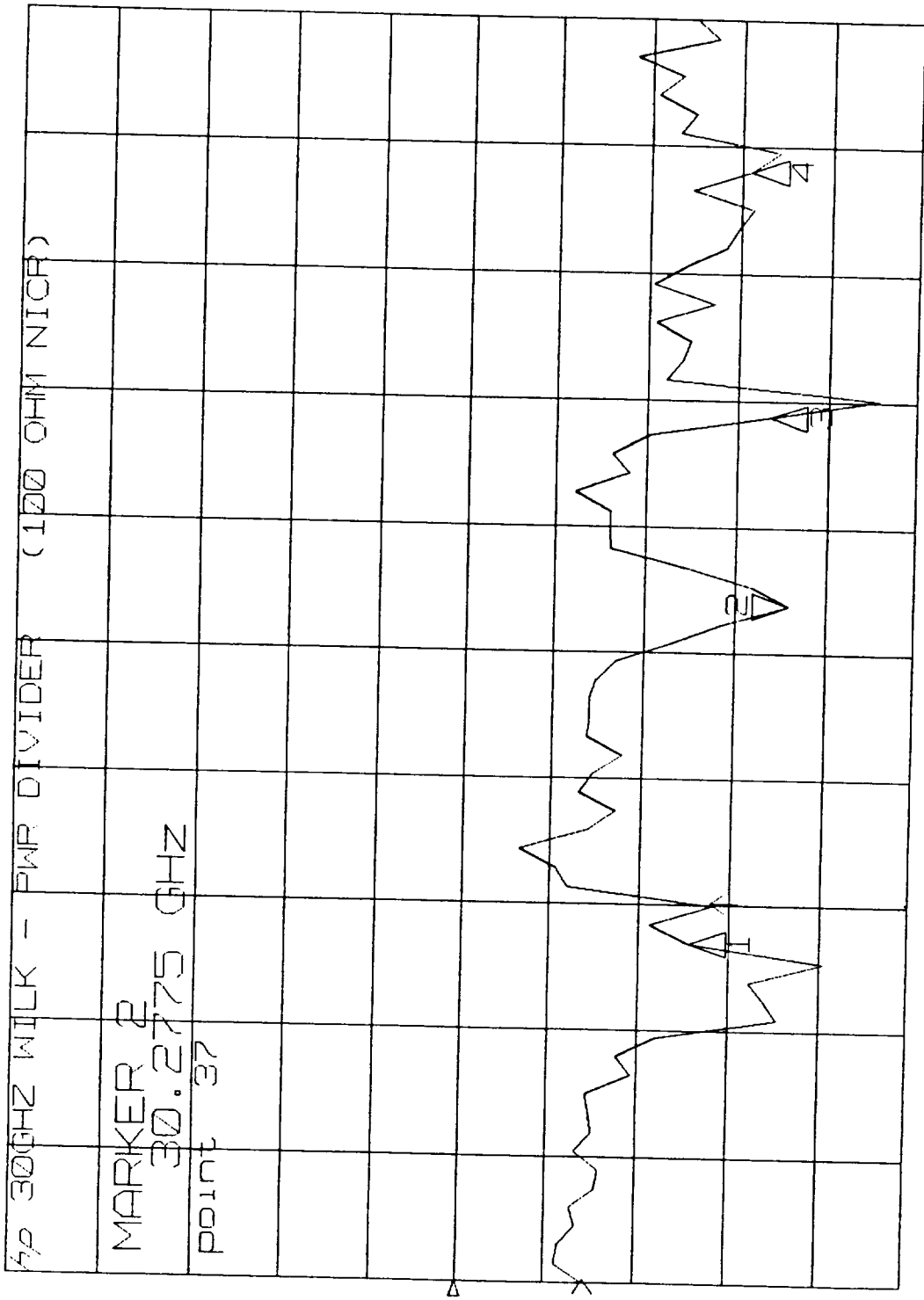
S11  
REF 0.0 dB  
2 5.0 dB  
▽ -17.916 dB

MARKER 1  
28.072 GHz  
-12.799 dB

MARKER 2  
30.277 GHz  
-17.916 dB

MARKER 3  
31.502 GHz  
-16.759 dB

MARKER 4  
33.095 GHz  
-15.477 dB



START 25.867500000 GHz  
STOP 34.075000000 GHz

15 JAN 92  
17:09:13

▲ S12 & M3  
 REF 0.0 dB  
 2 ▽ 3.0 dB  
 ▽ -4.3054 dB

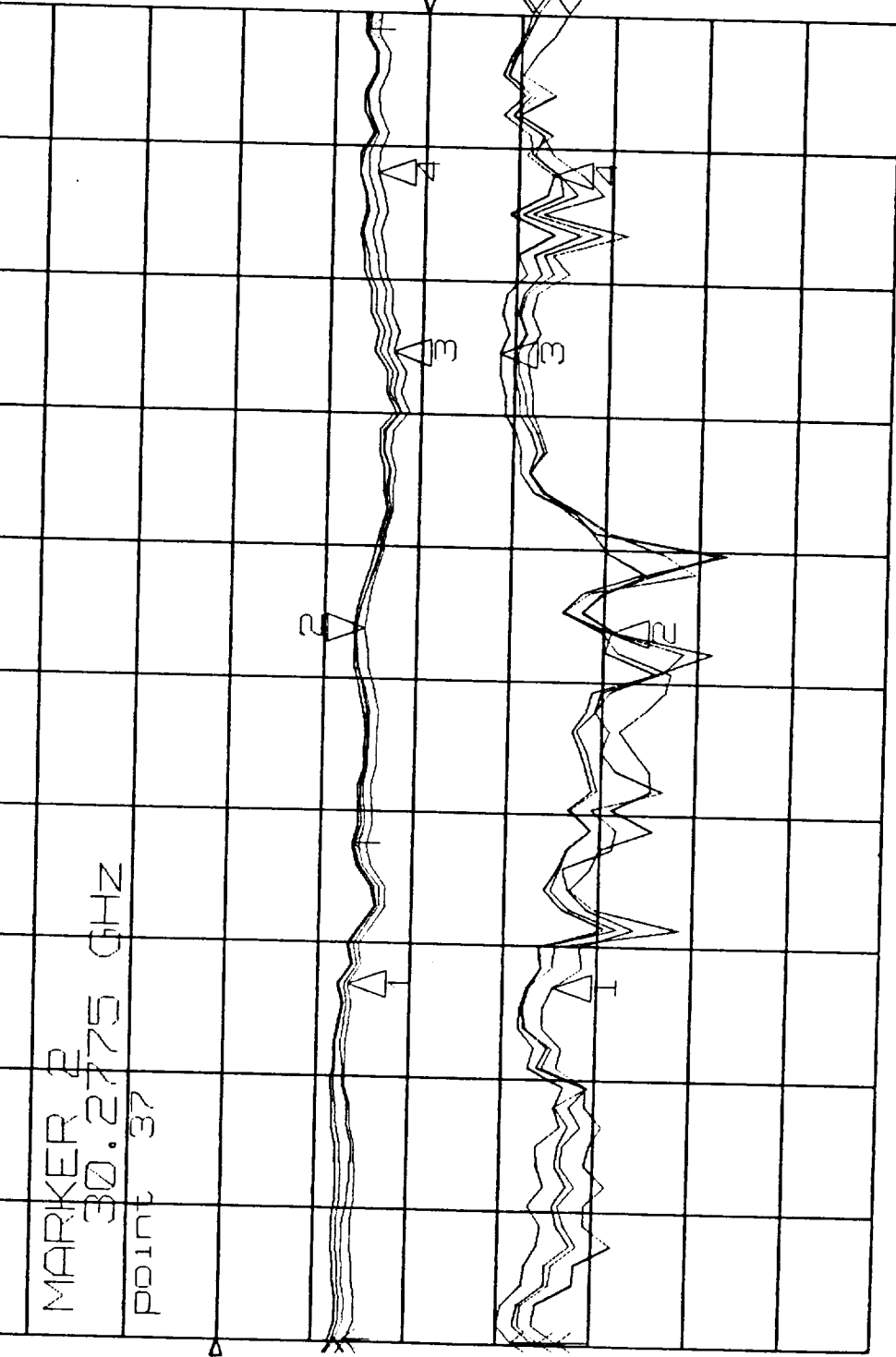
109 MAG

▲ S22 & M8

REF 0.0 dB  
 2 ▲ 10.0 dB  
 ▽ -20.765 dB

109 MAG

4p30GHZ WIUK - PAR DIVIDER (100 OHM NICR)



MARKER 2  
 30.2775 GHz  
 point 37

MARKER 1	28.072 GHz	-3.9968 dB
MARKER 2	30.277 GHz	-4.3054 dB
MARKER 3	31.992 GHz	-5.0671 dB
MARKER 4	33.095 GHz	-4.4272 dB

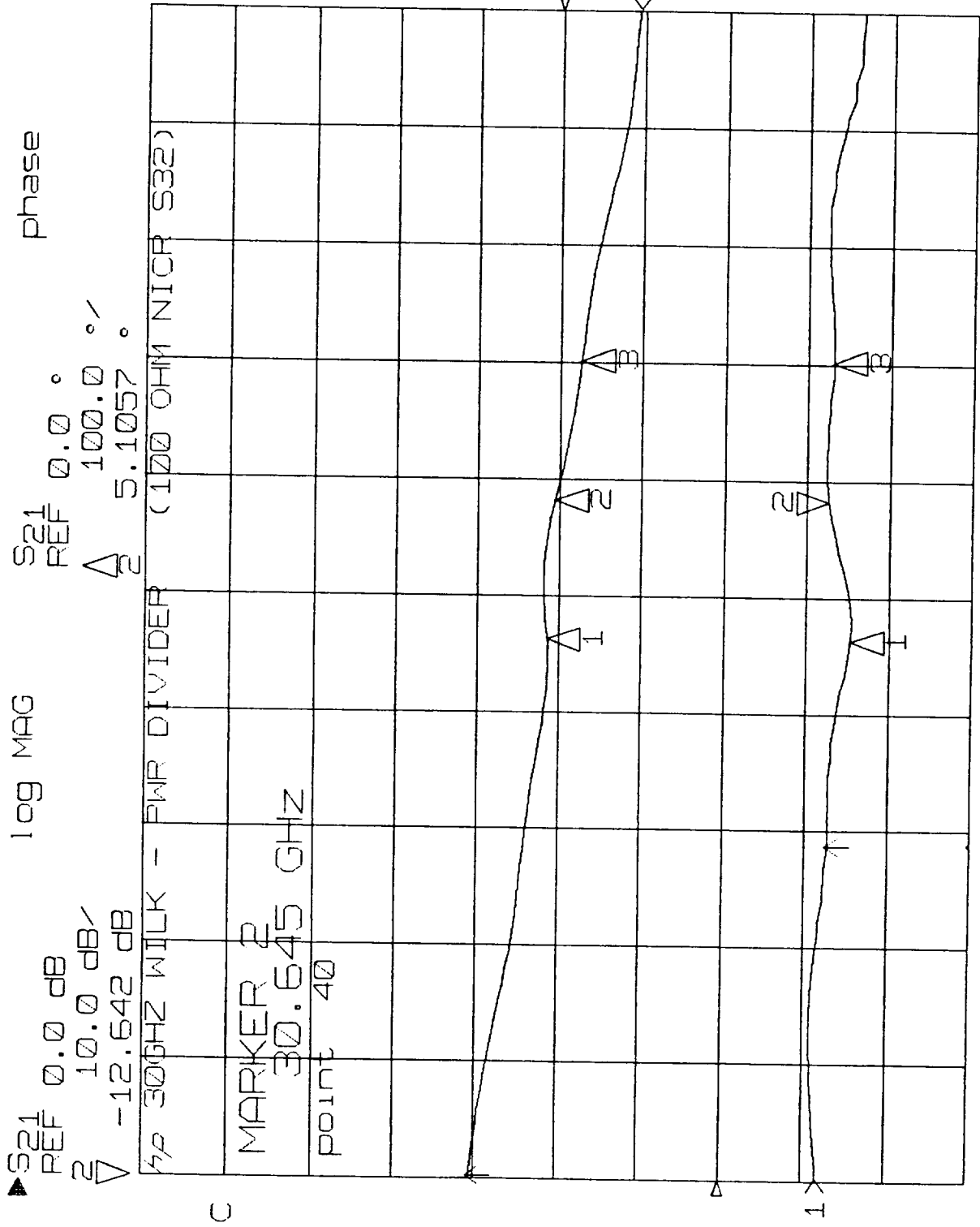
START 25.867500000 GHz  
 STOP 34.075000000 GHz

21 JAN 92  
 20:08:08

MARKER 1  
 29.665 GHz  
 -15.333 dB

MARKER 2  
 30.645 GHz  
 -12.642 dB

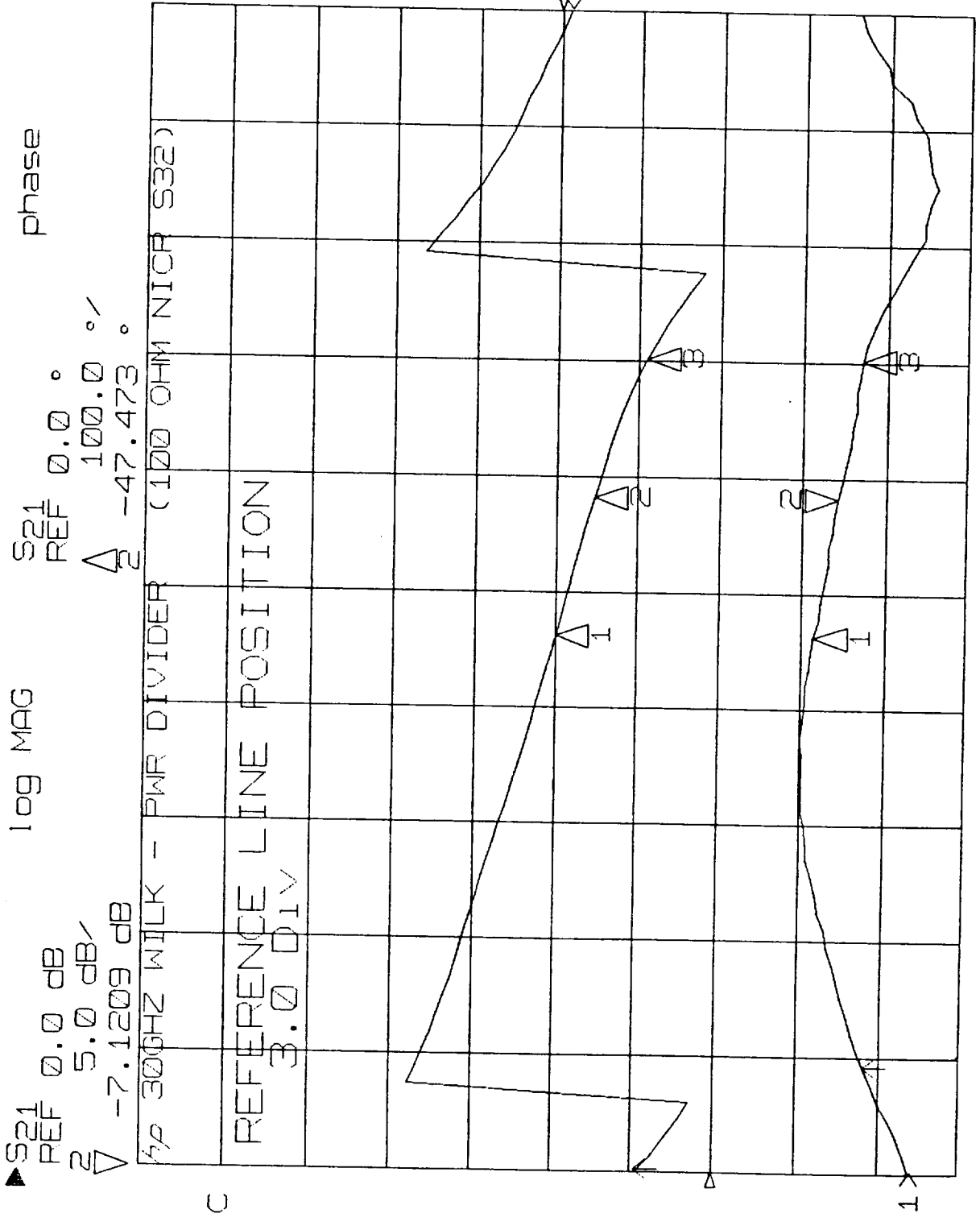
MARKER 3  
 31.625 GHz  
 -13.015 dB



START 25.867500000 GHz  
 STOP 34.075000000 GHz

15 JAN 92  
 16:01:44

MARKER 1  
 29.665 GHz  
 -5.707 dB  
 MARKER 2  
 30.645 GHz  
 -7.1209 dB  
 MARKER 3  
 31.625 GHz  
 -8.4902 dB



START 25.867500000 GHz  
 STOP 34.075000000 GHz

15 JAN 92  
 15:58:57

log MAG

521

REF 0.0 dB

1 2.0 dB

-6.6826 dB

30GHZ WILK - PWR DIVIDER (100 OHM)

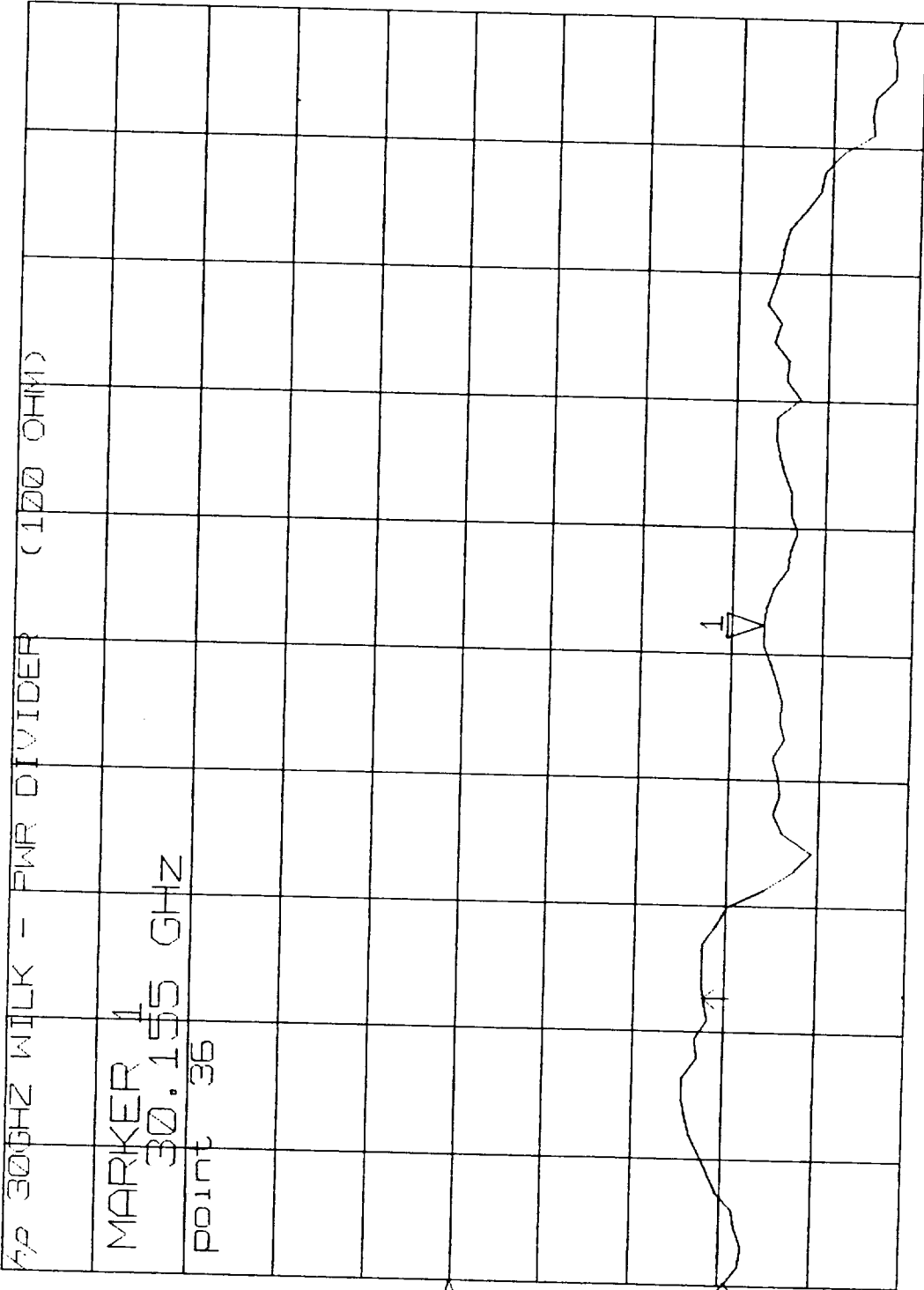
C

MARKER 1

30.155 GHZ

point 36

MARKER 1  
30.155 GHZ  
-6.6826 dB



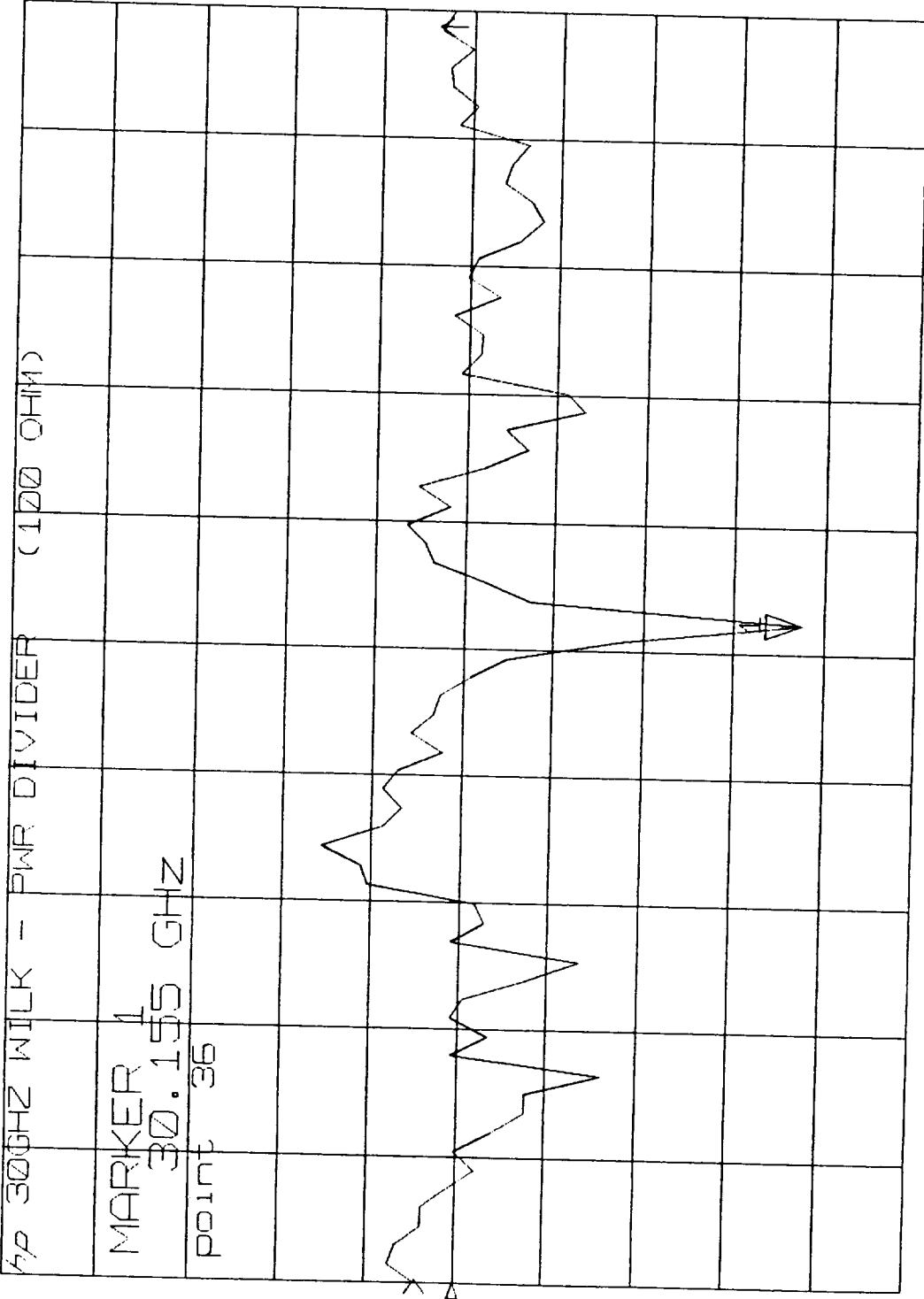
1X

START 25.867500000 GHZ  
STOP 34.075000000 GHZ

14 JAN 92  
19:11:00

log MAG

S11  
REF: -10.0 dB  
1 5.0 dB  
-28.726 dB



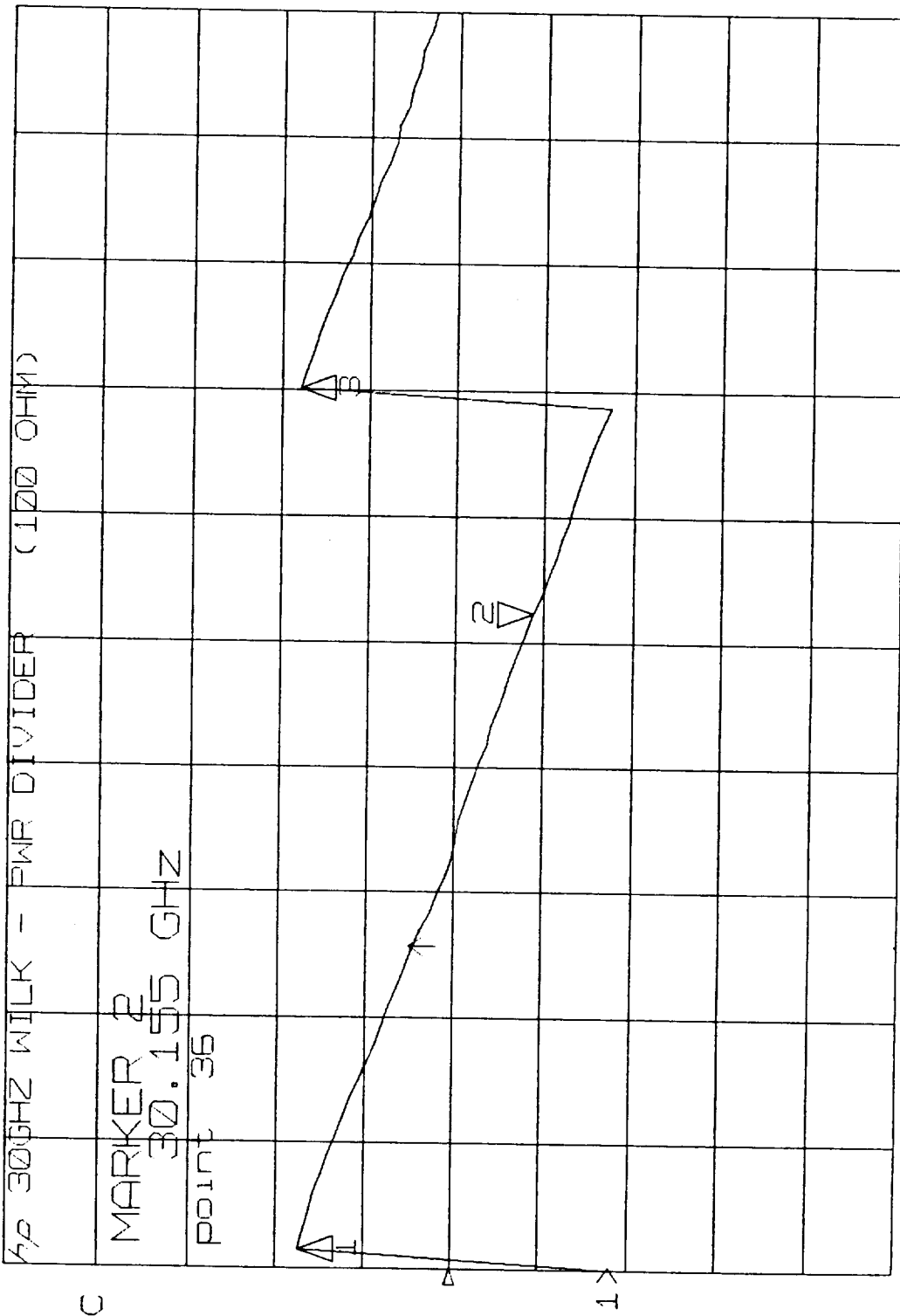
MARKER 1  
30.155 GHZ  
-28.726 dB

START 25.867500000 GHZ  
STOP 34.075000000 GHZ

14 JAN 92  
19:03:26

521 phase

REF 0.0 °  
2 100.0 °  
-88.055 °



MARKER 2  
30.155 GHz  
point 36

MARKER 1  
25.99 GHz  
173.97 °

MARKER 2  
30.155 GHz  
-88.055 °

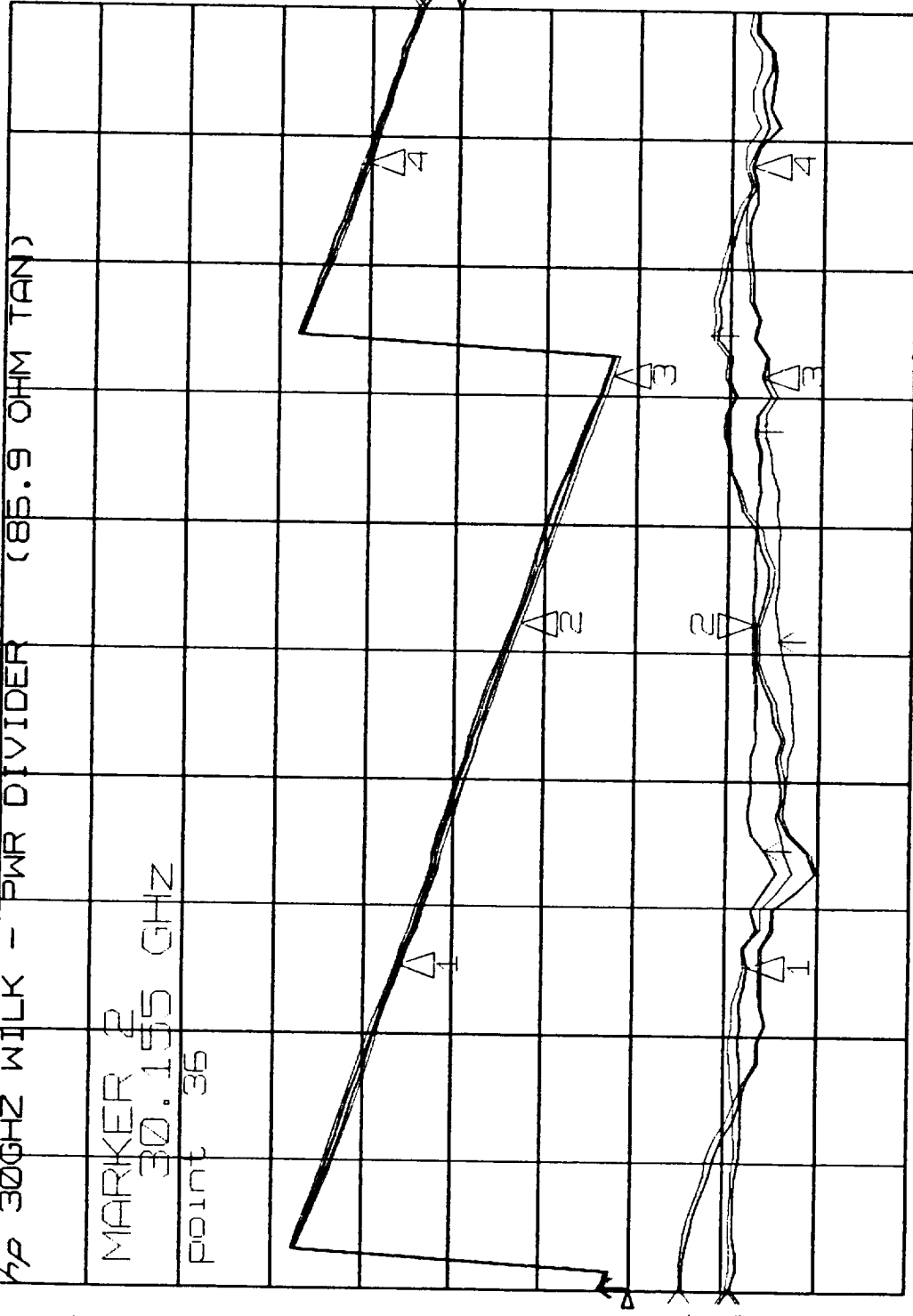
MARKER 3  
31.625 GHz  
179.04 °

START 25.867500000 GHz  
STOP 34.075000000 GHz

14 JAN 92  
19:20:19



▲ S21 & M2    109 MAG    ▲ S21 & M6    phase  
 REF 0.0 dB    REF 0.0 °  
 2    3.0 dB    100.0 %  
 ▽ -3.863 dB    -72.965 °



MARKER 1  
 27.95 GHZ  
 -3.7256 dB  
 MARKER 2  
 30.155 GHZ  
 -3.863 dB  
 MARKER 3  
 31.747 GHZ  
 -3.9948 dB  
 MARKER 4  
 33.095 GHZ  
 -3.6599 dB

START 25.867500000 GHZ  
 STOP 34.075000000 GHZ

20 JAN 92  
 19:27:08

109 MAG

phase

▲ S21 REF 0.0 dB  
3 ▽ 3.0 dB

S21 REF 0.0 °  
3 ▽ 100.0 %  
96.449 °

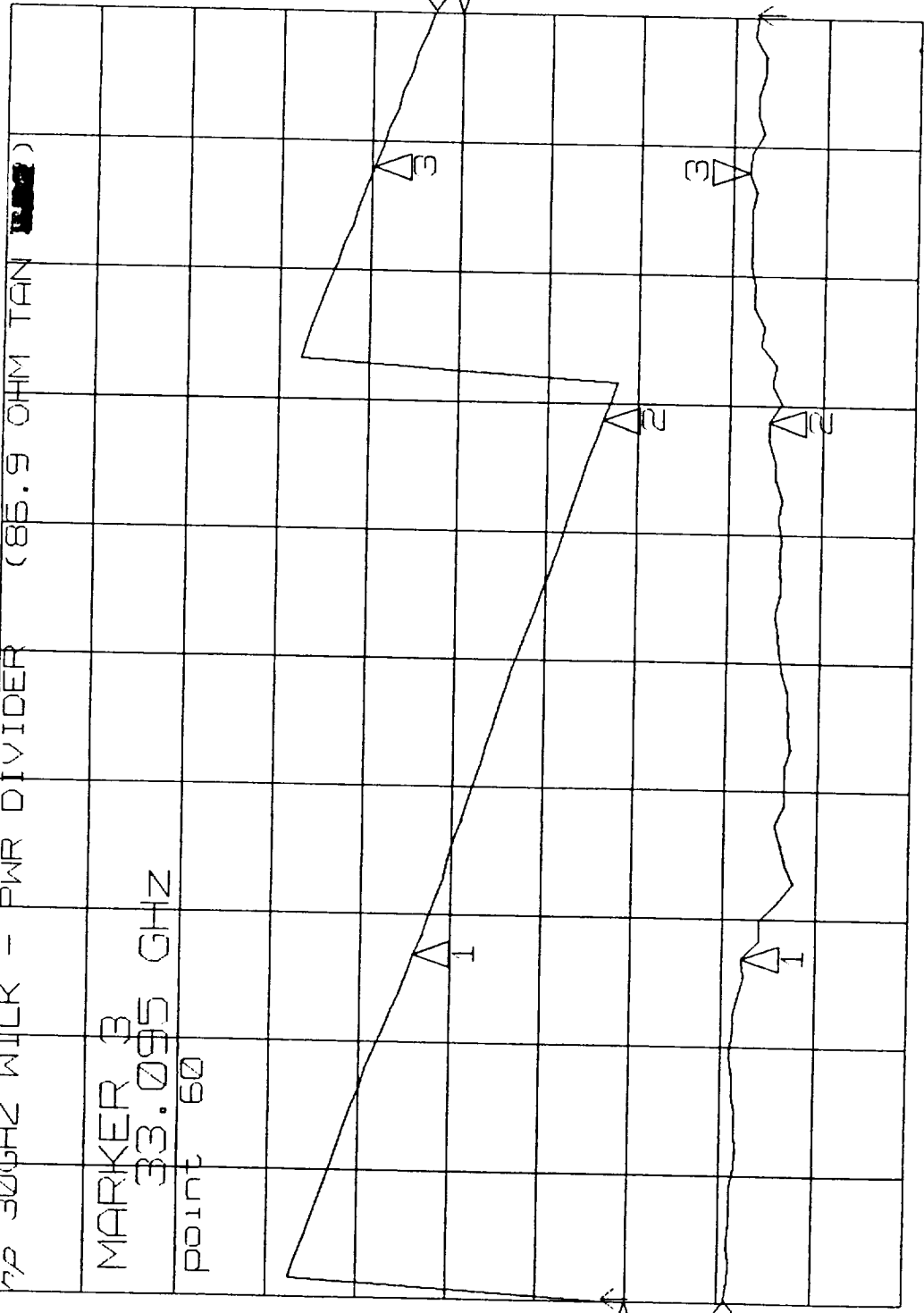
HP 300GHZ WILK - PWR DIVIDER (86.9 OHM TAN 1.22)

MARKER 3  
33.095 GHZ  
point 60

MARKER 1  
28.072 GHZ  
-3.6117 dB

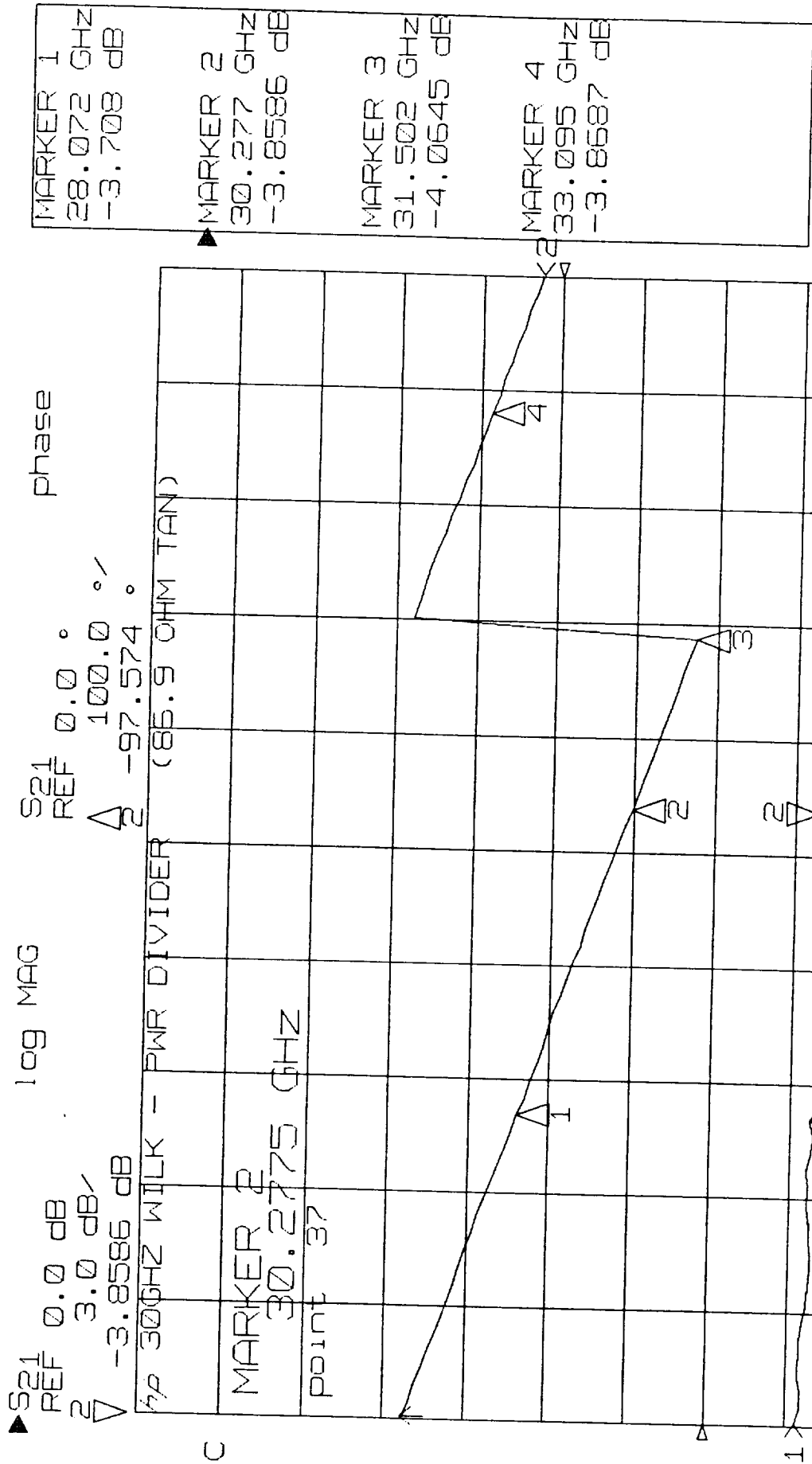
MARKER 2  
31.502 GHZ  
-4.2534 dB

MARKER 3  
33.095 GHZ  
-3.4937 dB



START 25.867500000 GHZ  
STOP 34.075000000 GHZ

15 JAN 92  
16:34:51



START 25.867500000 GHz  
 STOP 34.075000000 GHz

15 JAN 92  
 16:55:14

109 MFG

S11 & M1

REF 0.0 dB

5.0 dB

-21.759 dB

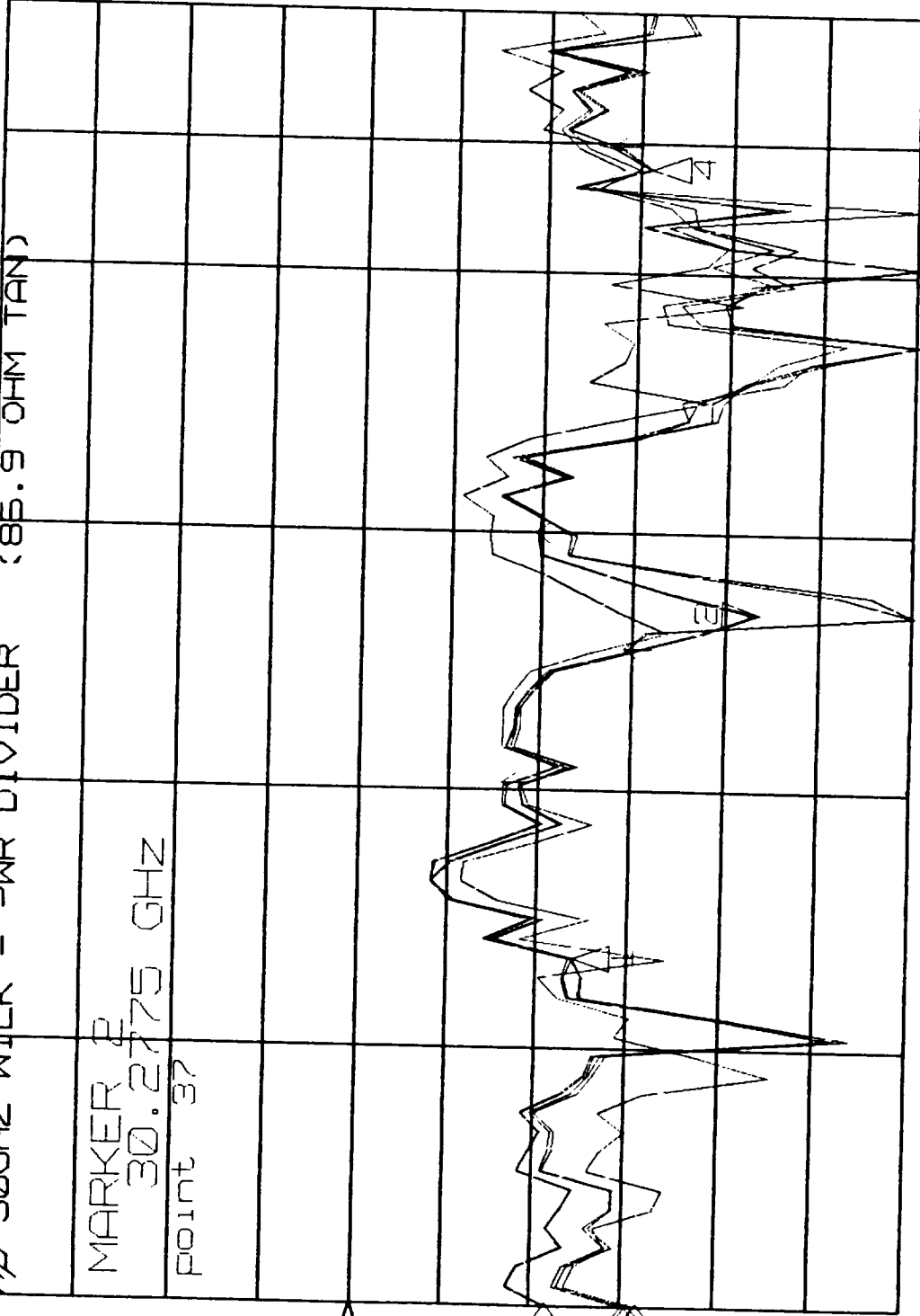
30GHZ WILK - PWR DIVIDER (85.9 OHM TAN)

C

MARKER 2

30.2775 GHZ

point 37



START 25.867500000 GHZ  
STOP 34.075000000 GHZ

MARKER 1  
28.072 GHZ  
-12.05 dB

MARKER 2  
30.277 GHZ  
-21.759 dB

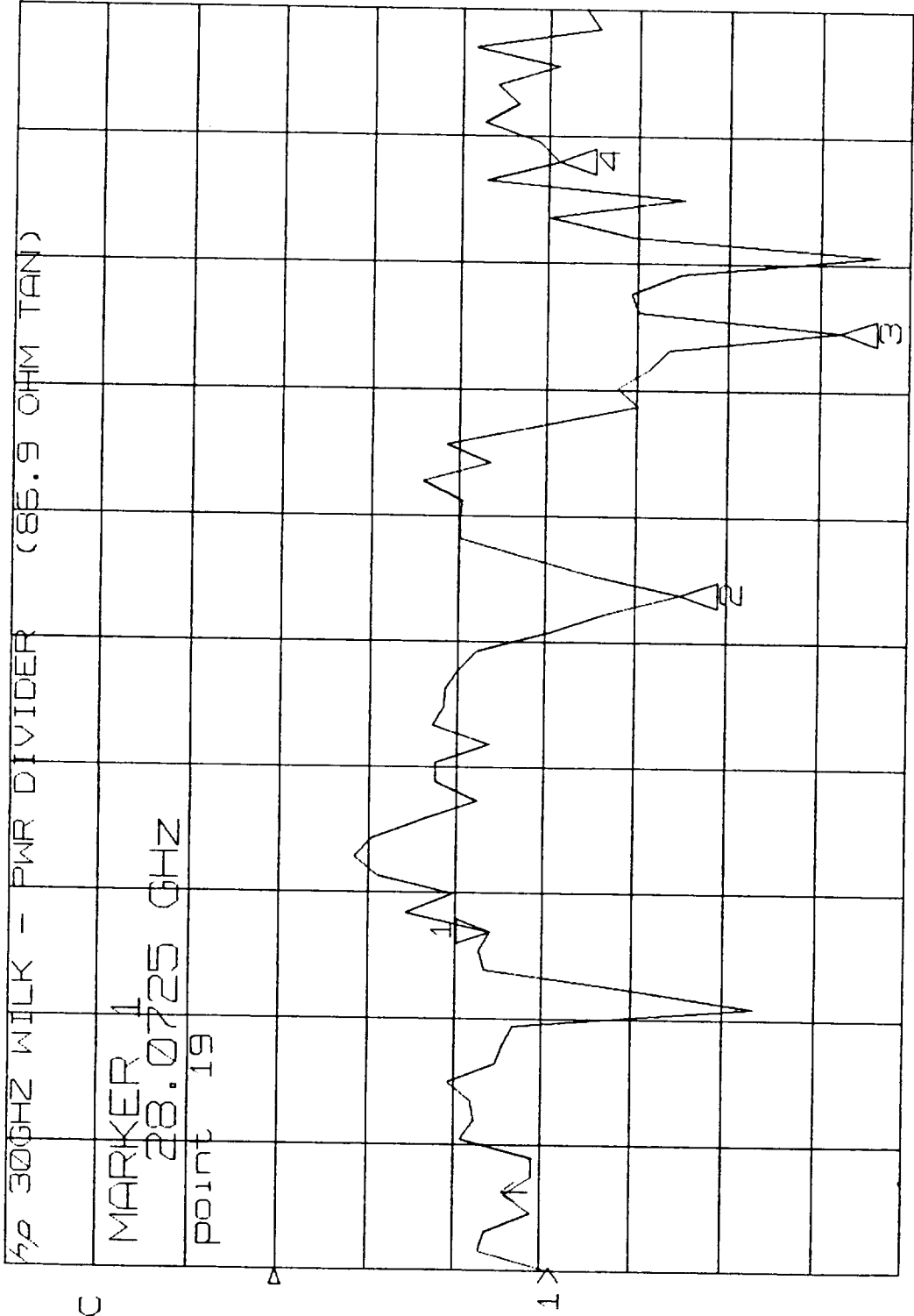
MARKER 3  
31.992 GHZ  
-35.09 dB

MARKER 4  
33.095 GHZ  
-15.594 dB

20 JAN 93  
19:43:05

log MAG

S11  
REF 0.0 dB  
1 5.0 dB  
-12.011 dB



MARKER 1	28.072 GHz	-12.011 dB
MARKER 2	30.277 GHz	-22.477 dB
MARKER 3	31.992 GHz	-31.147 dB
MARKER 4	33.095 GHz	-15.596 dB

START 25.867500000 GHz  
STOP 34.075000000 GHz

15 JAN 92  
16:41:35

▶ S11 1log MAG

REF 0.0 dB

2 10.0 dB

▽ -41.008 dB

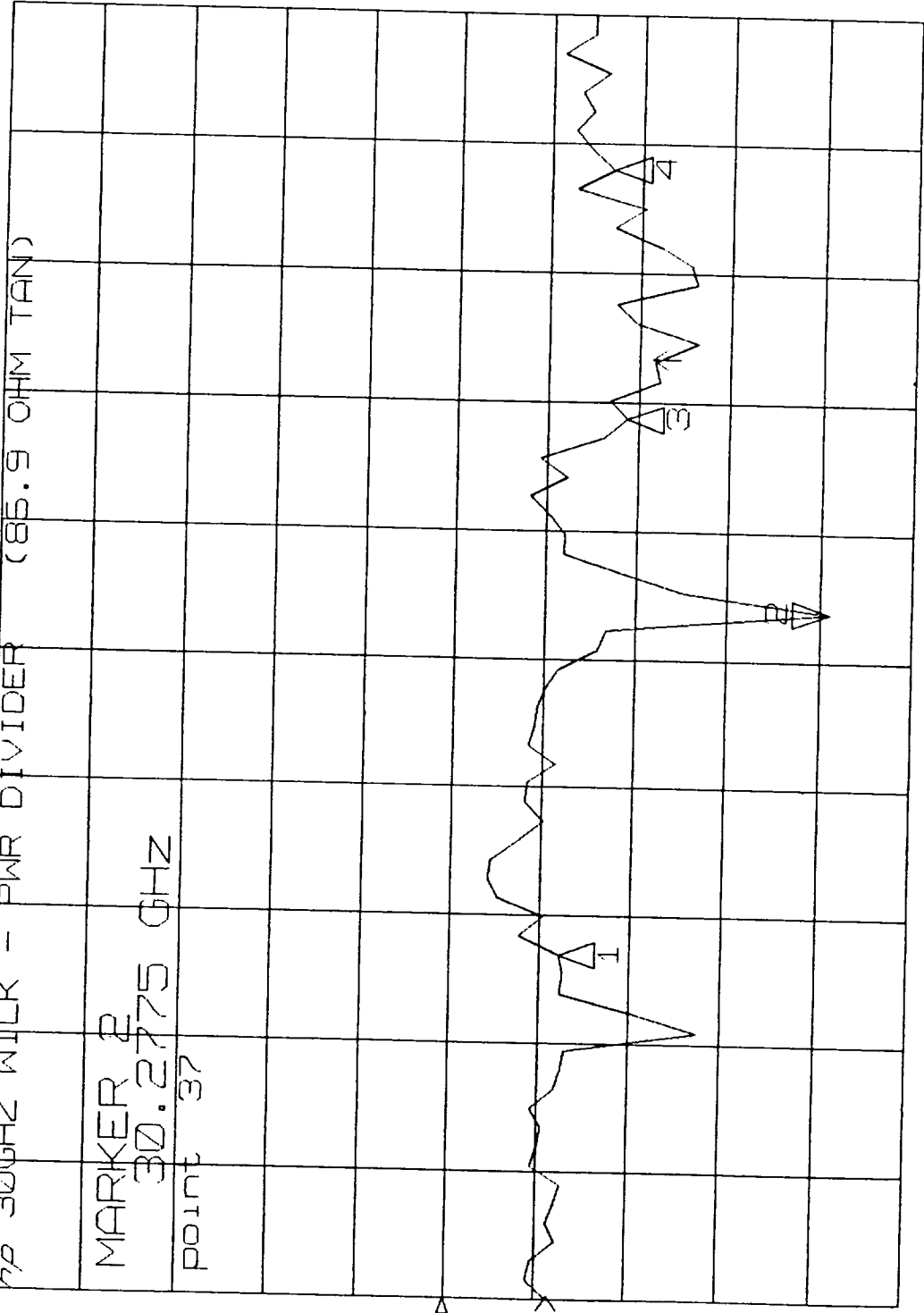
30GHZ WILK - PWR DIVIDER (86.9 OHM TAN)

C

MARKER 2

30.2775 GHZ

point 37



START 25.867500000 GHZ  
STOP 34.075000000 GHZ

MARKER 1  
28.072 GHZ  
-12.161 dB

MARKER 2  
30.277 GHZ  
-41.008 dB

MARKER 3  
31.502 GHZ  
-18.695 dB

MARKER 4  
33.095 GHZ  
-16.93 dB

15 JAN 92  
16:49:49

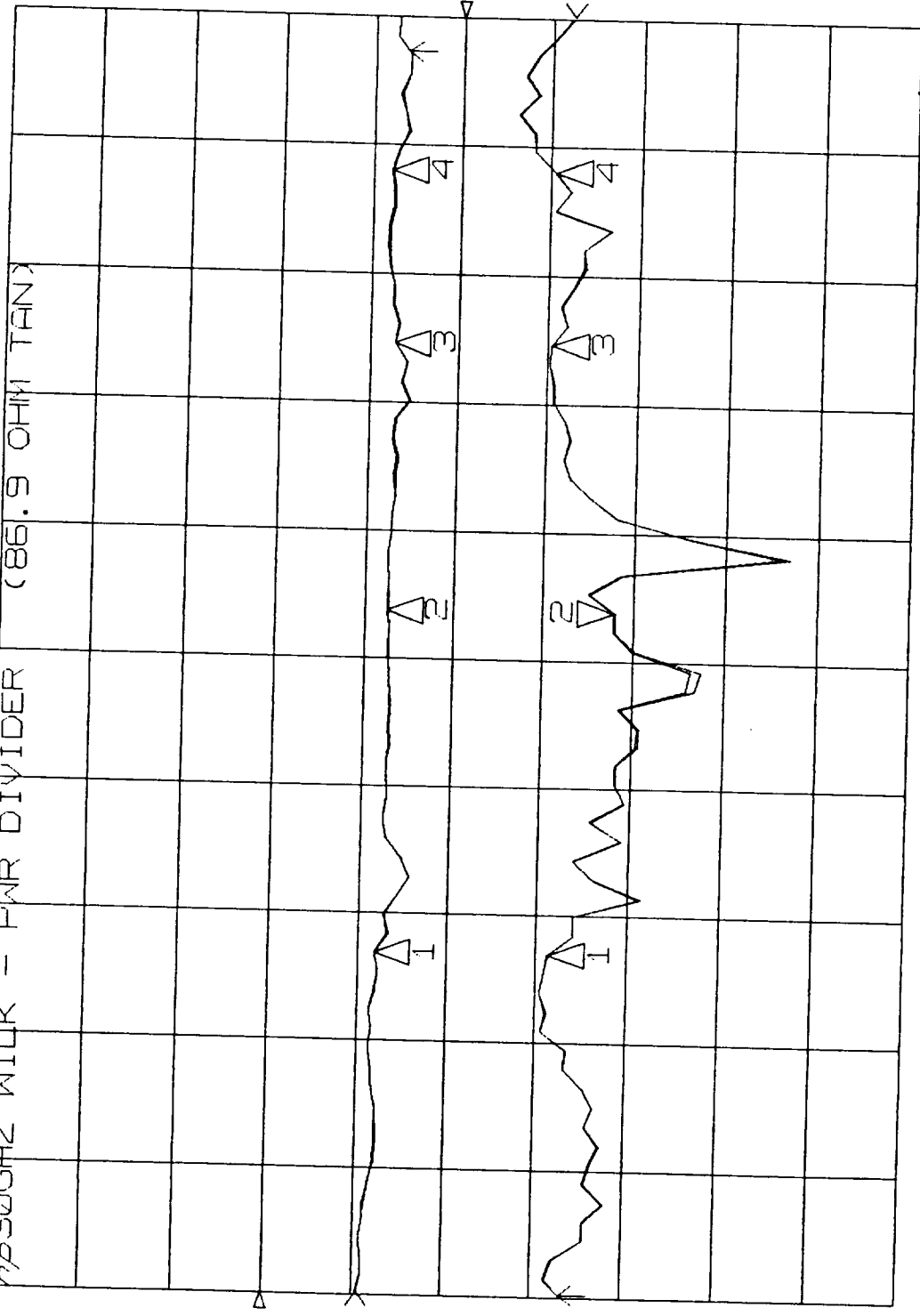
S12 & M3  
 REF 0.0 dB  
 Δ 3.0 dB  
 ▽ -3.7625 dB

log MAG

S22 & M8  
 REF 0.0 dB  
 Δ 10.0 dB  
 ▽ -17.807 dB

log MAG

4p30GHZ WILK - PWR DIVIDER (86.9 OHM TAN)



MARKER 1	28.072 GHz	-11.317 dB
MARKER 2	30.277 GHz	-17.807 dB
MARKER 3	31.992 GHz	-10.466 dB
MARKER 4	33.095 GHz	-10.557 dB

START 25.867500000 GHz  
 STOP 34.075000000 GHz

21 JAN 92  
 20:23:54

▲ S21 phase

REF 0.0 °

2 100.0 %

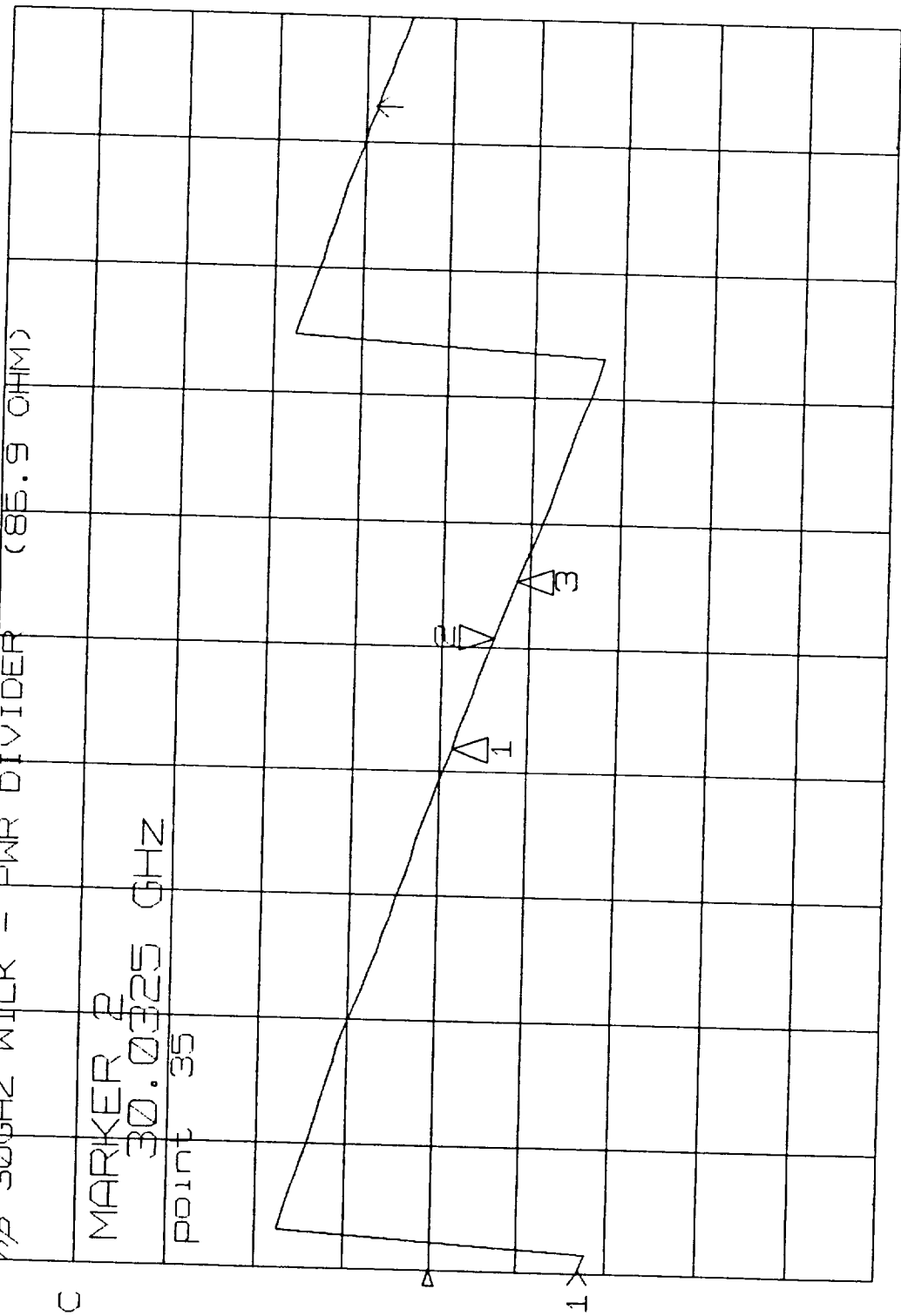
▽ -59.771 °

4P 30GHZ WILK - PWR DIVIDER (85.9 OHM)

MARKER 2

30.0325 GHZ

point 35



MARKER 1  
29.297 GHZ  
-14.743 °

MARKER 2  
30.032 GHZ  
-59.771 °

MARKER 3  
30.4 GHZ  
-84.527 °

START 25.867500000 GHZ  
STOP 34.075000000 GHZ

14 JAN 92  
20:23:26

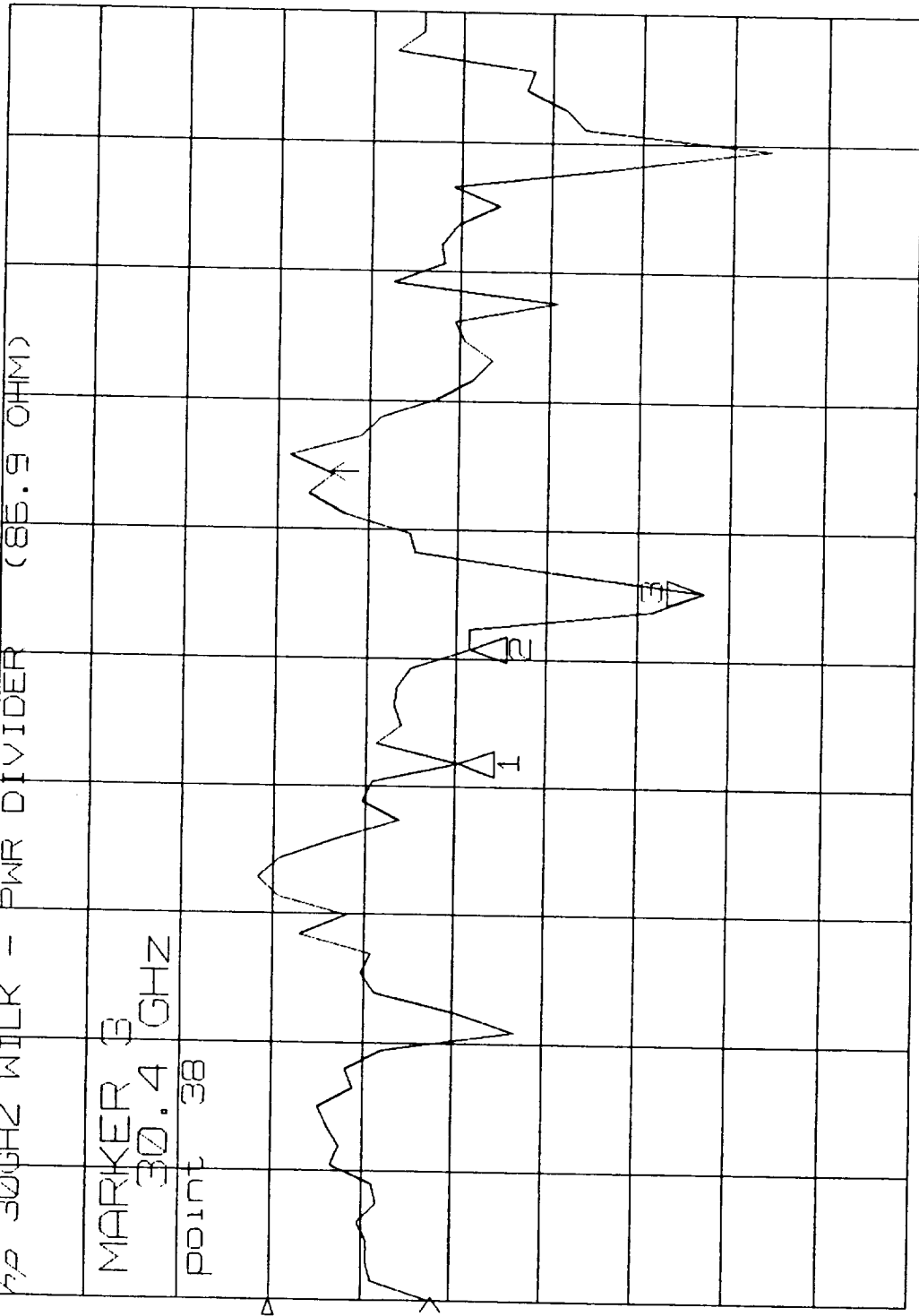


log MAG

S11  
REF -5.0 dB  
3 5.0 dB  
▽ -28.611 dB

HP 300GHZ WILK - PWR DIVIDER (85.9 OHM)

MARKER 3  
30.4 GHZ  
point 38



MARKER 1	29.297 GHz	-15.155 dB
MARKER 2	30.032 GHz	-15.761 dB
MARKER 3	30.4 GHz	-28.611 dB

START 25.867500000 GHz  
STOP 34.075000000 GHz

14 JAN 98  
20:19:11

log MAG

S21

REF 0.0 dB

2 1.0 dB

3 -3.1086 dB

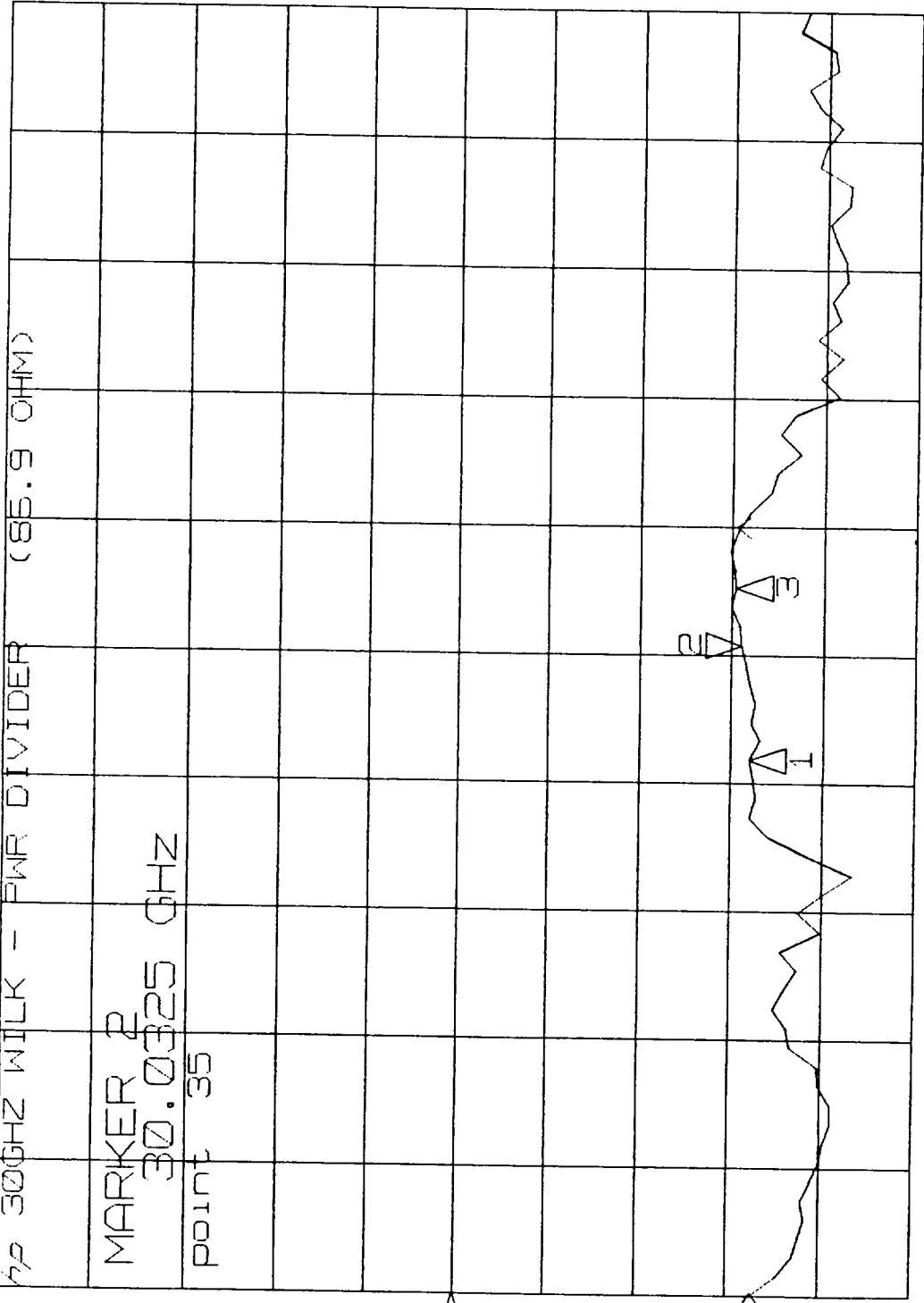
79 30GHZ WILK - PWR DIVIDER (85.9 OHM)

MARKER 2

30.0325 GHZ

point 35

MARKER 1	29.297 GHZ	-3.1998 dB
MARKER 2	30.032 GHZ	-3.1086 dB
MARKER 3	30.4 GHZ	-3.0424 dB



START 25.867500000 GHZ  
 STOP 34.075000000 GHZ

14 JAN 92  
 20:22:05

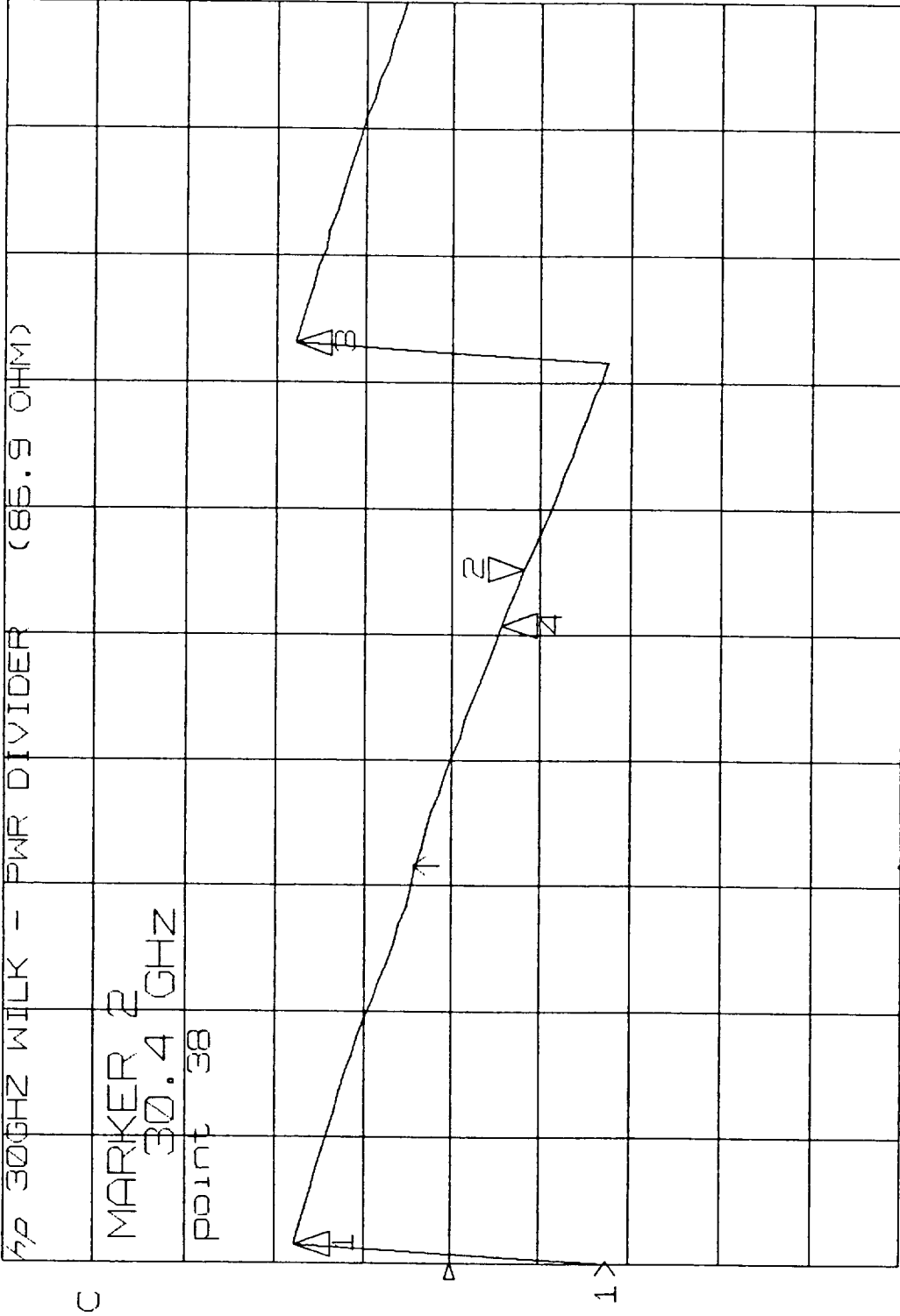
phase

▲ S21  
REF 0.0 °  
2 100.0 %  
▽ -81.828 °

30GHZ WILK - PWR DIVIDER (86.9 OHM)

MARKER 2  
30.4 GHZ

point 38



MARKER 1  
25.99 GHZ  
178.52 °

▲ MARKER 2  
30.4 GHZ  
-81.828 °

MARKER 3  
31.87 GHZ  
178.8 °

MARKER 4  
30.032 GHZ  
-56.477 °

START 25.867500000 GHZ  
STOP 34.075000000 GHZ

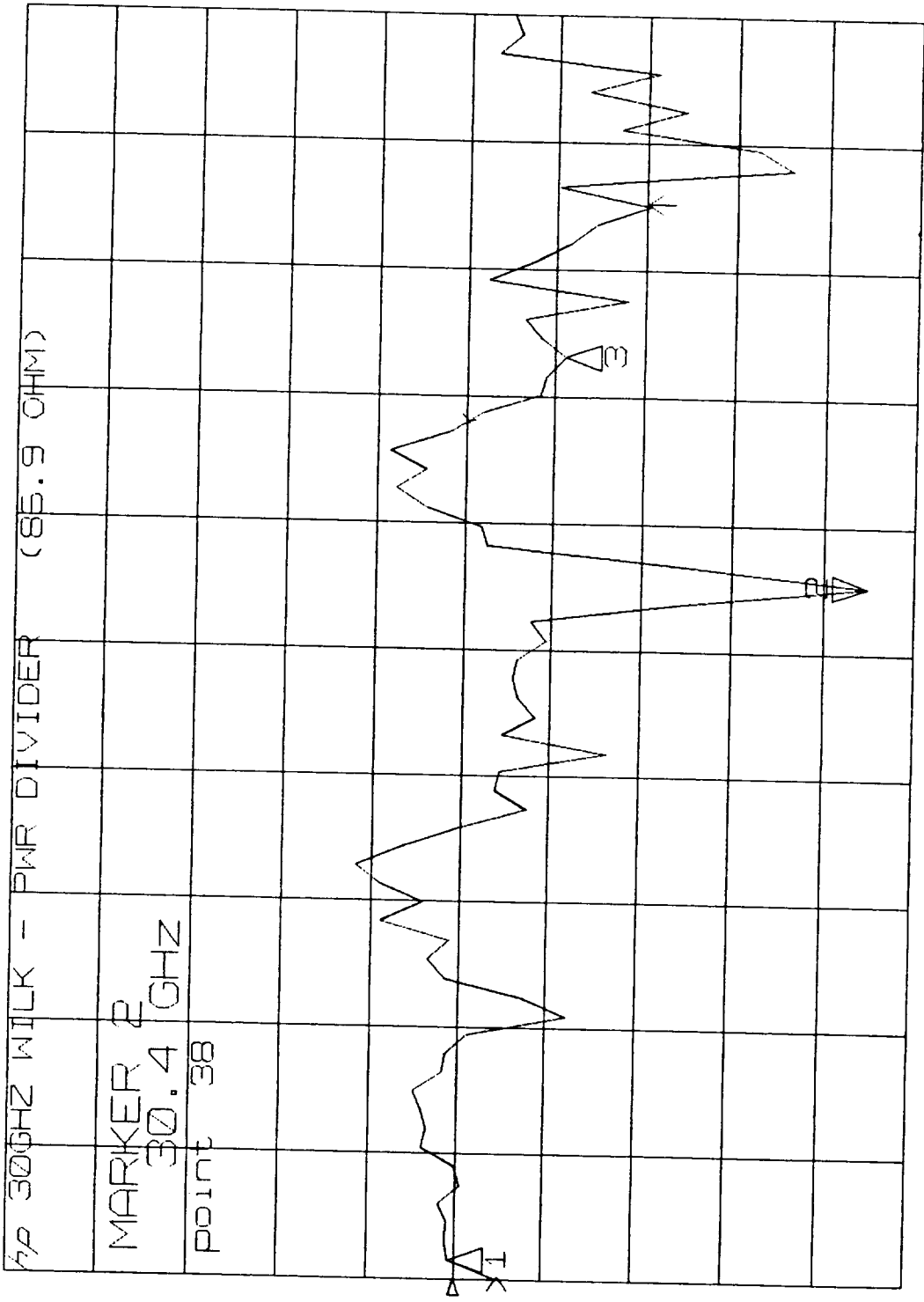
14 JAN 92  
19:48:03

S11 REF -10.0 dB  
 2 5.0 dB  
 ▽ -32.455 dB

MARKER 1  
 25.99 GHz  
 -9.6362 dB

MARKER 2  
 30.4 GHz  
 -32.455 dB

MARKER 3  
 31.87 GHz  
 -15.578 dB



MARKER 2  
 30.4 GHz  
 point 38

START 25.867500000 GHz  
 STOP 34.075000000 GHz

14 JAN 92  
 19:38:31

109 MAG

▶ S21  
REF 0.0 dB  
2 2.0 dB  
▽ -7.5972 dB

30.4 GHz WILK - PWR DIVIDER (85.9 OHM)

MARKER 2  
30.4 GHz  
point 38

2

1

3

START 25.867500000 GHz  
STOP 34.075000000 GHz

MARKER 1  
25.99 GHz  
-8.6709 dB

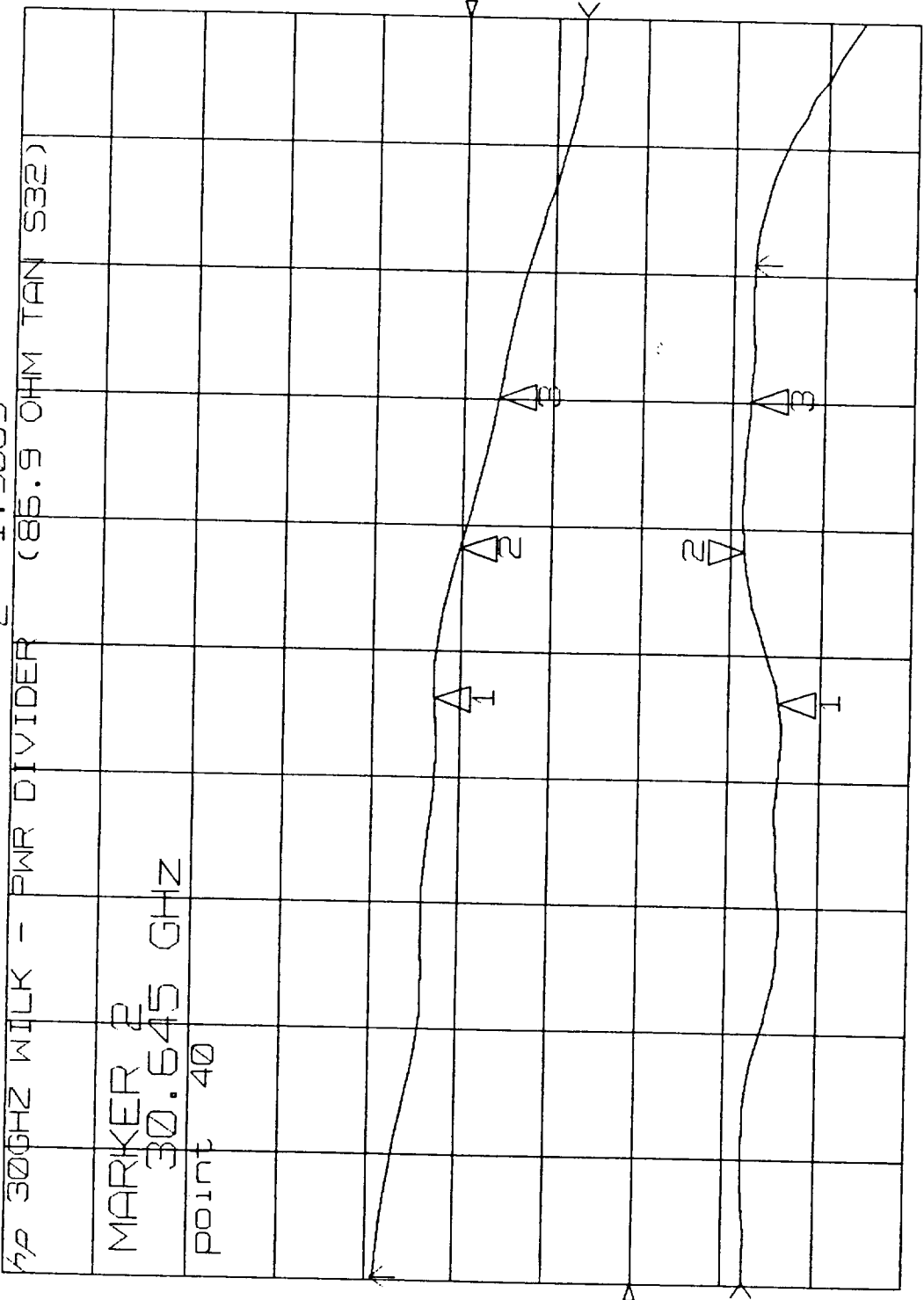
MARKER 2  
30.4 GHz  
-7.5972 dB

MARKER 3  
31.87 GHz  
-9.3418 dB

14 JAN 92  
19:43:27

▲ S21 REF 0.0 dB  
 2 ▽ 10.0 dB  
 ▽ -11.45 dB  
 log MAG  
 S21 REF 0.0 °  
 2 ▲ 100.0 °  
 ▽ 1.9089 °  
 phase

PWR DIVIDER (85.9 OHM TAN S32)  
 MARKER 2  
 30.645 GHZ  
 point 40  
 MARKER 1  
 29.665 GHZ  
 -15.493 dB  
 MARKER 2  
 30.645 GHZ  
 -11.45 dB  
 MARKER 3  
 31.625 GHZ  
 -11.988 dB



START 25.867500000 GHZ  
 STOP 34.075000000 GHZ

15 JAN 92  
 16:10:56

**APPENDIX C**

**1/3 and 1/4 Wavelength Power Divider Results**

## INTRODUCTION

This section of the report will discuss the design, analysis, and measurement of the Wilkinson power divider incorporated into the T/R module. Included will be the reasoning for the design, the assumptions made in order to optimize, and the comparison to the actual devices.

## DISCUSSION

The Wilkinson power divider was an obvious choice for balanced distribution of power from a single source to a set of 4 phase shifters. The Wilkinson, by theory, would evenly split the source power into 2 equal half power source units. This can be accomplished if the source transmission line and two split transmission lines maintain the characteristic impedance of the source, namely 50 ohms. The power of each branch would be ideally 50% of that of the input source. A simple resistive network determines that a delta resistance across the branches of 100 ohms would result in maximum transfer of power with zero reflective loss.

The modeling of the power divider was performed using the Touchstone simulator from EEsof (Appendix A). Once the concept was proven from the ideal case, the models were transferred from electrical to physical parameters. This meant including line length, and both conductor and dielectric losses. Another analysis was performed across the frequency band of interest, and the design of the power divider was optimized. The analysis resulted in differences from fundamental theory in that the physical length of divider branches was not  $1/4$  wavelength (the theoretical optimum) and the branch resistor was not 100 ohms. Experiments were set up to measure both the theoretical and the analytical designs.

There were two type of thin film on  $\text{SiO}_2$  Wilkinson power dividers fabricated and tested. The first was a 100 ohm NiCr resistor,  $1/4$  wavelength substrate. The second was a 86.9 ohm TaN resistor,  $1/3$  wavelength substrate. Both designs used a thin film gold conductor and thin film resistors.

## RESULTS

The measurement results of the two different power divider designs are included (Appendix B). It was determined that the modified design of the  $1/3$  wavelength TaN power divider performed better across the frequency band. This design was then incorporated into the final T/R module.

A complete module was assembled with microstrip feedthrus ribbon bonded into the cavities reserved for the phase shifters. The RF ports were configured to facilitate microwave coplanar probing.



Based on a previous MMIC package design, the probe pitch was 400 microns. Three of the four output ports were terminated with high frequency 50 ohm chip resistors connected by wirebonds. The package was measured at each of the ports to determine the effectiveness of the Wilkinson power divider. The return loss node was in an acceptable frequency range, but the insertion loss through the two sets of power dividers was excessively high relative to theory. Since the power was transferring through two different power dividers, there should be a 6 dB difference between the input and output ports. The measured results show a drop of approximately 11 dB across the frequency band.

## ISSUES AND CONCERNS

Since the concept, design and fabrication of the Wilkinson power divider were transferred through many people, some of the information needed to produce an optimal module may have been lost. What was learned about the design of the power divider from the measured versus modeling exercise, was that, based on materials, process, frequency, and testing methodology, there was some discrepancy. More understanding of the process and materials needs to be attained to produce an accurate model used to predict an actual results. The difference between theoretical and actual insertion loss of the module was so dramatic that a number of questions need to be answered in order to determine where important information was left out. For example: a) was the value of resistance changed when processing the module, b) was the probing technique and calibration adequate to measure the module, c) was the  $1/3$  wavelength TaN design really optimal, d) were the microstrip insert, bonding, and terminations reasonable?

## RESULTS AND CONCLUSIONS

The results of designing, fabricating, and testing a 30 GHz Wilkinson Power Divider for integration into a multi-element phased array application indicate that there is the potential to use a power divider approach for efficiency and densification within a T/R module. From the information available about materials and processes, it was determined that the theoretical  $1/4$  wavelength, 100 ohm resistor power divider network may not be optimal at 30 GHz.

More work needs to be performed in a follow-on manner to fabricate variations of the power divider design, using different materials and measurement techniques. This will result in identifying the potential deteriorating effects caused by the physical and material boundaries used in power divider development. Initial results from a small database indicate potential success of incorporating a Wilkinson Power Divider into a 30 GHz T/R module.