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N94-21347

A LOW COST ALTERNATIVE TO HIGH PERFORMANCE PCM BIT SYNCHRONIZERS

Bruce DeShong
AlliedSignal Technical Services Corporation, ATSC
Data Systems Group, DXG
Design and Development Section, DDS
Columbia, Maryland 21045

SUMMARY

The Code Converter/Clock Regenerator (CCCR) provides a low-cost alternative to high-performance Pulse Code Modulation (PCM) bit synchronizers in environments with a large Signal-to-Noise Ratio (SNR). In many applications, the CCCR can be used in place of PCM bit synchronizers at about one fifth the cost. The CCCR operates at rates from 10 bps to 2.5 Mbps and performs PCM code conversion and clock regeneration. The CCCR has been integrated into a stand-alone system configurable from one to six channels and has also been designed for use in VMEbus compatible systems.

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ABSTRACT

The Code Converter/Clock Regenerator (CCCR) provides a low-cost alternative to high-performance Pulse Code Modulation (PCM) bit synchronizers in environments with a large Signal-to-Noise Ratio (SNR). In many applications, the CCCR can be used in place of PCM bit synchronizers at about one fifth the cost. The CCCR operates at rates from 10 bps to 2.5 Mbps and performs PCM code conversion and clock regeneration. The CCCR has been integrated into a stand-alone system configurable from one to six channels and has also been designed for use in VMEbus compatible systems. This paper compares the functions and performance of the CCCR to those of the higher-cost PCM bit synchronizers and describes typical applications of each device as well as the use of the CCCR to reduce system costs at the Merritt Island (MIL) Tracking Station.

1. BACKGROUND

The primary functions of the CCCR and PCM bit synchronizer are identical; however, each device has been designed to operate in different environments. To provide a clearer identification of the differences between these units, some background information is presented on their basic functions.

Pulse Code Modulation

Applicability. This discussion of PCM is limited to the encoding scheme as it applies to standardized binary/digital symbol based systems.

PCM. The CCCR and PCM bit synchronizer perform functions in support of the serial transmission of digital data. *Pulse Code Modulation* (PCM) is a method commonly employed in this form of data communication. For the purpose of understanding PCM, consider a simple communication system consisting of a data source and a data receiver connected via a single conductor, as shown in Figure 1.

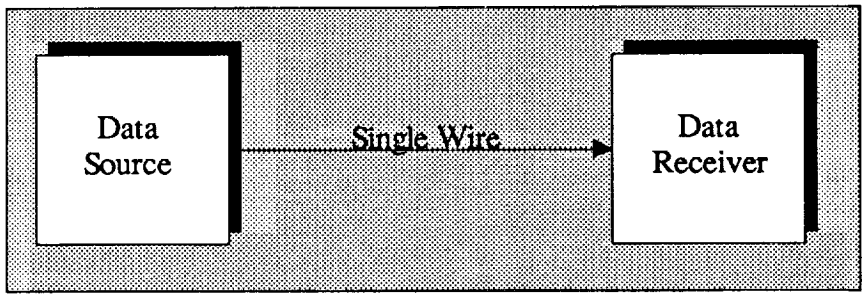

Figure 1. Communications System

For a binary system, PCM defines a set of simple rules governing the transmission of digital data (i.e., a logical "one" or logical "zero") from the source to the receiver by varying the potential on the wire over a period of time referred to as the *bit period.*

Although there are a number of different standardized binary PCM coding schemes, all are based on two simple characteristics of the signal being transmitted: voltage levels and voltage transitions. Assume that the potential in the wire can only assume one of two discrete voltages (V_1,V_2) at any time. In addition, if you were to view the signal over the entire bit period, changes in the signal voltage level occur only at the beginning and/or center point of the bit period. The voltage level and voltage transitions from one level to another represent the logical data value being transmitted.

PCM. For example, two binary PCM codes that are most frequently used in serial communications are Non Return-to-Zero-Level (NRZ-L) and Biphase-Level (BiΦ-L).

NRZ-L. The simplest PCM format is NRZ-L. NRZ-L PCM specifies that when the transmitted signal has a voltage of V_1, a logical "one" is being transmitted and when the signal has a voltage of V_2, a logical "zero" is being transmitted. Figure 2 shows the relationship of the digital data being transmitted versus the corresponding PCM signal.

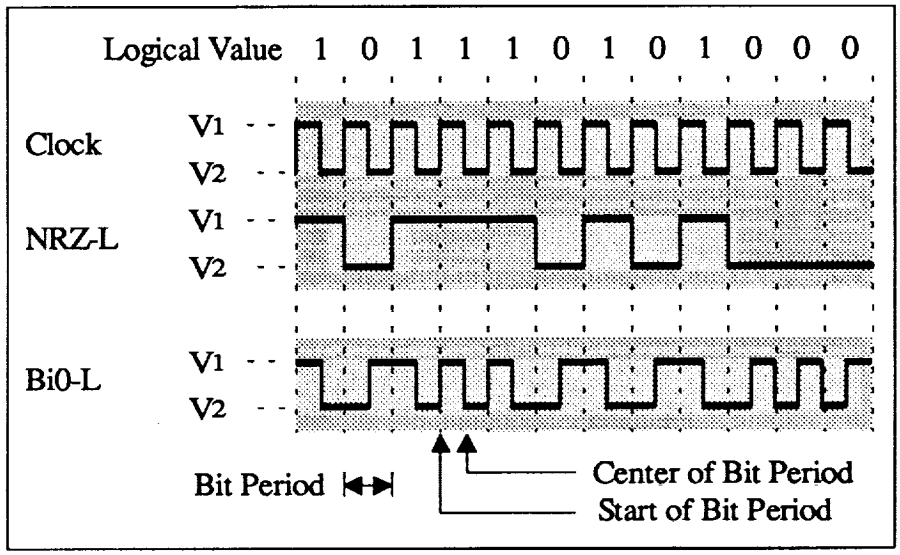

Figure 2. Examples of NRZ-L and BiΦ-L PCM Codes

NRZ-L and Clock. One of the deficiencies of NRZ-L is that during transmission of a long sequence of all "zeros" or all "ones", the signal's transition density becomes low causing errors at the data receiver. These errors are due to timing variations between the data source and the data receiver. In this case, the data receiver is not able to identify the bit period boundaries due to the non-transitions within the transmitted signal, thus causing bit errors. To eliminate this problem in using NRZ-L, most digital equipment requires that a synchronous clock signal also be transmitted with the data signal. The clock and NRZ-L data signal relationship is also shown in Figure 2.

BiΦ-L. BiΦ-L is another popular PCM format because it eliminates the need for transmitting a clock signal with the data signal as in the case of NRZ-L. BiΦ-L accomplishes this by combining the timing and data information into one signal. The bit period is divided into the start of the bit period and the center-bit period. A transition must always occur at the center-bit period location in the signal. These transitions are used

by the receiver equipment to extract or recover the synchronous clock from the PCM signal. The logical data value being transmitted is also represented during the center-bit period transition. A transition from V_1 to V_2 indicates a logical-one value and a transition from V_2 to V_1 indicates a logical-zero value.

PCM Code Conversion and Clock Regeneration

Much of the equipment used by the Ground Network (GN) accept only serial data in NRZ-L format with a synchronous clock signal provided; however, in some applications, the use of BiΦ-L format has several advantages over NRZ-L. For example, since BiΦ-L does not require an associated clock signal, the complexity of data switching systems is greatly reduced. In addition, BiΦ-L eliminates the problem of data errors that can be caused by clock and data skew arising from the data and clock signal being transmitted across paths of different lengths.

In systems that use both NRZ-L with clock and BiΦ-L, special interface devices are required to marry the PCM signals and receiver equipment (refer to Figure 3). These interface devices need to have the capability of accepting data in either NRZ-L or BiΦ-L and providing a PCM code conversion to the alternative PCM format. This function is referred to as *PCM code conversion*. The devices must also be capable of extracting the clock information and producing a synchronous clock signal with the converted NRZ-L data for the receiver equipment. This function is referred to as *clock regeneration* or *clock recovery*. The CCCR and PCM bit synchronizer are two of these interface devices capable of both PCM code conversion and clock regeneration.

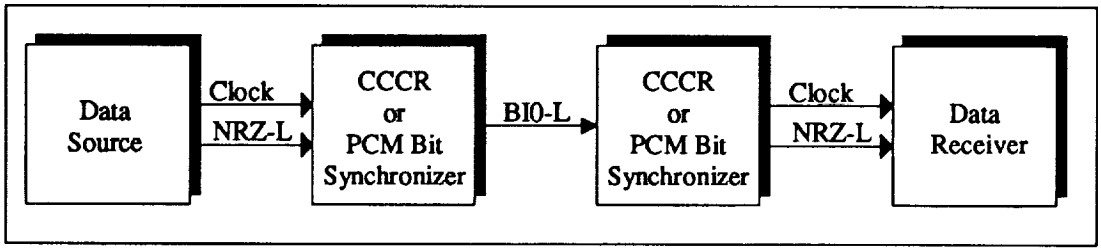

Figure 3. Example of PCM Code Conversion and Clock Regeneration

2. CCCR SYSTEM

General Description

The CCCR was designed and developed for the National Aeronautics and Space Administration (NASA) by AlliedSignal Technical Services Corporation (ATSC). The CCCR was designed and developed under the Bit Synchronizer Reduction (BSR) project for MIL. The BSR project and its applicability is detailed in Section 4. The CCCR consists of a 19-inch-wide by 10.5-inch-high by 23-inch-deep chassis housing two redundant power supplies and one to six CCCR Printed Circuit Boards (PCB). Local operation is performed through a front panel keyboard and fluorescent display. Figure 4 provides an illustration of the CCCR.

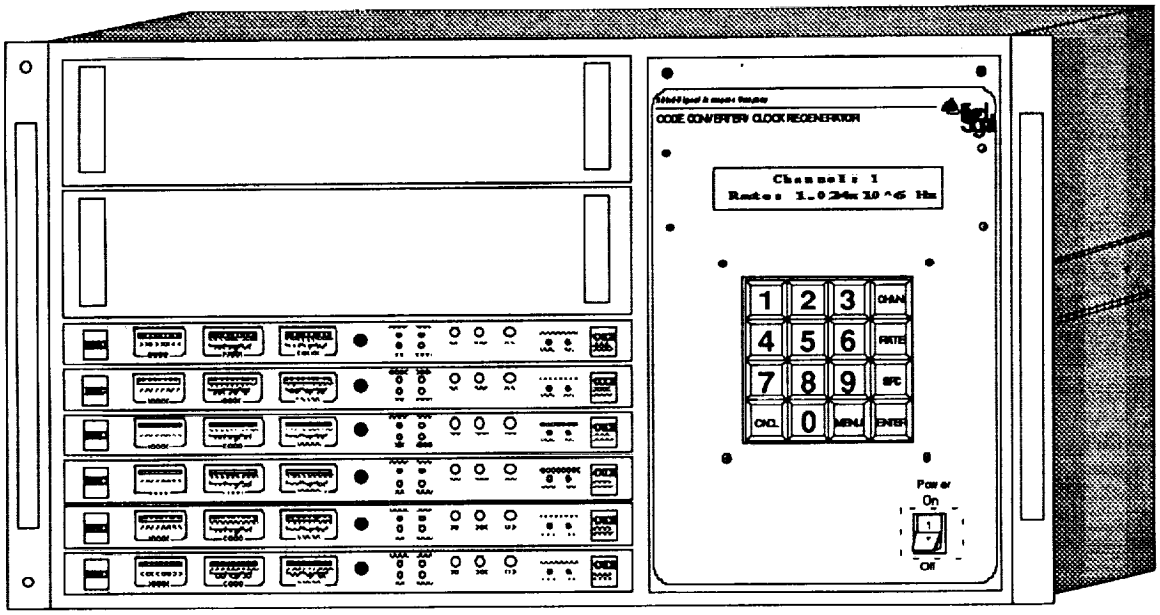

Figure 4. Code Converter/Clock Regenerator

Functional Capabilities

The following summarizes the capabilities of the CCCR:

Multiple-Channel. The CCCR system is configurable from one to six independent channels of PCM code conversion and clock regeneration.

Code Conversion and Clock Regeneration. Each CCCR channel is capable of accepting and performing PCM code conversion and clock regeneration on any of the following PCM codes: NRZ-L,M,S; BiΦ-L,M,S; and Delay Modulation (DM)-M,S.

Source Input. Each CCCR channel is capable of accepting eight independent data sources and performing source selection.

Input Characteristics. The CCCR is configured to accept input signals with either Unipolar (TTL) or Bipolar (1 Vpp to 10 Vpp) voltage levels.

Dedicated NRZ-L and Clock Output. The CCCR provides a dedicated output signal pair consisting of the NRZ-L representation of the input data with a synchronous clock.

PCM Coded Output and Clock. A PCM coded output is provided for each CCCR channel and can be configured for any of the following PCM formats: NRZ-L,M,S, BiΦ-L,M,S and DM-M,S. A synchronous clock associated with this output is also provided.

Fault Tolerance. Fault tolerance is provided by the use of redundant power supplies and in-line fuses on the power lines of each CCCR PCB.

Remote Operation. Remote configuration and monitoring is provided by a separate parallel data port for each CCCR channel.

VMEbus Compatibility. The CCCR PCBs have been designed such that they may also be used as a slave device in a VMEbus system.

Design Overview

The intent of the CCCR design is to provide the code conversion and clock regeneration capability at a low cost for environments in which signal conditioning is not required. Additionally, the intended application required the CCCR to provide a programmable data rate, thus the CCCR is capable of supporting data rates from 10 bps to 2.5 Mbps. Most low cost commercial code converter/clock recovery units can only be configured for one or several fixed rates.

Code Conversion and Clock Regeneration. The CCCR implements a simple algorithm for the code conversion and clock regeneration function. The algorithm only requires two Integrated Circuits (IC): a Numerically Controlled Oscillator (NCO) and a Electrically Programmable Logic Device (EPLD). A block diagram of this circuitry is shown in Figure 5.

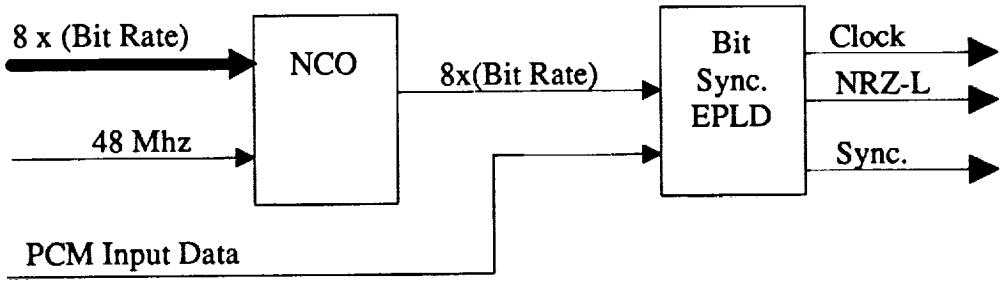

Figure 5. Code Conversion/Clock Regenerator Circuit Block Diagram

The NCO is loaded with a phase-value which is used with the input reference clock of 48 MHz to generate a precise frequency of 8 times the expected PCM bit rate. The 8 times clock is used by the EPLD to perform the actual code conversion and clock regeneration of the signal. The EPLD also produces a status signal indicating the synchronization (Sync.) status of the device to the incoming signal. A detailed block diagram of the Bit Sync. EPLD logic is shown in Figure 6.

For the eight PCM codes that are accepted by the CCCR (NRZ-L,M,S; BiΦ-L,M,S and DM-M,S), three pieces of information must be accumulated by the EPLD logic on the incoming PCM signal in order to identify the logical data values. Transitions in the signal need to be identified along with the direction of the transition (i.e. High-to-Low or Low-to-High). In addition, the Bit Synchronizer EPLD must correctly identify the beginning and center of the bit period based on the signal voltage transitions and the associated rules for the PCM format being accepted.

The algorithm used in the bit synchronizer EPLD is based on an eight times sampling of the signal over the bit period. Depending on the PCM code being received, the clock Generator is able to divide the eight times clock into a clock consistent with the bit period

of the data. The Clock Generator also synchronizes the clock to the incoming signal based on transitions in the data signal and the specified PCM characteristics.

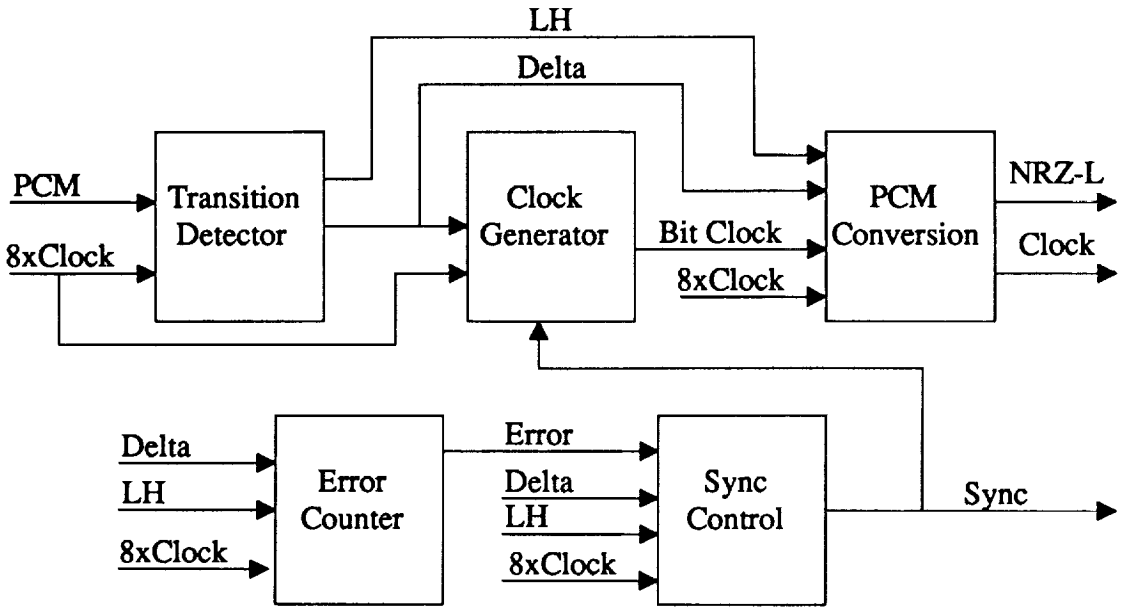

Figure 6. Functional Diagram of the Bit Synchronizer EPLD Logic

Using the generated clock, transition information and input PCM format the PCM Conversion functional block determines the logical data value associated with the input signal. Based on the rules for the selected PCM format being accepted, the Sync Control block indicates a lock on the incoming signal as long as the input PCM signal does not violate these rules. Each violation of the PCM rules, is registered by the Error Counter. If the Error Counter reaches its maximum value, an error signal is generated causing the Sync Control logic to indicate a loss of lock on the incoming PCM signal. Figure 7 provides a timing diagram for the internal bit synchronizer EPLD for an input in BiΦ-L format.

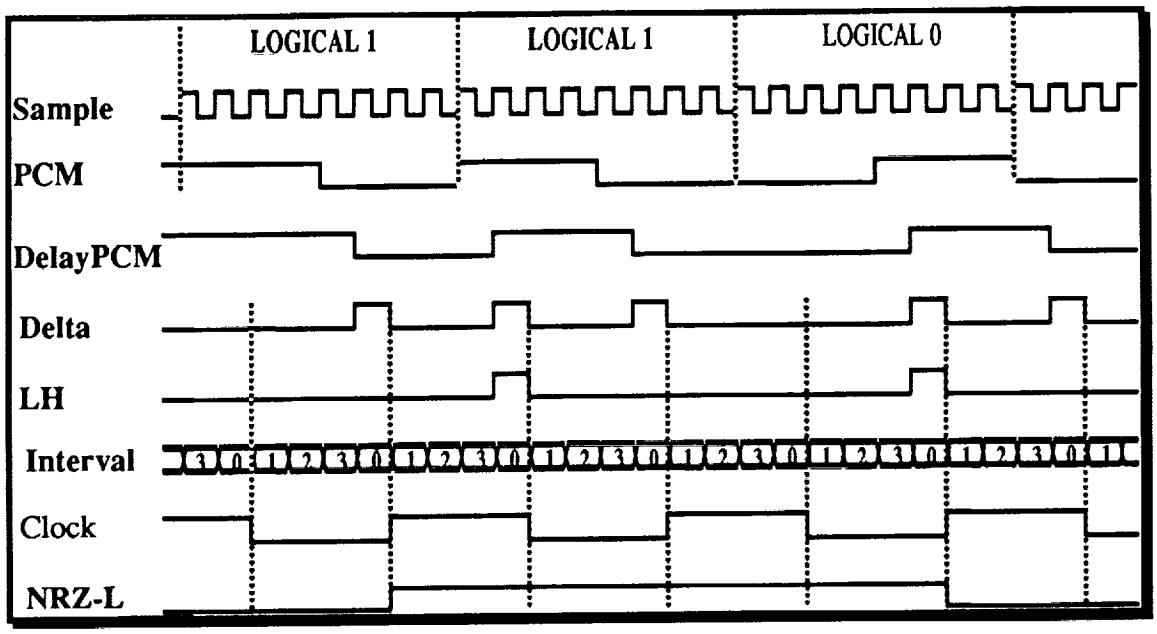

Figure 7. Bit Sync. EPLD Timing Diagram

This sampling method is a simple algorithm for determining the logical value of the input PCM signal; however, the output from the Bit Sync EPLD will contain jitter on the clock and NRZ-L data of up to one quarter of the bit period due to the sampling. To reduce the jitter on the output of the CCCR, the NRZ-L data is clocked into a data buffer prior to output. The data is then clocked out of the data buffer using a reduced rate clock from the NCO.

Since the clock used to shift data in and out of the buffer may vary slightly in frequency, a rate-adjust algorithm is implemented to prevent exceeding the storage capacities of the buffer, resulting in a loss of data. An embedded controller on the CCCR is used to calculate the approximate incoming data rate based on the clock generated in the Bit Sync EPLD. The following equation is used to determine this rate:

Calculated Rate = Counter Value/Sample Time

where *Sample Time* = 1/[(Desired Precision)*(Configured Bit Rate)].

The NCO is then adjusted either slightly above or slightly below the calculated rate (taking into account the error of the calculation: Error = 2/[Sample Time]) based on a half-full signal generated by the data buffer.

In order to prevent excessive delays due to the buffering of data, a size programmable buffer was designed. The buffering is accomplished using two First-In-First-Out (FIFO) IC's and a buffer controller EPLD. A 64x8 bit FIFO is used for lower data rates. The buffer controller EPLD is capable of varying the data width into and out of the FIFO from 1 to 8 bits based on the input rate. For higher data rates, a 512x8 bit FIFO is used. Again the buffer controller is configured to operate at a word width from 1 to 8 bits. The embedded controller calculates the size of the buffering required and sets up the buffer controller based on the configured data rate. The buffer size required is calculated as follows:

Buffer Size = Configured Bit Rate/[(FIFO Width)/(Maximum Allowable Delay)].

Figure 8 shows a diagram of the variable size buffer as implemented on the CCCR.

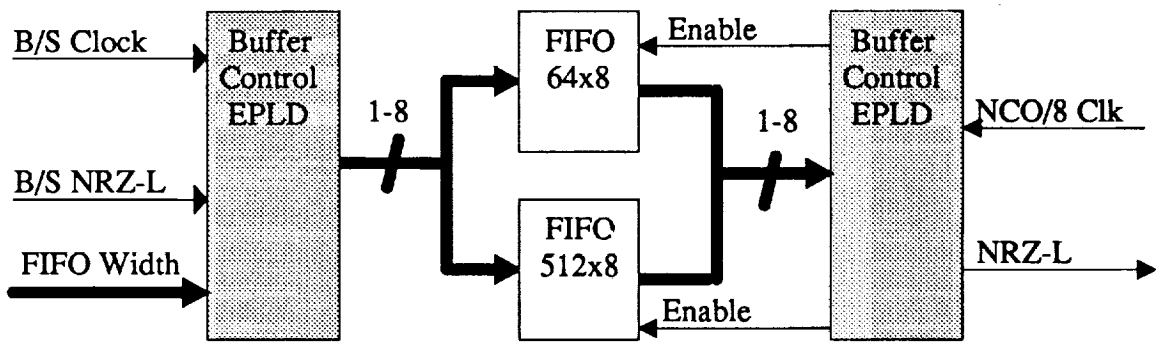

Figure 8. Variable Buffer Diagram

Finally, the NRZ-L data from the buffer is converted to one of the eight possible PCM formats by a code converter EPLD. The general rules used to generate the PCM data are described in Table 2. The entire design supporting all eight PCM codes is implemented in 12 ICs.

Table 2. PCM Format Definitions

PCM Format	Definition
NRZ-L	"One" is represented by V_1. "Zero" is represented by V_2.
NRZ-M	"One" is represented by a change in level. "Zero" is represented by no change in level.
NRZ-S	"One" is represented by no change in level. "Zero" is represented by a change in level.
BiΦ-L	*Level change occurs at center of every bit period.* "One" is represented by a transition from V_1 to V_2. "Zero" is represented by a transition from V_2 to V_1.
BiΦ-M	*Level change occurs at beginning of every bit period.* "One" is represented by a center bit period transition. "Zero" is represented by no center bit period transition.
BiΦ-S	*Level change occurs at beginning of every bit period.* "One" is represented by no center bit period transition. "Zero" is represented by a center bit period transition.
DM-M	"One" is represented by a level change at the center bit period. "Zero" followed by a "zero" is represented by a level change at the end of the first "Zero" bit. No level change occurs when a "zero" is preceded by a "one".
DM-S	"Zero" is represented by a level change at the center bit period. "One" followed by a "one" is represented by a level change at the end of the first "one" bit. No level change occurs when a "one" is preceded by a "zero".

3. CCCR VERSUS PCM BIT SYNCHRONIZERS

Although the CCCR and PCM bit synchronizer perform the identical functions of PCM code conversion and clock regeneration, the devices are not interchangeable in all applications. The CCCR was designed specifically to provide a low-cost PCM code converter and clock regenerator unit that operates from 10 bps to 2.5 Mbps. The CCCR is also intended to be used in environments where noise considerations are negligible and signal voltage levels are deterministic.

PCM bit synchronizers have the additional capability of filtering, Automatic Gain Control (AGC), and direct current (dc) offset adjustments for noisy environments were signal characteristics may vary. In applications where cost is a major consideration and the added features of the PCM bit synchronizer are not required, the CCCR provides a low-cost alternative to the high-cost PCM bit synchronizer. Table 1 provides a comparison between features of the CCCR and PCM bit synchronizer.

Table 1. Summary of CCCR vs. PCM Bit Synchronizer Functions and Cost

Function	CCCR	PCM Bit Synchronizer
Filtering (Noise)	No	Yes
Input Amplitude	1 Vpp to 10 Vpp	.25 Vpp to 15 Vpp
Maximum dc Offset (based on a zero volt center)	40%	100%
Automatic Gain Control	No	Yes
PCM Code Conversion	Yes	Yes
Clock Recovery	Yes	Yes
Sync with External Clock	1 bit	< 1000 bits
Max. Input Sources	8	1-6
Remote Configuration	Yes	Yes
Bit Delay	Variable	Fixed
Per Channel Cost	**$2,400**	**$5,000 - $12,000**

The following sections provide examples highlighting those applications best suited for the CCCR and those applications where the full features of a PCM bit synchronizer are required.

An Application Using PCM Bit Synchronizers

PCM bit synchronizers are extensively used at tracking stations and serve as interface devices between the RF equipment and data processing equipment. Figure 9 provides a simplified block diagram of this process. RF modulated spacecraft data is down-linked to the ground station where the receiver/demodulator RF equipment extract the serial PCM data stream. PCM bit synchronizers are then used to perform the PCM code conversion to NRZ-L format and the clock recovery function required for the data-processing equipment. It is common for the output from the receivers/demodulators to contain some undesirable signal characteristics such as noise, dc offset, varying amplitude and wave form rounding. Because of these signal characteristics, high performance PCM bit synchronizers with filtering, dc offset adjustment, AGC, and wave squaring are required for *signal conditioning*.

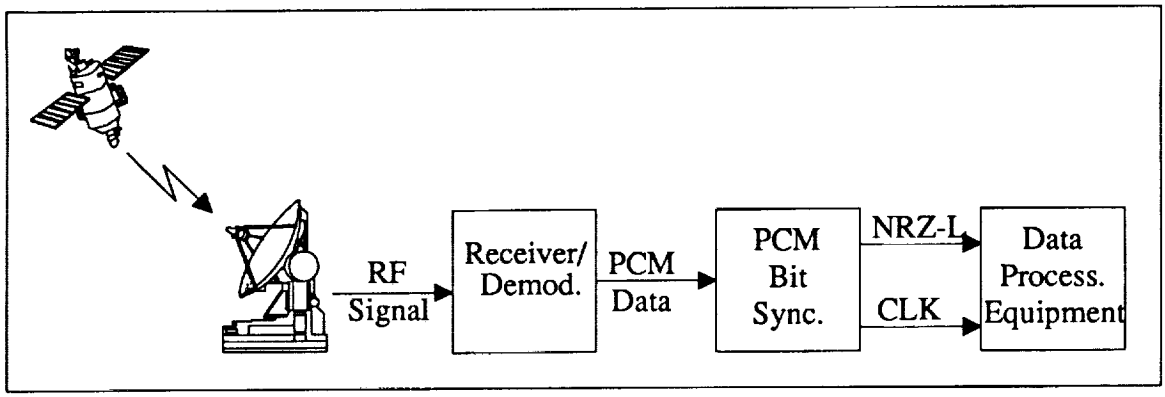

Figure 9. An Application of PCM Bit Synchronizers

An Application Using The CCCR

Figure 10 provides a detailed diagram of the tracking station example described in the previous section (Figure 9). The use of the high performance PCM bit synchronizer is the same as in the previous application; however, in this example, a switching system has been added along with a variety of data sources and data sinks. BiΦ-L is used for routing the signal throughout the tracking station since the transfer of data only requires one signal for this code (refer to background section). The data-processing equipment require input in NRZ-L with a synchronous clock, so a single channel of the CCCR is provided for each input to the data equipment.

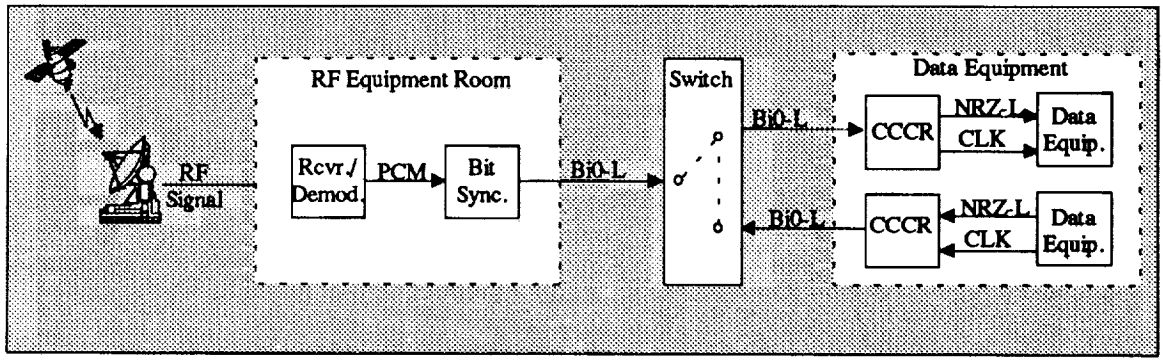

Figure 10. Application of the CCCR

Although high cost PCM bit synchronizers could be used for the code conversion and clock regeneration performed by the CCCR, in this example, this would have been expensive and unnecessary. Signal conditioning has been performed by the PCM bit synchronizers located in the RF equipment room and the distributed BiΦ-L signal has a fixed voltage level (TTL or Bipolar) with minimal variations. This application is best suited for the lower cost CCCR units.

4. BIT SYNCHRONIZER REDUCTION PROJECT

The CCCR was designed and developed under the Bit Synchronizer Reduction (BSR) project for the Merritt Island Tracking Station (MIL). A total of 48 PCM bit synchronizers are used at MIL, configured as shown in Figure 11.

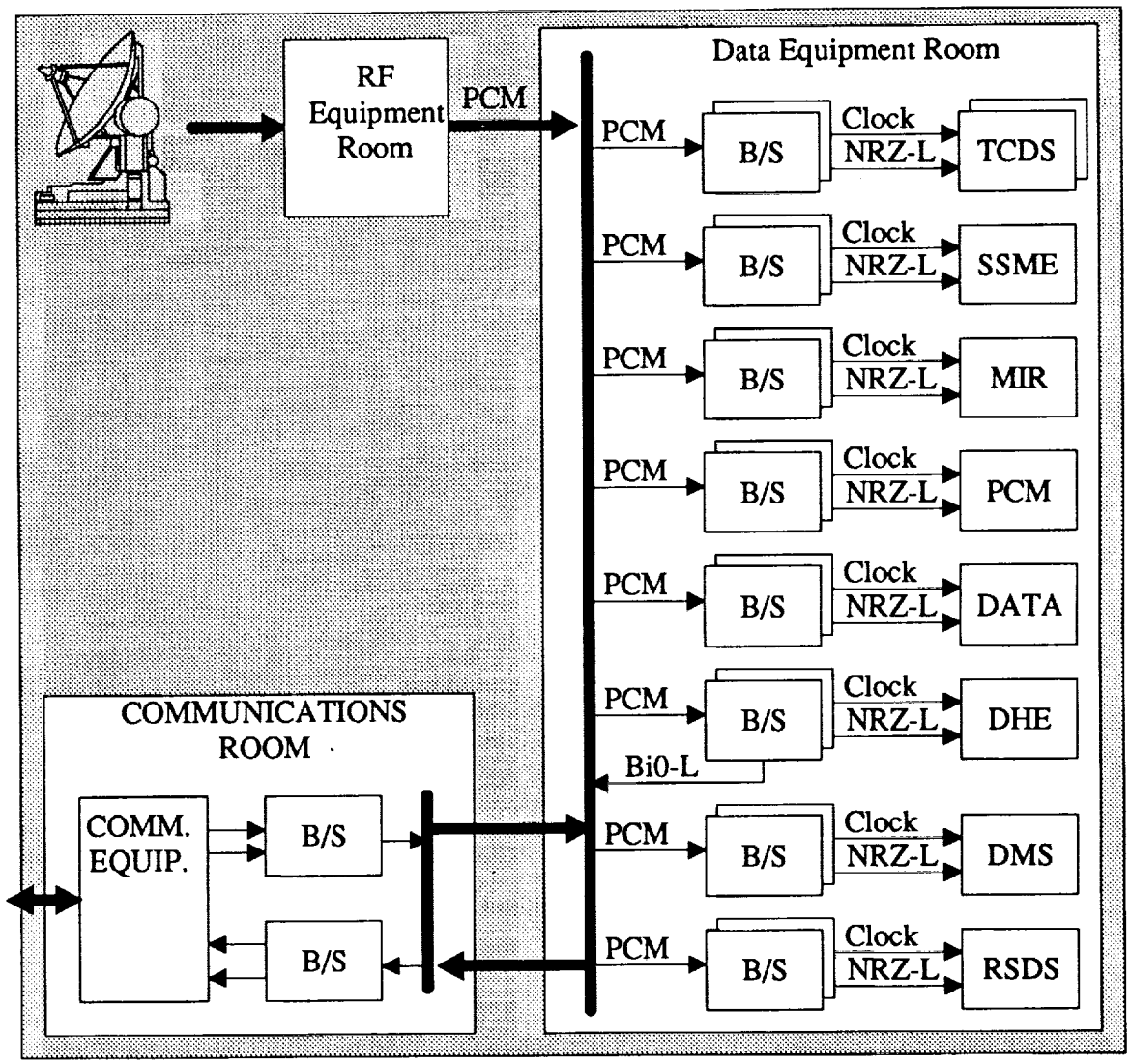

Figure 11. MIL PCM Bit Synchronizer Configuration Before (BSR)

In this application, the high performance PCM bit synchronizers are not located within the RF system, but are distributed within the data processing system. Every input to each of the data systems shown uses a high-performance PCM bit synchronizer for signal conditioning and PCM code conversion of the signals from the RF equipment room. Two models of PCM bit synchronizers are used in this system: an earlier series with lower performance (37 units) and a newer digital model with higher performance capability (11 units).

The increasing age and obsolescence of the older model PCM bit synchronizer is resulting in an increased cost in sustaining these units. A considerable cost savings would be achieved by reducing the maintenance required for the PCM bit synchronizers. The most direct method of reducing the maintenance cost is to replace all the older PCM bit synchronizers with newer, low maintenance PCM bit synchronizers. This approach was determined to be too costly based on current commercial prices.

Instead of replacement, an alternate approach to reduce the number of PCM bit synchronizers was selected for MIL. In this approach, the newer model PCM bit synchronizer will be used to accept and perform signal conditioning on the signals from the RF Equipment Room. The output from these high performance PCM bit synchronizers would then be distributed to the other data equipment. The many channels of code conversion required for the data equipment will to be performed by lower cost CCCR systems developed specifically for this application. Figure 12 shows the MIL configuration using the CCCR systems.

Using the CCCR units, all 37 of the older PCM bit synchronizers will be eliminated. The remaining 11 higher performance PCM bit synchronizers will be combined with 7 similar spare units to provide the initial processing of the PCM data originating from the RF Equipment Room (refer to Figure 12). Nine CCCR units will be delivered for use as PCM code converters and clock regenerators for the remaining data processing equipment.

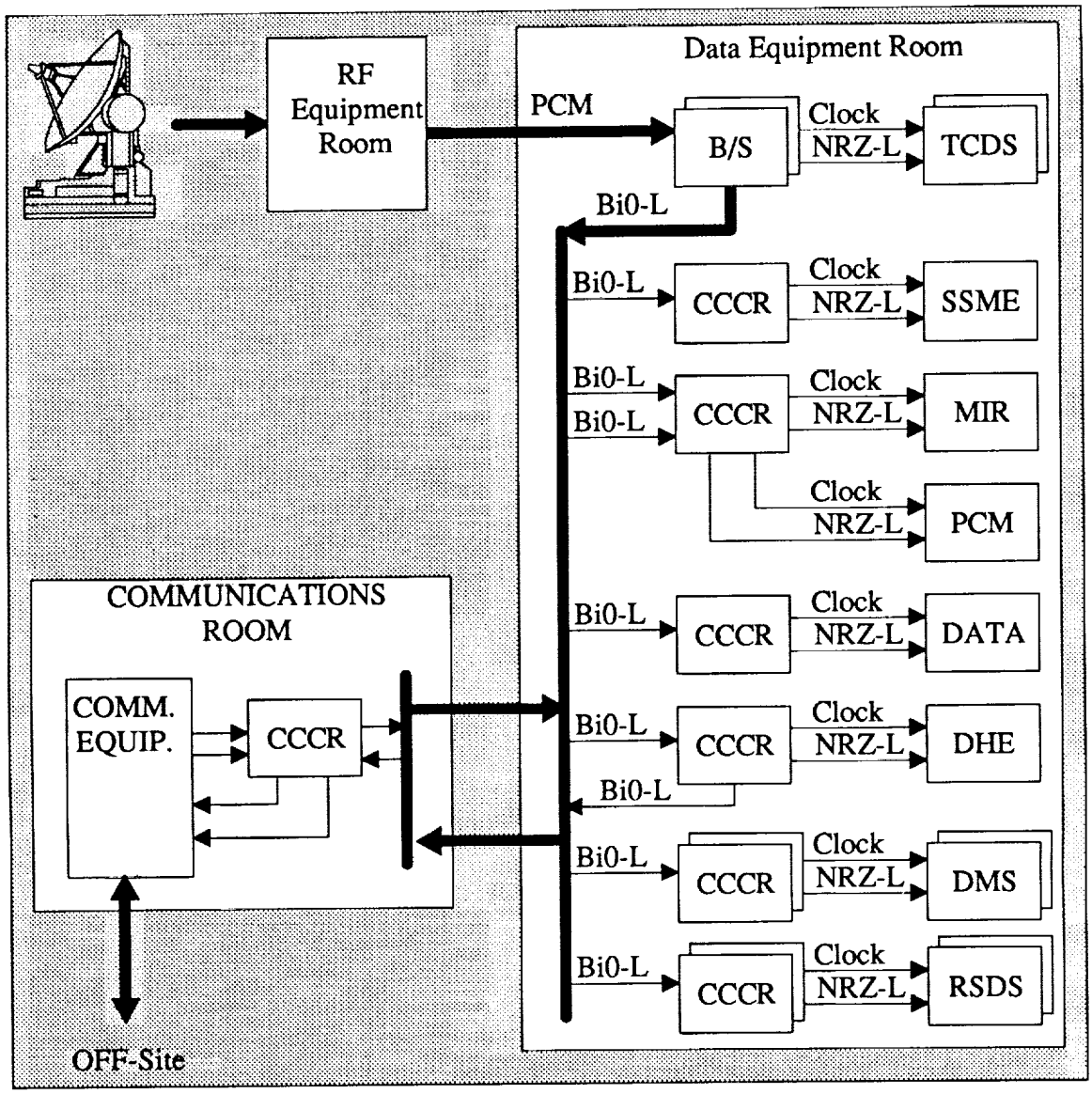

Figure 12. MIL Configuration Using CCCR Systems

5. SUMMARY

The low cost benefits of the CCCR are exemplified by the application of the units at MIL. It is estimated that approximately $56,000 a year is being expended in maintenance at MIL on the older PCM bit synchronizers. By implementing the reduction using CCCR units as described in Section 4, a cost savings of $150,000 to $350,000 is achieved over estimated replacement cost of $250,000 to $450,000. In addition, since the CCCR requires essentially no adjustments, the maintenance cost for MIL is reduced by approximately $56,000 per year. The CCCR units are expected to be used until the MIL system is completely redesigned in approximately four years, which results in a total savings from maintenance of $224,000.

Another benefit resulting from the implementation of the CCCR units is that an overall performance increase in the system was obtained. The maximum bit rate supported by the older PCM bit synchronizers was 1.2 Mbps. With the use of the CCCR units at MIL, the overall maximum bit rate is 2.5 Mbps, an increase of over 50 percent.

6. CONCLUSION

The CCCR is a low-cost PCM Code Converter/Clock Regenerator that has been specifically designed for communications systems not requiring signal conditioning. Often, high-cost PCM bit synchronizers are used in these applications since commercial code converters and clock recovery units operate only at fixed frequencies. The CCCR provides an alternative to the PCM bit synchronizers by performing code conversion and clock regeneration at rates from 10 bps to 2.5 Mbps.