Defect-Sensitivity Analysis of an SEU Immune CMOS Logic Family [1]

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Abstract - **Fault testing of resistive manufacturing defects is done on a recently developed single event upset immune logic family. Resistive ranges and delay times are compared with those of traditional CMOS logic. Reaction of the logic to these defects is observed for a NOR gate and an evaluation of its ability to cope with them is determined.**

1 Introduction

This paper reviews prior research on the effects of manufacturing defects in CMOS logic. CMOS logic was chosen because it is becoming the technology of choice for digital microelectronics as it is well suited for VLSI designs. It requires low power while still providing high performance. It has been shown that stuck-at fault models do not accurately characterize all manufacturing defects, particularly for CMOS technology [5]; therefore, there exists an array of single fault physical models which cover critical manufacturing defects. This paper focuses upon resistive fault models as described in [3]. The goal is to apply these physical models to a newly developed SEU (single event upset) immune logic family [1]. Standard CMOS is sensitive to radiation effects in space, thus a robust CMOS logic family was developed which could tolerate this environment. The purpose of applying these physical models to this new SEU immune logic family is to observe how it deals with manufacturing defects as compared to traditional CMOS logic. Such information will be useful in evaluating the manufacturability of the technology.

2 Manufacturing Defects

Manufacturing defects are upsets in the fabrication process or environmental contaminations which affect the layout or the material of an IC causing it to function incorrectly. These manufacturing defects are physically represented by fault models. Fault models are used to generate test sets which in turn are used to determine faults in IC's. There are two types of manufacturing defects: global and local [6], [2]. Global defects involve major fabrication errors such as cracks or scratches on the wafer, mask misalignments, etc. These are easily detectable since many sections of the IC are damaged. Local defects, on the other hand, affect a localized area on an integrated circuit layer. These are seen as changes of the electrical properties at a point. Local (spot) defects are explored in this paper.

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V_{ILMAX}	1.84V
V_{IHMIN}	2.76V

Table 1: Noise Margin Parameters for Traditional CMOS

Manufacturing defects can generally be attributed to the absence or excess of material in one of the conductive, semiconductive, or insulating layers [4]. Airborne particles and droplets are the most predominant causes of spot defects as they contaminate the lithographic mask. Thus, most spot defects are generated during the lithographic process [6].

3 The SEU Immune Logic Family

While CMOS logic has many benefits, it is sensitive to radiation. In space applications, a high radiation level environment, particles pass through the electronic circuitry and momentarily alter the electrical properties in the area of penetration, thereby creating potential failures. The failure occurs when a particle passes through a diffusion region of one logic level to the substrate at the opposite logic level. This results in a short which gives rise to a glitch. An SEU immune (SEU-I) logic family was developed to provide radiation immunity, while maintaining many of the benefits of traditional CMOS logic [1]. In the SEU-I logic family, additional weak feedback transistors momentarily maintain the logic level in the impacted area and thus prevent the glitch. Figure 2 shows an SEU-I NOR gate and three SEU-I inverters. For more information on this family please see [1].

4 Fault Simulation Methods

Schematics were entered using PIGLET, an artwork and schematic editor, and translated to SPICE input using SCIP, a schematic translator and SPICE interface. Simulation was performed using HPSPICE with CMOS26 process models on a Hewlett Packard 9000/385 workstation. CMOS26 is a 1μm CMOS N-Well process. All simulations were done in the HPSPICE "slow case" in order to provide worst case conditions.

Resistive shorts were simulated on a two input NOR gate, driven by two inverters and driving an inverter. The shorts simulated for each transistor were drain-to-source, gate-to-source and gate-to-drain. Transistors were sized to provide a two to one β ratio between the NMOS and PMOS transistors and between the strong and weak transistors of the n and p networks. The process parameters were left as the HPSPICE CMOS26 default values.

The simulated input sequence was AB=(01 00 10 11). Each input was applied for 100ηsec with a transition time of 3ηsec. Input logic levels ranged from 0 to 4.5 volts, while the Vdd supply was set to 5 volts. The delay times for the faulted gates were determined for the 01 to 00 and 00 to 10 patterns since these are the only valid delay times for the sequence.

Resistive shorts have two primary effects upon a logic gate, depending upon the input pattern: one, the output voltage level may degrade, and two, the transition (delay) time may change. Minimum and maximum input levels for logic high and low were determined by applying a ramp input signal to an inverter and observing the input voltage levels corre-

	POUT	NOUT
V_{ILMAX}	2.93V	.57V
V_{IHMIN}	4.41V	2.65V

Table 2: Noise Margin Parameters for SEU-I CMOS

Input Pattern	Traditional OUT	SEU-I POUT	SEU-I NOUT
00→01	1	7.5	1.5
00→10	1	15	3
00→11	.5	6.5	1
01→00	1	1.5	3
11→00	1	1.5	3
10→00	1	1.5	3.5

Table 3: Fault Free Delay Time (ηsec). Resolution $\mp.5\eta$sec

sponding to a negative one slope on the output voltage [7]. This was done for both traditional CMOS and SEU-I CMOS, as shown in Tables 1 and 2. These levels separate the output voltage range into determinate and indeterminate regions. Careful considerations were made to maintain the same transistor parameters between the traditional CMOS gates, the SEU-I gates, and their respective noise margin inverters.

Simulations were performed to identify the critical short resistance at which a gate produced a valid output, meaning the output voltage fell within the determinate region. Below this resistance, the output was in the indeterminate region, while above this resistance the output voltage was always valid. For simulated shorts in which the output was affected for several input states, this resistance was recorded for each of the affected states, resulting in a resistive range. The smallest number in a resistive range indicates the short resistance at which the output was valid for one of the affected input states and the largest number indicates the short resistance at which the output was valid for all input states.

For shorts resulting in a valid output, delay times were recorded which indicate the time required for the output to transition. As the simulated short resistance was increased, the delay time eventually returned to that observed for a fault-free gate.

Capacitive loading was only provided through the driving of an inverter. If additional loading was simulated, the delay of both the traditional and SEU-I CMOS gates would increase.

5 Results

The output steady state level, resistance range, and delays were evaluated for the given shorts of the traditional and SEU-I logic. Fault free delay times are given in Table 3. The circuit used for the traditional CMOS simulations can be seen in Figure 1, whereas that used for SEU-I CMOS simulations is shown in Figure 2.

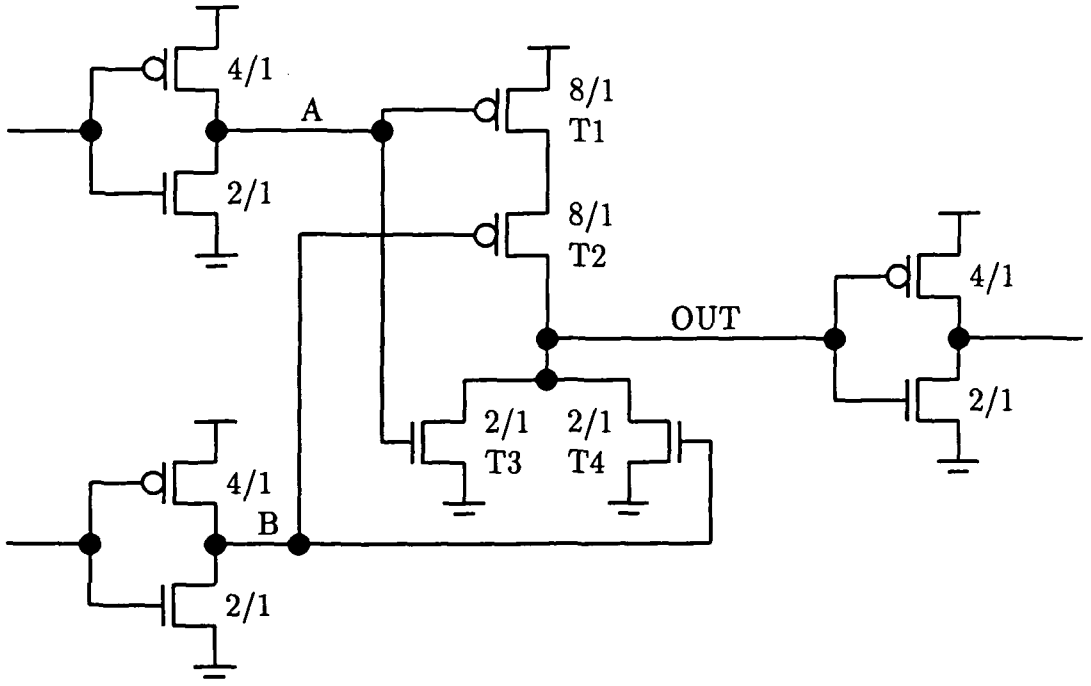

Figure 1: Traditional CMOS Circuit

5.1 Traditional CMOS Shorts

Drain-to-source shorts (DS) have the least effect since they only involve one transistor, meaning that they do not alter the electrical characteristics of other transistors. The output for each short was faulty under only a single input pattern, namely, 01(T2), 00(T3 and T4) and 10(T1). The input 00 activated the fault for both NMOS transistors because they are in parallel.

Gate-to-source shorts (GS), on the other hand, affect two transistors in the NOR gate, the first being the shorted transistor itself and the second being the transistor that connects to the shorted gate node (each input connects to two transistors, one n and one p). Again the output was only affected under a single input pattern, specifically 00(T1 and T2), 10(T3) and 01(T4). As the simulated resistance is decreased, the shorted transistor can not "turn on" completely. Consequently, the transistor's channel resistance is higher. Furthermore, the other transistor connected to the shorted node does not "turn off" completely.

Gate-to-drain (GD) shorts have the greatest effect since most of the shorts connect between the gate and the output, as opposed to the gate-to-source shorts which connect to supply nodes. Therefore, the input has a direct influence on the output while also altering the logic levels at other gates. For this reason, gate-to-drain shorts affect the output for multiple input states, those of 01(T2 and T4), 00(T1, T2, T3 and T4), 10(T1 and T3), and a mild effect (not enough to reach noise margin limits) from 11(T2, T3 and T4). As was the case for DS shorts, the GS short at T2 is identical to the GS short at T4. The delays are limited by the physical characteristics of the affected transistor. As the short's resistance is decreased, the gate and drain approach equipotential, causing the channel resistance to change. This resistance will continue to change until an equilibrium is reached between the

	T1	T2	T3	T4
DS	3.30	5.60	7.10	7.10
GS	6.25	5.76	7.84	7.08
GD	2.30→3.80	6.0→8.0	4.60→8.20	6.0→8.0

Table 4: Resistances for traditional CMOS (in K ohms)

	T1	T2	T3	T4
DS	(10)1.5...	(01)*N.S.*	(00)1.0...	(00)1.0...
GS	(00)4.0...	(00)3.0...	(10)6.5...	(01)*N.S.*
GD	(00)1.5...	(00)1.5...	(00)1.0...	(00)1.5...
	(10)1.5...	(01)*N.S.*	(10)1.5...	(01)*N.S.*

Table 5: Delay times for traditional CMOS (in ηsec). Resolution $\mp.5\eta$sec

"on" (channel) resistance and the short resistance. For example, PMOS transistors (i.e. T1) pass ones, thus, a GD short would cause the transistor to begin turning off, causing the channel resistance to increase. This is the same idea as the gate to source short except that the drain potential is dependent on how fully "on" the transistor is. It is for this reason that the channel resistance will reach an equilibrium with the fixed short resistance. This prevents the delay from becoming large. The NMOS transistors behave similarly.

Tables 4 and 5 show resistance values and delay times respectively. The affected input states are shown as (AB). Take for example entry T4/GD where the input (00) has a delay of 1.5ηsec. As the resistance increases the delay time drops to its fault free value of 1.0ηsec. The N.S. (Not Simulated) for input (01) means that although the DS short did cause faulty behavior for the input A=0 and B=1 it was not possible to calculate a delay time because input (01) was the starting input of the sequence. All delay times return to the fault free times as the resistance goes towards infinity.

5.2 SEU-I CMOS Shorts

As can be expected, the common transistors between the SEU-I and the traditional CMOS behave in a similar manner to the same input patterns for the given faults. For this reason, only the differences will be presented.

Drain-to-source shorts in the feedback transistor affect several input patterns, those where the output is high (00) for T5 and those where the output is low (01 10 and 11) for T6. T5 pulls POUT low while T6 pulls NOUT high. This short type, as can be seen, has a higher resistive range since there is a direct influence on the output. Delays occur for the T6 feedback gate where the output is low and the T5 feedback gate where the output is high. As T6 is shorted, NOUT is pulled up causing T5 to turn off and thus increasing the resistance to ground. Since T5 is the means by which POUT is pulled low, any effect upon this gate would greatly affect the fall time. For the case of T5, POUT is driven by the pull up transistors, thus, shorting T5 has little effect outside of causing POUT to be pulled down. When POUT is pulled down the resistance from NOUT to Vdd is increased, thereby

5.2.6

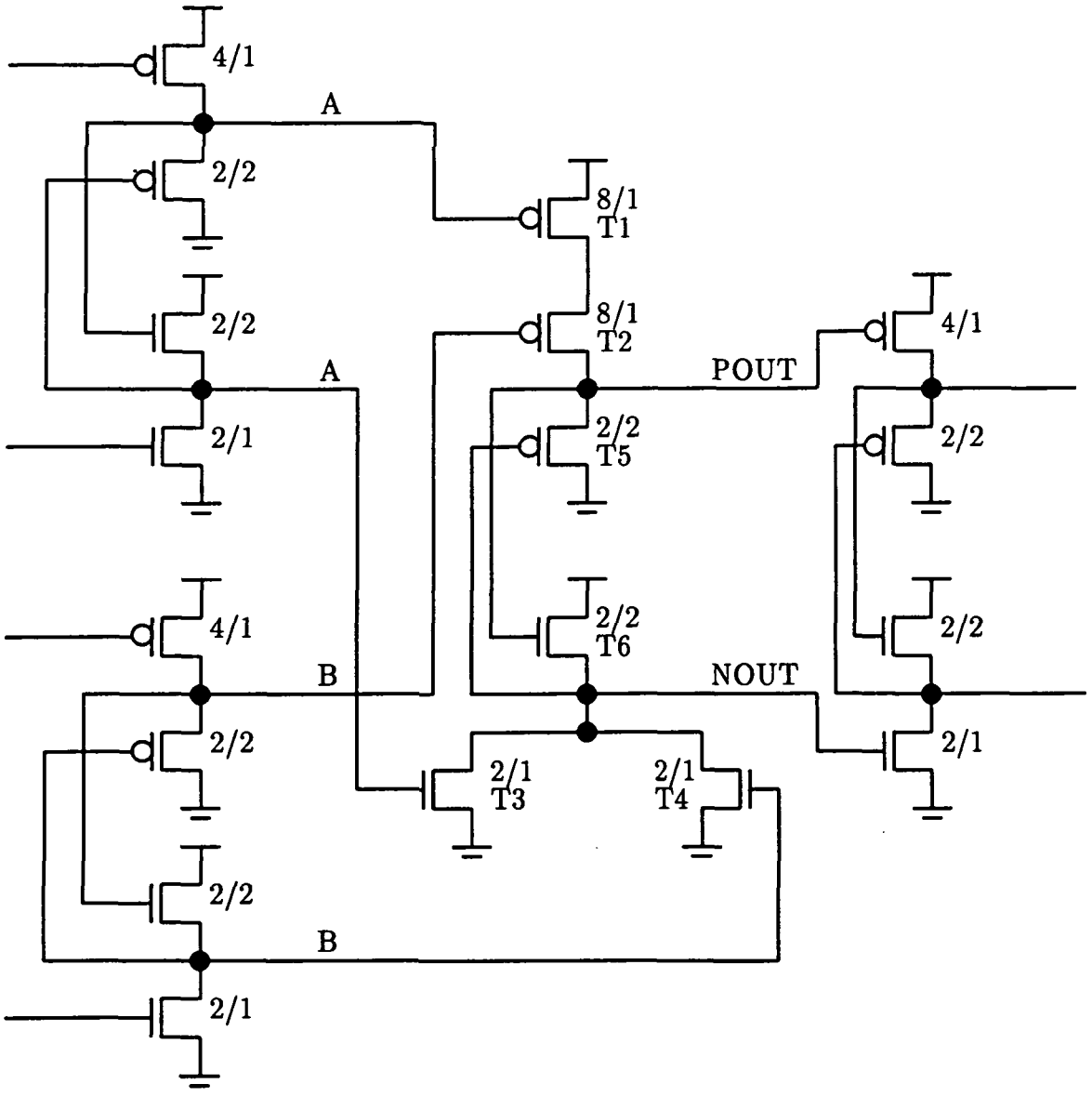

Figure 2: SEU-I Circuit

		T1	T2	T3	T4
DS	POUT	140.0	150.0	No Effect	No Effect
	NOUT	30.0	30.0	100.0	100.0
GS	POUT	26.0	30.0	6.0	5.0
	NOUT	22.0	24.0	10.0	9.0
GD	POUT	33.0→136.0	39.0→140.0	10.0	5.0
	NOUT	15.0→27.0	16.0→35.0	6.0→95.0	5.0→95.0

Table 6: Resistances for SEU-I CMOS common transistors (in K ohms)

		T5	T6
DS	POUT	50.0	10.0→15.0
	NOUT	30.0	20.0→40.0
GS	POUT	No Effect	No Effect
	NOUT	No Effect	No Effect
GD	POUT	No Effect	120.0→140.0
	NOUT	100.0	40.0

Table 7: Resistances for SEU-I CMOS feedback transistors (in K ohms)

increasing the rise time for NOUT.

Gate-to-source shorts for the feedback transistors have no effect on the outputs. This type of short connects POUT to NOUT; because these nodes are always at the same logic levels, the result is to simply to pull both nodes to the appropriate rail. The resistive range, for the common transistors, is the lowest of all SEU-I transistor shorts. These shorts affect the transistor's gate as opposed to affecting the output directly, as is the case for the DS and GD shorts (i.e. the transistors "on" state is manipulated instead of the transistor being bypassed).

Gate-to-drain shorts of the feedback transistors affect several input states, which are the same as those of the drain-to-source short. In this case the T5 transistor pulls NOUT down while T6 pulls POUT up. This happens when POUT is low. This fault type has a high resistive range much like the DS short, where the input to the gate affects the output directly. As a result of the shorted feedback transistors, there is a minimum effect upon the delays. A GD short on T5 has no effect since it occurs at the input pattern (00) where the transistor is not driving the output. However, it is also the DS short for T3, but this short too has virtually no influence on the rise time. The feedback transistor T6 has an influence for the input patterns (01,10 and 11), although, the effect to the output is again minimal. For these input cases the output NOUT is driven by either transistor T3, T4 or both; thus, as T6's resistance increases the effect is not noticed in output's fall time.

Tables 6 and 7 show resistance values for SEU-I CMOS common and feedback transistors. Tables 8 and 9 present delay times for the common and feedback transistors. Shorts that did not have an effect on the circuit are indicated by "No Effect".

		T1	T2	T3	T4
DS	POUT	(10)5.0...	(01)*N.S.*	(00)1.5...	(00)1.5...
	NOUT	(10)1.5...	(01)*N.S.*	(00)2.0...	(00)2.0...
GS	POUT	(00)21.0...	(00)12.5...	(10)45.0...	(01)*N.S.*
	NOUT	(00)25.0...	(00)24.0...	(10)32.5...	(01)*N.S.*
GD	POUT	(10)4.5... (00)2.5...	(01)*N.S.* (00)2.5... (11)*N.S.*	(00)1.5... (10)20.5... (11)*N.S.*	(01)*N.S.* (00)1.5... (11)*N.S.*
	NOUT	(10)1.5... (00)6.5...	(01)*N.S.* (00)2.0... (11)*N.S.*	(00)2.0... (10)8.5... (11)*N.S.*	(01)*N.S.* (00)2.0... (11)*N.S.*

Table 8: Delay times for SEU-I CMOS common transistors (in ηsec). Resolution $\mp.5\eta$sec

		T5	T6
DS	POUT	(00)2.5...	(01)*N.S.* (10)21.0... (01)*N.S.*
	NOUT	(00)4.5...	(01)*N.S.* (10)3.0... (01)*N.S.*
GS	POUT	No Effect	No Effect
	NOUT		
GD	POUT	(00)1.5...	(01)*N.S.* (10)5.0... (11)*N.S.*
	NOUT	(00)2.0...	(01)*N.S.* (10)1.5... (11)*N.S.*

Table 9: Delay times for SEU-I CMOS feedback transistors (in ηsec). Resolution $\mp.5\eta$sec

5.3 Discussion of Results

The results have shown that there are some considerable differences between the behavior of the SEU-I and traditional CMOS logics. The differences are due to the weak feedback transistors and, most importantly, the SEU-I gates which drive them.

Feedback transistors by their design have a higher resistance (this is required for SEU-I operation [1]) which results in higher delays when driving the output, as in, the output POUT during a 01, 10 or 11 input. This transistor feedback also provides a means by which the faulted output can return and intensify the faulting effect. An example would be a drain-to-source short on T1 with an input of 10. As the short's resistance decreases, POUT gets pulled up from its ground level causing the feedback transistor T6 to start turning "on". With this event NOUT gets pulled up from its ground level causing the feedback transistor T5 to start turning "off". The result of T5 not being fully "on" leads to an increase of POUT, thus intensifying the fault.

Since SEU-I logic is driven by SEU-I logic, an increase in delay and resistive range occurs. This can be seen in the gate-to-source and gate-to-drain shorts. For example, consider the gate-to-source short on T1 for the input 00. As the simulated resistance is decreased, T1 begins to shut "off", causing the rise time to increase. For traditional CMOS, T1's gate is being driven low by a strong (lower channel resistance) NMOS transistor in the preceeding inverter. In the case of the SEU-I CMOS, T1's gate is being driven low by a weak (higher channel resistance) PMOS transistor. The result of being driven by a weak transistor is an increased rise time since it takes longer for the driving transistor to pull the driven transistor (T1) low. The high SEU-I delay is not confined to only faulted conditions, as can be seen from the fault free values. SEU-I logic transistors are driven "on" by weak gates which pass poor signals. An example would be the PMOS transistor T1, the gate of which is driven low by a weak PMOS transistor in the preceeding logic gate. PMOS transistors do not pass good zeros. Thus T1 is never fully "on". The increase in resistive range, as compared to the traditional CMOS, is due to the resistive ratio between the short of the driven transistor and the channel of the driving transistor. A higher channel resistance must be matched by a corresponding increase in the short resistance in order to maintain the same voltage level at the gate. This means that traditional CMOS, because it drives the output with "strong" transistors, can overcome, or tolerate, lower resistance shorts.

It is important to note that resistive shorts will also effect the gate being driven. For example, if T6's channel resistance increases due to a short then a gate being driven by it will experience a much greater delay time on its output. This can propagate through the circuit.

6 Summary

As the results show, SEU-I CMOS logic is more sensitive to resistive shorts than its traditional CMOS counterpart. It is, however, important to note that realistic manufacturing faults may not span from zero to infinity. That is to say that resistive faults may only occur for a small range of values. Consequently, the fact that the SEU immune logic is more sensitive may not be a concern. The higher rise time is, on the other hand, a concern in the

area of performance since a circuit is dependent on its worst case time. A reduction of the RC time constant could be achieved by strengthening the feedback transistors. However, strengthening the feedback transistors affects the transient suppression abilities [1].

This research has only covered the narrow field of resistive faults. The author wishes to continue exploring other manufacturing faults such as bridging, stuck-at's and stuck-on's to make a more complete judgment on the logic's ability to tolerate such defects.

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