Behavior of Faulty Double BJT BiCMOS Logic Gates [1]

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Abstract - **Logic Behavior of Double BJT BiCMOS device under transistor level shorts and opens is examined. In addition to delay faults, faults that cause the gate to exhibit sequential behavior were observed. Several faults can be detected only by monitoring the current. The faulty behavior of Bipolar (TTL) and CMOS logic families is compared with BiCMOS, to bring out the testability differences.**

1 Introduction

Combining the advantages of CMOS and Bipolar, BiCMOS is emerging as a major technology for many high performance digital and mixed signal applications. The main advantages of CMOS technology over bipolar are lower power dissipation and higher packing density. Bipolar technology offers better output current drive, switching speed, I/O speed and analog capability. Combining the advantages of bipolar and CMOS, BiCMOS offers the following advantages [1]; improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability and latch up immunity. Compared to the CMOS counterparts, BiCMOS circuits can be faster by a factor of upto two for the same level of technology. Access times of less than 10ns have been reported for 0.8 μm BiCMOS ECL input/output 256K and 1M-bit SRAMs [2]. BiCMOS is even being considered for high performance microprocessors and dynamic RAMs, and it is felt that it will be one of the main technologies to drive almost all functions in the decade ahead [3].

In the present day integrated circuits, most of the defects and failures can be abstracted to shorts and opens in the interconnects and degradation of devices [4]. Transistor level shorts and opens model many of the physical failures and defects in ICs [5]. A study by Gailiay [6] on 4-bit MOS microprocessor chips revealed that many of the faults were shorts and opens at the transistor level. Analysis of faults in elementary static storage elements suggest that transistor level testing provides a higher coverage of faults compared to that at the gate level [7]. Thus, it is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [5].

The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects [8]. It has been shown [9, 10] that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults. In this paper, we present the behavior of double BJT BiCMOS device under stuck-ON and stuck-OPEN failures for all transistors and bring

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out the testability differences between the three logic families, namely; TTL, CMOS and BiCMOS. Levitt et. al. [9] presented inadequacy of stuck-at fault models for BiCMOS. Testing of BiCMOS circuits and a design for testability scheme for current testing of BiCMOS circuits was presented in [11]. In this study, we present detailed behavior of BiCMOS device under various faults along with a comparison with CMOS and TTL logic families.

Several different designs of BiCMOS circuits exist. The most common type of BiCMOS circuits employ bipolar transistors to perform the function of driving output loads and CMOS to perform logic functions. In this paper, we briefly review the operation of a double BJT (D-BJT) BiCMOS NAND device. Logic behavior of D-BJT BiCMOS NAND devices are examined under different faults and their comparison is presented with other logic families (TTL and CMOS).

This paper is organized as follows. The operation of D-BJT BiCMOS NAND devices is described in Section 2. Section 3 deals with the analysis of physical failures in D-BJT BiCMOS devices, where the logic behavior of D-BJT BiCMOS devices are examined under different faults. Comparison of the three logic families (TTL, CMOS and BiCMOS) are done in Section 4. Finally, conclusions drawn from the study are given in Section 5.

2 BiCMOS Devices

BiCMOS circuits employ one or two Bipolar Junction Transistors (BJTs) to perform the function of driving output loads and CMOS to perform logic functions. In this section, the operation of a double BJT (D-BJT) NAND device is presented.

A Double BJT BiCMOS NAND realization is shown in Figure 1. There are many other realizations possible and we have investigated the above realization. The BiCMOS NAND realization shown in Figure 1 uses two output BJTs (Bipolar Junction Transistor) and there are other implementations that use single BJT. In this study, we deal with only double BJT BiCMOS devices. The functioning of the BiCMOS NAND can be explained by first applying logic '0' to one or both of the inputs which would cause at least one P-device to be ON and at least one N-device in each serial N-pairs to be OFF. With at least one N-device in each serial N-pairs being OFF, no current is supplied to the base of Q_2 resulting in transistor Q_2 being OFF. With the P-devices (P_1 and/or P_2) ON, the base of the bipolar NPN (Q_1) transistor would be about 5V supplying base current and turning ON the bipolar transistor (Q_1) providing logic '1' at the output. With either of the inputs being at logic '0' and the other input at logic '1' would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still supply base current to the bipolar transistor Q_1 causing logic '1' at the output. With both the inputs at logic '1', the P-devices (P_1 and P_2) would be turned OFF, and the N-devices N_1, N_2, N_3 and N_4 would be turned ON, supplying base current to Q_2 which discharges the load. Transistor N_1 and N_2 draw current from the base of Q_1 thus rapidly turning this device OFF. This will cause the output to be a logic '0'. Thus the circuit realizes the NAND function. It may be noted that during output High to Low transition, transistor N_5 turns OFF as a result of transistors N_1 and N_2 discharging Q_1 base, causing the gate of N_5 to be low [12], this results in all the current through N_3 and N_4 to be provided as base current to transistor Q_2. During output Low to High transition, transistor N_5 turns ON to discharge the base of Q_2 quickly

to speed up the transition. It may also be noted that the static power consumption of the circuit is negligible neglecting reverse biased leakage currents. Block diagram of a general D-BJT BiCMOS device is shown in Figure 2. A D-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, and two output BJTs for driving the output node.

D-BJT BiCMOS devices do not have the full V_{DD} to Ground logic swing of CMOS devices. The output High voltage (V_{OH}) is limited to V_{DD}-$V_{BE(Q1)}$ and output Low voltage (V_{OL}) is limited to Gnd+$V_{BE(Q2)}$. V_{ILmax} and V_{IHmin} were determined to be 2.2V and 2.7V respectively [13]. The logic levels for D-BJT BiCMOS are 0.6V to 2.2V for logic level '0' and 2.7V to 4.4V for logic level '1' [13]. Any voltage between 2.2V and 2.7V is considered indeterminate. The device characteristics given for Fujitsu BiCMOS gate array devices [14] are V_{IHmin}=2V, V_{OHmin}=2.4V, V_{ILmax}=0.8V and V_{OLmax}=0.5V.

3 Analysis of Physical Failures in D-BJT BiCMOS devices

The response of the D-BJT BiCMOS NAND shown in Figure 1 is evaluated for hard failures of the bipolar & MOS transistors and their results are presented in this section. Possible failures considered are stuck-ON and stuck-OPEN of transistors. The output of the BiCMOS gate is obtained by simulating one failure at a time for all possible stuck-ON and stuck-OPEN failures for all transistors. Stuck-ON and stuck-OPEN were simulated by turning ON and turning OFF the respective transistors. Open (OP) in bipolar transistor terminals (emitter, base & collector) were simulated by connecting a resistance of R>1MΩ in series with the respective node and short (SH) were simulated by connecting a hard short of R<0.01Ω between the respective terminals. The BiCMOS gate outputs obtained analytically have been compared with SPICE simulation outputs to ensure correctness.

The fault-free and faulty behavior of BiCMOS NAND is summarized in Table 1. The length and width of pMOS (L_p,W_p) and nMOS (L_n,W_n) transistors used for BiCMOS devices in this study are (L_p=1.5μm,W_p=30μm) and (L_n=1.5μm,W_n=26μm), similar to the values used in [9], for consistency. Simultaneous current monitoring was performed during SPICE simulation and the observed I_{DDQ} values are listed in the Table along with the output logic levels. In Table 1, the subscript represents the transistor number for the BiCMOS circuit shown in Figure 1 and superscript represents the type of hard failure under consideration where ON indicates stuck-ON failure and OP indicates stuck-OPEN failure. For example, N_1^{ON} indicates transistor N_1 stuck-ON, N_1^{OP} indicates transistor N_1 stuck-OPEN, Q_{1c}^{OP} indicates transistor Q_1 collector open and Q_{1c-e}^{SH} indicates transistor collector to emitter short.

In order to make the analysis a true representative of circuit conditions, CMOS inverters were used to drive the BiCMOS device and CMOS inverters were used as load to the BiCMOS device as shown in Figure 3. Gates G_1 and G_2 are CMOS inverters used to drive the BiCMOS NAND gate G_3. CMOS inverter G_4 is used as load to the BiCMOS NAND. The length and width of pMOS (L_p,W_p) and nMOS (L_n,W_n) transistors used as CMOS driver devices in this study are (L_p=5μm,W_p=60μm) and (L_n=5μm,W_n=20μm). The sizes for the CMOS load devices used are (L_p=5μm,W_p=40μm) and (L_n=5μm,W_n=15μm). To study the effects of

output fan-out on BiCMOS devices, analysis was conducted with one CMOS load alone and also with an RC (Resistor Capacitor) load along with a CMOS load as shown in Figure 3. R=100Ω and C=1pF were chosen for this study and RC load referred to henceforth in this paper refers to the above values.

3.1 Stuck-ON faults in D-BJT BiCMOS NAND

Referring to the D-BJT BiCMOS NAND shown in Figure 1, for the physical failure P_1^{ON}, input vector '11' causes the N-devices (N_1, N_2, N_3 and N_4) to be ON. This causes transistor Q_2 to be ON, providing a conduction path from V_{DD} to V_{SS}(Gnd), resulting in enhanced I_{DDQ}. The current drawn by the device with this vector for the fault under consideration is 2mA instead of the normal 0.2μA. Current testing technique can be employed to detect this fault. Similar result is observed for transistor P_2 stuck-ON failure (P_2^{ON}). SPICE simulation indicates the output voltage level to be ≈1.63V, which is logic '0' level for BiCMOS devices indicated as '0' in Table 1. For transistor N_1 stuck-ON and input vector 01, transistors P_2, N_2 and N_4 would be turned ON and with transistor N_1 stuck-ON leads to transistor Q_2 to be ON. This provides a conduction path between V_{DD} and V_{SS}(Gnd), resulting in an increased current flow (enhanced I_{DDQ}). SPICE simulation indicates the output voltage to be 1.86V, which is logic '0' for D-BJT BiCMOS devices. For transistor N_2 stuck-ON, input vectors 00, 01 or 11 would exhibit fault-free behavior. With input vector 10, transistors P_1 and N_1 would be turned ON and due to the transistor N_2 stuck-ON under consideration, causes transistor Q_2 to be ON. This results in a conduction path to exist between V_{DD} and V_{SS}(Gnd) resulting in enhanced I_{DDQ}. SPICE simulation indicates the output voltage level to be ≈1.86V, which is logic '0' level for D-BJT BiCMOS devices. Stuck-ON failures of transistors N_3 and N_4 result in enhanced I_{DDQ} for input vectors 01 and 10 respectively. The fault-free and faulty logic levels for N_3 and N_4 stuck-ON failures exhibit logic '1' at the output. Since the fault-free and faulty logic levels are the same, current testing alone can detect the failures. Transistor N_5 stuck-ON failure does not cause any appreciable effect for output Low to High transitions. However, during output High to Low transitions, with input vector '11', the output finds a low resistance path through transistors N_3, N_4 and N_5. Due to this low resistance path, transistor Q_2 does not turn ON and hence, High to Low transition gets delayed. This delay is dependent upon the output load. For RC load, the High to Low transition delay was observed to be 1.45ns instead of the normal 0.89ns. It may be noted that due to the low resistance path through transistors N_3, N_4 and N_5, output goes all the way to ground instead of $Gnd+V_{BE(Q2)}$. Transistor Q_{1c-e} and Q_{1b-c} shorts result in enhanced I_{DDQ} and causes a faulty output logic level '1' for input vector 11. Transistor Q_{2c-e} and Q_{2b-c} shorts also result in enhanced I_{DDQ} and causes a faulty output logic level '0' for input vectors 00, 01 and 10. Transistor Q_{1b-e} and Q_{2b-e} shorts result in delay faults for Low to High transition and High to Low transitions respectively, as the base to emitter junction of the transistors do not get forward biased and hence do not get turned ON. The Low to High transition delay observed for Q_{1b-e} short with RC output load is 1.98ns compared to the fault-free delay of 1.07ns. The High to Low transition delay observed for Q_{2b-e} short with RC output load is 1.47ns compared to the fault-free delay of 0.89ns.

Table 1. Behavior of D-BJT BiCMOS NAND with Stuck-ON and Stuck-OPEN faults.

BiCMOS NAND Stuck-ON and Stuck-OPEN results														
Input	*ff*	P_1^{ON}	P_2^{ON}	N_1^{ON}	N_2^{ON}	N_3^{ON}	N_4^{ON}	N_5^{ON}	Q_{1c-e}^{SH}	Q_{1b-c}^{SH}	Q_{1b-e}^{SH}	Q_{2c-e}^{SH}	Q_{2b-c}^{SH}	Q_{2b-e}^{SH}
A B	X i	X i	X i	X i	X i	X i	X i	X i	X i	X i	X i	X i	X i	X i
0 0	1 n	1 n	1 n	1 n	1 n	1 n	1 n	1 n	1 n	1 n	D_{0-1} n	0 a	0 a	1 n
0 1	1 n	1 n	1 n	0 a	1 n	1 a	1 n	1 n	1 n	1 n	D_{0-1} n	0 a	0 a	1 n
1 0	1 n	1 n	1 n	1 n	0 a	1 n	1 a	1 n	1 n	1 n	D_{0-1} n	0 a	0 a	1 n
1 1	0 n	0 a	0 a	0 n	0 n	0 n	0 n	D_{1-0} n	1 a	1 a	0 n	0 n	0 n	D_{1-0} n
Input	*ff*	P_1^{OP}	P_2^{OP}	N_1^{OP}	N_2^{OP}	N_3^{OP}	N_4^{OP}	N_5^{OP}	Q_{1e}^{OP}	Q_{1b}^{OP}	Q_{1c}^{OP}	Q_{2e}^{OP}	Q_{2b}^{OP}	Q_{2c}^{OP}
A B	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0 0	1	1	1	1	1	1	1	D_{0-1}	R	R	D_{0-1}	1	1	1
0 1	1	1	Q^n	1	1	1	1	D_{0-1}	R	R	D_{0-1}	1	1	1
1 0	1	Q^n	1	1	1	1	1	D_{0-1}	R	R	D_{0-1}	1	1	1
1 1	0	0	0	D_{1-0}	D_{1-0}	D_{1-0}	D_{1-0}	0	0	0	0	D_{1-0}	D_{1-0}	D_{1-0}

X = Output, i = Current drawn by the device, Q^n = Previous State,
ON = Stuck-ON, OP = Stuck-Open, SH = Short,
ff = fault free, I^* = Indeterminate (2.2-2.7Volts), (e, b, c = emitter, base, collector),
n (Normal Current) = 2e-7A, a (Abnormal Current) > 2.00e-2A, R = Stuck-at-0 after initialization,
D_{0-1} = Low to High transition delay, D_{1-0} = High to Low transition delay.

Current testing can be very effective for testing failures which result in elevated I_{DDQ} from a normal $\approx 0.2\mu$A to enhanced $\approx$2mA, an increase by a factor of $\approx 10^4$. Since stuck-ON failures P_1^{ON}, P_2^{ON}, N_3^{ON} and N_4^{ON} provide same logic level for faulty as well as fault-free operations, current testing alone can detect the failures. Transistor N_1 and N_2 stuck-ON as well as Q_{1c-e}^{SH}, Q_{1b-c}^{SH},Q_{2c-e}^{SH}, and Q_{2b-c}^{SH} failures exhibit dissimilar outputs under faulty and fault-free conditions, conventional logic testing can detect the failure. However, current testing would detect this failure mode. Transistors Q_1 & Q_2 base to emitter shorts manifest as Low to High and High to Low transition delays respectively and hence delay test alone would detect the failure modes.

3.2 Stuck-OPEN faults in D-BJT BiCMOS NAND

Two faults in the D-BJT BiCMOS NAND exhibit sequential behavior (Q_n), similar to the behavior seen in CMOS circuits. Presence of the fault P_1 stuck-OPEN with input vector '10' causes the previous state to be retained resulting in sequential behavior. Similar sequential behavior is observed for P_2 stuck-open with input vector '01'. Two pattern tests can be applied to detect these stuck-open failures.

S-OPEN failures of transistors N_1 and N_2 exhibit unique delay faults, as observed in S-BJT BiCMOS NAND. A first glance would lead one to expect that with input vectors '11', the output parasitic capacitance would be discharged by turning ON of transistors N_3, N_4 and Q_2. However, due to the OPEN fault of N_1 or N_2 under consideration, the vectors 00, 01 or 10 would charge up the parasitic capacitors at the base as well as the emitter nodes of the bipolar transistor Q_1. With the application of input vector 11, the series path of N_3 and N_4 will be turned ON but the series path of N_1 and N_2 will not be turned ON due to the

fault. This will cause transistor Q_1 to remain ON for sometime because of the charge stored at the base of the bipolar transistor Q_1. Transistor Q_1 would be discharged slowly through N_3, N_4 and Q_2 path alone causing delay in the output response. The slow to fall delay fault is shown in Figure 4a,b,&c. This type of fault has been observed in [9]. Figures 4a&b show the response of the D-BJT BiCMOS NAND to N_1^{OP} failure with one CMOS output load and input pulse width t_{pw} of 10ns and 4ns respectively. Figure 4a shows the response of the BiCMOS NAND to N_1^{OP} with only one CMOS connected to the BiCMOS output. The inputs shown in this figure are the inputs applied to the BiCMOS NAND and the input pulse width (t_{pw}) is 10ns wide. The response of the BiCMOS NAND with N_1^{OP} fault with input t_{pw}=10ns shows slow to fall delay (t_{hl2}) of 4.5ns instead of the normal propagation delay (t_{hl1}) of 0.526ns. Response of the BiCMOS output with the same one CMOS load and with t_{pw} of 4ns causes a High to Low delay of 7.2ns instead of the normal propagation delay of 0.58ns. As the clock period is small, it should be noticed here that the output barely reaches the switching threshold and the logic level does not have a chance to drop to logic '0' range. If the clock period is further reduced or if the output load is increased, the output level will not have a chance to reach even the switching threshold. An example of which is shown in Figure 4c where an RC load is used in addition to a CMOS load. It can be seen that the output does not have a chance to reach the switching threshold. The response of the fault-free BiCMOS NAND with t_{pw}=4ns and RC load gives a propagation delay of 0.79ns.

Response of stuck-OPEN failure of N_4 are shown in Figures 5a,b&c. For the stuck-OPEN failure of N_4 shown in Figure 5a, with input vector '11' exhibits a delay (t_{hl2}) of 1.204ns and output logic level of 1V instead of the normal propagation delay of 0.526ns and logic level of 0.6V, with one CMOS load and input pulse width t_{pw} of 10ns. Reducing the pulse width t_{pw} to 4ns exhibits a delay (t_{hl2}) of 1.25ns in place of the normal t_{hl1} of 0.58ns as shown in Figure 5b. The output level is observed to be $\approx$1.5V instead of the normal output level of $\approx$0.6V, however, the output logic level is still a valid logic '0' level of D-BJT BiCMOS devices. With RC load and input pulse width t_{pw} of 4ns, the output logic level does not fall below the logic threshold as shown in Figure 5c. Hence, the fault appears as stuck-at-1 for logic testing purposes.

Bipolar transistor Q_1 emitter and base open faults manifest as stuck-at-0 after initialization (shown as R in Table 1). It can be seen that with either of the above faults, output cannot go to logic '1' (other than during power up) as no path exists between output and V_{DD}. With Bipolar transistor Q_1 collector open, the output exhibits Low to High transition delay (D_{0-1}) as shown in Figures 6ab&c. Figure 6a shows the response of BiCMOS NAND to Q_1 collector open with one CMOS load connected to the BiCMOS output and with input pulse width t_{pw} of 10ns shows Low to High transition (t_{lh2}) delay of 1.08ns instead of the normal Low to High transition (t_{hl1}) of 0.823ns. Response with the same one CMOS load and with input pulse width (t_{pw}) of 4ns exhibits Low to High transition delay (t_{lh2}) of 1.105ns instead of the normal propagation delay (t_{lh1}) of 0.72ns as shown in Figure 6b. Figure 7c shows the response of the BiCMOS NAND with input t_{pw}=4ns and RC load where the faulty output exhibits a larger delay for the Low to High transition. The faulty Low to High transition delay is seen to be t_{lh2}=2.3ns instead of the normal Low to High transition delay of t_{lh1}=0.91ns.

Bipolar transistor Q_2 emitter, base & collector open faults manifest as High to Low delay

faults. Base and emitter opens are shown in Figures 6a,b&c. With one CMOS load and input t_{pw} of 10ns shows a delay (t_{hl2}) of 1.059ns instead of the normal propagation delay (t_{hl1}) of 0.526ns for Q_2 base open. However, Q_2 emitter exhibits a lower delay compared to Q_2 base open. With input t_{pw} of 4ns and with one CMOS load, the output exhibits a delay (t_{hl2}) of 1.68ns instead of the normal propagation delay (t_{hl1}) of 0.58ns. With RC load at the output of the BiCMOS NAND input t_{pw} of 4ns, the output exhibits a delay (t_{hl2}) of 3.22ns instead of the normal propagation delay (t_{hl1}) of 0.79ns, for transistor Q_2 base open. Transistor Q_2 emitter open with input t_{pw} of 4ns exhibits stuck-at-1 behavior since before the input can make a transition to output low, the input undergoes transition to opposite logic level. If the input pulse width (t_{pw}) is made wider, the output would go to the other side of the logic threshold.

Transistor N_5 serves the purpose of discharging the base of Q_2 quickly to speed up the output Low to High transition [12]. Stuck-OPEN failure of transistor N_5 can be expected to result in delayed Low to High transition.

There is an interesting observation during output High to Low transition which needs mentioning. During output High to Low transition and with N_5 stuck-OPEN, it is observed that the output transition speeds up and causes enhanced dynamic current (I_{DD}) as shown in Figure 7. This can be explained as follows. Under normal operation with N_5 fault-free, any of the input vectors 00,01 or 10 causing output high(1), turns ON transistor N_5, thereby base of Q_2 remains discharged, keeping transistor Q_2 OFF. With transistor N_5 stuck-OPEN, any of the input vectors 00, 01 or 10 causing output high(1), will not be able to turn ON transistor N_5 and discharge base of Q_2. This causes some base bias to exist at the base of transistor Q_2. The base bias existing at the base of Q_2 may be sufficient enough to turn ON the device partially. Since the input vectors 00, 01 or 10 are intended to turn ON transistor Q_1 to provide output High, with Q_2 also partially ON, enhanced dynamic I_{DD} is observed. It may be noted that given sufficient time the current may decay to Zero. Hence, this probably cannot be termed as enhanced I_{DDQ} fault and so this is being termed as enhanced dynamic I_{DD} fault. I_{DDQ} testing may detect this fault as the enhanced dynamic I_{DD} current is about 2 orders of magnitude greater than fault-free current, just after the initial transient. Due to the existence of residual base bias on transistor Q_2, with input vector 11, turns transistor Q_2 ON faster than fault-free where no residual base bias exists. Hence, the speed up for output High to Low transition. The fault-free output High to Low transition delay is observed to be 0.90ns and with transistor N_5 stuck-OPEN 0.43ns, resulting in 0.47ns early transition than that of fault-free.

4 Comparison of the three logic families (TTL, CMOS, BiCMOS)

Summary of faulty behavior of double BJT BiCMOS NAND, TTL NAND and CMOS NAND is provided in Table 2, where transistor stuck-ON and stuck-OPEN faults have been examined. It was shown [9] that some of the open failures manifest themselves as delay faults. Apart from delay faults, we have observed sequential behavior, stuck at 0/1 and some faults that cause degraded signal levels. Most of the stuck-ON faults can be tested in a definite way

using power supply current monitoring. Some of the stuck-OPEN failures exhibit sequential behavior which require two pattern tests to detect the failure.

Table 2. Summary of faulty behavior in BiCMOS, CMOS and Bipolar NAND Gates.

Summary of BiCMOS, CMOS & TTL			
Type of faulty Behavior	BiCMOS NAND (D-BJT)	CMOS NAND	TTL NAND
Stuck-at-0 or 1	7.7 %	$\approx$ 25 %	> 90 %
Sequential Behavior	7.7 %	$\approx$ 25 %	—
Current Testable Fault	38.5 %	$\approx$ 50 %	—
Delay Fault	46.1 %	—	—

Conclusions that are drawn from the above summary is that almost $\approx$38.5% of the physical failures in D-BJT BiCMOS devices manifest as current testable faults, which does not include N_5 open fault manifesting as enhanced dynamic I_{DD} current. Hence, a good number of physical failures can be detected using current monitoring techniques [15, 16, 10]. A scheme for current monitoring in BiCMOS devices is presented in [11]. Apart from faults manifesting as abnormal I_{DDQ}, majority of failures manifest as delay faults.

5 Conclusions

Physical failures causing transistor stuck-OPEN in Double BJT BiCMOS devices were examined. In addition to sequential behavior observed in CMOS devices, BiCMOS devices also exhibit delay faults. Some of the stuck-ON faults can be detected by observing voltage level, however, power supply current (I_{DDQ}) monitoring would definitely detect the fault. Faulty behavior of the three different families, namely, TTL, CMOS and BiCMOS were compared to bring out the testability differences between the three logic families.

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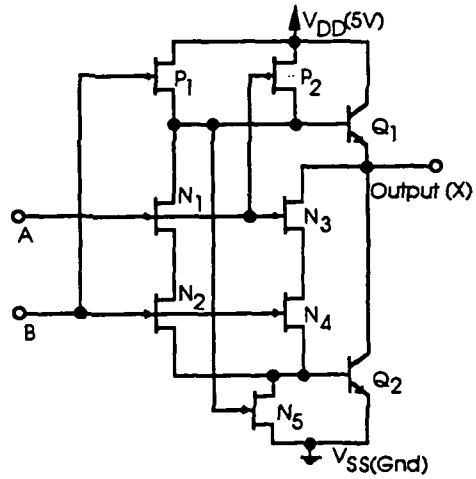


Figure 1: A D-BJT BiCMOS NAND.

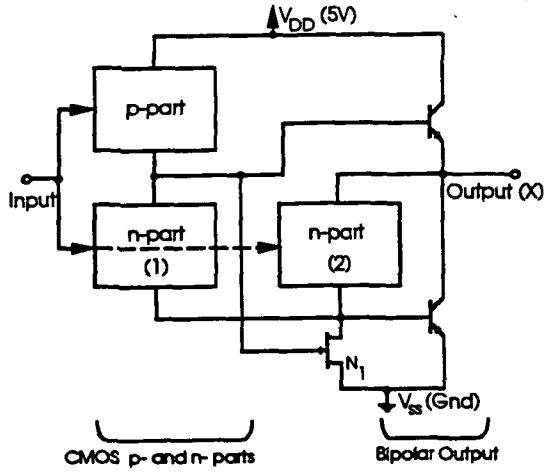


Figure 2: A general D-BJT BiCMOS device.

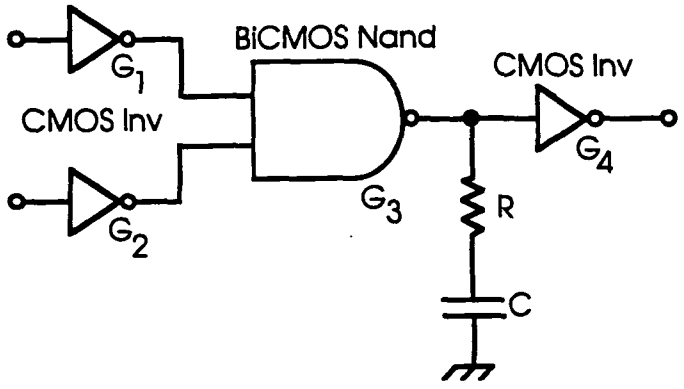
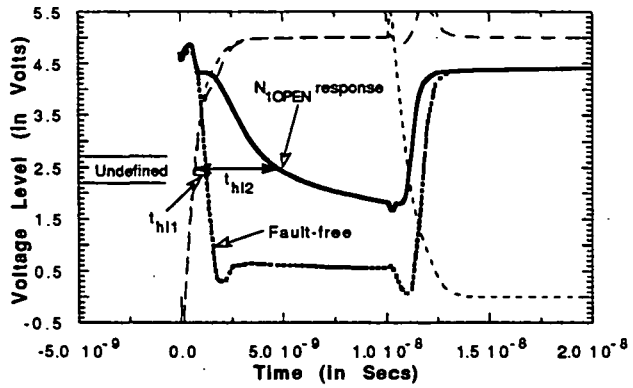
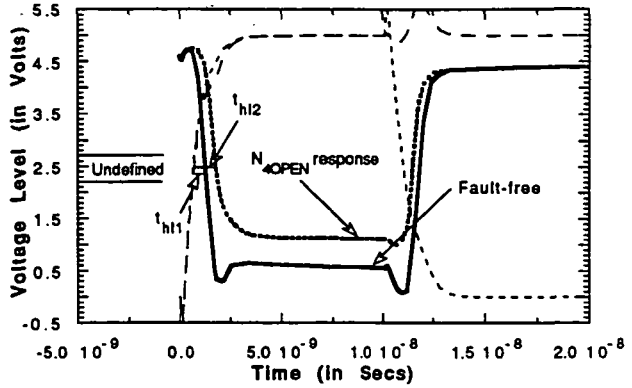
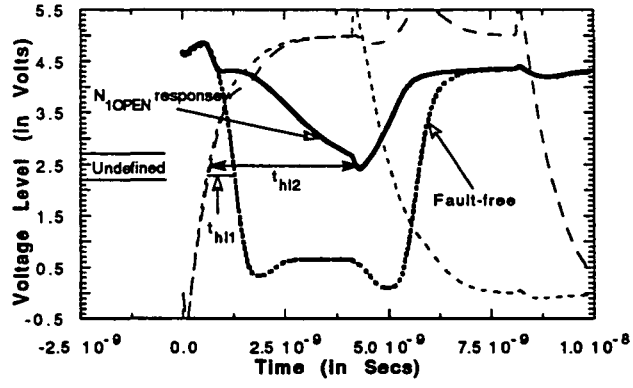
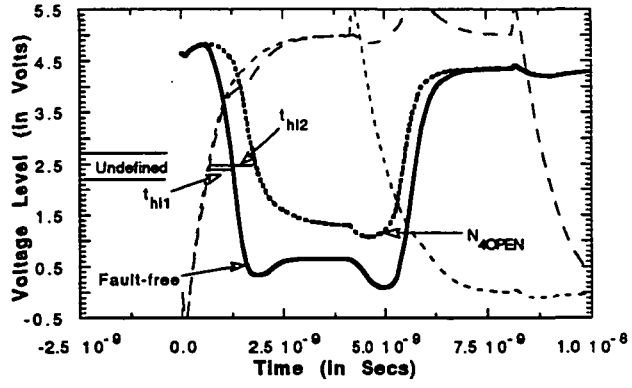


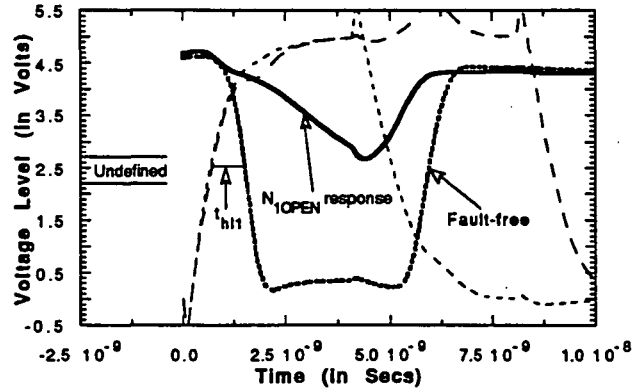
Figure 3: S-BJT BiCMOS NAND with CMOS inverter load and driver











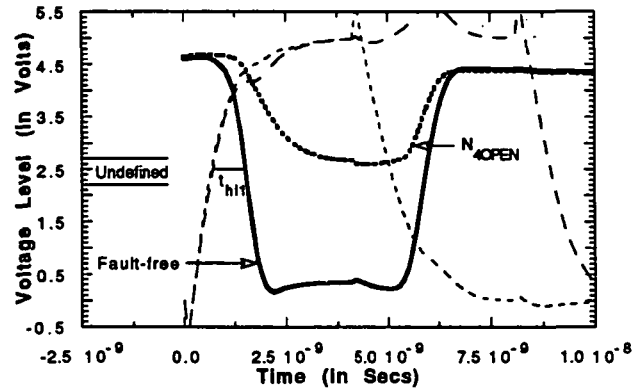
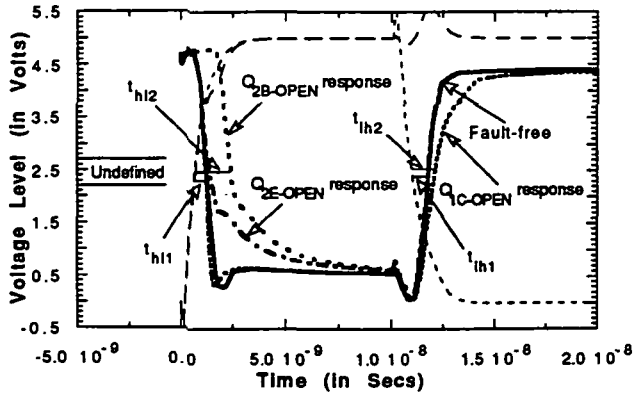
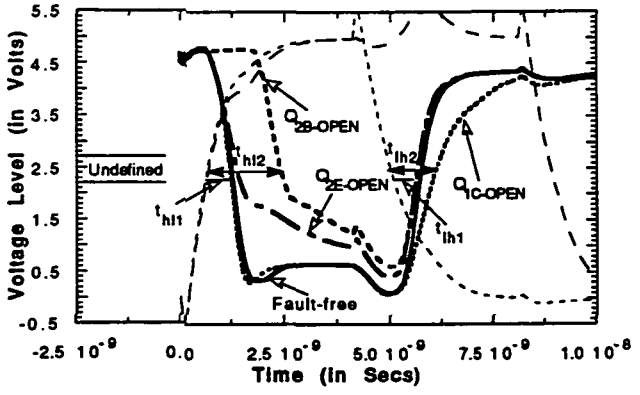


Figure 4: (a) BiCMOS response to N_1^{OPEN} with t_{pw}=10ns & One CMOS Load (b) t_{pw}=4ns & One CMOS Load (c) t_{pw}=4ns & RC Load.

Figure 5: (a) BiCMOS response to N_4^{OPEN} with t_{pw}=10ns & One CMOS Load (b) t_{pw}=4ns & One CMOS Load (c) t_{pw}=4ns & RC Load.





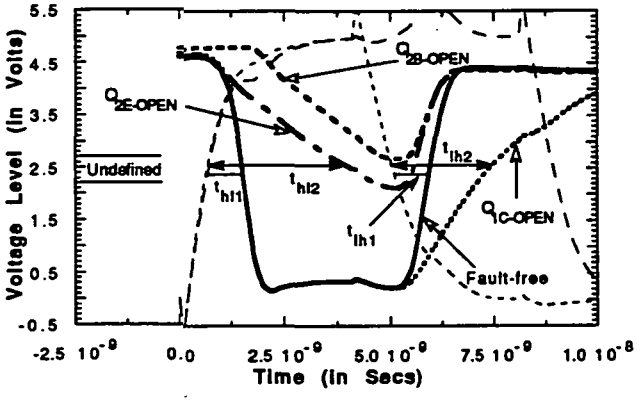
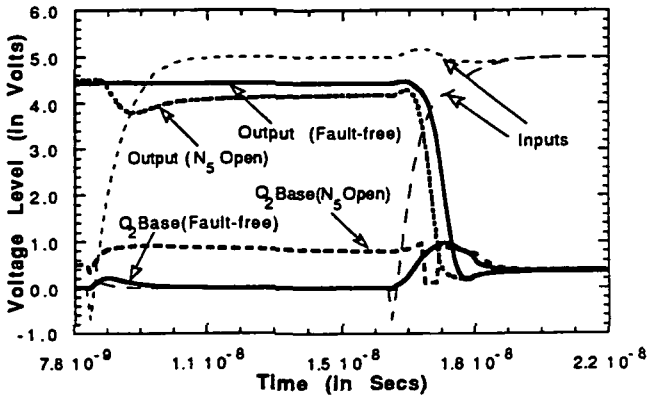


Figure 6: (a) BiCMOS response to $Q1_C^{OPEN}$ and $Q2_{BE}^{OPEN}$ with t_{pw}=10ns & One CMOS Load (b) t_{pw}=4ns & One CMOS Load (c) t_{pw}=4ns & RC Load.



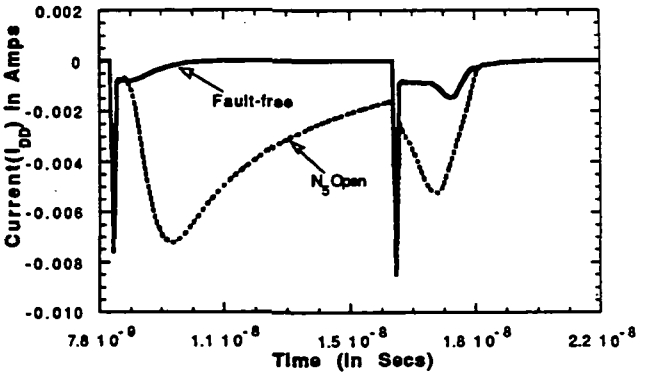


Figure 7: BiCMOS response to N_5^{OPEN} and Fault-free with RC Load (a) Voltage levels at BiCMOS output and Q_2 base (b) Plot illustrating enhanced dynamic I_{DD}.