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**MODULATION AND SYNCHRONIZATION
TECHNIQUE FOR MF-TDMA SYSTEM**

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Executive Summary

This report addresses modulation and synchronization techniques for a multi-frequency time-division multiple-access (MF-TDMA) system with onboard processing. The application of the MF-TDMA system is for VSAT-type terminals with mesh connectivity and destination-directed packet switching onboard the satellite. In such a system, short TDMA bursts are desirable in order to reduce onboard storage requirements and onboard processing delays. The short TDMA burst requirement directly translates into a low burst overhead requirement in order to keep the TDMA frame efficiency high. Since most of the burst overhead is associated with timing and carrier synchronization functions, this report addresses alternate methods of synchronization, and evaluates their impact on the overall system design.

The types of synchronization techniques analyzed are:

- asynchronous (conventional) TDMA synchronization, in which carrier phase and burst timing are derived from a preamble pattern,
- preambleless asynchronous TDMA, in which synchronization is achieved by storing and demodulating the received burst in two passes, where carrier and bit timing estimates are derived from the data in the first pass and then used for detection and demodulation in a second pass,
- bit synchronous timing with burst preamble, in which transmit timing is tightly controlled at the user terminal so that all bursts arrive at the satellite synchronized to onboard reference timing, and where the preamble pattern is only used for carrier recovery, and
- bit synchronous timing without a burst preamble, which is similar to bit synchronous timing with burst preamble, except that carrier phase estimation is performed on the burst data instead of a preamble pattern.

Among the above alternatives, the preambleless bit synchronous approach simplifies onboard multicarrier demultiplexing and demodulation design (about 2:1 reduction in mass and power), requires smaller onboard buffers, and provides better frame efficiency as well as lower onboard processing delay. These advantages are achieved at the expense of an additional requirement for tight user terminal transmit timing control, generally to within 5% of a symbol time from the onboard reference timing phase.

There are several techniques that can be used at the user terminal to achieve bit synchronous timing. These are classified according to the source of transmit timing used at the terminal, and the timing correction technique implemented to track the onboard reference timing. The user terminal timing source can be either an independent local clock or a phase-locked clock which is locked to the receive clock from the satellite.

Both sources of transmit timing require timing correction to compensate for clock drift, Doppler, and other sources of timing error. User terminal timing corrections are generally based on timing error measurements made on the satellite and relayed on the downlink to the user terminal. A less accurate timing correction technique which utilizes

precision ranging does not require onboard measurements, however it does not constitute a practical option for the TDMA system under consideration due to its low accuracy.

User terminal timing corrections may be implemented by using one of several devices, including a programmable phase shifter, a voltage controlled oscillator, a programmable delay line, and a digitally controlled oscillator. While all corrections are based on the onboard timing phase error measurements, the actual correction technique used may include making intermediate corrections between measurements, averaging multiple measurements, and Doppler / clock drift prediction based on the onboard measurements.

Keeping in mind the requirement of a low cost user terminal, the report examines alternate user terminal transmit timing sources and correction techniques for low cost implementation. The phase-locked clock approach with programmable phase shifter correction is identified as the better alternative. Analysis and computer simulations show that bit synchronous timing is achievable for bit rates of up to 10 Mbit per second (or higher) with proper selection of design parameters. The recommended modulation technique for bit synchronous timing is coherent QPSK with differential encoding for the uplink and coherent QPSK for the downlink. The cost impact of implementing bit synchronous timing on the user terminal is fairly low (a few hundred dollars) which is in keeping with the low-cost user-terminal requirement.

Table of Contents

1. Introduction	1
1.1 Purpose of the Study	2
1.2 Study Approach	3
2. Satellite System Architecture	5
3. Alternative Synchronization Approaches	8
3.1 Conventional TDMA Synchronization	9
3.2 Preambleless TDMA Synchronization	9
3.3 Bit Synchronous TDMA with Preamble	10
3.4 Preambleless Bit Synchronous TDMA	10
3.4.1 Bit Timing Accuracy	11
3.4.2 User Terminal Timing Control	11
3.4.3 Onboard Timing Measurements	13
3.5 Onboard Hardware Tradeoffs	13
3.6 Frame Efficiency Tradeoffs	14
3.7 Summary Comparisons	16
4. Impact on Onboard Demultiplexing and Demodulation	18
4.1 Onboard Demultiplexing	18
4.1.1 Demultiplexer Algorithm and Architecture	18
4.1.2 Cases Considered	22
4.1.3 Polyphase Demultiplexer and Interpolation Filter Complexity	23
4.1.4 Power and Mass Estimates	24
4.1.5 Example	24
4.2 Onboard Demodulation	25
4.2.1 Onboard Demodulator Operation	25
4.2.2 Demodulator comparisons	26
4.2.3 Mass and Power Estimates	27
4.3 Onboard Timing Error Measurement	27
4.3.1 Error Measurement Technique	28
4.3.2 Equation for Timing Measurement Error	28
4.4 Onboard Hardware Conclusions	30
5. Ground Terminal Timing Correction Techniques	31
5.1 Timing Issues	31
5.1.1 Ground Terminal Timing	32
5.1.2 Clock Correction Methods	32
5.2 Independent Clock Source	32
5.2.1 Independent Clock - Programmable Phase Shifter (IC-PPS)	34
5.2.2 Independent Clock - Voltage Controlled Oscillator (IC-VCO)	34

5.2.3	Independent Clock - Digitally Controlled Oscillator (IC-DCO)	36
5.2.4	Independent Clock - Programmable Delay Line (IC-PDL).....	37
5.3	Phase Locked Clock	37
5.3.1	Phase Locked Clock - Programmable Phase Sifter (PLC-PPS).....	38
5.2.2	Digitally Controlled Oscillator (DCO)	39
5.4	Open Loop Synchronization (OLS)	39
6.	Timing Accuracy	41
6.1	Acquisition and Synchronization Overview	41
6.2	Timing Error Analysis.....	43
6.2.1	General Model	43
6.2.2	Independent Clock (IC) Control Technique.....	44
6.2.2.1	IC Timing Analysis	45
6.2.2.2	IC Numerical Examples.....	48
6.2.2.4	IC Simulation Results	50
6.2.2.5	Stability Problem	52
6.2.2.6	Summary of IC Approach	53
6.2.3	Phase Locked Clock (PLC) Control Technique.....	53
6.2.3.1	PLC Timing Analysis.....	54
6.2.3.2	PLC Numerical Examples	56
6.2.3.3	PLC Parametric Analysis	57
6.2.3.4	PLC Simulation Results	59
6.2.3.5	Techniques for reducing phase error in PLC approach	61
6.2.3.5.1	Multiple Error Measurements in Correction Period	61
6.2.3.5.2	Doppler Correction	62
6.2.3.5.3	Parametric Analysis with Doppler Correction	64
6.2.3.5.4	Simulation Results with Multiple Measurements and Doppler Correction	65
6.2.3.6	Summary of PLC Approach	66
6.3	Summary of Timing Analysis.....	68
7.	Conclusions	69
8.	References.....	71

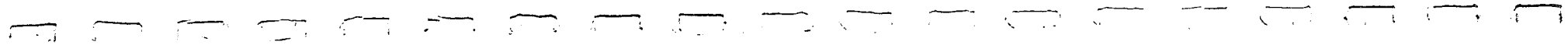
List of Figures

Figure 2.1	Network Architecture.....	5
Figure 2.2	Uplink and Downlink Frame Structure	6
Figure 3.1	Performance Degradation Caused by Symbol Timing Error	11
Figure 3.2	Bit Synchronous Concept	13
Figure 3.3	Bit Synchronous TDMA Frame	15
Figure 4.1	Illustration of uniform channelization	19
Figure 4.2	High level block diagram of polyphase filter.....	21
Figure 4.3	Block diagram of polyphase presummer	22
Figure 4.4	Timing Error Measurement Technique.....	28
Figure 5.1	Independent Clock Timing Corrections.....	33
Figure 5.2	Independent Clock with Programmable Phase Shifter (IC-PPS)	34
Figure 5.3	Example of Voltage Variable Phase Shifter Characteristics	35
Figure 5.4	Independent Clock with Voltage Controlled Oscillator (IC-VCO)	35
Figure 5.5	Example of Voltage Controlled Oscillator Characteristics.....	36
Figure 5.6	Independent Clock with Digitally Controlled Oscillator (IC-DCO).....	36
Figure 5.7	Independent Clock with Programmable Delay Line (IC-PDL)	37
Figure 5.8	Phase Locked Clock Timing Corrections.....	38
Figure 5.9	Phase-Locked Clock with Programmable Phase Shifter (PLC-PPS).....	39
Figure 5.10	Phase-Locked Clock with Digitally Controlled Oscillator (PLC-DCO).....	39
Figure 5.11	Clock Correction Based on Open Loop Synchronization	40
Figure 6.1	Acquisition and Synchronization Slot Allocation in LR-TDMA.....	42
Figure 6.2	General Clock Control Model for Bit Synchronous System	44
Figure 6.3	Timing Correction Procedure for IC	45
Figure 6.4	Linearized Clock Control Model	46
Figure 6.5	Optimal Clock Control Model with Various Timing Error Sources	47
Figure 6.6	IC-PPS Simulation Results	51
Figure 6.7	IC-VCO Simulation Results	51
Figure 6.8	IC-DCO Simulation Results	52
Figure 6.9	Illustration of Potential Stability Problem in IC techniques	53
Figure 6.10	Timing Correction Procedure for PLC	54
Figure 6.11	Analytical Model for PLC Timing Control	55

Figure 6.12	Phase Error (E3s) vs. Bit Rate (PLC-PPS, $T_c = 512$ ms).....	58
Figure 6.13	Phase Error (E3s) vs. Bit Rate (PLC-DCO, $T_c = 512$ ms).....	58
Figure 6.14	PLC-PPS Simulation Results	60
Figure 6.15	PLC-DCO Simulation Results	60
Figure 6.16	Effect of Averaging on Statistical Phase Error	61
Figure 6.17	Transmit and Receive Frame Time Difference Measurements	62
Figure 6.18	Linear Prediction Error for Doppler Correction	63
Figure 6.19	Parametric Analysis Results with Doppler Correction	64
Figure 6.20	Parametric Analysis Results with Doppler Correction	64
Figure 6.21	PLC-PPS Simulation Results with Multiple Measurements.....	65
Figure 6.22	PLC-PPS Simulation Results with Doppler Correction	66
Figure 6.23	PLC-PPS Simulation Results with Doppler Correction and Multiple Measurements	67

List of Tables

Table 2.1	Summary of System Parameters	7
Table 3.1	Degradation in SNR vs. Static Timing Error	12
Table 3.2	TDMA Frame Length Comparison	16
Table 3.3	TDMA Synchronization Summary Comparisons.....	17
Table 4.1	Demodulator Power and Mass Estimates	27
Table 4.2	System Mass and Power Comparisons	30
Table 6.1	IC Error Components and Statistical Characteristics	48
Table 6.2	Typical Timing Error Parameter values and Estimated Phase Errors	49
Table 6.3	Independent Clock Simulation Parameters.....	50
Table 6.4	PLC Error Components and Statistical Characteristics	55
Table 6.5	Typical Timing Error Parameter Values and Estimated Phase Errors	57
Table 6.6	Phase-Locked Clock Simulation Parameters	59
Table 6.7	Supportable Data Rates (PLC-PPS)	67



Section 1

Introduction

VSAT networks have traditionally been implemented using a star topology in which a large size hub earth station communicates with smaller size VSAT terminals, but with no direct communications between the VSAT terminals themselves. The hub earth station is needed to keep the transmit power requirements for the VSAT terminals low, and thus allow low cost implementations of these terminals. These star topology VSAT systems are generally adequate for low rate communications between a central site and remote stations, and are usually used for centralized data networks or one way distribution systems which require lower rate feedback channels on the return links. On the other hand, mesh VSAT networks which allow VSAT terminals to communicate with one another, would alleviate many of the restrictions that are inherent in star networks. However, mesh connectivity between small size terminals presents more of a technical challenge. With a conventional (bent-pipe) type satellite, mesh connectivity generally requires larger antennas and/or higher transmit power, which moves the size and cost of these terminals out of the realm of VSATs.

One approach to reducing the size and power requirements for mesh connectivity is to use onboard processing. Onboard regeneration in itself provides significant advantages in terms of the link requirements, however it becomes even more advantageous when used to interconnect hopping spot beams which afford higher receive gain and higher transmit power than traditional wide coverage beams.

Recognizing the need for low cost VSAT mesh connectivity in both scientific and commercial applications, NASA has performed a number of system studies which addressed this requirement [1-6]. The emerging system architecture [7] comprises a large number of low-cost VSAT terminals and an onboard processing hopping beam satellite architecture. In order to keep the cost of terminals down, low rate MF-TDMA carriers are used on the uplink to keep the power requirements low and hence the HPA/antenna size small. Multi-carrier demultiplexing and demodulation is performed onboard the satellite. An onboard information switching processor (ISP) switches the incoming data onto the destination downlink carriers. The downlink transmission format is high speed single carrier TDM which affords the highest utilization efficiency of the satellite power resources. The key to the economic viability of such a system is keeping the cost of the VSAT terminals low and distributing the cost of the space segment among a large number of users.

The switching functions of the ISP can be performed either on a packet or circuit switched basis, or a combination of the two. Packet switching seems to offer many potential advantages in terms of its flexibility in accommodating different types of traffic and its efficiency in utilizing space segment resources. Although circuit switching has not been ruled out, it is in the context of a destination directed packet switched ISP that the current system architecture framework is defined.

The combination of multi-frequency low rate TDMA on the uplink and fast packet switching onboard the satellite imposes a requirement for short frame length and hence

short data bursts. This requirement stems from the fact that onboard storage is generally at a premium and hence should be minimized, and that processing delays will be higher for longer frames. With short data bursts, frame efficiency becomes critical in that burst overhead should be kept as low as possible. Most of the overhead in a conventional TDMA system is associated with the burst preamble required to obtain timing and phase synchronization and to identify the start of the burst. By eliminating or reducing the burst preamble, frame efficiency can be substantially increased. However, alternate means of timing synchronization, carrier synchronization, and burst synchronization must be utilized, with timing synchronization being perhaps the most critical of these three functions in terms of hardware and computational requirements.

1.1 Purpose of the Study

The objectives of this study are to identify alternate timing synchronization techniques for the onboard demodulation of low-rate MF-TDMA carriers, and to select an optimal approach based on evaluation of the proposed techniques. The asynchronous timing approaches are more in keeping with traditional TDMA timing where variations in bit timing among different TDMA bursts are resolved by the onboard processor and the inclusion of adequate guard time between bursts to prevent collisions. The synchronous timing approaches rely on bit timing (or symbol timing) at the satellite to be synchronous among all bursts so that the onboard demultiplexer and demodulator subsystems do not have to resolve any timing variations. However, to achieve bit synchronous timing, the ground terminal transmit timing should be tightly controlled. This could entail making timing error measurements at the satellite which are relayed to the ground terminals, and implementing some means of timing error correction at the ground terminals.

The synchronous nature of the bursts in a bit synchronous system can eliminate the burst overhead associated with bit timing recovery in a conventional TDMA system. In a preambleless TDMA system, bit synchronous transmissions can greatly simplify onboard burst demodulation by eliminating the timing recovery and correction function which otherwise would have to be done on the data portion of the burst. This would allow shorter data bursts and consequently shorter TDMA frame durations. Hence, the advantages of the bit synchronous timing approach can be found in higher frame efficiency, shorter frame length which translates to lower onboard buffering requirements, and simpler onboard demodulation and demultiplexing.

The above advantages however are accompanied by potential drawbacks in terms of additional onboard processing functions for timing error measurement and timing acquisition/synchronization processing. Other drawbacks include the requirement to implement precision timing correction at the ground terminals which may have some impact on the complexity and cost of the ground terminals. Also, because of inherent residual onboard timing errors, there may be a slight performance degradation compared to conventional TDMA demodulation. Keeping in mind the requirement for a low cost VSAT terminal design, this study examines the trade-offs involved in adopting a bit synchronous system versus an asynchronous system, and having preambleless burst operation versus a full preamble burst structure.

The study emphasis centers on timing issues which have the most impact on onboard demodulation, and on reducing the overhead and hence increasing the frame utilization efficiency through the use of a shortened burst preambles or through the elimination of burst preambles altogether.

The objectives of the study are to:

1. study the system impact on the space and ground segments of synchronous and asynchronous MF-TDMA comparing access techniques and implementation mechanisms, and choose either a synchronous or asynchronous approach based on their merits; and
2. develop and analyze acquisition, synchronization, and tracking methodologies for MF-TDMA, recommend suitable modulation formats, analyze performance and determine the limitations on the maximum practical burst rate that can be supported by an MF-TDMA uplink.

1.2 Study Approach

This study is organized into the following sections:

Section 1 presents an introductory overview of the study objectives and approach.

Section 2 provides a description of the satellite system architecture which forms the background for the study. It provides the system parameters such as beam coverages, frequency bands, access schemes, onboard routing, bit/burst rates, FEC coding, frame structure, burst format, etc.

Section 3 examines alternative timing synchronization approaches for their feasibility, system impact, and benefits. It describes the general concept and major design issues for each approach. This section provides a high level and mainly qualitative description which would allow a general selection of a preferred synchronization approach. The first four subsections correspond to the four alternative synchronization approaches being considered:

- Conventional TDMA system
- Preambleless TDMA system
- Bit synchronous TDMA with preamble system
- Preambleless bit synchronous TDMA system

A description of each approach is presented including a general concept, acquisition and synchronization technique, frame format, benefits, system impact, feasibility, and other design issues. The following subsections include a high level tradeoff analysis which addresses tradeoff issues such as frame efficiency, potential impact on onboard hardware, and potential impact on ground terminal design. This section concludes with a

comparison summary and a recommended approach to timing synchronization within the proposed system architecture.

Section 4 addresses the specific impact of the selected approach on the onboard demultiplexing and demodulation. It also addresses onboard timing error measurement techniques which would be applicable in a bit synchronous system, and examines their impact on the onboard hardware.

Section 5 examines ground terminal timing derivation and correction techniques, including sources of ground terminal clock, clock correction options, and open loop synchronization.

Section 6 begins with an overview of acquisition and synchronization methods for the selected technique. It then provides analysis of timing accuracy, supplemented by computer simulation results, for each of the timing correction methods being considered. Comparisons are made between the different timing correction methods in terms of supportable bit rates. A recommended timing correction method is selected based on the comparisons.

Section 7 provides the conclusions of the study.

Section 8 includes a list of references.

Section 2

Satellite System Architecture

The proposed architecture framework for this study is described in [7]. The space segment consists of up to four onboard processing geostationary satellites interconnected by inter-satellite links (ISLs). Coverage is provided through eight fixed uplink spot beams, and eight hopping downlink spot beams. Each downlink beam hops among eight dwell locations. Figure 2.1 shows an illustration of the system architecture.

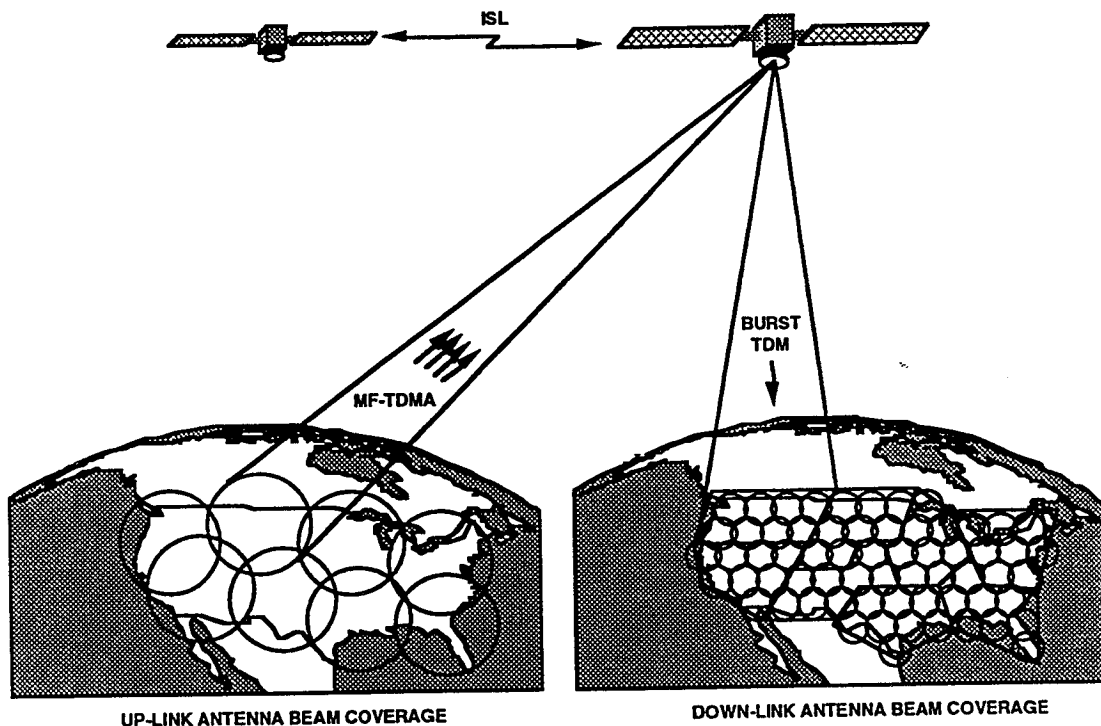


Figure 2.1: Network Architecture

The ground segments is comprised of VSAT type terminals using low rate TDMA on the uplink and TDM on the downlink. The uplink TDMA baseline carrier information rate is 2.048 Mbps, which can accommodate up to thirty-two 64 Kbps channels. There are up to thirty-two LR-TDMA carriers in each uplink beam. The downlink TDM information rate is 160 Mbps.

Associated with each uplink beam is a multi-carrier demultiplexer and demodulator/decoder capable of handling up to thirty-two 2.048 Mbps carriers. Associated with each downlink beam is an encoder and a high speed burst modulator. Coherent QPSK is used on both the uplink and downlink due to power efficiency considerations and relatively low implementation complexity. A high throughput information switching processor (ISP) onboard the satellite provides switching and interconnection between the uplink beams and downlink beams. Although both circuit

and packet switching are being considered, the current architecture employs a destination-directed fast packet switch design.

The current baseline packet format consists of fixed length packets containing 2048 bits. Each packet is further divided into 16 subpackets, 128 bits each. The first subpacket is the header subpacket which carries the packet routing information. The remaining fifteen subpackets carry the actual information payload along with some parity check overhead.

In the current design, a packet is transmitted on the uplink in a 64 Kbps slot within a single TDMA frame. The TDMA frame length is 32 ms, which is further divided into sixteen 2-ms subframes. Each subframe contains one 128-bit subpacket per channel, up to thirty-two subchannels. The first subframe within a frame carries the header subpackets for the respective 32 channels which establish the onboard routing configuration for that frame. The remaining fifteen subframes then carry the information subpackets.

The downlink format consists of a 32-ms TDM frame which is divided among eight downlink dwell time slots. The minimum dwell time is 80 microseconds which corresponds to a minimum of 100 packets per dwell. A reference burst is included in each frame for each dwell. The reference bursts could be transmitted either at the beginning of the frame or at the beginning of each dwell in the frame.

The uplink and downlink frame structure is shown in Figure 2.2. Table 2.1 provides a summary of the system parameters in the current design.

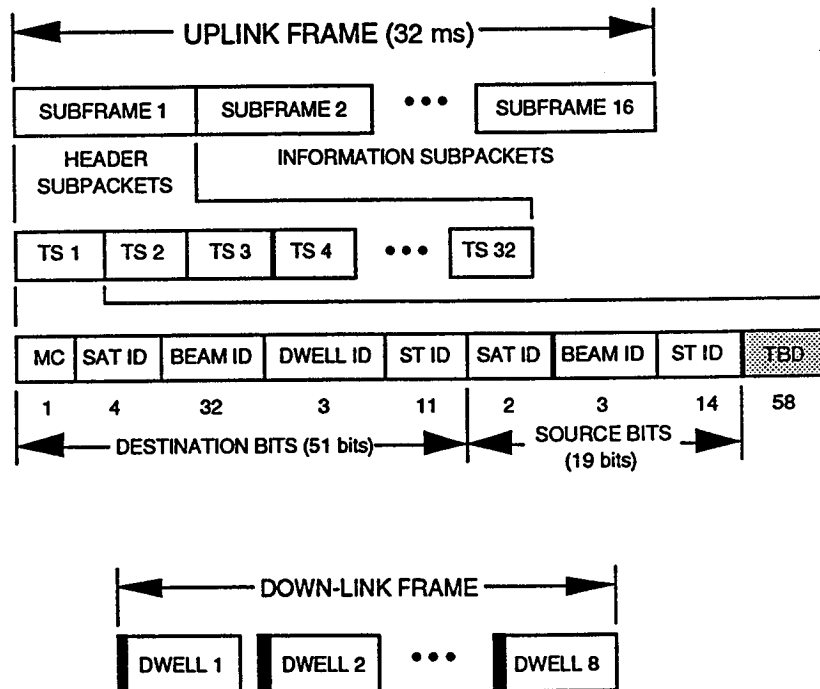
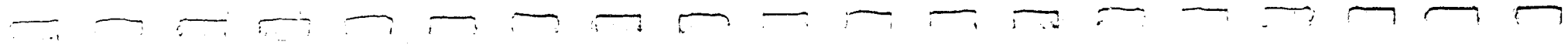


Figure 2.2: Uplink and Downlink Frame Structure

Table 2.1: Summary of System Parameters

number of uplink beams	8	beams
uplink format	MF-TDMA	
uplink frequency	30	GHz
uplink frame	32	ms
uplink sub frame	2	ms
TDMA carriers per uplink beam	32	carriers
uplink carrier rate	2.048	Mbps
uplink capacity per beam	65.536	Mbps
total uplink capacity	524.288	Mbps
number of downlink beams	8	beams
number of dwells per downlink beam	8	dwells
downlink format	TDM	
downlink frequency	20	GHz
downlink carrier rate	160	Mbps
available downlink capacity	1280	Mbps
minimum dwell time	80	microsecs



Section 3

Alternative Synchronization Approaches

Coherent demodulation of MF-TDMA carriers onboard the satellite requires synchronization of carrier phase and symbol timing between the received signals and the onboard reference. Because of the TDMA nature of the uplink signals in which several terminals time-share the TDMA frame, synchronization is required for each terminal transmission. There are a number of approaches to matching the carrier and timing references to the received burst timing and carrier. These approaches can be categorized under one of the following:

- conventional TDMA with preamble/ unique word (UW), which would allow derivation of correct burst timing from a preamble pattern
- conventional TDMA without preamble, which would involve storing and demodulating the received burst in two passes, with interpolation of bit timing
- bit synchronous TDMA with burst preamble, where the preamble pattern is only used to derive the carrier phase
- bit synchronous TDMA without burst preamble, with carrier phase estimation based on the received burst data

The advantages of a bit synchronous approach is that it simplifies the demodulation and demultiplexing onboard the satellite, and allows for a shorter (possibly zero-length) preamble. A short preamble increases the TDMA frame efficiency, especially for short data bursts. Short data bursts are desirable in order to keep the TDMA frame length short and hence minimize onboard storage and processing delay. The disadvantage of a bit-synchronous system is that it adds some complexity to the ground segment.

The following sections describe each of the four approaches to TDMA synchronization outlined above. All four approaches are based on burst synchronization in which carrier and timing estimation is performed on each burst individually. Continuous synchronization techniques in which carrier phase and symbol timing estimates are stored and tracked from one frame to the next are not considered to be feasible due to the following reasons:

- a. there may be significant changes in carrier phase and bit timing from one frame to the next so that timing and phase coherence is not possible; or
- b. earth stations do not necessarily transmit successive bursts in the same time slot and at the same carrier frequency.

3.1 Conventional TDMA Synchronization

The first alternative considered in this study is a conventional TDMA approach in which a preamble pattern is used to perform carrier recovery and bit timing recovery over the preamble portion of the received burst. The preamble consists of a carrier and bit timing recovery (CBR) pattern which generally includes an alternating bit pattern, followed by a unique word pattern which is used for deriving the start of the data portion of a burst. Because burst timing may vary from one burst in a frame to the next, a guard time must be allocated between bursts to prevent inter burst interference.

The onboard demodulator uses the CBR pattern to establish carrier phase and bit timing estimates. It uses the unique word pattern to identify the start of the data portion in the burst and to resolve any phase ambiguity in the carrier phase estimate. Once these estimates are calculated, they can be used to demodulate the information portion of the burst or to initialize a digital phase lock loop which can track the phase variations over the length of the burst. In general, if the frequency offsets between the received carrier and the onboard reference are large enough to cause significant variations in the phase over the length of the burst then some kind of phase tracking mechanism must be used. However, if the frequency offsets are small enough, then the phase estimates which are determined over the preamble can be used to demodulate the entire burst.

A conventional TDMA approach usually utilizes QPSK modulation without any need for differential encoding since the unique word pattern is used to resolve phase ambiguity. A typical value of the preamble length is 96 symbols. Guard time between bursts will depend on the accuracy of the user terminal clocks, and is generally a few symbols long.

3.2 Preambleless TDMA Synchronization

In this approach, the earth station bursts are not synchronized with the satellite clock, however no CBR pattern is included in the TDMA burst. Carrier and clock phase estimates are derived from the received burst data patterns. This is usually done using a two pass approach in which burst data is stored while it is used to obtain the bit timing and phase estimates, then the recovered estimates are used to demodulate the stored data. While this approach eliminates the preamble overhead, its shortfall is that it requires a relatively long data sequence to derive a reliable timing estimate due to the so called pattern noise. This imposes a limit on how short a data burst can be, and requires enough additional onboard storage for performing the two pass demodulation.

Bit timing estimates can be derived from the received data independently of the carrier phase by using the algorithm outlined in [8]. Carrier phase can be derived from the data using a nonlinear phase estimation algorithm [9] if bit timing is known. The phase estimation algorithm can generally yield reliable estimates over a few symbols provided there are no significantly large frequency offsets .

Due to the absence of a preamble pattern to resolve phase ambiguity, this alternative will generally utilize differentially encoded QPSK. DQPSK exhibits twice the

bit error rate of QPSK, however the doubling in the bit error rate translates to only a slight degradation in the required signal to noise ratio.

As with the conventional TDMA approach, this approach will require a guard time between consecutive bursts to absorb any differences in burst timing between user terminals.

3.3 Bit Synchronous TDMA with Preamble

In bit synchronous TDMA, system timing is maintained so that all transmissions arrive at the satellite synchronized to the same clock. This symbol synchronous system also allows frame synchronization and burst synchronization, thus eliminating the need for guard time between bursts and eliminating the requirement for a unique word pattern to identify the start of the burst. A description of the overall concept of bit synchronous operation is given in the following subsection.

If desired, a carrier synchronization pattern can be used to obtain a carrier phase estimate, as in the conventional TDMA system. However, the preamble length will generally be less than it would be in an asynchronous system since reliable carrier phase estimation requirements are generally less stringent than the bit timing estimation requirements.

The preferred modulation format for this alternative is coherent QPSK. Because burst timing is known, the alternating pattern used for carrier recovery can also be used for phase ambiguity resolution so there will be no need for differential encoding.

3.4 Preambleless Bit Synchronous TDMA

In bit synchronous TDMA, bit timing is maintained by controlling the transmit terminal timing in such a way as to have all transmissions arrive at the satellite in a bit synchronous fashion. This implies that some form of bit timing adjustment must be implemented at the transmit terminal based on the difference in bit timing at the satellite between the onboard clock and the received burst.

User terminal clock correction is generally done by making bit timing error measurements onboard the satellite and relaying those measurements back to the transmit terminal. The user terminal implements some form of local clock correction based on the received feedback from the satellite. The feedback information from the satellite can be either an early / late type of signal or could include more information on the desired value of timing correction. Other methods of ensuring bit synchronous timing at the satellite include precision ranging or self monitoring of the received signals, however these methods will generally require some guard time between bursts to absorb any timing uncertainties and are only practical for very low rate transmissions.

With bit synchronous operation, carrier phase estimation can be performed on the TDMA data burst using the Viterbi and Viterbi algorithm [9] which is capable of producing fairly reliable phase estimates based on a small number of symbols in the received data pattern. This algorithm has been shown to be very well suited for use in a

low-rate TDMA (LR-TDMA) bit synchronous system [10] similar to the one being considered in this study.

3.4.1 Bit Timing Accuracy

Burst timing in a bit synchronous system must be accurate to within a small fraction of a symbol time. To get an idea of the performance sensitivity to bit timing inaccuracies, a simplified analysis of non-filtered coherent QPSK is performed as shown in Figure 3.1. Using an integrate-and-dump filter on a rectangular pulse, the performance degradation is given by

$$\frac{E'_b}{N_o} = \frac{P_b(T_s - 2\Delta t)}{N_o} = \left(1 - \frac{2\Delta t}{T_s}\right) \frac{E_b}{N_o}$$

Table 3.1 shows the expected degradation in performance based on the above equation for (non-filtered) coherent QPSK as a function of static bit timing error. From Table 3.1, it is evident that a 5% (or 1/20) timing error for example would provide adequate performance within 0.5 dB from theoretical. In order to achieve a required bit timing accuracy, a capability to accurately measure bit timing errors on board the satellite is required, as well as a capability to accurately correct the transmit terminal timing to within the required accuracy.

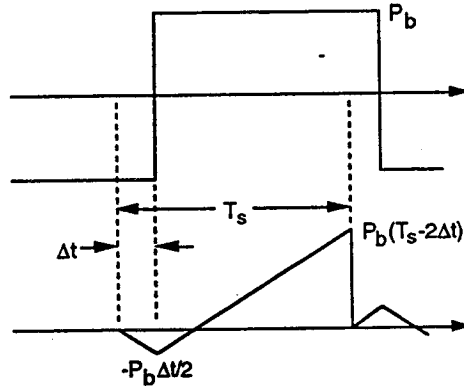


Figure 3.1: Performance Degradation Caused by Symbol Timing Error

3.4.2 User Terminal Timing Control

In order to achieve the required timing accuracy, two steps are required at the user terminal. The first step involves initial timing acquisition which is performed by sending an acquisition burst in a specified time slot (channel) on an assigned TDMA carrier. The acquisition burst contains a preamble pattern to allow precise measurement of symbol timing onboard the satellite. Due to the initial timing uncertainty, the acquisition time slot also includes a guard time long enough to absorb the timing uncertainty. Based on the acquisition burst timing measurement a timing correction signal is sent back from the onboard processor to the ground terminal specifying the timing offset in symbols as

Table 3.1: Degradation in SNR vs. Static Timing Error

Phase Error $\Delta T/T_s$	Degradation (dB)
0%	0.00
1%	0.09
2%	0.18
3%	0.27
4%	0.36
5%	0.46
6%	0.56
7%	0.66
8%	0.76
9%	0.86
10%	0.97

well as in fractions of a symbol. The ground terminal corrects its timing and sends another acquisition burst. This process is repeated until the correct timing (to within a specified tolerance) is reached and acknowledged by the onboard processor. Once a terminal has acquired the correct bit timing, synchronization is maintained by performing periodic corrections in fractions of a symbol, based on bit timing error measurements. In general, these measurements are performed by the onboard processor on a special synchronization burst which is transmitted periodically by the ground terminal. Figure 3.2 illustrates the concept of bit synchronous timing corrections using onboard timing error measurements.

As mentioned above, bit timing measurements onboard the satellite can be made on a special synchronization burst that each transmit terminal sends in turn in a specified synchronization time slot in the TDMA frame. The frequency of these measurements, and hence the frequency of transmitting the synchronization burst for each terminal depends on several factors such as the stability of the onboard and terminal clocks, the satellite motion Doppler, and other factors such as the method used to derive the ground terminal timing. Section 6 of this report, which deals with timing analysis for bit synchronous system, addresses the frequency with which these corrections should be made. It should be noted here however that these are fine timing adjustments that are made after initial course timing acquisition is made, including burst timing and symbol timing acquisition.

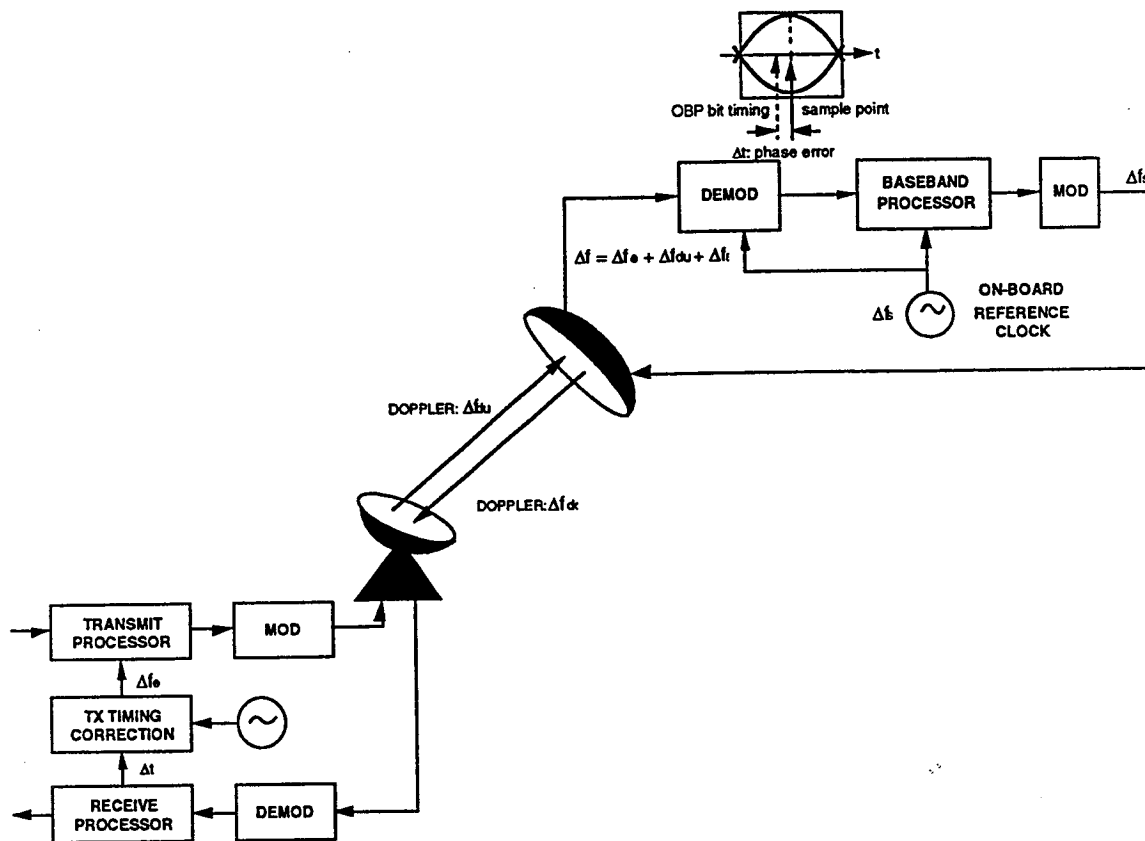


Figure 3.2: Bit Synchronous Concept

3.4.3 Onboard Timing Measurements

To allow accurate bit timing measurements onboard the satellite, the timing synchronization (or timing maintenance) burst will consist of a special sequence consisting of alternating pairs of identical symbols. This in effect halves the received symbol rate for the synchronization burst, which effectively doubles the onboard sampling rate. With the higher sampling rate, accurate timing error measurements are made by an onboard timing error measurement processor. A more detailed analysis of the timing error measurement technique will be given in subsection 4.3.

3.5 Onboard Hardware Tradeoffs

The advantages of using bit synchronous TDMA in terms of onboard processing is derived mainly in the demultiplexing and demodulation process, especially for multi-carrier demultiplexing/demodulation.

From an onboard demodulation standpoint, when symbol timing is known on a burst by burst basis, the demodulator could operate at the symbol rate. Whereas in a conventional TDMA system, the demodulator would operate at or above the Nyquist sampling rate of the demultiplexed carriers. This is at best higher than the symbol rate

by the rolloff factor of the pulse shaping filter, which would generally be from thirty to fifty percent. It is not uncommon to have the demodulator operating a twice the symbol rate, which is a factor of one-hundred percent higher than the symbol rate. In a bit synchronous system where the sampling rate could be at the symbol rate, the sampling rate reduction translates into savings in mass and/or power.

Another advantage of bit synchronous operation in terms of onboard demodulation is the elimination of the bit timing recovery process. In conventional (asynchronous) TDMA, bit timing recovery has to be performed on the receive burst, which entails either the addition of a bit timing recovery pattern to the preamble, or storing the burst (or part of the burst) and deriving a bit timing estimate from the stored samples before doing the demodulation in a second pass. Both approaches may be wasteful of resources. The first approach requires a bit timing recovery pattern which increases the burst preamble overhead. The second approach involves storing enough data to allow reliable estimation of the received bit timing. Since bit timing is usually derived from the zero crossing of the received waveform, and since for filtered QPSK the zero crossings depend on the pattern noise (ISI) at the zero crossing instant which is not null even in the absence of thermal noise, a reliable estimate may require a long averaging interval over which many zero crossings are averaged. This added processing also translates into onboard mass and power increases.

Related to the increase in processing requirements and burst overhead in a conventional (asynchronous) TDMA system is the correction of bit timing once an estimate of the bit timing is made. This involves an interpolation filter for the received samples which is used to interpolate the sample value of the received signal at the sampling instant. An alternative for a system with a long bit timing recovery pattern is to adjust the sampling point over the data portion of the burst based on the bit timing estimate derived during the bit timing preamble pattern. Both approaches involve added complexity and reduced flexibility, especially in the implementation of an onboard multi-carrier demodulator.

Finally, multicarrier demultiplexing can be made simpler when only a single sample per symbol is required at the output of the demultiplexer (as in a bit synchronous operation). This also translates to mass and power savings over conventional TDMA.

Section 4 of this report deals specifically with the impact of bit synchronous operation on the onboard hardware, including mass and power estimates and comparisons.

3.6 Frame Efficiency Tradeoffs

The elimination of burst preamble in a bit synchronous system results in high frame efficiency which is crucial for short burst length. From another viewpoint, elimination of burst preamble allows much shorter bursts for a given frame efficiency. Figure 3.3 illustrates a bit synchronous TDMA frame and compares the required burst overhead with that of conventional TDMA bursts.

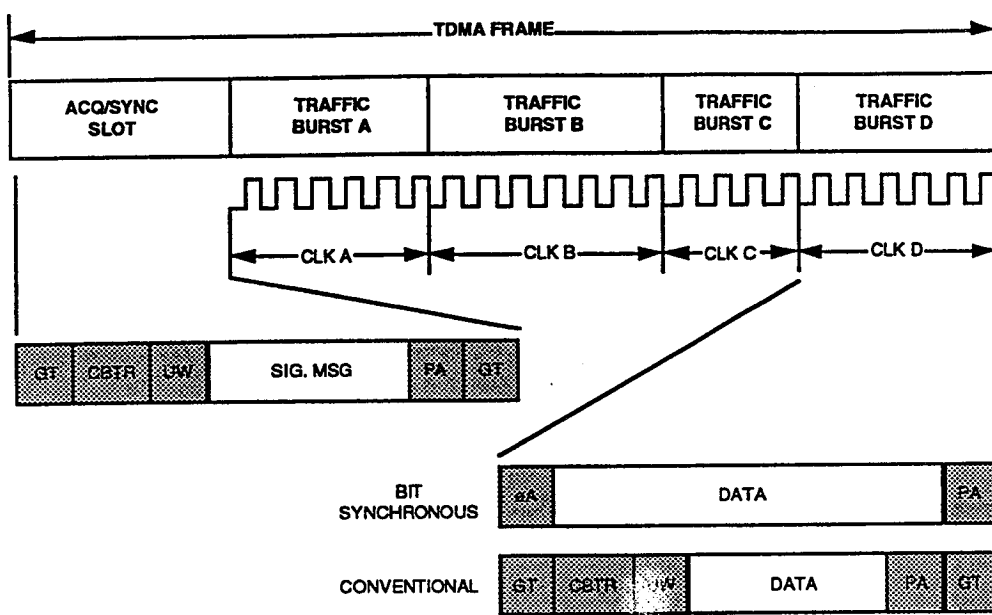


Figure 3.3: Bit Synchronous TDMA Frame

A quantitative comparison between the bit synchronous TDMA approach and the conventional TDMA approach is shown in Table 3.2. In this comparison, frame length is calculated based on the required frame efficiency for a given number of bursts per frame. The results show the sizable difference in the required frame length between the conventional TDMA approach and the bit synchronous approach.

The tradeoffs given in Table 3.2 focus on the required TDMA frame length for a given frame efficiency. In the current system design however, the frame length is fixed at 2 ms (subframe duration) with a subburst length of 128 symbols. In such a system, the preamble length of 96 symbols assumed in Table 3.2 plus all other overhead terms included in the comparison, would result in a frame efficiency which is less than 50 %. Hence, the elimination of burst preamble in the current system design is even more critical in terms of frame efficiency compared to the cases considered in Table 3.2.

Table 3.2: TDMA Frame Length Comparison

Transmission:	QPSK	UW:	24 sym
Information Rate:	2.048 Mbps	Post Amble:	8 sym
Acquisition Window:	80 μ s	Acq/Synch:	128 sym
Guard Time:	8 sym	SCPB Header:	40 sym
CBTR:	96 sym		

	Frame Effic.	Conventional TDMA					Single Channel Per Burst				
		No. of Bursts/Frame					No. of Bursts/Frame				
		20	40	60	80	100	20	40	60	80	100
Non-Bit Sync. Frame Length (ms)	70%	2.5	4.8	7.1	9.3	11.6	3.2	6.2	9.1	12.0	15.0
	75%	3.0	5.8	8.5	11.2	13.9	3.9	7.4	10.9	14.4	18.0
	80%	3.8	7.2	10.6	14.0	17.4	4.9	9.3	13.7	18.1	22.5
	85%	5.1	9.6	14.1	18.7	23.2	6.5	12.3	18.2	24.1	29.9
	90%	7.6	14.4	21.2	28.0	34.8	9.7	18.5	27.3	36.1	44.9
	95%	15.2	28.8	42.4	56.0	69.6	19.4	37.0	54.6	72.2	89.8
Bit Sync TDMA Frame Length (ms)	70%	0.4	0.5	0.7	0.8	0.9	1.1	1.9	2.7	3.5	4.3
	75%	0.5	0.6	0.8	1.0	1.1	1.3	2.3	3.2	4.2	5.2
	80%	0.6	0.8	1.0	1.2	1.4	1.7	2.9	4.1	5.3	6.5
	85%	0.8	1.1	1.3	1.6	1.9	2.2	3.8	5.4	7.0	8.6
	90%	1.2	1.6	2.0	2.4	2.8	3.3	5.7	8.1	10.5	12.9
	95%	2.4	3.2	4.0	4.8	5.6	6.6	11.4	16.2	21.0	25.8
Ratio of Frame Length		6.3	9.0	10.6	11.7	12.4	2.9	3.2	3.4	3.4	3.5

3.7 Summary Comparisons

In conclusion, Table 3.3 summarizes the salient features of each of the four approaches to TDMA synchronization described above. In Table 3.3, the term 'conventional TDMA' is used to refer to a non-bit synchronous TDMA system.

Based on the comparisons in Table 3.3, the bit synchronous approach to TDMA synchronization is selected for further study. Further evaluation of the impact of this approach on onboard hardware will be given in the next section.

Table 3.3: TDMA Synchronization Summary Comparisons

	option A Conventional TDMA (with Preamble)	option B Conventional TDMA (no Preamble)	option C Bit Synchronous TDMA (with Preamble)	option D Bit Synchronous TDMA (no Preamble)
preamble overhead	yes	no	yes (less)	no
guard time overhead	yes	yes	no	no
timing recovery required	yes	yes	no	no
tight ground timing control	no	no	yes	yes
short bursts possible	no (limited by ratio of data to overhead)	no (limited by data symbols required for timing recovery)	yes (although still limited by ratio of data to preamble overhead)	yes
onboard hardware complexity	more complex	most complex	simplest	simpler
added ground terminal complexity	none	none	some	some

Section 4

Impact on Onboard Demultiplexing and Demodulation

This section addresses the impact on onboard hardware of each of the TDMA synchronization options presented in section 3. Qualitative and quantitative comparisons of mass, power, and complexity, are made between the four options considered. The section also addresses onboard timing error measurements which is relevant for bit synchronous systems.

4.1 Onboard Demultiplexing

Onboard demultiplexing complexity is affected by several factors which may differ between bit synchronous and asynchronous TDMA. These include the bandwidth to symbol rate ratio, the number of samples per symbol required at the demultiplexer output, and the interpolation requirement following demultiplexing to obtain samples at the correct time instant.

In order to obtain meaningful comparisons between the two approaches, a demultiplexer algorithm and general architecture is first presented. Based on the proposed architecture, several cases which are applicable to bit synchronous and conventional TDMA are considered. Demultiplexer and interpolation filter complexity is addressed and mass and power estimates are then obtained for representative cases.

4.1.1 Demultiplexer Algorithm and Architecture

Demultiplexing uniformly loaded frequency bands, as in a MF-TDMA system, is considerably simpler than demultiplexing a flexible region. Indeed, it is well known that for demultiplexing uniform bands the approach known as polyphase is the least computationally intensive, and hence the preferred choice [11]. This approach is similar to that used in digital transmultiplexers where a group of frequency-division multiplexed (FDM) channels are transformed to time-division multiplexed (TDM) channels (and vice versa). The similarity lies in the signal processing techniques used to perform the frequency demultiplexing. COMSAT is thoroughly familiar with all the details of this approach, having designed and built a 60-channel polyphase transmultiplexer [12].

The polyphase approach takes full advantage of the fact that the different selective bandpass filters needed for the demultiplexing are equally spaced frequency replicas of a baseband prototype. Thus, this approach is ideally suited to applications where all carriers have the same allocated bandwidth B . Figure 4.1 illustrates the various bandpass filters needed to demultiplex a uniformly loaded band as exact replicas of the baseband prototype H_0 . (H will be used to denote a filter's frequency response, and h will denote its impulse response).

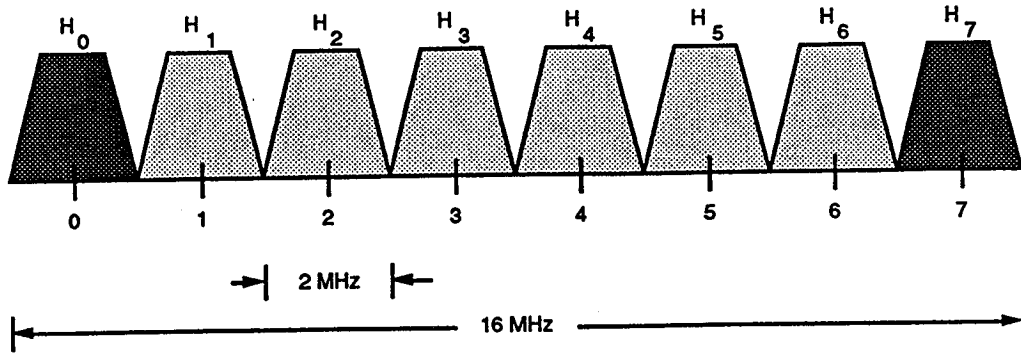


Figure 4.1: Illustration of uniform channelization

From Figure 4.1 it is clear that the frequency response of filter k is related to the baseband prototype's response by

$$H_k(f) = H_0(f - kB) \quad k = 0, \dots, N-1$$

Therefore

$$\begin{aligned} h_k(n) &= h_0(n) e^{-j2\pi k B n T_s} \\ &= h_0(n) e^{-j2\pi k n / N} \end{aligned}$$

where:

T_s is the sampling interval,

f_s is the sampling frequency, and

N is the total number of carriers (including guard bands)

A typical case may be:

$$f_s = 16 \text{ MHz}$$

$$B = 2 \text{ MHz}$$

$$N = 8$$

After filtering, carrier k is given by

$$y_k(n) = x(n) * h_k(n)$$

where $x(n)$ is the composite frequency-multiplexed signal and $*$ denotes convolution. Thus,

$$y_k(n) = \sum_{m=0}^{L-1} x(n-m) h_k(m)$$

Where L is the number of filter taps. Substituting for h_k gives

$$y_k(n) = \sum_{m=0}^{L-1} x(n-m) h_o(m) e^{-j2\pi km/N}$$

For the square root raised cosine filters, the impulse response must be truncated after an appropriate number of symbols. Computer simulations and actual measurements at COMSAT Laboratories have shown that negligible degradation results when the extent of the impulse response is limited to five symbols in the 50-percent rolloff case. Therefore, the number of filter taps, L , is given by

$$L = 5 \frac{T}{T_s} = 5T \cdot N \cdot B$$

where T is the symbol duration; thus,

$$L = 7.5 N$$

To simplify the implementation, the slightly larger value of $8N$ will be taken for L . By writing

$$L = N \cdot N_s$$

it follows that

$$N_s = 8$$

Substituting for L gives

$$y_k(n) = \sum_{m=0}^{(N \cdot N_s)-1} x(n-m) h_o(m) e^{-j2\pi km/N}$$

To reduce the above expression for $y_k(n)$ to a form involving a discrete Fourier transform (and hence use the efficient FFT algorithm), the index m is written as

$$\begin{aligned} m = N \cdot i + r & \quad i = 0, \dots, N_s - 1 \\ & \quad r = 0, \dots, N - 1 \end{aligned}$$

Therefore,

$$y_k(n) = \sum_{i=0}^{N_s-1} \sum_{r=0}^{N-1} x(n - N \cdot i - r) h_o(N \cdot i + r) \cdot e^{-j2\pi kr/N}$$

where use was made of the identity

$$e^{-j2\pi kN \cdot i/N} = 1$$

Interchanging the order of summations gives,

$$y_k(n) = \sum_{r=0}^{N_s-1} e^{-j2\pi kr/N} \left[\sum_{i=0}^{N_s-1} x(n - N \cdot i - r) h_o(N \cdot i + r) \right]$$

Defining

$$z_n(r) = \sum_{i=0}^{N_s-1} x(n - N \cdot i - r) h_o(N \cdot i + r)$$

gives

$$y_k(n) = \sum_{r=0}^{N-1} e^{-j2\pi kr/N} z_n(r)$$

This last expression simply says that $y_k(n)$ is the N -point discrete Fourier transform of $z_n(r)$. The relation between the quantities x , y , and z is illustrated in Figure 4.2.

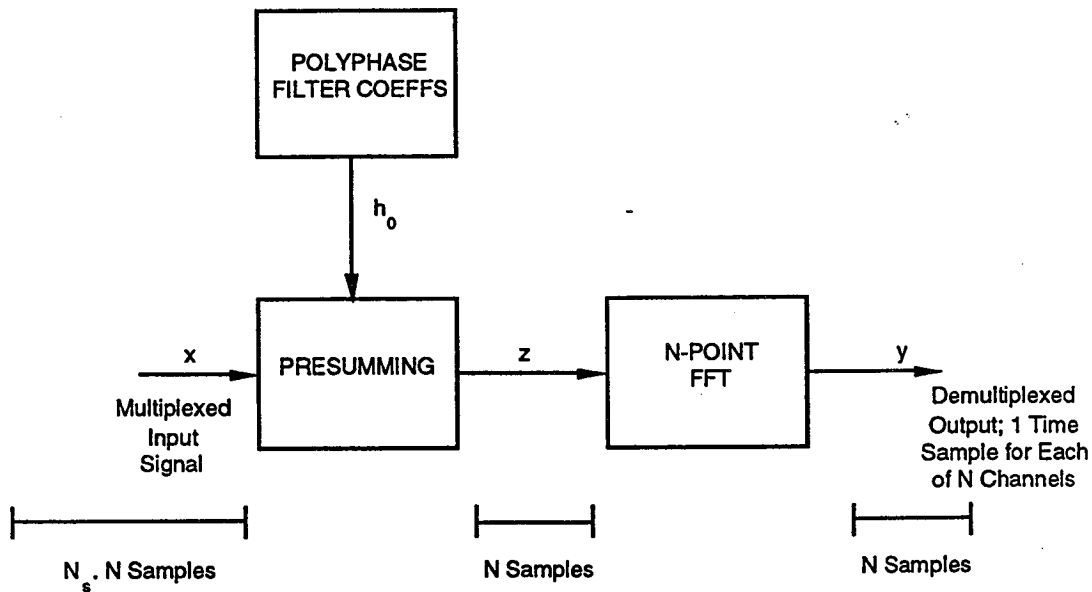


Figure 4.2: High level block diagram of polyphase filter

Note that the result of the Fourier transform is

$$y_0(n), y_1(n), \dots, y_{N-1}(n)$$

that is, all values are obtained for a fixed time n , one value for each carrier k .

To summarize, the 16-MHz signal x is fed to a digital presumming filter to obtain the intermediate signal z , as given by the equation for z above. The 16-MHz signal z is then input to an 8-point FFT. The output eight points represent one point for each

carrier (six actual carriers plus two guard bands). The output signals are thus sampled at 2 MHz each.

A proposed implementation of the presummer using four ASIC chips is shown in Figure 4.3. When used in this combination, the ASIC chips compute the quantity z from the input values x according to the equation for z above. The sequence z is computed in the following order:

$$z_n(r), z_n(r-1), z_n(r-2), \dots, z_n(r-7), z_{n+8}(r), z_{n+8}(r-1), z_{n+8}(r-2), \dots, z_{n+8}(r-7), \dots$$

This sequence is readily obtained from the serial stream x fed to the shift registers by setting the variable delays between the register stages to seven samples each. At each clock, a new set of coefficients is loaded into the ASICs, with the coefficients repeating after eight clocks. Each set of 8 values for z with the same subscript, n , constitute the input to the 8-point FFT that follows the presummer, as described above.

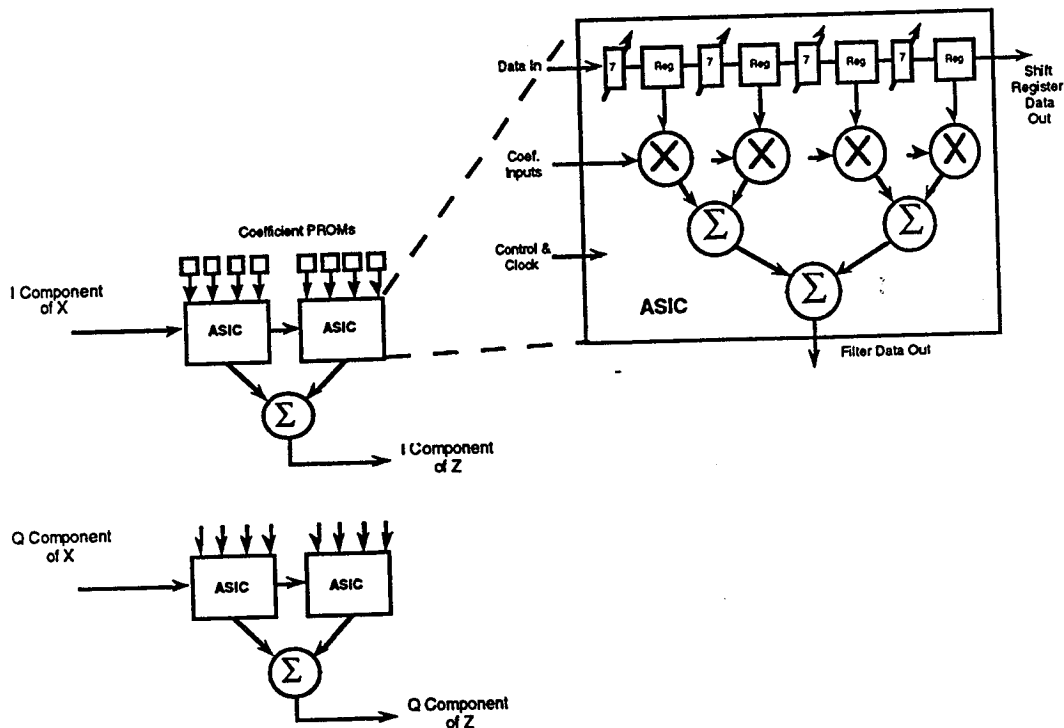


Figure 4.3: Block diagram of polyphase presummer

4.1.2 Cases Considered

Four separate cases are considered below to cover the range of options of interest as far as the filtering operations are concerned. These cases are as follows:

A) $B = 2 R_s$, Demux output 2 s/s

Here the carriers are spaced by twice the symbol rate. The demultiplexer produces 2 samples per symbol at its output. For an asynchronous network, the demultiplexer may

be followed by an interpolation filter and a demodulator, or alternatively the interpolation filter may be removed and a demodulator operating directly on the asynchronous samples may be used [13]. For a synchronous network, the samples at the demultiplexer output have the desired phase relation to the symbol, and hence a simple demodulator is used.

B) $B = 2 R_s$, Demux output 1 s/s

Here the carriers are spaced as in A) above, but the demultiplexer only produces 1 sample per symbol at the output. This results in reducing the power requirement of the demultiplexer to approximately half its value in A) above. However, since only 1 sample is produced per symbol, this case is only applicable to a synchronous network.

C) $B = 1.5 R_s$, Demux output 1.5 s/s

Here the carriers are spaced by 1.5 times the symbol rate. In addition to the bandwidth savings (which may or may not be important), the demultiplexer power requirements are also reduced since the sampling frequency is now reduced compared to A) and B) above. As in A), several possibilities exist for the demodulator.

D) $B = 1.5 R_s$, Demux output 2 s/s

In this case, the carriers are spaced by 1.5 times the symbol rate, but the demultiplexer output is 2 samples per symbol. This results in increased complexity in the demultiplexer compared to C) above. On the other hand, the demodulator and interpolating filter, if any, are simpler.

4.1.3 Polyphase Demultiplexer and Interpolation Filter Complexity

The four cases denoted by A, B, C, D above are of particular interest. The complexity of the multiplexer in each case is determined primarily by the desired output rate, assuming that the number of carriers is the same in all cases. This is attributed to the fact that the polyphase FFT, as well as the multipliers and adders in the polyphase summer operate at the output sampling rate. Therefore, cases A and D are the most power consuming for the demultiplexer, with case B consuming about half the power, and case C 75% of the power of cases A and D.

When used, the interpolation filter contributes significantly to the processor complexity. The filter has an FIR structure with an impulse response that is constantly sliding to satisfy the desired phase relationship between input and output samples. To make matters more difficult, this filter should be shared among several carriers to avoid duplication of hardware.

Two cases are of particular interest. In the first case, the input sampling rate of each carrier is $1.5 R_s$ and in the second, it is $2 R_s$. The output in both cases is $2R_s$. Note that in the second case, the number of input samples equals the number of output samples, and only the relative position of those samples within a symbol differ. (The output samples are desired at mid-symbols and symbol edges.)

The complexity of the interpolation filter is approximately the same in these 2 cases, since it tends to be dominated by the number crunching requirement which is itself determined by the output sample rate. The slight simplifications afforded by the lower input sampling rate of $1.5 R_s$ are offset by the slightly larger control complexity in that case.

4.1.4 Power and Mass Estimates

The power and mass estimates given below are very preliminary, but are helpful in performing tradeoffs between various configurations.

The following benchmarks can be used in estimating the power requirement for the polyphase demultiplexer. For 32 channels, and a sampling frequency of 20 MHz, the polyphase demultiplexer would require approximately 2 watts. The FFT chip and the summer chip would have roughly equal contributions to the power. These numbers are based on CMOS radiation hard technology with a power figure of 2 microwatts per gate per MHz. For different sampling frequencies, the scaling should be linear.

Note that it is the aggregate output frequency that impacts the power requirement most directly, since it determines the rate at which the number crunching operations must take place. The scaling with the number of channels is approximately logarithmic. With these benchmarks, one can obtain a rough estimate of the demultiplexer power requirements for different configurations and parameter values.

Similar approximate estimates can be obtained for the interpolation filter. The complexity of this FIR filter is dominated by the multiplier requirements, as roughly half the total interpolation power goes into the multipliers. A one point estimate of the power required indicates that an interpolation filter chip shared among 16 carriers, running at 20 MHz would require about 1 watt of power, again assuming CMOS radiation hard technology with a power figure of 2 microwatts per gate per MHz. Again the scaling with the speed is roughly linear, and with the number of carriers roughly logarithmic.

Mass estimates, at this preliminary stage, can be obtained by using extrapolations from similar digital technology developments. Previous experience indicates that for similar developments, approximately 7.5 W of power correspond to 1 kg of mass. Using this correspondance, an overall mass estimate is quickly obtained once an overall power estimate is computed.

4.1.5 Example

As an example of the approximate estimation procedure of power and mass outlined above, consider 16 frequency multiplexed carriers of 1 Msymbol per second each (12 actual carriers and 4 guard bands). The estimates for power and mass of the demultiplexer and interpolation filter (if used) are given below for the 4 cases considered.

A) $B = 2 R_s$, Demux output 2 s/s

Sampling frequency = $16 B = 32$ MHz
Power for demultiplexer = 2.5 watts
Mass for demultiplexer = 0.33 kg
Power for interpolation filter = 1.2 watts
Mass for interpolation filter = 0.16 kg

B) $B = 2 R_s$, Demux output 1 s/s

Sampling frequency = $16 B/2 = 16$ MHz
Power for demultiplexer = 1.25 watts
Mass for demultiplexer = 0.17 kg

C) $B = 1.5 R_s$, Demux output 1.5 s/s

Sampling frequency = $16 B = 24$ MHz
Power for demultiplexer = 2 watts
Mass for demultiplexer = 0.25 kg
Power for interpolation filter = 1.2 watts
Mass for interpolation filter = 0.16 kg

D) $B = 1.5 R_s$, Demux output 2 s/s

Sampling frequency = $16 B \times 4/3 = 32$ MHz
Power for demultiplexer = 2.5 watts
Mass for demultiplexer = 0.33 kg
Power for interpolation filter = 1.2 watts
Mass for interpolation filter = 0.16 kg

4.2 Onboard Demodulation

Onboard demodulator complexity is generally somewhat lower than the onboard demultiplexer complexity, especially for "well behaved" AWGN channels which do not suffer from multipath fading and large frequency offsets. This is due to the computationally intensive nature of demultiplexing inherent in digital filtering operations. Nevertheless, onboard demodulator complexity is still critical since it translates directly into how many carriers at a given rate can be demodulated using a single chip.

4.2.1 Onboard Demodulator Operation

Demodulator complexity is generally determined by whether or not the following operations are performed by the demodulator, and the manner in which they are performed:

- unique word detection
- carrier synchronization
- symbol timing synchronization
- sample interpolation
- detection

The four TDMA synchronization options being considered will have different requirements on each of the above functions.

Conventional TDMA (option 1) requires unique word detection, carrier and symbol timing synchronization, and detection. Unique word detection and carrier and timing synchronization are done in real time over the preamble portion of the burst as the TDMA burst is being received. Detection is also done in real time after synchronization using the carrier phase and timing reference derived from the preamble pattern.

Preambleless (asynchronous) TDMA (option 2) demodulation also requires unique word detection, carrier and bit timing estimation, and detection. However, carrier and bit timing estimation is performed on the data portion of the burst. This involves storing the received burst for two pass demodulation, in which detection is done in a second pass after carrier phase and timing estimates are obtained. In addition, sample interpolation is required for detection based on the timing estimates.

Bit synchronous TDMA demodulation on the other hand only requires carrier synchronization and detection. Carrier synchronization can be performed in real time on a short preamble pattern (option 3), or can be estimated using a small portion of the burst data if the burst does not include a preamble pattern (option 4). In the latter case, a few data symbols will have to be stored to get the phase estimate before detection can be done.

4.2.2 Demodulator comparisons

Based on the above discussion, demodulator complexity comparisons can be made among the four synchronization options being considered.

Option 3 (bit synchronous with preamble) is by far the least complex from an onboard demodulation standpoint and will be assigned a relative complexity value of 1.

Option 4 (preambleless bit synchronous) is slightly more complex since it involves carrier phase estimation based on the random data in the received burst (e.g. using Viterbi and Viterbi algorithm [9]). This added complexity however is minimal and will have little impact on the comparisons. Therefore this option is also assigned a relative complexity value of 1.

Option 1 (conventional TDMA) is more complex in terms of onboard demodulation since it requires unique word detection, as well as carrier phase and timing synchronization. This option is assigned a relative complexity value of 2.

Finally, option 2 (preambleless asynchronous TDMA) is the most complex from the onboard demodulation standpoint since it requires all the above demodulation functions. In addition, demodulation and detection is performed in a two pass approach which involves onboard storage and sample interpolation. This option is assigned a relative complexity value of 4.

4.2.3 Mass and Power Estimates

Based on the comparisons in the previous subsection, mass and power estimates are shown in Table 4.1 for each one of the four TDMA options considered. Power estimates assume 1 watt per chip. Mass estimates are based on 1 Kg to 7.5 watts of power. The number of carriers per chip is based on 1 Msym/sec carrier rate. All estimates scale linearly with symbol rate and number of carriers.

Table 4.1: Demodulator Power and Mass Estimates

	Option 1	Option 2	Option 3	Option 4
relative complex.	2	4	1	1
carriers/chip	8	4	16	16
32 carriers power	4 W	8 W	2 W	2 W
8 x 32 carr. power	32 W	64 W	16 W	16 W
8 x 32 carr. mass	4.26 Kg	8.52 Kg	2.13 Kg	2.13 Kg

In the above table, the last two rows represents the overall estimates of demodulator power and mass for the entire system assuming 8 uplink beams with 32 carriers per beam.

4.3 Onboard Timing Error Measurement

The above comparisons have shown the impact of bit synchronous operation on onboard demultiplexing and demodulation in terms of complexity, mass, and power. Another impact of bit synchronous TDMA on onboard hardware is the requirement of onboard error measurements. This subsection examines onboard timing error measurements.

4.3.1 Error Measurement Technique

Onboard timing error measurements have to be performed on user terminal acquisition and synchronization bursts to determine timing phase error. However, since the onboard demultiplexers operate with one output sample per symbol, these measurements can not be performed at the symbol rate R_S .

An onboard timing error measurement technique is shown in Figure 4.4. In this technique, the user terminal acquisition and synchronization bursts consist of an alternating pattern of symbol pairs which effectively halves the symbol rate. The transmitted filtered pattern consists of two tones as shown in Figure 4.4 at R_S and $R_S/2$. The onboard acquisition and synchronization processor effectively filters out the R_S component and performs timing estimation at half the symbol rate (two samples per symbol) as shown in the figure.

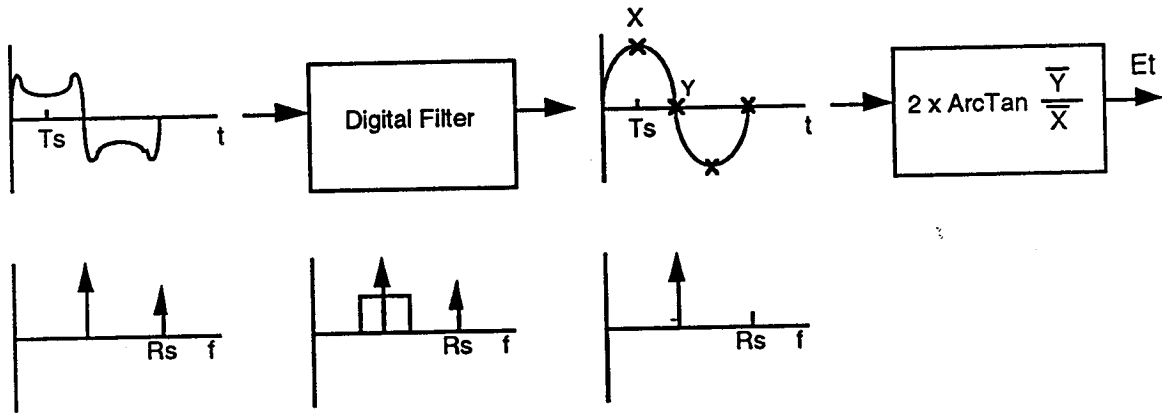


Figure 4.4: Timing Error Measurement Technique'

The phase error measurement process is affected by two main sources of inaccuracy. These are thermal noise and quantization noise. It is generally desirable to keep the inaccuracy to within 1% of a symbol duration. Thermal noise is generally the dominant source of inaccuracy provided there is a reasonable number of quantization levels are used (e.g. 8-bit quantization). Narrow band filtering of $R_S/2$ component also yields some improvement in the signal to noise ratio for timing estimation in proportion to the filter bandwidth. The next subsection presents an analysis of the timing error measurement.

4.3.2 Equation for Timing Measurement Error

The phase error of an uplink signal relative to an onboard clock is given by

$$\theta = 2 \tan^{-1} \left(\frac{y_2}{y_1} \right)$$

where y_1 and y_2 are values of a clock signal sampled at times 0 and $\pi/2$. The major causes of phase measurement error are quantization noise and uplink noise. Since these terms are generally small compared with a signal component, the above equation may be expressed in the following form:

$$\theta = \theta_0 + \Delta\theta$$

where θ_0 and $\Delta\theta$ are respectively an actual phase and measurement error and are related to y_1 and y_2 as follows:

$$y_1 = y_{10} + \Delta y_1$$

$$y_2 = y_{20} + \Delta y_2$$

$$\theta_0 = 2 \tan^{-1} \left(\frac{y_{20}}{y_{10}} \right)$$

$$\Delta\theta = 2 \left[\left(\frac{1}{y_{10}} \right) \Delta y_2 - \left(\frac{y_{20}}{y_{10}^2} \right) \Delta y_1 \right]$$

A sinusoidal timing signal with noise is expressed in the following form:

$$y(t) = A \sin \left(\frac{\omega_s t}{4} + \theta_0 \right) + n(t)$$

where $\omega_s = 2\pi / T_s$ is an angular frequency and T_s is a symbol period. The value of $y(t)$ after quantization is y_1 and y_2 at $t=T_s$ and $t=0$:

$$y_1 \approx A + \Delta y_{q1} + n(t_1)$$

$$y_2 \approx \theta_0 A + \Delta y_{q2} + n(t_2)$$

where Δy_{q1} and Δy_{q2} are quantization errors. Simple calculation shows that the standard deviation of $\Delta\theta$ is given by the following expression:

$$\sigma_{\theta} = 2 \sqrt{\frac{1 + \theta_0^2}{m} (\sigma_q^2 + \sigma_n^2)}$$

For n -bit quantization

$$\sigma_q = \frac{1}{\sqrt{3}} \cdot \frac{1}{2^{n+1}}$$

$$\sigma_n = \frac{1}{\sqrt{2a \left(\frac{E_b}{N_0} \right)}}$$

where a is a noise reduction factor (or improvement in E_b/N_0) due to narrowband filtering for clock recovery.

4.4 Onboard Hardware Conclusions

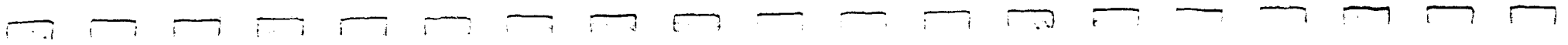
Table 4.2 shows a side by side mass and power comparison among the four options considered for TDMA synchronization. These comparisons are based on 8 uplink beams, 32 carriers per beam, and 1 Msps symbol rate for each carrier.

Table 4.2: System Mass and Power Comparisons

	Option 1 (Conventional TDMA)	Option 2 (Preambleless Asynch TDMA)	Option 3 (Bit Synch TDMA w/ Preamble)	Option 4 (Preambleless Bit Synch TDMA)
Demux Power	51.2 W	51.2 W	20 W	20 W
Demux Mass	6.8 Kg	6.8 Kg	2.6 Kg	2.6 Kg
Demod Power	32 W	64 W	16 W	16W
Demod Mass	4.26 Kg	8.52 Kg	2.13 Kg	2.13 Kg
Total Power	83.2 W	115.2 W	36 W	36 W
Total Mass	11.06 Kg	15.32 Kg	4.73 Kg	4.73 Kg

The impact of onboard timing error measurement on mass and power in the above comparisons is considered to be negligible.

From the above comparisons it is obvious that bit synchronous operation simplifies onboard demultiplexing and demodulation compared to conventional TDMA. Although the relative impact of this on mass and power is substantial (e.g. 50% reduction in mass and power), the impact in terms of absolute saving in mass and power, while significant, can not be considered critical.



Section 5

Ground Terminal Timing Correction Techniques

This section examines methods for deriving and correcting ground terminal transmit timing so that it closely tracks onboard reference timing. It addresses alternate sources of ground terminal timing and timing correction techniques which are applicable for synchronization of the transmit clock to the onboard clock after initial timing acquisition has been performed.

5.1 Timing Issues

For a bit synchronous system to operate properly, the ground terminal transmit timing should closely track the onboard reference timing to within a small fraction of a symbol (typically 5%). This requires initial timing acquisition over which the ground terminal adjusts its timing over a number of symbols and fraction of a symbol to bring it within the specified timing tolerance. Following initial timing acquisition, the ground terminal can transmit its data bursts, however, timing synchronization should be maintained in order for the onboard processor to be able to receive the data without added errors due to timing offset.

During the synchronization phase, the two main sources of timing errors between the ground terminal transmit clock and the onboard reference clock are the ground terminal internal clock inaccuracy and the Doppler shift. The onboard clock is generally a high accuracy clock with a typical worst case drift on the order of $5.0E-11$ per day. In order to keep ground terminal cost down, the ground terminal clock will be less accurate with an aging rate on the order of $1.0E-6$ to $1.0E-7$ over one year. This introduces one source of timing errors between the ground terminal timing and the onboard timing reference. Another source of timing error is the variation in distance from the ground terminal to the satellite due to satellite motion. This variation introduces a Doppler component into the receive clock at the satellite as well as the receive clock at the ground terminal.

To compensate for these two sources of timing errors, ground terminal timing will have to be slaved to the onboard timing through one of several timing correction techniques. These corrections can be made based on received feedback from the satellite regarding onboard phase error measurements, as well as possible Doppler and clock drift prediction algorithms when applicable. These techniques are discussed in the next two sections. Additionally, an open loop clock synchronization technique which utilizes precision ranging to compensate for Doppler is discussed in section 5.4. The precision ranging technique theoretically does not require onboard timing error measurements, however it is much less accurate and could result in substantial timing errors. Therefore, it is only included in the discussion for completeness.

Finally, it should be noted here that although the discussion in the rest of this section focuses on compensation for clock drift and Doppler, there are other sources of timing errors which will contribute to the overall achievable timing synchronization accuracy. These include onboard timing measurement errors, clock correction quantization errors, clock correction device inaccuracy, and clock circuit logic jitters.

5.1.1 Ground Terminal Timing

Ground terminal transmit timing can be derived from either an independent clock (IC) source or a phased locked clock (PLC) source which is locked to the received downlink clock. In either case, once initial acquisition is made, ground terminal timing correction is performed to ensure that different TDMA bursts from the various terminals arrive at the satellite at the proper timing instants to within a small fraction of a symbol. This implies that ground terminal timing should track the onboard timing source by implementing corrections for sources of timing error.

5.1.2 Clock Correction Methods

There are four alternatives to implementing transmit clock timing corrections which are considered in this study. These are:

- a. programmable clock phase shifter (PPS) which produces a phase shift of a clock signal by varying a control voltage,
- b. voltage controlled oscillator (VCO) correction approach where the transmit clock phase is adjusted by varying the frequency of a VCO,
- c. digital controlled oscillator (DCO) approach where a DCO running at a several times the clock speed is used to perform phase adjustments on the transmit clock by varying the number of DCO clock cycles which comprise a transmit clock cycle, and
- d. the programmable delay line (PDL) technique in which corrections are made through a delay line that covers a symbol period with adequate delay adjustment resolution.

In the following subsections, these methods are considered with each of the timing sources (IC and PLC) when applicable.

5.2 Independent Clock Source

The first alternative in deriving transmit timing at the ground terminal is to base the transmit clock on an independent clock source which is a stand-alone clock. The terminal transmit timing clock will thus have the same nominal frequency as the onboard symbol clock, however due to clock inaccuracies and drift, a certain frequency offset will be present. The ground terminal attempts to compensate for the timing phase

shifts introduced by this frequency offset and by other sources of timing error such as Doppler.

Due to a requirement of low cost ground terminals, the ground terminal clock could be a crystal oscillator with typical long-term accuracy of $\pm 1.0E-6$. The onboard clock accuracy is better than that by three to four orders of magnitude. Hence, at a symbol rate of 2.048 Mbps, the worst case frequency offset between the terminal clock and the onboard clock due to clock inaccuracy would be 2.048 Hz. In the absence of any correction, this frequency offset alone would result in approximately two symbol timing offset every one second which far exceeds the 5% maximum symbol offset requirements for a bit synchronous system. Since other sources of timing error may also contribute to the overall symbol timing inaccuracy, it is desirable to keep the timing error due to frequency offset to less than 1 or 2 % of a symbol time. For a 1 % offset, a periodic timing correction is then required every 5 ms. It is therefore clear that in order to perform these periodic corrections, some type of frequency offset prediction algorithm is required which relies on satellite feedback to estimate the frequency offset. This prediction algorithm can also be used to estimate the frequency offset due to Doppler.

Figure 5.1 illustrates the intermediate timing corrections for frequency drift which are required for the IC source within a correction interval T.

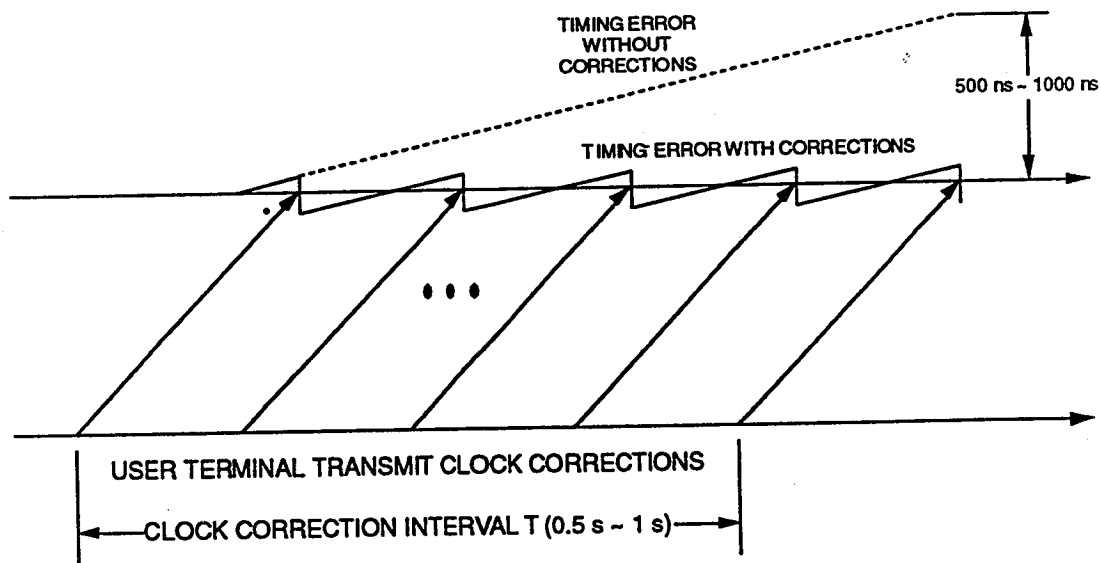


Figure 5.1: Independent Clock Timing Corrections

In addition to the periodic corrections which are performed every 5 ms in the example above, additional symbol timing correction is needed to compensate for any residual timing errors at the satellite. These corrections could be made every time interval T_c where T_c is the correction period which is the time between satellite feedback messages. The combination of periodic timing corrections vis-a-vis the prediction algorithm and the corrections based on the satellite error signal should result in a tolerable timing error (i.e. within 5% of a symbol duration).

It should be noted here that a small residual timing offset may always be present due to sources of timing error that are not compensated for by the prediction algorithm and which can not be removed entirely due to the inherent delay in the time the error measurements are made onboard the satellite to the time the correction is received and implemented on the ground. However, as long as the timing offset does not exceed a tolerable value (e.g. 5%), performance should be acceptable.

5.2.1 Independent Clock - Programmable Phase Shifter (IC-PPS)

Timing corrections to compensate for frequency offset, Doppler, and other sources of timing error, could be done with a programmable phase shifter which provides a phase shift of the internal clock by a desired amount. This approach is shown in Figure 5.2.

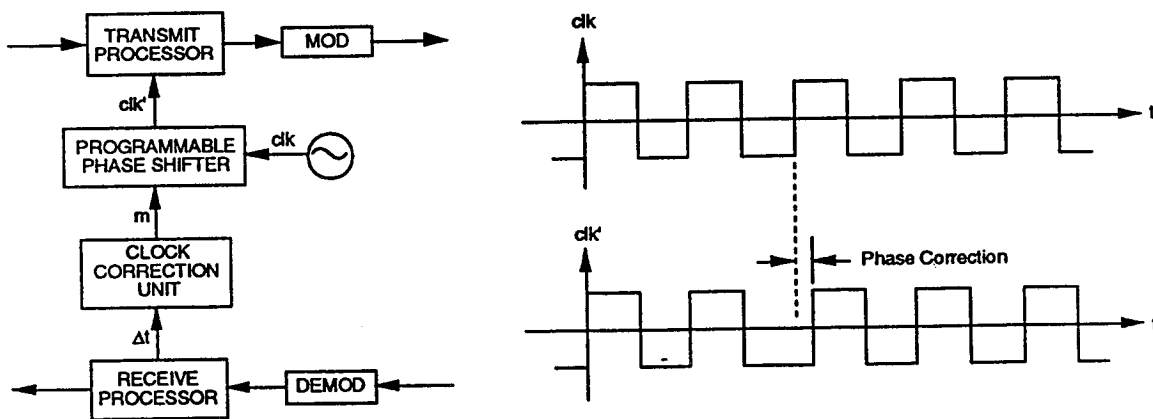


Figure 5.2: Independent Clock with Programmable Phase Shifter (IC-PPS)

A number of voltage variable phase shift devices are commercially available. Figure 5.3 shows typical voltage variable phase shifter characteristics. An m -bit quantizer (digital to analog converter) can be used to provide programmable control of the phase shift. Fine phase adjustments down to a given resolution can be achieved by choosing a large enough value for m . However, the inherent nonlinearity in the phase shifter characteristics may introduce device inaccuracy errors. Hence, PPS calibration may be necessary.

5.2.2 Independent Clock -Voltage Controlled Oscillator (IC-VCO)

Another approach to implementing timing corrections at the ground terminal is to use a voltage controlled oscillator as a clock source and to implement the timing corrections through changes to the VCO frequency. This approach is shown in Figure 5.4.

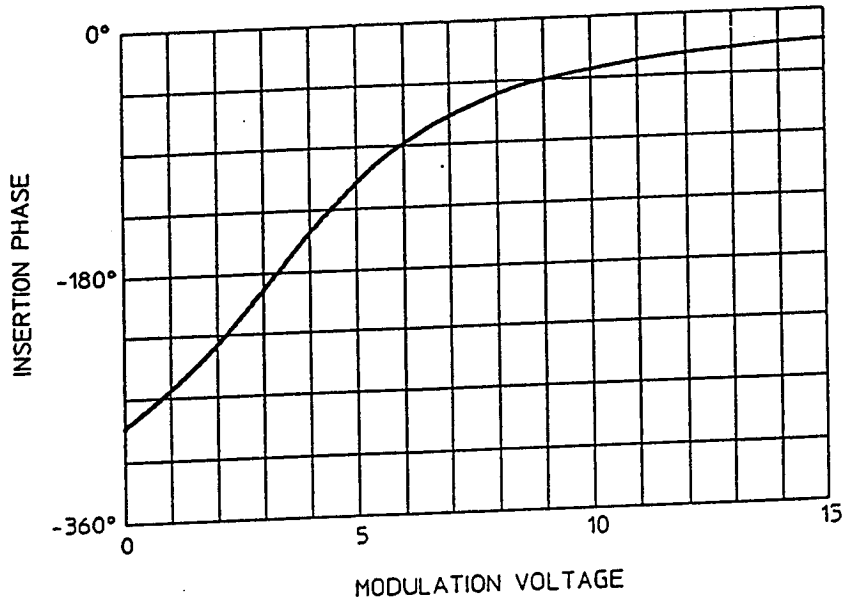


Figure 5.3: Example of Voltage Variable Phase Shifter Characteristics

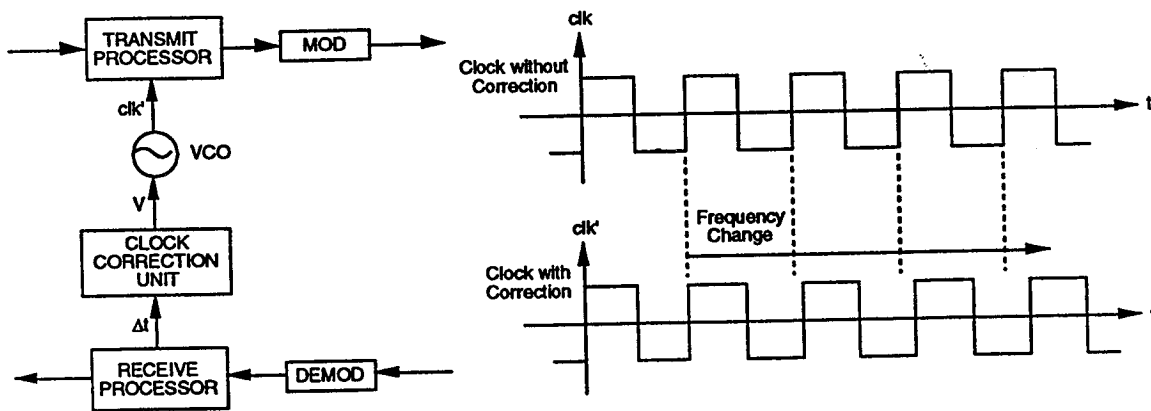


Figure 5.4: Independent Clock with Voltage Controlled Oscillator (IC-VCO)

Using this approach, long term frequency offsets can be easily compensated for by setting the VCO control voltage and hence frequency. Also, since phase adjustments are made continuously, this approach eliminates discrete phase jumps upon correction. Figure 5.5 shows typical VCO voltage - frequency characteristics. These characteristics typically exhibit some non-linearity as shown in the figure.

The IC-VCO technique is very sensitive to the linearity of the voltage - frequency characteristic since phase errors caused by frequency inaccuracy are magnified over the correction period. High linearity VCOs are available but are more costly. Device calibration is one option, however this also adds to the cost. Furthermore, aging may result in changes in the VCO characteristics which may require recalibration.

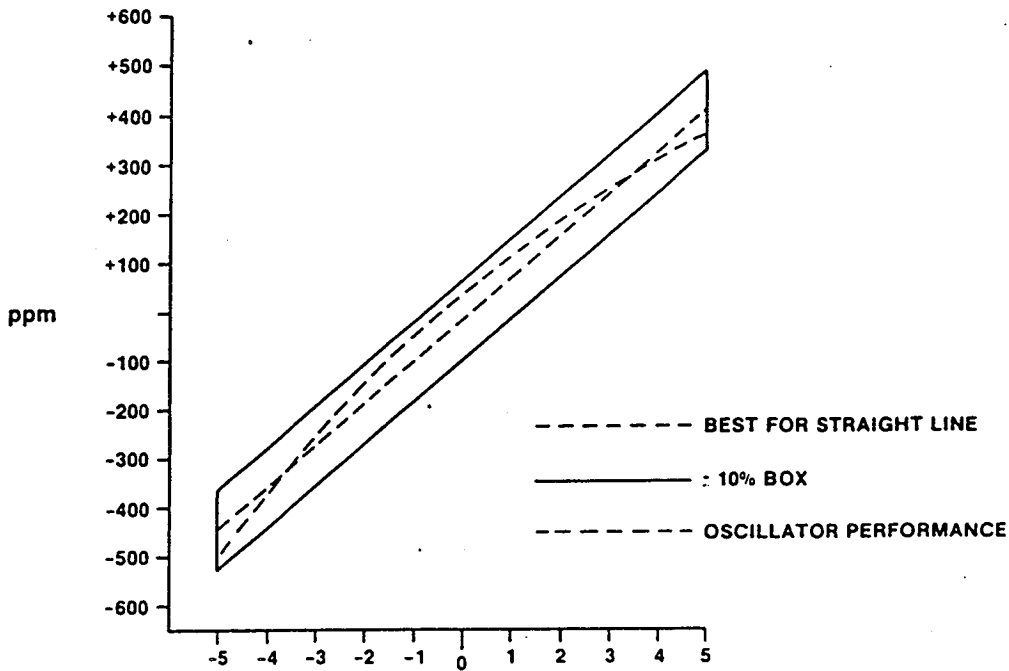


Figure 5.5: Example of Voltage Controlled Oscillator Characteristics

5.2.3 Independent Clock - Digitally Controlled Oscillator (IC-DCO)

The digital controlled oscillator (DCO) operates at a higher rate, e.g. 50 times faster, than the symbol clock. Hence, for a 2.048 MHz symbol clock, the DCO clock rate would be around 100 MHz. The transmit clock is derived from the high frequency clock through the use of a programmable divider. Clock phase adjustments are made by deleting a clock pulse of the high frequency oscillator. The IC-DCO concept is shown in Figure 5.6.

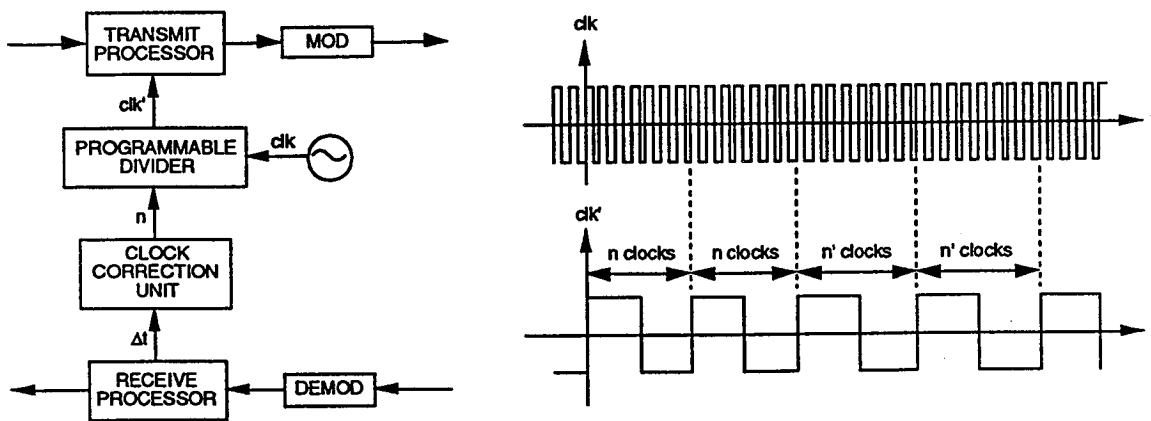


Figure 5.6: Independent Clock with Digitally Controlled Oscillator (IC-DCO)

Obviously, this approach requires a much faster running clock than the other two approaches. One concern with this approach is the frequency stability of the DCO oscillator which is running at a substantially higher rate than the symbol clock. Also,

timing corrections introduce a discrete albeit very predictable phase jump. The magnitude of this phase jump (and hence the correction resolution) is directly proportional to the ratio of the DCO clock to the symbol clock.

5.2.4 Independent Clock - Programmable Delay Line (IC-PDL)

Timing corrections to compensate for frequency offset, Doppler, and other sources of timing error, could be done using a combination of frame counter and tapped delay line. The frame counter is used to advance or retard the frame timing by an integer number of symbols. The tapped delay line covers a symbol delay with a sufficiently large number of delay taps (e.g. 50 for 2% resolution or 20 for 5% resolution). Figure 5.7 shows how this timing correction is implemented using a programmable delay line.

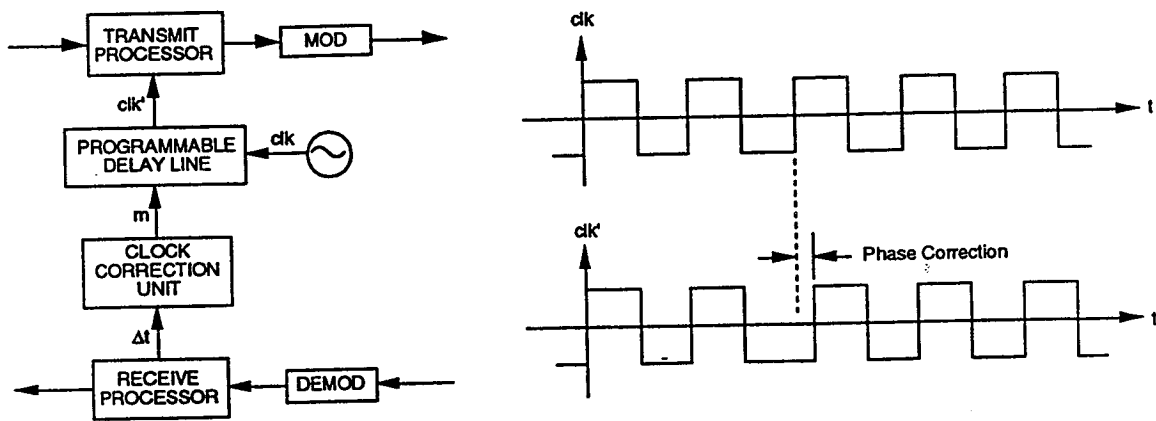


Figure 5.7: Independent Clock with Programmable Delay Line (IC-PDL)

The programmable delay lines typically can provide up to 2 ns resolution with 8 bit control. Hence timing corrections up to 520 ns can be implemented in multiples of 2 ns using a single PDL. Several PDLs can be cascaded to cover a range equal to one symbol, or lower resolution PDLs (i.e. > 2 ns) can be used. For example, for a symbol rate of 1 Msym per second, a PDL with 2 ns resolution will give a timing correction capability of approximately 0.2 %.

One problem with the PDL approach is that it may produce a superfluous clock pulse when a correction is made. If the correction comes after the clock pulse has been delayed by the initial delay setting but before the new delay setting, the delay line output will consist of two pulses instead of just one. Because of this problem and other potential device inaccuracy problems, the PDL approach is not considered further.

5.3 Phase Locked Clock

An alternative to using an independent symbol timing clock at the ground terminal is to derive the symbol clock from the receive carrier clock. This could be done by a phase lock loop which tracks the receive signal clock or by a direct clock extraction circuit. In

either case, a phase locked clock (PLC) source would eliminate frequency offset due to clock inaccuracy as a source of timing error provided the derived clock is closely aligned with the received clock. It would however include a two fold Doppler component due to both the uplink and downlink contributions.

Since the PLC approach eliminates timing offsets due to ground terminal clock inaccuracy, the major source of timing error becomes the Doppler. Depending on the magnitude of Doppler, compensation for Doppler shifts between correction intervals may be necessary to achieve a higher accuracy, although relatively high bit rates can be supported without intermediate Doppler compensation.

Figure 5.8 illustrates timing corrections for the PLC source which are made once every correction interval T_c . For a typical Doppler value of 16 ns/s (0.1 deg orbit inclination), one clock correction per correction period is sufficient for low to medium symbol rates (e.g. 2.048 Msym/s).

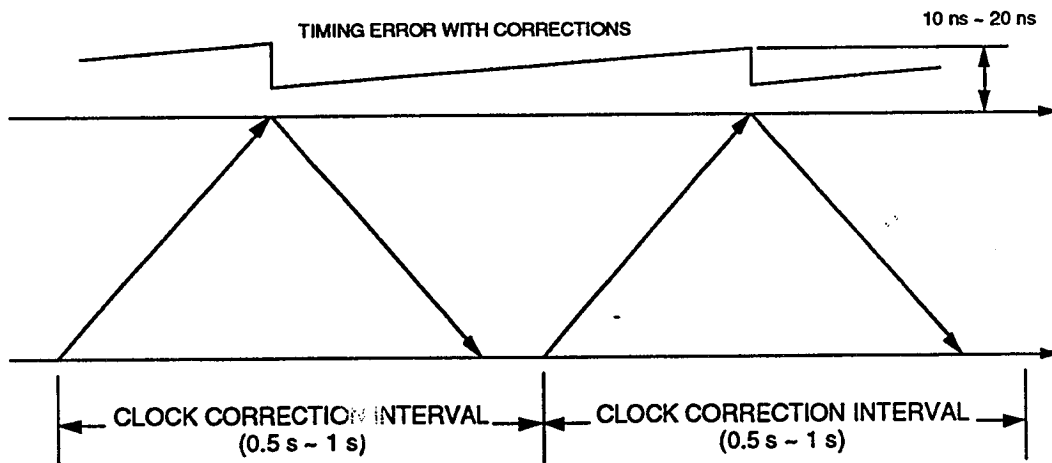


Figure 5.8: Phase Locked Clock Timing Corrections

One issue in the phase locked clock approach is the ability to maintain and/or recover timing after a loss of the receive signal clock. Hence, determination of the PLL bandwidth becomes a trade-off between tracking performance and response time.

Timing corrections for the PLC approach can be done either by a PPS or a DCO. The PDL method is not considered feasible due to the pulse insertion and device inaccuracy problems mentioned before. The VCO method does not seem to be applicable since the transmit clock is locked to the receive clock and hence can not be controlled independently.

5.3.1 Phase Locked Clock - Programmable Phase Sifter (PLC-PPS)

A programmable phase shifter can be used with the phase locked clock source to achieve timing phase corrections in a manner similar to the IC-PPS approach described earlier. This is shown in Figure 5.9. Here the phase shifter provides a discrete phase

adjustment to the transmit clock, which in turn is locked to or derived from the receive clock.

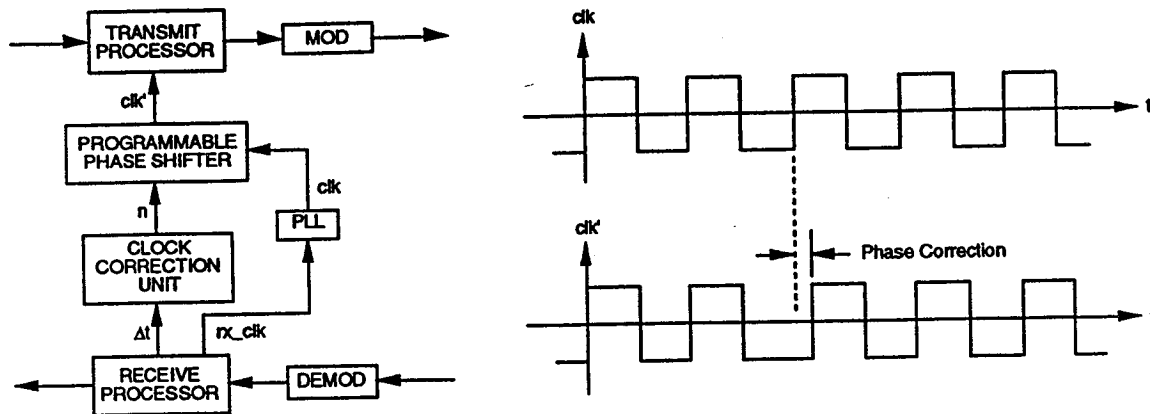


Figure 5.9: Phase-Locked Clock with Programmable Phase Shifter (PLC-PPS)

5.2.2 Digitally Controlled Oscillator (DCO)

Figure 5.10 shows an alternative to PLC timing phase corrections using a DCO. As in the IC-DCO approach described earlier, timing phase corrections are implemented by controlling the number of DCO clock cycles within a transmit clock cycle.

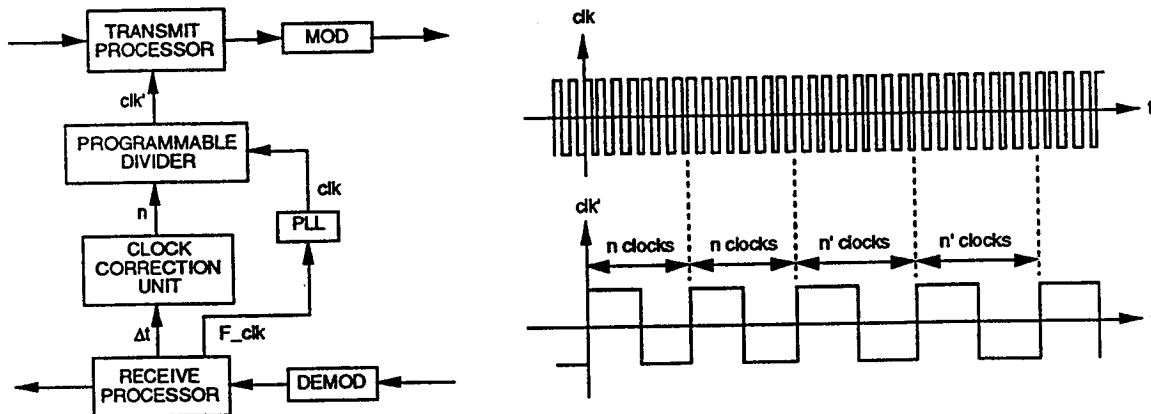


Figure 5.10: Phase-Locked Clock with Digitally Controlled Oscillator (PLC-DCO)

5.4 Open Loop Synchronization (OLS)

Open loop synchronization (OLS) which is shown in figure 5.11 is performed by deriving clock corrections from precision ranging of the satellite location to compensate for satellite motion. Technically, OLS does not require onboard phase error measurement. However, in practice it might be necessary to monitor abnormal timing

error caused by ground terminal malfunction or other sources of timing error. Thus, this technique is not attractive for actual implementation.

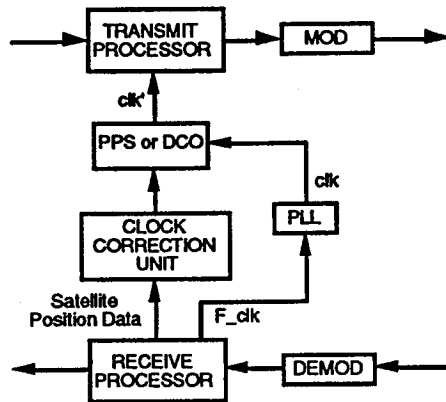


Figure 5.11: Clock Correction Based on Open Loop Synchronization

Since OLS can only compensate for the Doppler component in timing errors, the transmit clock must be derived from a phase-locked clock source to eliminate timing errors due to clock frequency offsets.

The limitation of the OLS approach lies in the ranging accuracy required at moderate bit rates. For example, a ± 10 m range error, which is not uncommon in a practical ranging system, results in ± 33 ns phase error. Other errors include delay calibration errors (both RF and baseband) of user terminals and onboard equipment, range prediction uncertainty, and implementation errors. These error terms would limit the supportable bit rate to no more than 500 Kbit/s. Because of the low supportable bit rates and the lack of onboard monitoring of the ground terminal transmit timing, this option is not recommended.

Section 6

Timing Accuracy

This section presents an overview description of acquisition and synchronization procedure, analytical models for timing analysis, numerical values for expected timing errors and computer simulation results. A general conclusion is also made for the maximum supportable bit rate in a bit synchronous system.

6.1 Acquisition and Synchronization Overview

Acquisition and synchronization of system timing in a bit synchronous system is performed through specialized acquisition and synchronization time slots. As a minimum, a single time slot on an LR-TDMA carrier may be used for both acquisition and synchronization by all the users in the system when the number of users is small. However, for a moderate to large number of users, several such time slots may be required, with some slots designated for acquisition and others for synchronization.

In a bit synchronous system, the purpose of acquisition is to achieve rough alignment of user terminal timing with the onboard timing in order to be able to start transmitting TDMA data bursts from the user terminal. An acquiring user terminal starts out by monitoring the downlink transmission from the onboard processor and deriving its timing from the downlink frame timing. Satellite range information may also be broadcast on the downlink to aid in initial acquisition. Based on the downlink frame timing, the terminal transmits an acquisition burst in a specified acquisition slot. The acquisition burst identifies the terminal and contains a preset data pattern that is used by a special acquisition/synchronization processor onboard the satellite to determine the burst timing offset in relation to the onboard reference timing. A correction message is then sent back to the acquiring terminal requesting a timing correction which may include an offset of several symbols plus a fraction of a symbol. The user terminal then proceeds to correct its timing and retransmits another acquisition burst which is again processed in the same manner onboard the satellite. This procedure is repeated if necessary until the user terminal timing is within a specified tolerance from the onboard timing (e.g. 10% of a symbol time), in which case the user terminal can begin transmitting its data bursts in their allocated time slots on one or several LR-TDMA carriers.

Once acquisition has been established and the user terminal is now transmitting its data bursts, a synchronization procedure is necessary to keep the ground terminal timing within the specified tolerance from the onboard timing. This is done through periodic timing error measurements onboard the satellite. User terminals which have already acquired system timing will periodically transmit a synchronization burst consisting of a predetermined pattern which allows measurement of the timing phase error onboard the satellite. The timing phase error is relayed back to the user terminal which implements timing error correction based on the received feedback from the onboard processor. Timing error correction may be accomplished in several ways, which are discussed in detail in the following sections.

Both acquisition and synchronization require timing error measurements onboard the satellite in a similar manner. The only difference between the two is the wider acquisition window which is required due to the larger timing uncertainty present during acquisition. The acquisition window size may span several symbol times in length. The actual acquisition window size will depend on how accurately the user terminal can derive its timing from the received downlink signal. For synchronization on the other hand, the burst timing is generally within 5 % of a symbol time and hence the synchronization burst can occupy the entire synchronization slot.

The procedure for performing onboard measurements of user timing in a bit synchronous system has been addressed in section 4.3. This includes the structure of the acquisition and synchronization bursts. Figure 6.1 shows an example of a possible allocation of acquisition and synchronization slots in an LR-TDMA system. In this example, the first TDMA time slot on carrier 1 serves as an acquisition slot and the next time slot on the same carrier serves as a synchronization slot. Other allocations of acquisition and synchronization time slots are possible, including allocation on a superframe basis and allocation among different carriers. In any case, TDMA data burst scheduling should avoid possible conflicts in using the same time slot for both synchronization and data burst transmission from the same user terminal.

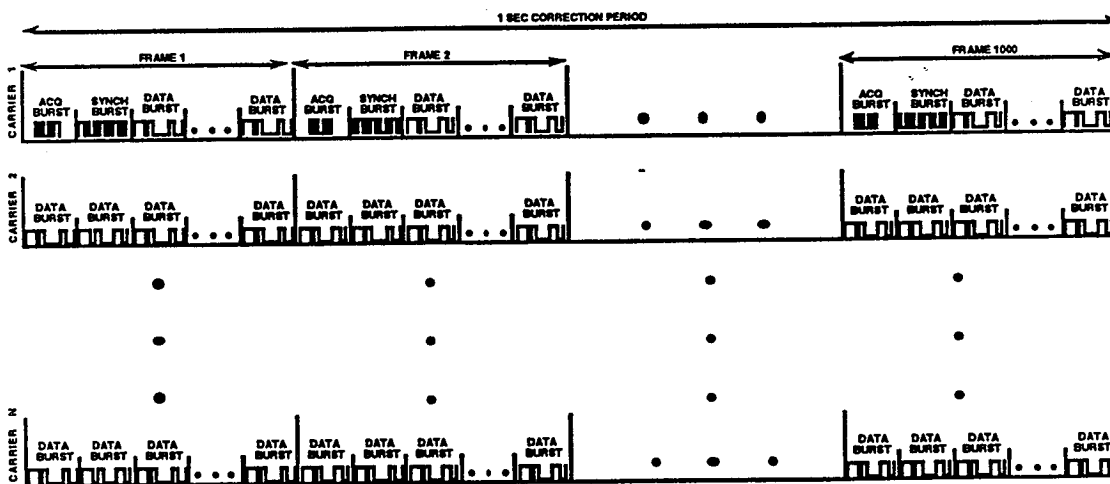


Figure 6.1: Acquisition and Synchronization Slot Allocation in LR-TDMA

The frequency of timing error measurements onboard the satellite depends on the correction period used and the number of required measurements in a correction period. The correction period is lower bounded by the round-trip propagation delay from the user terminal to the satellite plus any processing time that is required to perform the measurements. A typical correction period is on the order of 0.5 to 1 sec. Assuming one error measurement per correction period, and assuming an LR-TDMA frame period of 1 ms, a single channel on a single LR-TDMA carrier can thus support synchronization for up to 1000 active terminals for a correction period of one second. The required capacity for acquisition will generally be much less than that for synchronization since a terminal acquires in a few round trips (e.g. it may take 3 successive corrections to acquire) and only does so when it is ready to go active.

A possible concern in synchronization for an LR-TDMA system is that the data bursts may be transmitted on carriers which are different from the carrier over which the synchronization channel and consequently the timing error measurements are made. This may introduce a frequency dependent timing error. However, by examining the source of this timing errors, it becomes clear that this effect is negligible. The main sources of frequency dependent timing errors are filtering, HPA, and possible differences in delay through different onboard demodulators. Digital filtering is employed at the user terminal and equalization as well as operation away from the edges of the transponders may reduce the effect of group delay. HPA characteristics are usually wide band enough not to introduce any frequency dependent time delays within the range of interest. Finally, if a shared demodulator is used on all carriers then there is no problem in terms of different delay values, as will probably be the case in an LR-TDMA system. However, if individual demodulators are used, care must be taken to match the delays through these demodulators to within a tolerable limit. However, in the unlikely event that significant fixed frequency dependent delay differences are present, delay compensation may be implemented at the user terminal as a function of the transmit carrier frequency.

6.2 Timing Error Analysis

Timing analysis has been performed for the clock correction techniques described in the previous section. This section first describes a general clock control model and then presents specific models for the independent clock (IC) and phase locked clock (PLC) clock correction techniques. Each model analyzed includes numerical values to assess the feasibility of a bit synchronous system, identification of critical parameters, and illustrations of clock correction performance obtained from simulation.

6.2.1 General Model

A general clock control model is shown in Figure 6.2. The timing error of a TDMA burst is measured on the satellite by comparing the phase of the received clock against that of the onboard master clock, f_s . The measured phase error, denoted by "y" in the figure, is sent to the user terminal over a downlink signaling channel. The user terminal performs correction, w , on its transmit clock, f_u , in such a manner that TDMA bursts transmitted after the correction arrive at the satellite within a small fraction of a symbol period relative to the expected onboard timing. The heart of this system is a mechanism of performing clock correction.

The IC model includes only the uplink Doppler component, ρ_d , while the PLC model must consider both the downlink and uplink Doppler components. The control loop (satellite - user terminal - satellite) contains various error terms, in addition to the onboard phase measurement error. Also, the loop must be stable such that the phase error does not increase without a bound.

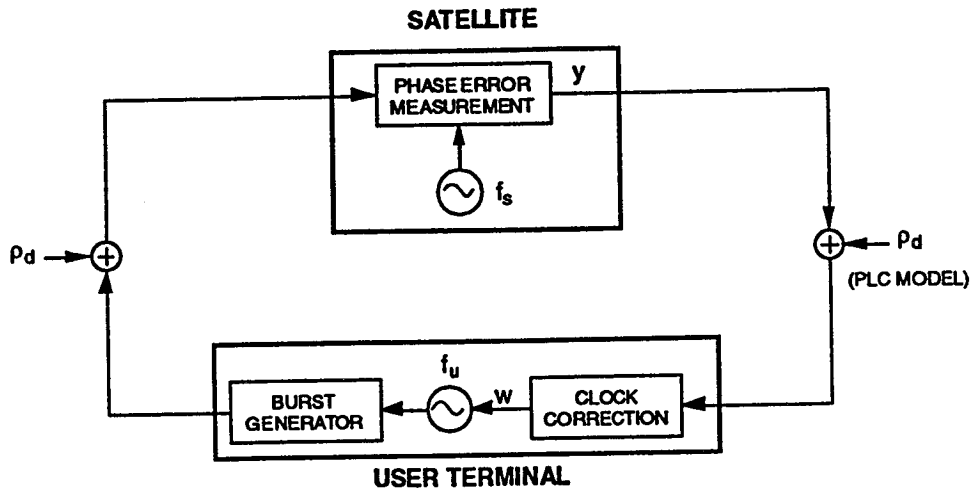


Figure 6.2: General Clock Control Model for Bit Synchronous System

6.2.2 Independent Clock (IC) Control Technique

The major issue associated with the IC control technique is the amount of drift of a user terminal clock, which must be compensated to assimilate with that of the onboard clock and Doppler shift. A typical low-cost crystal oscillator has an aging characteristic of about one part per 10^8 to 10^9 over 24 hours. With several months of operation, the clock accuracy will be reduced to 1×10^6 to 1×10^7 , producing a $1 \mu\text{s}$ to 100 ns of phase shift over one second. The clock control circuit must properly compensate for this large drift based on measured phase errors. Another factor which must also be taken into account in designing the IC system is the predictability of drift. Although long-term drift over several months can be fairly well characterized, its short-term component often exhibits a peculiar behavior, such as a sudden jump in the drift rate and changing its direction (positive to negative or negative to positive). Because of these reasons, the proposed control algorithm employs a robust technique, which has been considered previously for controlling an onboard clock in satellite-switched TDMA (SS-TDMA) and onboard processing systems.

The timing correction procedure for the independent clock is shown in Figure 6.3. To prevent a large phase jump due to a single clock correction, corrections are made in small steps during a correction period. The correction value is derived from the onboard error measurements which are performed once per correction period and transmitted down to the user terminal. A prediction algorithm is used at the ground terminal to predict the clock drift based on the received onboard error measurements, and to consequently determine the value of the intermediate corrections to ensure close tracking of the onboard timing.

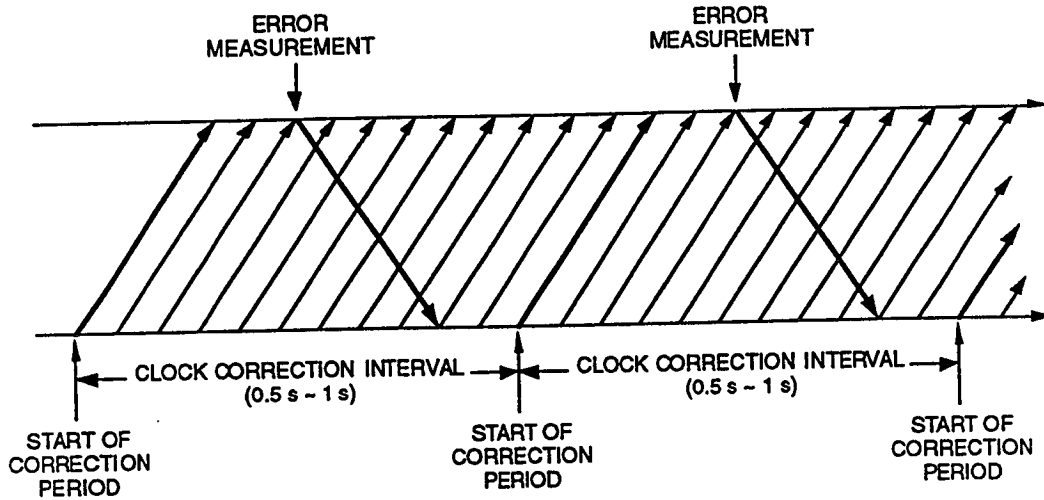


Figure 6.3: Timing Correction Procedure for IC

6.2.2.1 IC Timing Analysis

The IC clock correction technique is based on references [14-16]. The phase error at the end of the n th correction interval is

$$y_n = y_{n-1} + s_n$$

where s_n is the phase error in the current correction period and is given by

$$s_n = \int_{t_{n-1}}^{t_n} \{ \rho_u(\tau) + \rho_d(\tau) - \rho_s(\tau) - w_n \} d\tau$$

where $\rho_u(t)$, $\rho_d(t)$, and $\rho_s(t)$ are normalized user terminal clock drift, Doppler shift and satellite clock drift, respectively. The term w_n represents a normalized clock correction value for the current correction period. Integration in the above equation is over a clock correction period $T_c (=t_n - t_{n-1})$.

The drift and Doppler terms can be expressed in the following forms:

$$\rho_u(t) = \rho_{u0}t + \Delta\rho_u(t)$$

$$\rho_d(t) = \rho_{d0}\sin\left(\frac{2\pi t}{T_d}\right)$$

$$\rho_s(t) = \rho_{s0}t + \Delta\rho_s(t)$$

where

ρ_{u0} user terminal clock aging

- $\Delta\rho_u(t)$ user terminal clock short-term stability
- ρ_{do} maximum Doppler shift
- T_d a sidereal day (86164 s)
- ρ_{so} satellite clock aging
- $\Delta\rho_s(t)$ satellite clock short-term stability.

Using these parameters, the phase error s_n in the current correction period can be expressed in the following form:

$$s_n = r_n - \omega_n T_c$$

$$= r_n - \phi_n$$

where r_n includes the contribution of the user terminal clock drift, Doppler shift, and satellite clock drift. However, as will be pointed out later, the contribution of long term user terminal clock drift, long term onboard clock drift, and Doppler shift, to the IC analysis is rather negligible. This is because the IC technique relies on clock drift and Doppler prediction in which long term drift and Doppler are easy to predict since they do not change significantly over a clock correction period. This leaves the user terminal short term clock stability and the onboard clock short term stability as the major contributors to r_n . The term ϕ_n is the clock correction symbol timing term, which is simply obtained from the normalized clock frequency correction term ω_n by multiplying by the correction period T_c .

The above expression for s_n leads to the clock control model shown in Figure 6.4, where z^{-1} represents the delay of one correction period. As can be seen in this figure, the model further assumes a linearized clock correction function $H(z)$, which translates to a linear prediction algorithm of the required phase correction based on the received onboard phase error measurements.

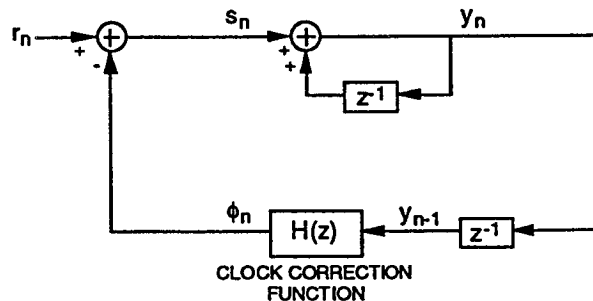


Figure 6.4: Linearized Clock Control Model

The clock correction problem is now reduced to finding a linear clock correction function $H(z)$ which minimizes the phase error y_n for all possible error values r_n . This

problem has been extensively analyzed in the past for onboard clock control in SS-TDMA and onboard processing systems [14-16]. The optimum function, according to [14], is given by

$$H(z) = \frac{2 - z^{-1}}{1 - z^{-1}} = 1 + \frac{1}{1 - z^{-1}}$$

The clock correction function $H(z)$ is essentially composed of an accumulator (i.e. a first order error predictor) and a constant (i.e. a 0th order predictor). The accumulator function results in long term corrections which remove the effects of long term drift and Doppler, while the 0th order prediction term attempts to compensate for short term errors.

Figure 6.4 now can be redrawn as Figure 6.5. This figure also includes the error components produced by the satellite, e_{sn} , and the user terminal, e_{un} . These terms account for error contributions from such factors as device inaccuracies, quantization, logic jitters, and measurement inaccuracies. A breakdown of the error components and their statistical characteristics are given later in this section.

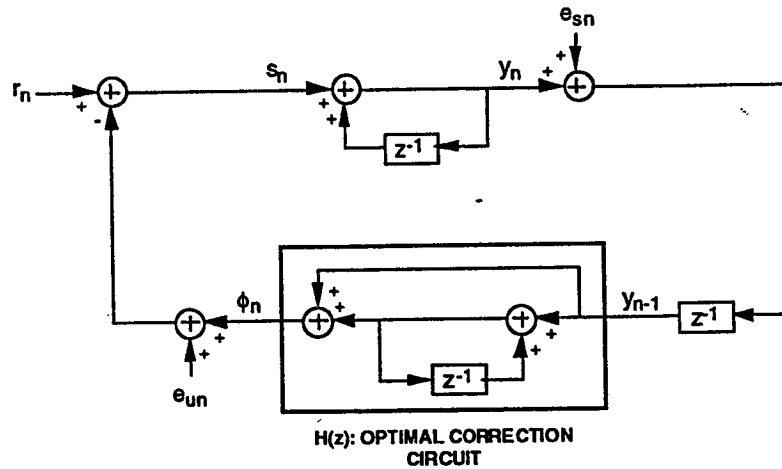


Figure 6.5: Optimal Clock Control Model with Various Timing Error Sources

From Figure 6.5, the z-transform of the measured error y_n is obtained as follows:

$$Y(z) = (1 - z^{-1})[R(z) - E_u(z)] - z^{-1}(2 - z^{-1})E_s(z)$$

where $R(z)$, $E_u(z)$ and $E_s(z)$ are respectively the z-transforms of r_n , e_{un} , and e_{sn} . The discrete time domain expression for $Y(z)$ is given by

$$y_n = r_n - r_{n-1} - e_{un} + e_{un-1} - 2e_{sn-1} + e_{sn-2}$$

The error terms shown in Figure 6.5 are further divided into various error components. Table 6.1 lists these error components and their statistical characteristics.

Table 6.1: IC Error Components and Statistical Characteristics

Term	Components	Distribution	Notation
r_n	User terminal clock short-term stability	Normal	σ_1
	Onboard clock short-term stability	Normal	σ_2
e_{un}	User terminal clock correction quantization error	Uniform	Δt_1
	User terminal clock correction device inaccuracy	Uniform	Δt_2
	User terminal transmit circuit logic jitters	Normal	σ_3
e_{sn}	Onboard phase error measurement inaccuracy	Normal	σ_4
	Onboard clock receive circuit logic jitters	Normal	σ_5

In the above table, the deterministic terms contained in the error ($r_n - r_{n-1}$) arising from Doppler shift and long term drift are ignored, since they are negligibly smaller than other terms for a typical clock correction period (0.5 s ~ 1 s). For example, the long term drift component of user terminal clock is 0.0001 ns, and the Doppler term is 0.0006 ns for a correction period of 1 s.

Three types of timing errors are derived in the following according to the statistical characteristic of each term. The first type, denoted by E_σ , is based the standard deviation and represents a typical error value. The second type, denoted by $E_{3\sigma}$, is the 3- σ value of the error and is a typical worst-case value. The third type, denoted by E_{max} , is the theoretical worst case which may rarely be seen in the actual system.

$$E_\sigma = \left[2(\sigma_1^2 + \sigma_2^2) + 2\left(\frac{1}{3}\Delta t_1^2 + \frac{1}{3}\Delta t_2^2 + \sigma_3^2\right) + 5(\sigma_4^2 + \sigma_5^2) \right]^{\frac{1}{2}}$$

$$E_{3\sigma} = 3E_\sigma$$

$$E_{max} = 6(\sigma_1 + \sigma_2) + 2(\Delta t_1 + \Delta t_2 + 3\sigma_3) + 3\sqrt{5}(\sigma_4 + \sigma_5)$$

In deriving E_{max} , three times the standard deviation was used for the error terms with normal distributions.

6.2.2.2 IC Numerical Examples

Table 6.2 shows typical error values and the resulting timing accuracy for IC-PPS, IC-VCO and IC-DCO techniques. The system parameters assumed are an uplink information bit rate of 2.048 Mbit/s with QPSK modulation and rate-1/2 FEC coding and a clock correction period of 1.024 s.

Table 6.2: Typical Timing Error Parameter values and Estimated Phase Errors for PLC-PPS, PLC-VCO and PLC-DCO Techniques

Term	Notation	Typical Value	IC-PPS	IC-VCO	IC-DCO
r_n	σ_1	0.3 ns	0.3 ns	0.3 ns	0.3 ns
	σ_2	~ 0	0 ns	0 ns	0 ns
e_{un}	Δt_1	see explanation below	2.7 ns	2.5 ns	5 ns
	Δt_2	see explanation below	1.4 ns	2 ns	0 ns
	σ_3	1 ns	1 ns	1 ns	1 ns
e_{sn}	σ_4	$T_s/100$	4.9 ns	4.9 ns	4.9 ns
	σ_5	1 ns	1 ns	1 ns	1 ns
		E_σ	11.5 ns	11.5 ns	12.0 ns
		$E_{3\sigma}$	34.5 ns	34.6 ns	35.9 ns
		E_{max}	55.5 ns	56.3 ns	57.3 ns

The numerical values in the above table are typical values which are based on manufacturers specification and/or implementation details. The user terminal short term stability (σ_1) of 3×10^{-10} (0.3 ns over 1.024 sec correction period) is typical for a low cost VCXO, while the onboard clock short term stability (σ_2) is typically two to three orders of magnitude better and hence is negligible in comparison.

User terminal clock correction quantization error (Δt_1) is assumed to be ± 2 degrees for the PPS which is typical with 8-bit control of phase shift. This translates to 2.7 ns at a symbol rate of 2.048 Msps. For the VCO, a $\pm 10^{-5}$ worst case normalized frequency accuracy (typical) and 12-bit control over that accuracy range results in a quantization error of 2.5 ns over the 1.042 s correction period. The DCO user terminal clock correction error (Δt_1) is based on a 100 MHz clock which is divided down to the 2.048 MHz symbol clock. Hence, a pulse deletion at 100 MHz results in a 10 ns phase step so that the quantization error from the desired clock phase will be at most half that value or 5 ns.

User terminal clock correction device inaccuracy (Δt_2) is a direct result of the nonlinearity and variations in characteristics among the clock correction devices which may even become more apparent with aging. For example, the VCO transfer characteristics exhibit a certain nonlinearity (see Figure 5.5) which may require initial calibration for precise frequency control. However, even with initial calibration, these characteristics may shift which would require additional compensation. If the change in characteristics is simply a linear translation (i.e. the actual shape does not change), compensation will be easier to implement. However, if the transfer characteristic also changes with aging, recalibration may become necessary. Hence it becomes clear that in a low cost implementation, precise frequency (or phase) control is impractical and certain allocation must be made for errors introduced by device inaccuracies. In the PPS case, a 1-deg additional error is assumed based on typical PPS characteristics which translates to 1.4 ns at a symbol rate of 2.048 Msps. For the VCO case, a 2-ns error is derived by assuming a worst case inaccuracy of 10% in the VCO characteristics, and a worst case

correction of 20 ns over a correction period (approx. 4% of a symbol period). The DCO technique, by virtue of digital pulse deletion control, does not suffer from device inaccuracy errors.

User terminal transmit circuit logic jitters (σ_3) and onboard clock receive circuit logic jitters (σ_5) are assumed to be 1 ns which is typical for CMOS/TTL technology. Onboard phase error measurement inaccuracy (σ_4) is assumed to be 1 % of a symbol period as discussed in section 4.3.

6.2.2.4 IC Simulation Results

Computer simulation of the three IC control techniques was performed with the same parameters used in the IC timing analysis numerical examples above. Table 6.3 provides a summary of the IC simulation parameters.

Table 6.3: Independent Clock Simulation Parameters

Information Bit Rate	2.048 Mbit/s
Modulation	QPSK with R-1/2 FEC Coding
Symbol Period (T_s)	488 ns
Clock Correction Interval	1.024 s
Onboard Measurement Error	$T_s/100$
Doppler Shift	8×10^{-9} (One Way Satellite to Earth)
Terminal Clock Drift	1×10^{-7}
Satellite Clock Drift	1×10^{-9}
DCO Frequency	100 MHz

Simulation results for IC-PPS technique are given in Figure 6.6. The simulation run was performed over 40 seconds and showed the phase error performance to be in agreement with the analysis results. All recorded values fall within the $E_{3\sigma}$ range of ± 34.5 ns as predicted in the analysis. This performance however may be inadequate for a bit synchronous system if the phase error values were limited to fall within $\pm 5\%$ of a symbol period (± 24.4 ns at 2.048 Msps). However, if a wider range of phase error (and consequently higher degradation in SNR) is tolerable, the IC-PPS performance may be adequate.

Figure 6.7 shows the simulation results for the IC-VCO technique over a 40 s simulation run. Here again the simulation results are within close agreement with the analysis results which predict an $E_{3\sigma}$ of 34.6 ns. As can be seen from this figure, the simulation values all fall within the expected range. However, as in the case of the IC-PPS technique, the performance is still short of the desirable timing error of 5% of a symbol period (± 24.4 ns at 2.048 Msps).

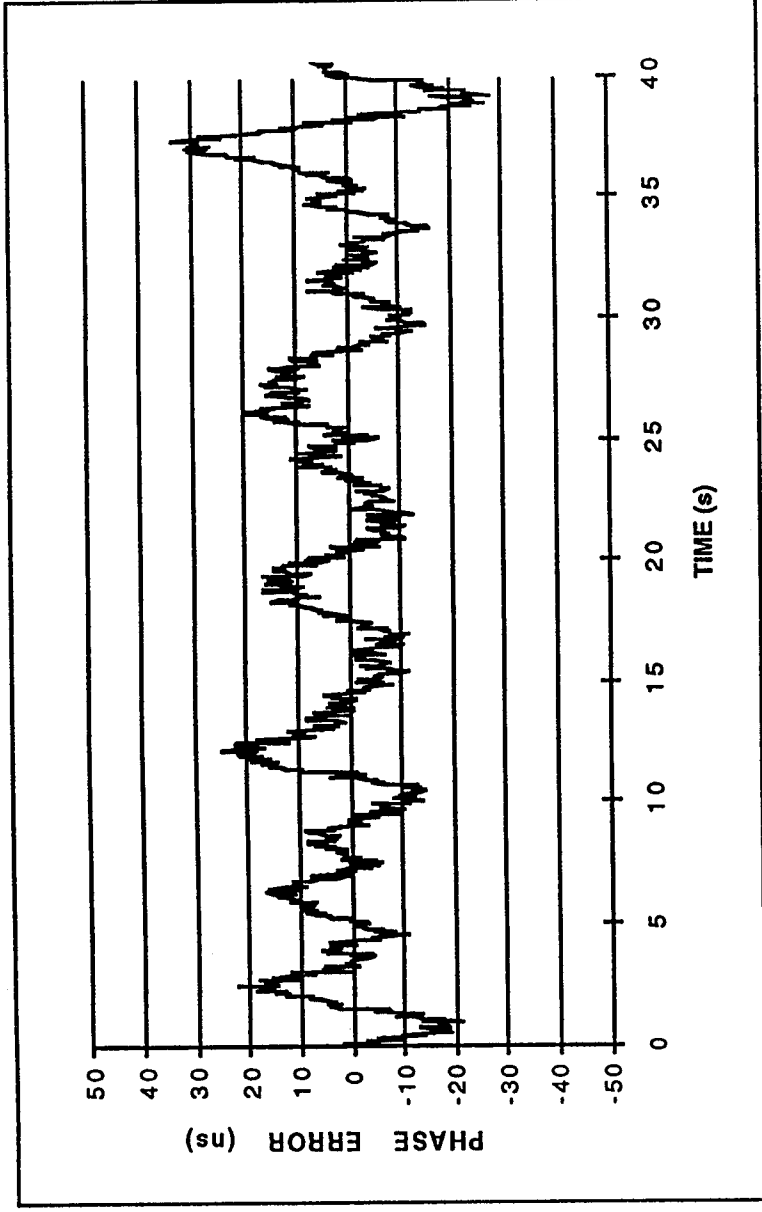


Figure 6.6: IC-PPS Simulation Results

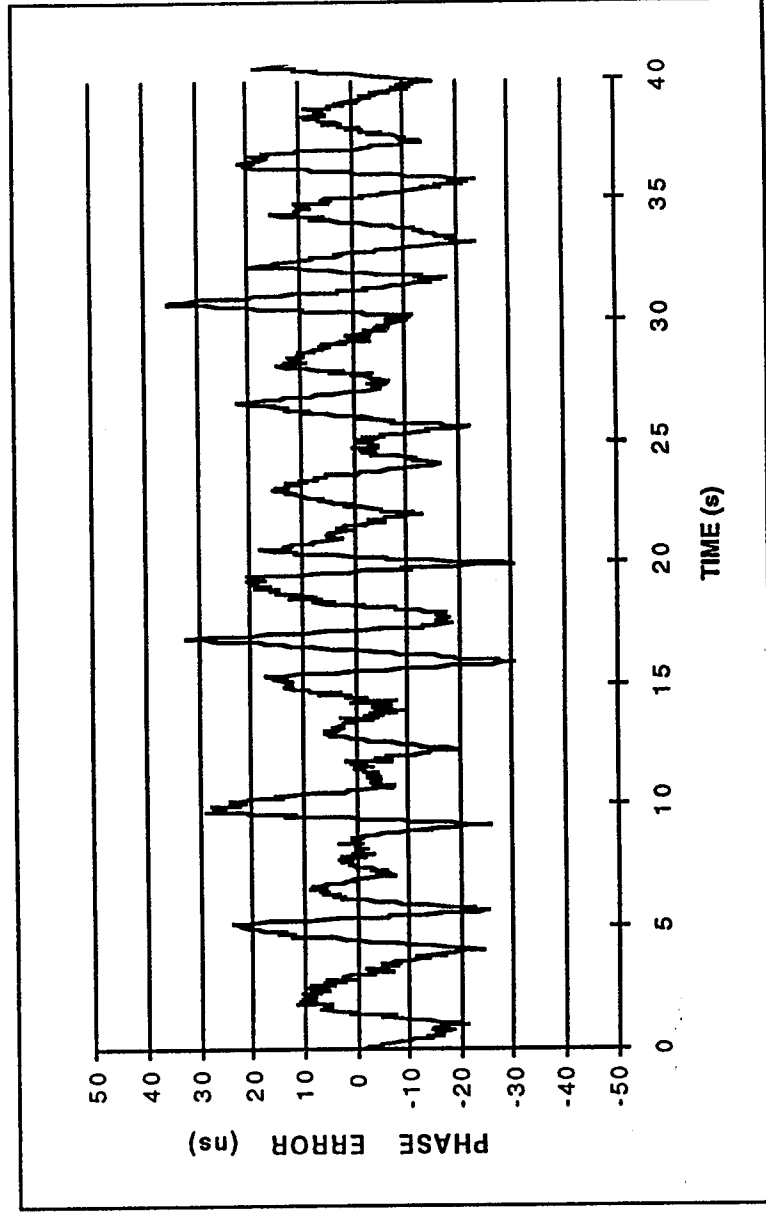


Figure 6.7: IC-VCO Simulation Results

Finally, Figure 6.8 shows the simulation results for the IC-DCO technique. Here too the simulation results seem to support the analytical value derived earlier in that all except one simulation value fall within the $E_{3\sigma}$ range predicted by the analysis. As in the case of the IC-PPS and IC-DCO techniques, the worst case timing error exceeds $\pm 5\%$ of the symbol period.

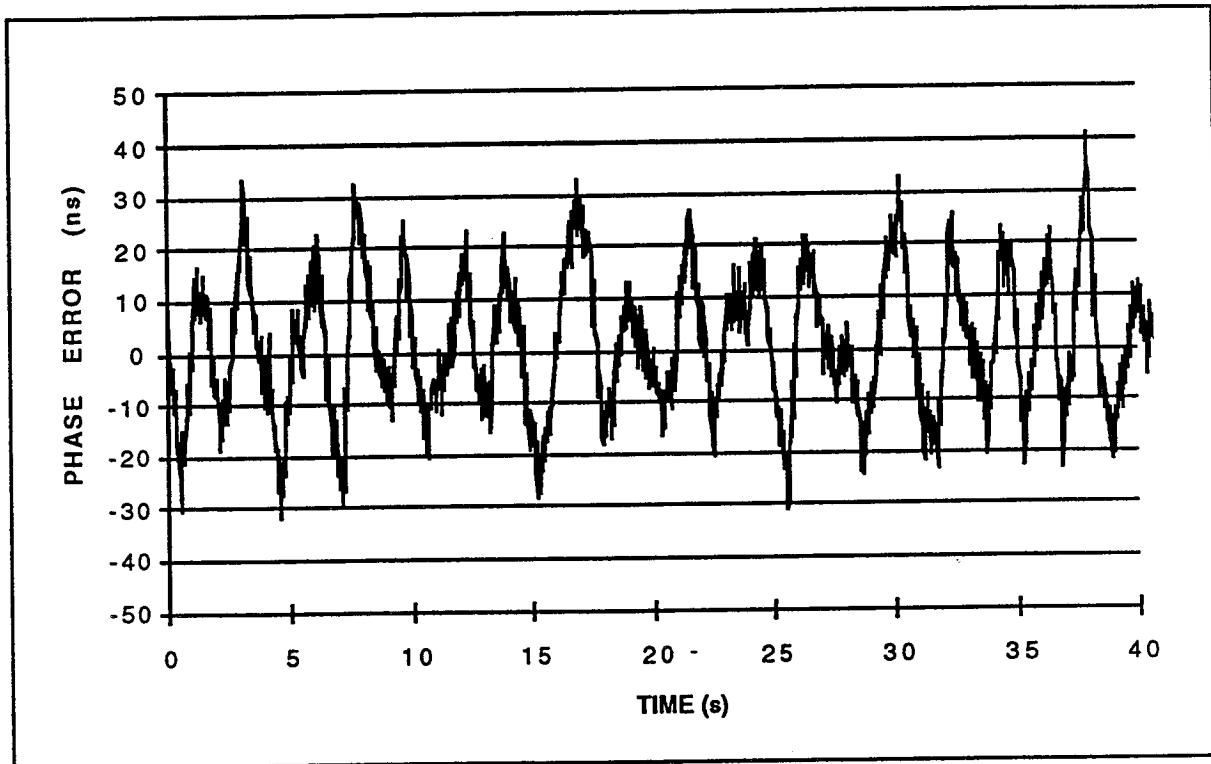


Figure 6.8: IC-DCO Simulation Results

6.2.2.5 Stability Problem

The previous analysis of the IC control techniques has demonstrated their inadequacy in meeting bit synchronous timing requirements at least with the representative parameters used in the simulation. The IC techniques also exhibit unstable operation under certain conditions. This is primarily due to the time lag between onboard phase error measurement and user terminal clock correction. Clock drift prediction is performed based on the phase error measurement made about 175 ms earlier (125-ms propagation delay and 50-ms processing time) and exhibits unstable operation for a short correction interval [15]. Figure 6.9 illustrates the instability problem in a simulation run using the IC-PPS technique with a shorter correction period of 512 ms and a terminal clock drift of $1.0E-6$. The instability problem may be avoided by selecting a long correction period, such as 1.024 s or longer.

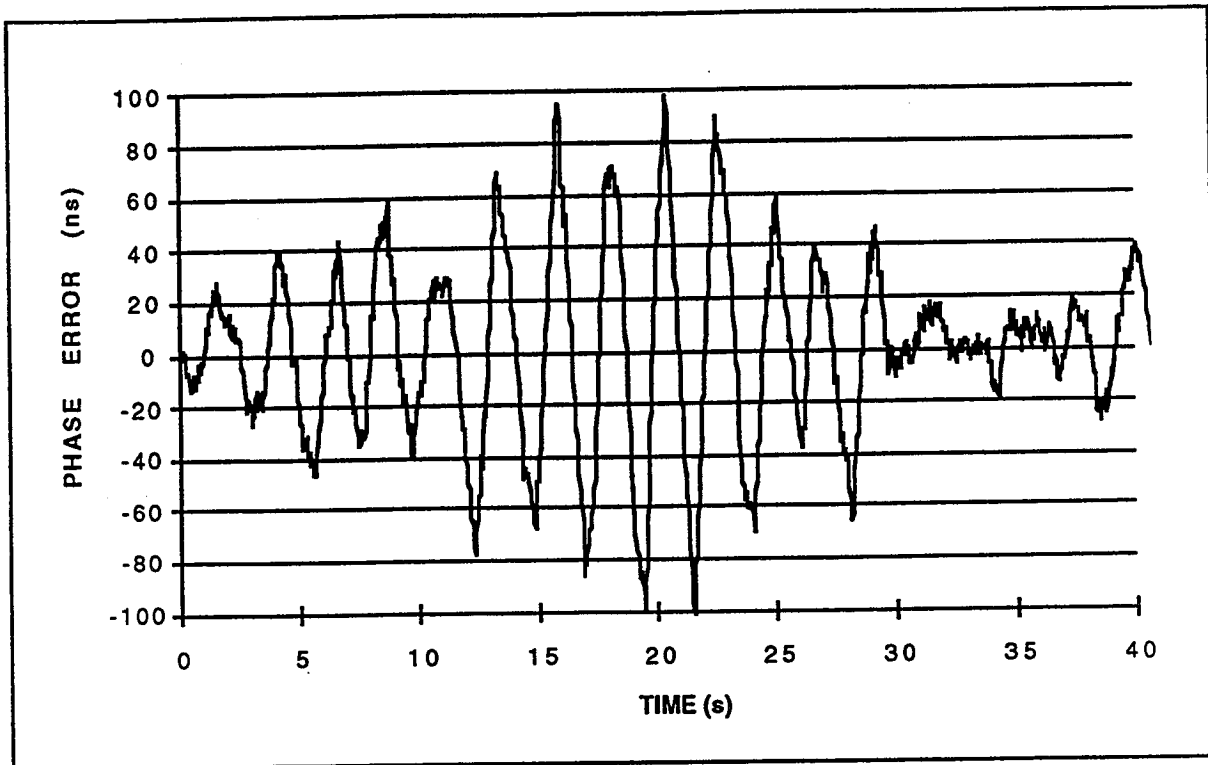


Figure 6.9: Illustration of Potential Stability Problem in IC techniques

6.2.2.6 Summary of IC Approach

The above analysis and simulation of the IC approach has shown that the control system is sensitive to the clock drift of the user terminal, especially its short term component. However, the dominant error component is the inaccuracy resulting from the onboard error measurement. In the absence of all other sources of error, the onboard error measurement accuracy must be better than $1/140$ of a symbol period to achieve a 5% accuracy or about a 0.5 dB degradation in E_b/N_0 performance. The strict error measurement accuracy requirement plus the potential instability problem discussed above, tend to preclude this approach from being recommended for implementation in a bit synchronous system.

6.2.3 Phase Locked Clock (PLC) Control Technique

The major advantage of the PLC clock control technique is the availability of onboard clock at the user terminal. Direct loopback of an onboard clock will exhibit a small phase offset at the satellite over a correction period. For example, a correction period of one second yields a phase shift of about 16 ns due to round-trip satellite Doppler. Thus, the user terminal is only required to adjust its transmit clock phase once in a correction period. Other advantages are low cost implementation and very predictable operation.

The timing correction procedure for the phase-locked clock is shown in Figure 6.10. Here, only one user terminal clock correction is made during a correction period. The value of the correction is derived directly from the onboard error measurement which is performed once per correction period and transmitted down to the user terminal.

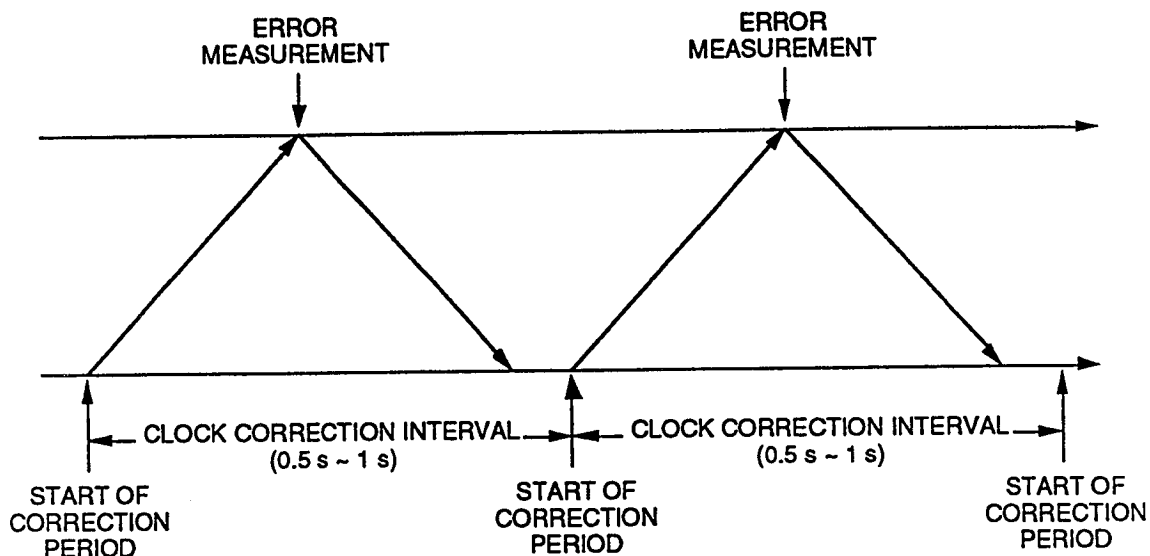


Figure 6.10: Timing Correction Procedure for PLC

The following subsections present the phased locked clock control model and derive expressions for timing accuracy. Timing errors are plotted as a function of TDMA bit rate and onboard timing measurement inaccuracy. Simulation results are also provided to verify analytical results.

6.2.3.1 PLC Timing Analysis

An analytical model for PLC timing control is shown in Figure 6.11. The onboard clock, f_s , generates a downlink signal with an injected timing error of e_{st} . The signal will incur a nominal one-way propagation delay of T_D and an additional delay, e_{dd} , due to satellite motion. The user terminal introduces an error, e_{ur} , in the process of demodulation and generation of a phase-locked terminal clock. This clock is adjusted by the amount of phase error measured at the satellite. The user terminal further adds a transmit error term e_{ut} in the process of generating and transmitting the TDMA bursts. The transmitted signal will be delayed by the amount of the nominal propagation delay, T_D , and uplink Doppler, e_{du} . The signal received at the satellite will experience various measurement errors, e_{sr} , caused by clock jitters, sampling quantization, non-ideal phase estimation and data quantization prior to the transmission of measured phase error.

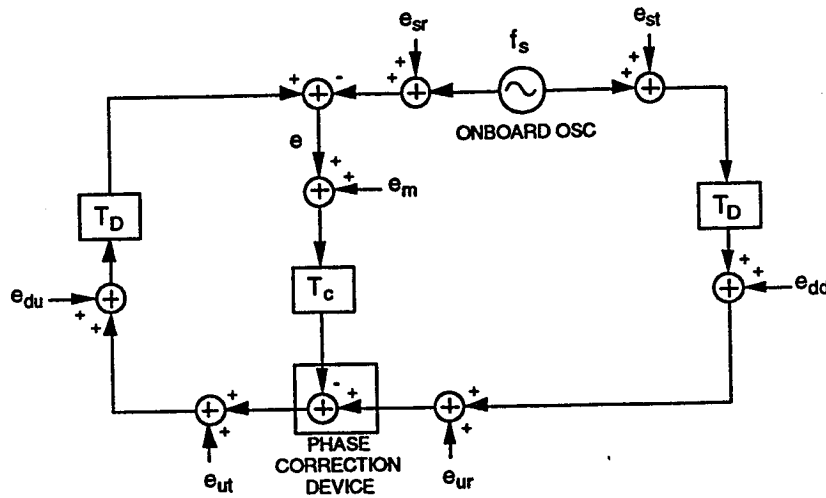


Figure 6.11: Analytical Model for PLC Timing Control

From this model, the onboard phase error is given by the following expression:

$$\begin{aligned}
 e &= -e_{sr} + e_{st} + e_{dd} + e_{ur} + e_m + e_{ut} + e_{du} \\
 &= -e_{sr} + e_{st} + e_d + e_{ur} + e_m + e_{ut}
 \end{aligned}$$

where $e_d (= e_{dd} + e_{du})$ is the combined downlink and uplink Doppler component. Each error term is further divided into error components with statistical characteristics as shown in Table 6.4.

Table 6.4: PLC Error Components and Statistical Characteristics

Term	Components	Distribution	Notation
e_{sr}	Onboard clock short-term stability	Normal	σ_1
	Onboard clock receive circuit logic jitters	Normal	σ_2
e_{st}	Onboard clock short-term stability	Normal	σ_3
	Onboard transmit circuit logic jitters	Normal	σ_4
e_d	Incremental time delay caused by Doppler during one correction period	Deterministic	$2\rho_d T_c$
e_{ur}	User terminal receive circuit logic jitters	Normal	σ_5
	User terminal PLL phase error	Normal	σ_6
e_m	Onboard phase error measurement inaccuracy	Normal	σ_7
e_{ut}	User terminal clock correction quantization	Uniform	Δt_1
	User terminal clock correction device inaccuracy	Uniform	Δt_2
	User terminal transmit circuit logic jitters	Normal	σ_8

In the above table, symbols ρ_d and T_c denote one-way Doppler shift (i.e., 8×10^{-9} for 0.1° inclination) and the clock correction period, respectively.

Three types of timing errors are derived in the following according to the statistical characteristic of each term. The first type, denoted by E_σ , is based the standard deviation and represents a typical error value. The second type, denoted by $E_{3\sigma}$, is the 3σ value of the error and is a typical worst-case value. The third type, denoted by E_{\max} , is the theoretical worst case which may rarely be seen in the actual system.

$$E_\sigma = \left(\sum_{n=1}^8 \sigma_n^2 + \frac{1}{3} \Delta t_1^2 + \frac{1}{3} \Delta t_2^2 \right)^{\frac{1}{2}} + 2\rho_d T_c$$

$$E_{3\sigma} = 3 \left(\sum_{n=1}^8 \sigma_n^2 + \frac{1}{3} \Delta t_1^2 + \frac{1}{3} \Delta t_2^2 \right)^{\frac{1}{2}} + 2\rho_d T_c$$

$$E_{\max} = 3 \sum_{n=1}^8 \sigma_n + \Delta t_1 + \Delta t_2 + 2\rho_d T_c$$

As in the IC error analysis, E_{\max} assumes a worst-case error value of 3σ for an error term with normal distribution.

The above equations are evaluated for typical system parameters in the following subsection.

6.2.3.2 PLC Numerical Examples

Typical system parameters for various timing error components are shown in Table 6.5 along with numerical examples for the PLC-PPS and PLC-DCO techniques.

The values given in the above table are based on the following assumptions. The phase measurement error, σ_7 , is assumed to be one hundredth of a symbol period and 4.9 ns for the information rate of 2.048 Mbit/s with rate-1/2 coding and QPSK modulation. This is equivalent to a typical worst-case value to 14.7 ns (3σ value). The Doppler term assumes a station keeping accuracy of $\pm 0.1^\circ$ in inclination and drift which yields about 8 ns/s of phase error. The clock correction cycle is 512 ms. The DCO output frequency is 100 MHz, corresponding to a basic correction inaccuracy of 5 ns. The PPS clock correction quantization accuracy of 0.1 ns is based on 12-bit quantization over a symbol period. PPS clock correction device inaccuracy is based on an assumption of 1 degree uncertainty in the voltage-phase transfer curve..

The typical worst-case phase errors, $E_{3\sigma}$, are 25.5 ns and 26.5 ns for PPS and DCO. These values correspond to 5.2 percent and 5.4 percent of a symbol period. This example illustrates that implementation of a bit synchronous system at 2.048 Mbit/s is feasible.

Table 6.5: Typical Timing Error Parameter Values and Estimated Phase Errors for the PLC-PPS and PLC-DCO Techniques

Term	Notation	Typical Value	PLC-PPS	PLC-DCO
e_{sr}	σ_1	~ 0	0 ns	0 ns
	σ_2	1 ns	1 ns	1 ns
e_{st}	σ_3	~ 0	0 ns	0 ns
	σ_4	1 ns	1 ns	1 ns
e_d	$2\rho_d T_c$	$2\rho_d T_c$	8.2 ns	8.2 ns
e_{ur}	σ_5	1 ns	1 ns	1 ns
	σ_6	1 ns	1 ns	1 ns
e_m	σ_7	$T_g/100$	4.9 ns	4.9 ns
e_{ut}	Δt_1	see explanation below	0.1 ns	5 ns
	Δt_2	see explanation below	1.4 ns	N/A
	σ_7	1 ns	1 ns	1 ns
		E_σ	13.6 ns	14.3 ns
		$E_{3\sigma}$	25.5 ns	26.5 ns
		E_{max}	39.3 ns	42.9 ns

Among the error components given in the above table, three terms are dominant: the phase measurement error, Doppler component and DCO correction resolution. The phase measurement error can be reduced significantly by an averaging technique, although this will consume some transponder capacity. The potential improvement factor with averaging will be described in a later section. The Doppler error term given in the table is a worst-case value and occurs only when the inclination approaches the station keeping maximum. This error term can be reduced with better station keeping and also with a Doppler prediction technique which will be described later. The DCO error component can be made smaller with the use of a higher frequency oscillator. However a higher frequency oscillator will add circuit complexity in the form of high-speed logic and a larger programmable divider.

6.2.3.3 PLC Parametric Analysis

Figures 6.12 and 6.13 illustrate the effect of the onboard phase measurement error on the overall phase error when supporting different bit rates ranging from 100 kbit/s to 10 Mbit/s. Figure 6.12 applies to the PLC-PPS technique while Figure 6.13 shows the parametric results for the PLC-DCO technique.

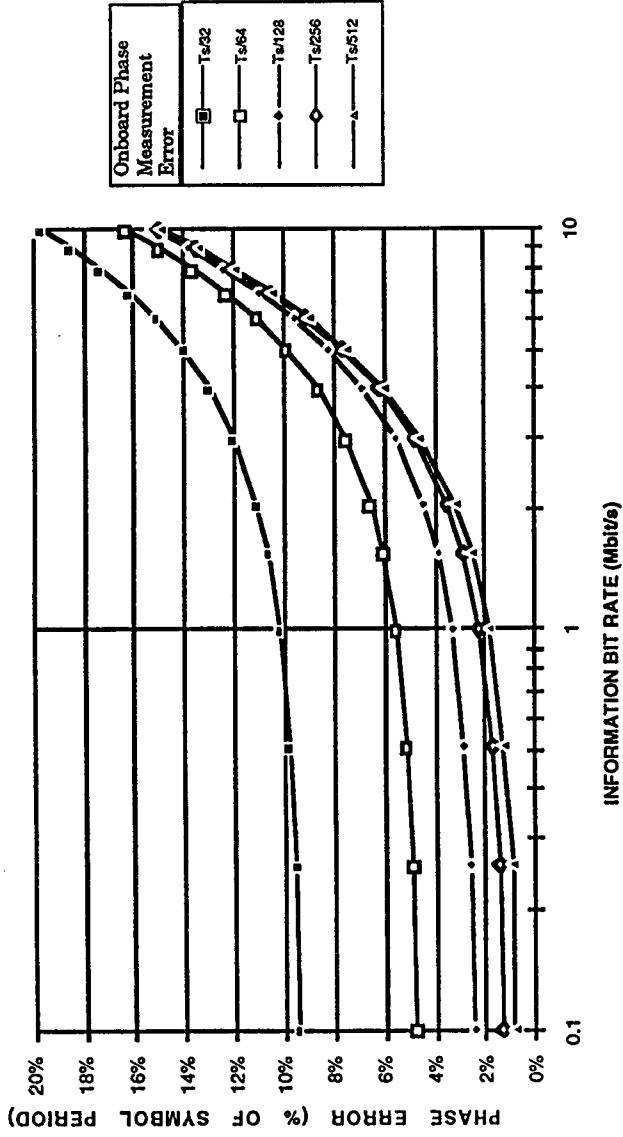


Figure 6.12: Phase Error ($E_{3\sigma}$) vs. Bit Rate (PLC-PPS, $T_c = 512$ ms)

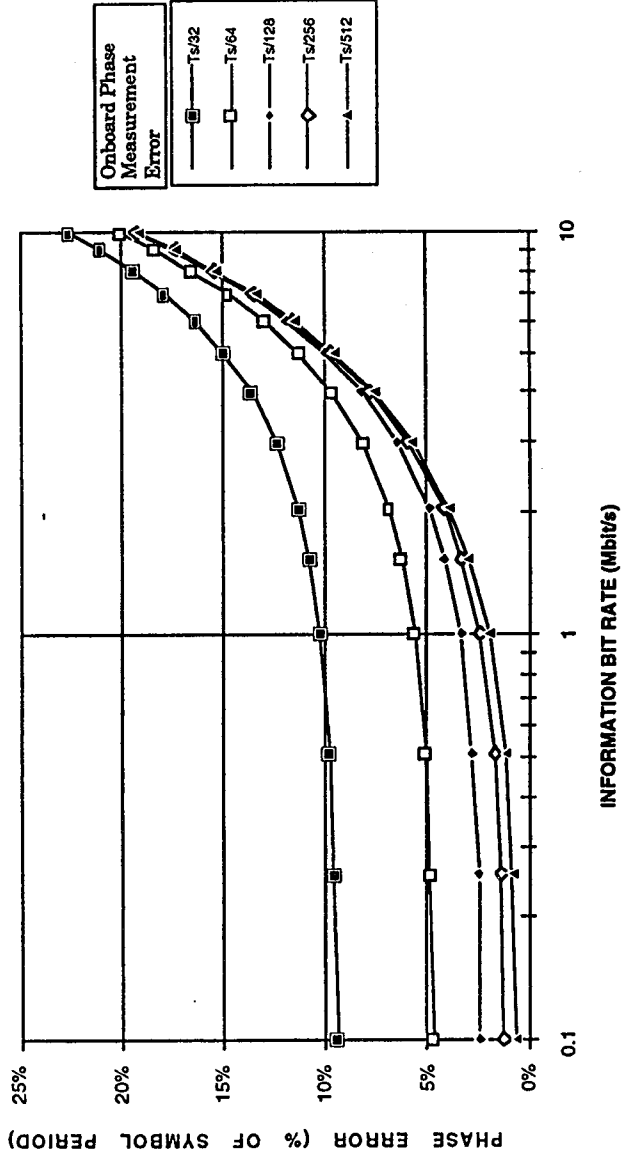


Figure 6.13: Phase Error ($E_{3\sigma}$) vs. Bit Rate (PLC-DCO, $T_c = 512$ ms)

The above figures show that both techniques can support bit rates over 2 Mbps when the onboard phase measurement error is limited to 1/128 of a symbol period and the overall phase error ($E_{3\sigma}$ value) is 5%. Slightly higher bit rates can be supported if the phase measurement accuracy is increased. On the other hand, a lower onboard phase

measurement accuracy results in a significantly lower supportable bit rate for the same phase error criterion.

6.2.3.4 PLC Simulation Results

Computer simulation of the two PLC control techniques was performed with the same parameters used in the PLC timing analysis numerical examples above. Table 6.6 provides a summary of the PLC simulation parameters.

Table 6.6: Phase-Locked Clock Simulation Parameters

Information Bit Rate	2.048 Mbit/s
Modulation	QPSK with R-1/2 FEC Coding
Symbol Period (T_s)	488 ns
Clock Correction Interval	512 ms
Onboard Measurement Error	$T_s/100$
Doppler Shift	8×10^{-9} (One-Way Satellite to Earth)
Satellite Clock Drift	1×10^{-9}
DCO Frequency	100 MHz

Simulation results for PLC-PPS technique are given in Figure 6.14. The simulation run was performed over 40 seconds. The phase error performance is in close agreement with the analysis results, and virtually all simulation values fall within the $E_{3\sigma}$ range of ± 25.5 ns as predicted in the analysis.

Simulation results for PLC-DCO technique are given in Figure 6.15. The simulation run was also performed over 40 seconds and shows the phase error performance to be in agreement with the analysis results. Almost all the simulation values fall within the $E_{3\sigma}$ range of ± 26.5 ns as predicted in the analysis.

It is clear from the above figures that the phase error values reflect a bias term which causes the average of the phase error to be non zero. This term is the incremental time delay caused by residual Doppler over one correction period. This residual error is due to the inherent delay between the time a correction is made at the ground terminal and the time a phase error measurement is made onboard the satellite. By the time the correction is made and measured onboard, the phase error due to Doppler would have already increased beyond the correction value.

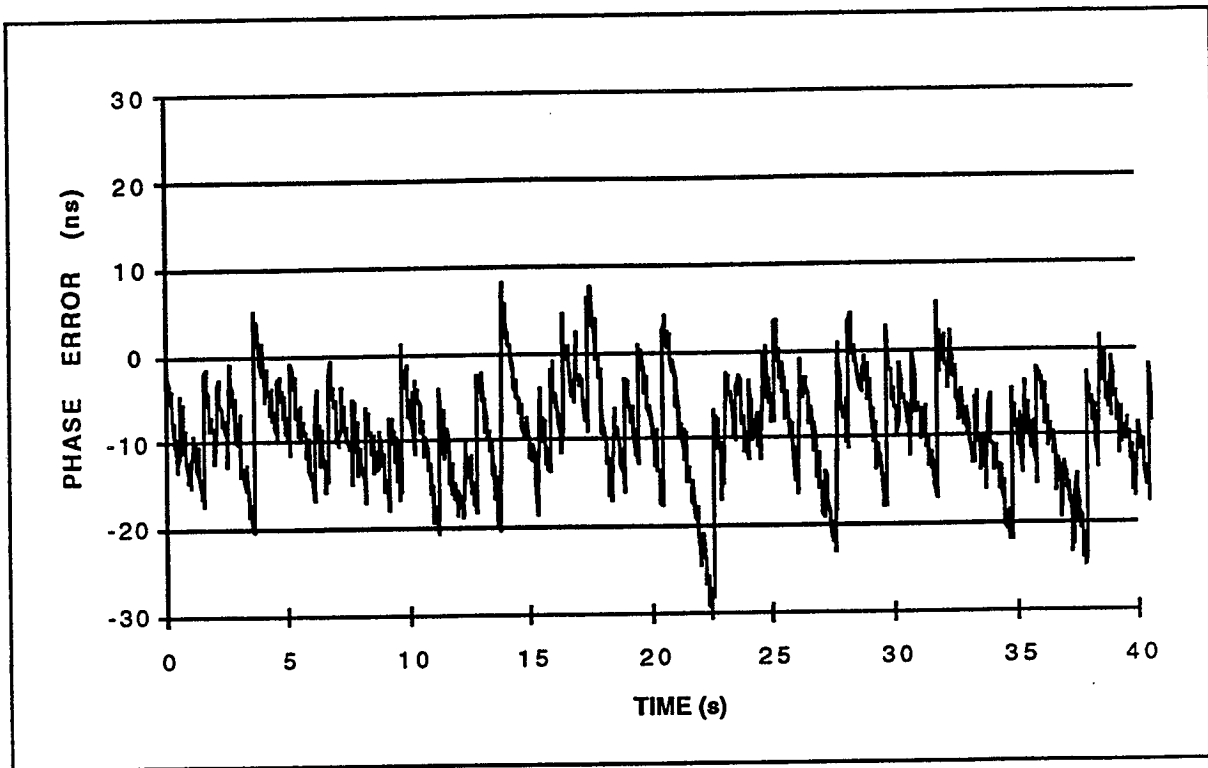


Figure 6.14: PLC-PPS Simulation Results

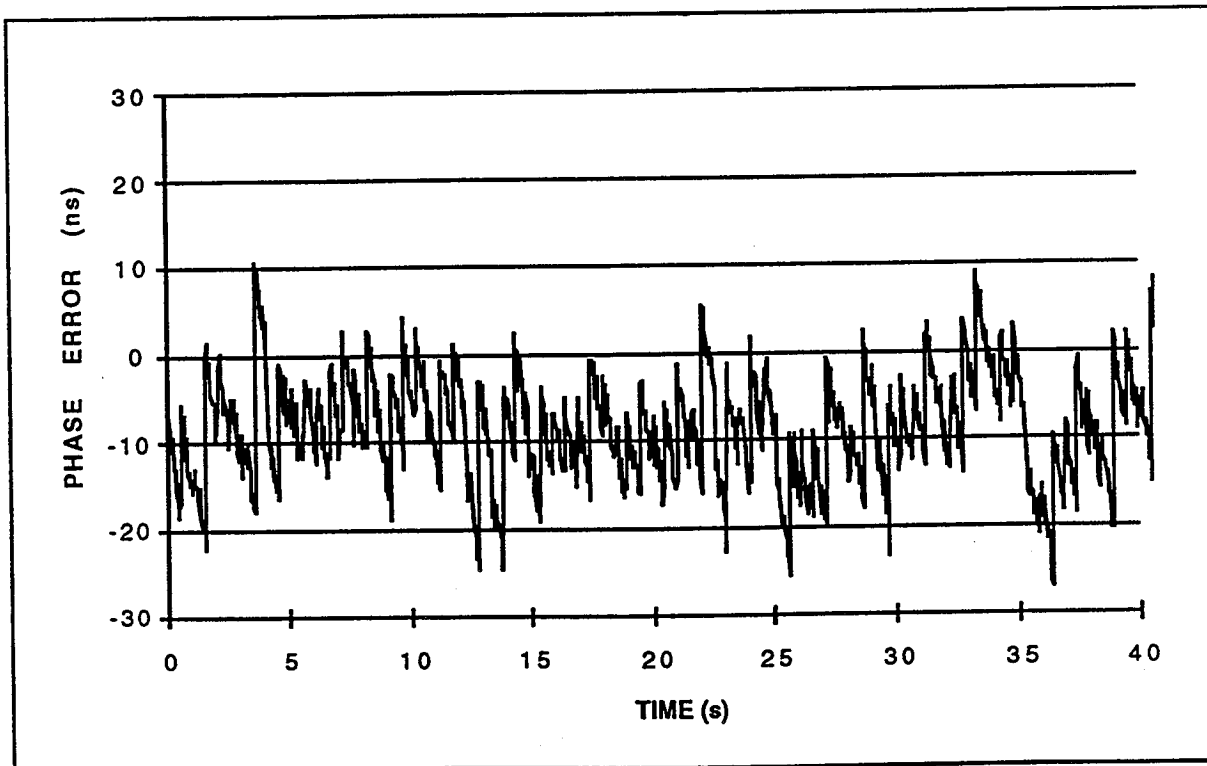


Figure 6.15: PLC-DCO Simulation Results

The increase in phase error due to incremental Doppler suggests that incorporating a Doppler prediction technique which will compensate for this effect can help reduce the overall phase error for a given supportable bit rate. Alternatively, it could increase the supportable bit rate for a given overall phase error value. This will be discussed in the next subsection which explores different techniques for further reducing the overall phase error.

6.2.3.5 Techniques for reducing phase error in PLC approach

There are two techniques that can be used with the PLC approach to further reduce the overall phase error. The first technique relies on averaging multiple onboard error measurements during the correction period which would reduce the variance of the random component in the error measurement. The second technique, which was alluded to earlier, involves residual Doppler prediction and correction to remove the deterministic fixed bias component from the phase error term.

6.2.3.5.1 Multiple Error Measurements in Correction Period

This is a simple technique which involves taking multiple error measurements in a correction period and averaging these measurements to reduce the variance of the phase error. As long as the error components in the averaged measurements are statistically independent, the variance of the error will be reduced by the square root of the number of averaged measurements. Figure 6.16 shows the effect of averaging on the variance of the error.

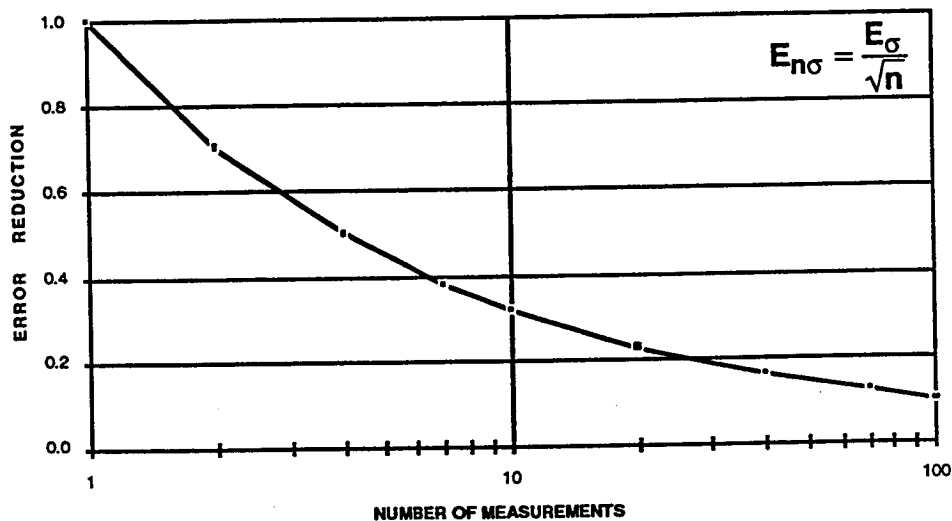


Figure 6.16: Effect of Averaging on Statistical Phase Error

The principal drawback to the above technique of averaging multiple onboard phase error measurements is that a user terminal would have to transmit multiple synchronization bursts in a correction period. This results in increased overhead associated with multiple measurements. However, the payoff in terms of a higher supportable bit rate may offset the required increase in overhead. Technically, the number of measurements is better kept small. However, even as few as three averaged measurements per correction period could potentially reduce the random component of phase error by up to 50 % (Figure 6.16).

Although the multiple error measurements naturally must be taken onboard the satellite, the averaging process may be performed either onboard the satellite or at the user terminal. In either case, the improvement will be the same.

6.2.3.5.2 Doppler Correction

There are two methods of performing Doppler correction at the user terminal so as to reduce or eliminate the incremental time delay caused by Doppler during a correction period. Both methods attempt to predict the magnitude of the Doppler component and to compensate for it.

The first method, shown in Figure 6.17, is based on measuring the difference between two delay values, where a delay value is the timing offset between the transmit frame and receive frame at the user terminal. The measured time difference is

$$\Delta T = T_u - T_n = 2(n-1)\rho_d T_c$$

where ρ_d is the Doppler shift. Small multiple corrections (e.g. 5 times) are then performed over a correction period to compensate for ρ_d .

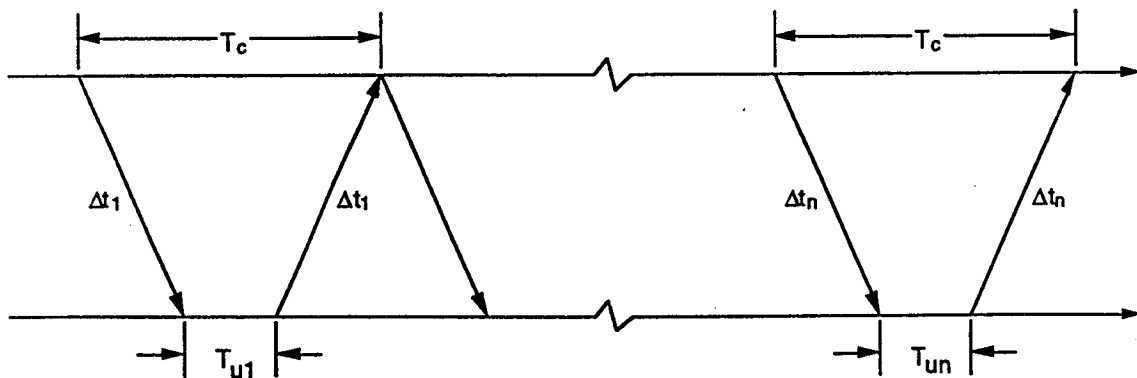


Figure 6.17: Transmit and Receive Frame Time Difference Measurements

This Doppler correction method helps reduce the incremental time delay caused by Doppler roughly by a factor of m , where m is the number of corrections over a clock correction period. The Doppler measurement error introduced by this method is very small on the order of ± 0.3 ns.

A linear prediction error is also introduced by assuming that the Doppler variations are linear in nature. This prediction error is also very small, especially for short prediction time intervals (on the order of minutes). Figure 6.18 shows the magnitude of the linear prediction error for Doppler correction as a function of the prediction time interval. From this figure, the worst case value over a ten minute prediction interval is still quite small (around 0.5 ns per second). For shorter prediction time intervals and during the zero crossing (zero phase) portion of the Doppler cycle, the linear prediction error becomes negligible.

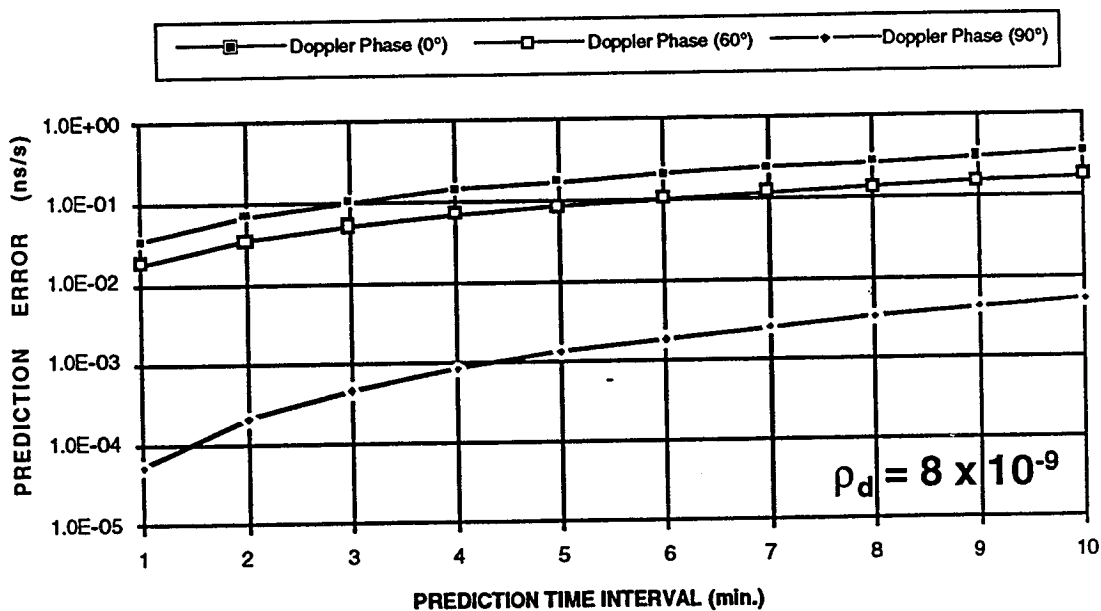


Figure 6.18: Linear Prediction Error for Doppler Correction

An alternative approach to Doppler correction is to use an averaging method where the onboard phase error measurements over n correction periods are averaged to get an estimate of the average phase error over one correction period. This estimate reflects the Doppler contribution in one correction period. Once an initial estimate is obtained and compensated for in the phase error corrections, a running average can then be taken to update an estimate of the residual error and further compensate for it.

The drawback of the averaging approach to Doppler prediction is that it is only effective for relatively small values of Doppler. For large Doppler values or high speed applications, the former Doppler prediction technique may be used first then the averaging technique may be applied to fine tune the estimates given by the first technique.

6.2.3.5.3 Parametric Analysis with Doppler Correction

The results of a parametric analysis of the PLC-PPS technique with Doppler correction are shown in Figures 6.19 and 6.20. The results in Figure 6.20 also include, in addition to Doppler prediction, averaging over multiple error measurements (3 to be exact) in a correction period.

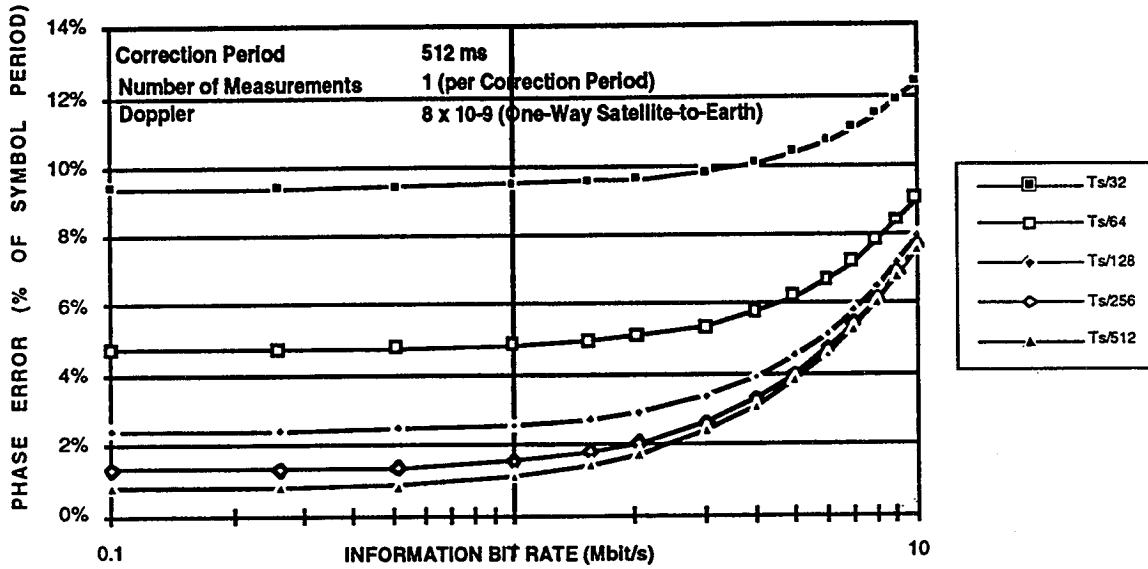


Figure 6.19: Parametric Analysis Results with Doppler Correction

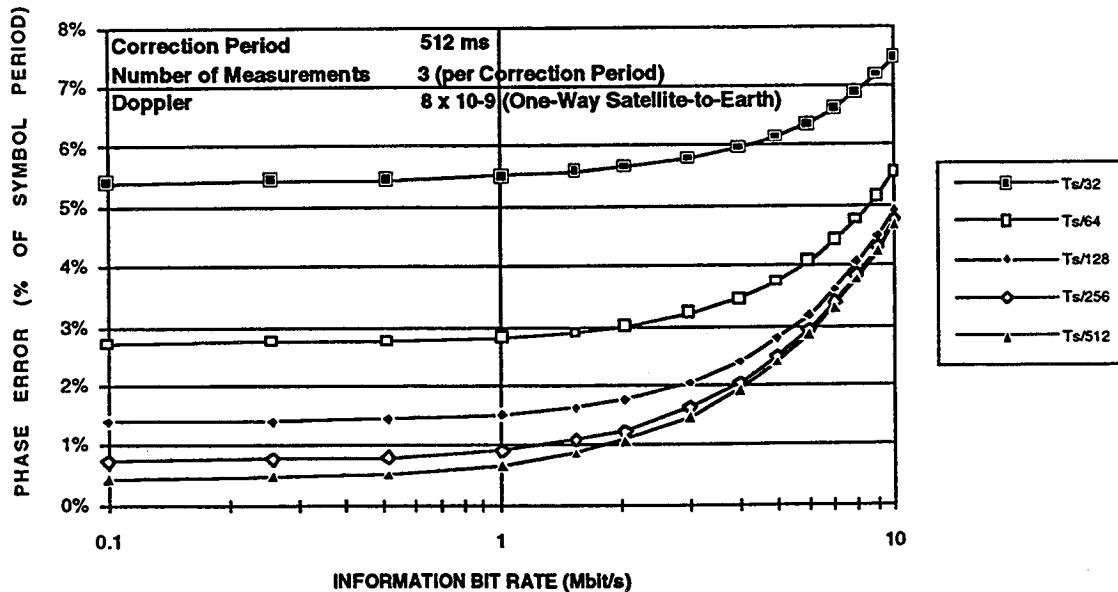


Figure 6.20: Parametric Analysis Results with Doppler Correction and Multiple Measurements

Both of the above figures show that with Doppler prediction, the PLC-PPS technique can support bit rates over 8 Mbps when the onboard phase measurement error is limited to 1/128 of a symbol period and the overall phase error ($E_{3\sigma}$ value) is 5%. This is a marked improvement over the results which were obtained without Doppler correction using the same PLC-PPS approach. The PLC-DCO approach is expected to give slightly lower values in terms of the maximum supportable bit rate. From an implementation standpoint the PLC-DCO approach would require a high frequency oscillator and high-speed logic, and hence the PLC-PPS approach would be more preferred.

6.2.3.5.4 Simulation Results with Multiple Measurements and Doppler Correction

In order to verify analytical results, computer simulations were made of the PLC-PPS approach both with multiple error measurements per correction period and with Doppler correction. Figure 6.21 shows the simulation results without any Doppler correction but with 3 phase error measurements in a 512 ms correction period. The improvement in the phase error performance can be clearly observed by comparing the results to those shown earlier in Figure 6.14 which are based on only one measurement per correction period. The incremental time delay error component caused by Doppler can still be seen in the results of this simulation run which did not include any Doppler correction.

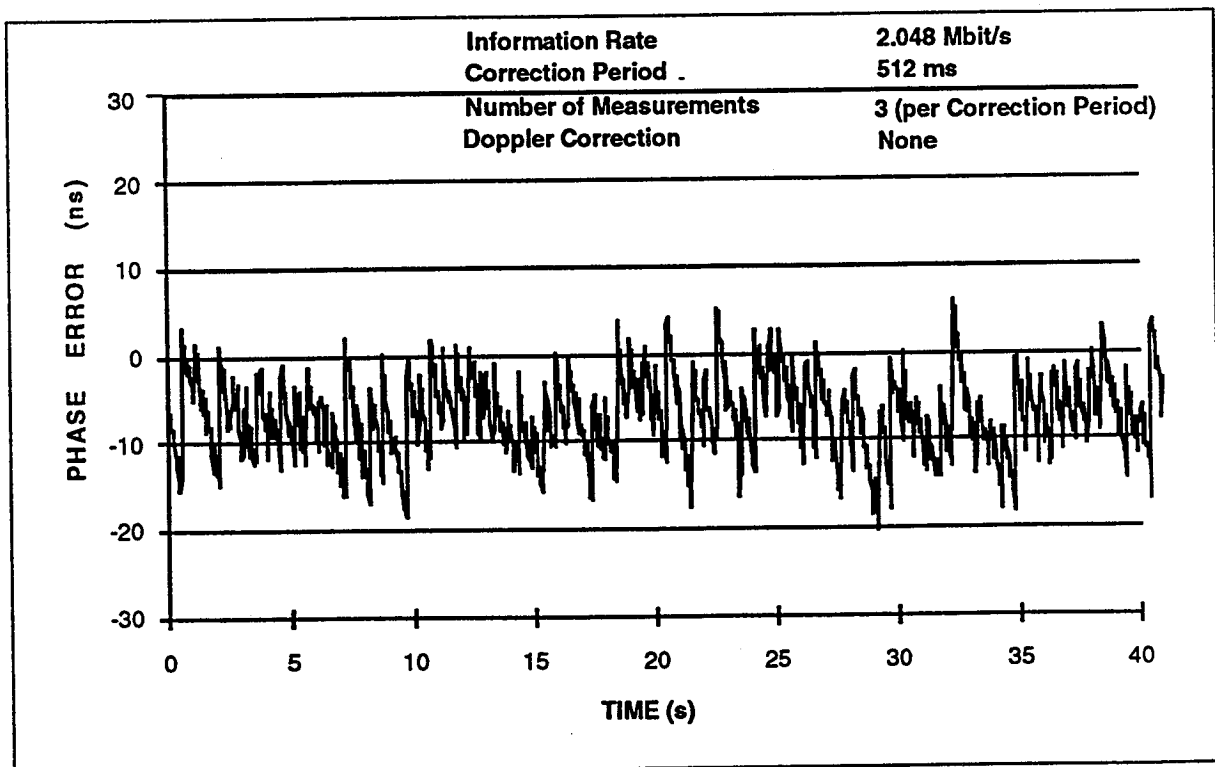


Figure 6.21: PLC-PPs Simulation Results with Multiple Measurements

Figure 6.22 shows simulation results which include Doppler correction but with only one phase error measurements in a 512 ms correction period. These results are similar in variance to those given in Figure 6.14 earlier except that the average phase error is now close to zero after Doppler correction (10 second averaging period for Doppler correction).

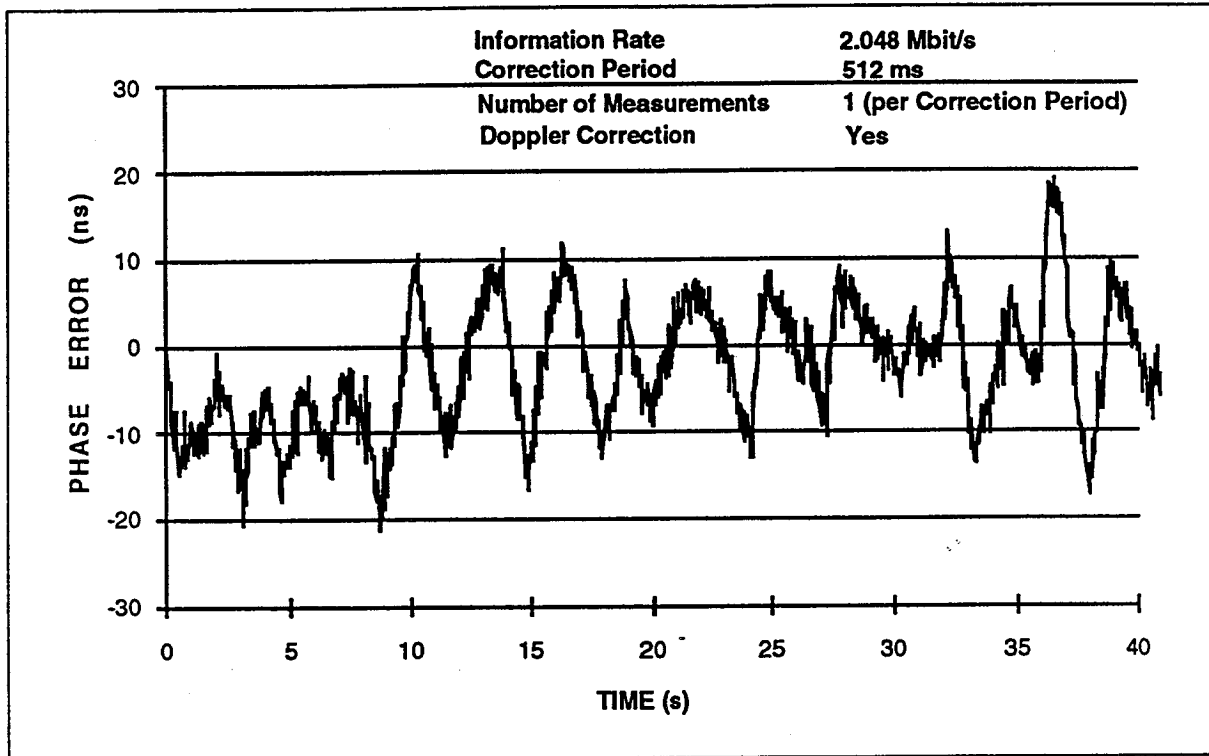


Figure 6.22: PLC-PPS Simulation Results with Doppler Correction

Finally, Figure 6.23 shows simulation results for 10 Mbps information rate which include Doppler correction as well as 3 phase error measurements in a 512 ms correction period. These results reflect the best error performance with small phase error variance and close to zero phase error average after Doppler removal (20 s Doppler prediction interval).

6.2.3 Summary of PLC Approach

Table 6.7 shows a summary of the maximum supportable data rates using the PLC-PPS approach. Slightly lower data rates are also supportable using the PLC-DCO approach. However, as mentioned earlier, higher frequency DCOs are required which makes the PLC-DCO technique less attractive compared to the PLC-PPS technique.

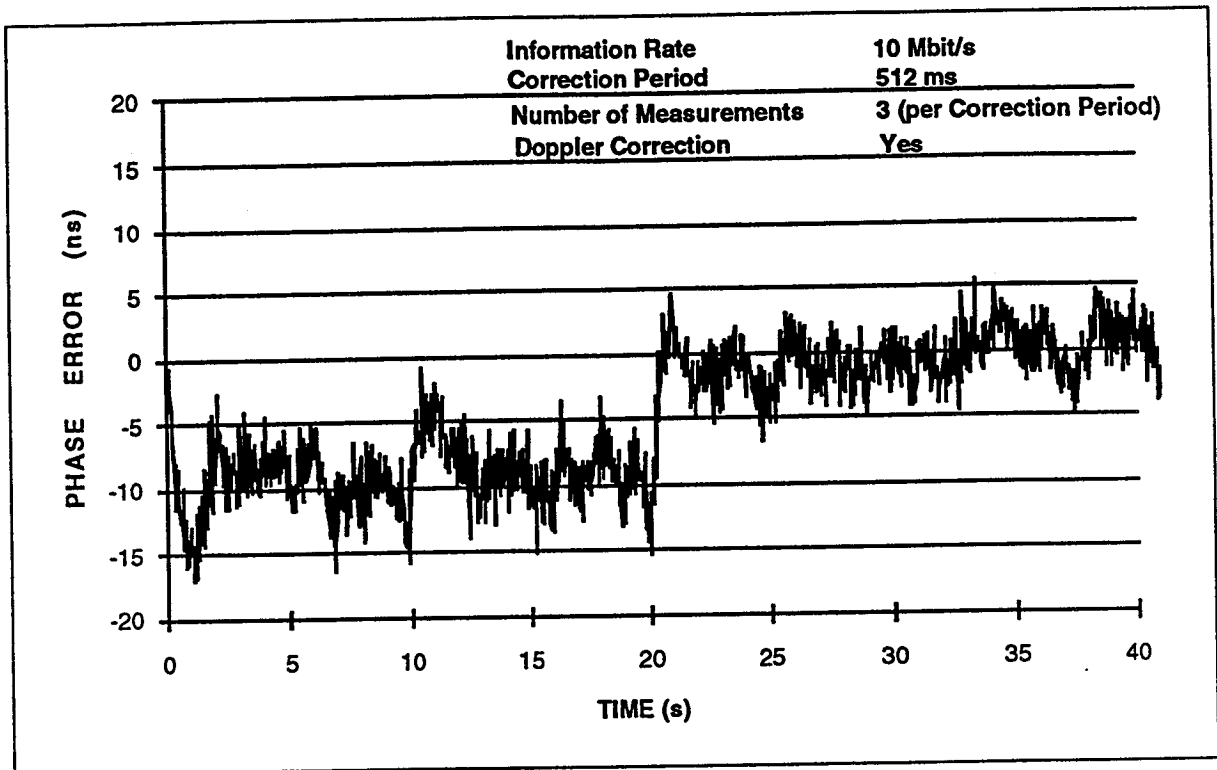


Figure 6.23: PLC-PPS Simulation Results with Doppler Correction and Multiple Measurements

Table 6.7: Supportable Data Rates (PLC-PPS)

No. of Measurements	Correction Period (1024 ms)		Correction Period (512 ms)	
	1	3	1	3
Without Doppler Correction	1.8 Mbit/s	2.2 Mbit/s	3 Mbit/s	4 Mbit/s
With Doppler Correction	5.5 Mbit/s	9 Mbit/s	9 Mbit/s	10 Mbit/s

The above table shows that a data rate of 5.5 Mbps can be supported by a single measurement technique with 1024-ms correction interval and Doppler correction. Doppler correction involves minor additional processing at the user terminal and virtually adds no cost to the user terminal hardware. A 1024 ms correction period can support synchronization for a large number of terminals on a superframe basis.

Higher bit rates may be achieved with a shorter correction period and multiple phase error measurements per correction period. However, this will somewhat reduce the number of supportable terminals per frame or would require more synchronization slots and thus higher overhead.

Finally, the cost impact of implementing bit synchronous operation using the PLC-PPS approach will be relatively low, on the order of a few hundred dollars per terminal.

6.3 Summary of Timing Analysis

Based on the analysis and simulation results presented in this section, the following conclusions can be made. The independent clock (IC) approach is more complex and yields worse performance than the phase locked clock (PLC) technique. The PLC system can be implemented using either a programmable phase shifter (PPS) or a digital controlled oscillator (DCO). The PPS provides slightly better performance than the DCO and is not restricted by the DCO high frequency limitations. The information bit rates supported by a bit synchronous system can be from about 2 Mbit/s to about 10 Mbps for QPSK modulation with rate-1/2 coding depending on the error correction technique selected. This is based on the worst-case phase error of 5 - 6 percent of a symbol period. Even higher bit rates can be accommodated but at the expense of higher performance degradation (more than 0.5 dB loss due to timing misalignment).

Section 7

Conclusions

A bit synchronous MF-TDMA system was initially deemed to be a high risk system concept that might accompany a number of critical system design issues. Through extensive analysis and simulation performed in the present study, this synchronization concept is found to be a practical as well as viable technique that will provide numerous advantages over conventional TDMA synchronization. The potential benefits of a bit synchronous system are simpler implementation of onboard multicarrier demultiplexers and demodulators, higher frame efficiency, smaller onboard buffer size, and smaller onboard processing/switching delay. In addition, the baseline network architecture necessitates the use of a bit synchronous technique; otherwise, frame efficiency will be reduced to about 50 percent, or a frame length must be increased by an order of magnitude to achieve a reasonable frame efficiency.

The bit synchronous technique allows demultiplexer operation with one output sample per symbol and further eliminates interpolation filtering. The impact on onboard hardware will be the reduction of mass and power by a factor of 2/3 relative to the asynchronous system. In addition, this technique eliminates a timing recovery and correction function in the multicarrier demodulator implementation and results in about a 50-percent reduction in mass and power. These estimates are based on the computational complexity of these devices, and actual reductions may be less than those cited above due to supporting logic circuits and PC boards common to both techniques.

The impact of a bit synchronous system on TDMA frame design is significant. For example, a conventional TDMA system with a variable burst length requires a TDMA frame length of about 28 ms to achieve a 90-percent frame efficiency at a bit rate of 2.048 Mbit/s and 40 bursts per frame, while the bit synchronous system only needs a 3-ms frame length to provide the same performance. This implies that the latter synchronization technique reduces the onboard buffer size and processing delay to about one-tenth of those of the conventional system. Also, the user terminal buffer size is reduced accordingly. Similar improvements, though not so drastic as above, can be observed for a single-channel-per-burst TDMA system with a bit synchronous technique.

Two types of clock control techniques to align transmitted TDMA bursts with an onboard reference clock were analyzed in the report. The first technique employs an independent user terminal clock (IC technique) and a simple prediction circuit to estimate clock correction values. The second technique derives a transmit clock from a received downlink clock by a phase lock technique (PLC technique). The PLC technique is simpler than the IC approach and provides a precise timing alignment with the onboard clock with an accuracy of about 5-percent of a symbol period. Timing correction is performed using either a programmable phase shifter (PPS) or a digitally controlled oscillator (DCO), where the former yields a slightly better accuracy. These devices are relatively inexpensive and contribute an additional few hundred dollars to the overall terminal cost.

A simple PLC technique, which is based on single phase error measurement without Doppler compensation, can support a bit rate of up to 3 Mbit/s. With multiple phase error measurements and Doppler compensation, the supportable bit rate exceeds 10 Mbit/s. These results were verified by analysis and computer simulation. The impact of higher bit rates on the user terminal cost is virtually none for the PPS implementation but will be higher for the DCO technique due to high-speed operation of oscillator and programmable divider circuits.

Based on the present study, two areas have been identified for future work. The first area is to perform a detailed analysis and simulation of onboard carrier and clock recovery circuit performance, including simulation of communication channel and demultiplexer/demodulator processing functions. For onboard burst recovery, the current study used the results published in the literature and a simple analysis. Thus, the proposed study will be useful in validating and/or refining onboard processor functions and performance. The second area of future work is to develop a proof-of-concept hardware device to perform user clock correction, using either a PPS or a DCO technique. This will be a necessary step of implementing a bit synchronous system in the future advanced onboard processing satellite.

Section 8

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13. ABSTRACT (Maximum 200 words) This report addresses modulation and synchronization techniques for a multifrequency time-division-multiple-access (MF-TDMA) system with onboard baseband processing. The types of synchronization techniques analyzed are asynchronous (conventional) TDMA, preambleless asynchronous TDMA, bit synchronous timing with a preamble, and preambleless bit synchronous timing. Among these alternatives, preambleless bit synchronous timing simplifies onboard multicarrier demultiplexer/demodulator designs (about 2:1 reduction in mass and power), requires smaller onboard buffers (10:1 ~ 3:1 reduction in size), and provides better frame efficiency as well as lower onboard processing delay. Analysis and computer simulation illustrate that this technique can support a bit rate of up to 10 Mbit/s (or higher) with proper selection of design parameters. High bit rate transmission may require Doppler compensation and multiple phase error measurements. The recommended modulation technique for bit synchronous timing is coherent QPSK with differential encoding for the uplink and coherent QPSK for the downlink.				
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